PID Summary

Frascati SuperB Meeting, December 15th 2011

Nicolas Arnaud, for the SuperB PID group

UNIVERSITÉ PARIS SUD
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LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

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Institut national de physique nucléaire et de physique des particules

- 3 parallel sessions, mainly barrel-oriented
  - S1: FDIRC prototype @ SLAC CRT + PMT tests
  - S2: status of the TDR PID chapter and related discussions
  - S3: others topics, including background and simulation

- Contributions to the background session as well

PID Parallel Sessions

- Three PID parallel sessions

Tuesday, 13 December 2011

15:00	[77] **FDIRC status** by Dr. Jerry VAVRA (SLAC) (Aula Seminari: 15:00 - 15:20)	slides
	[181] **FDIRC shielding** by Massimo BENETTONI (PD) (Aula Seminari: 15:20 - 15:40)	slides
	[79] **He effect in H8500** by Mario Nicola MAZZIOTTA (BA) (Aula Seminari: 15:40 - 15:50)	slides
	[80] **Magnet configuration for the H8500 studies** by Francesco LOPARCO (BA) (Aula Seminari: 15:50 - 16:00)	slides
16:00	[81] **Preliminary studies with H8500** by Fabio GARGANO (BA); Francesco GIORDANO (BA) (Aula Seminari: 16:00 - 16:10)	slides
	[88] **PMT testing** by Prof. Douglas ROBERTS (University of Maryland) (Aula Seminari: 16:10 - 16:20)	slides

Wednesday, 14 December 2011

09:00	[49] **FDIRC background analysis using the latest FullSim production** by Luis Alejandro PEREZ PEREZ (PI) (Aula Seminari: 09:00 - 09:20)	slides
	[89] **CRT simulation status** by Prof. Douglas ROBERTS (University of Maryland) (Aula Seminari: 09:20 - 09:40)	
	[83] **Preliminary results of the front-end block of the 16-channel WaveCatcher board** by Mr. Dominique BRETON (LAL ORSAY); Mrs. Jihane MAALMI (cNRS-LAL) (Aula Seminari: 09:40 - 10:00)	
10:00	[87] **Studies on H8500 PMT** by Dr. Gabriele SIMI (PD) (Aula Seminari: 10:00 - 10:10)	

Tuesday, 13 December 2011

17:00	[180] **Status of the PID TDR chapter** by Dr. Jerry VAVRA (SLAC) (Aula Seminari: 17:00 - 17:20)	slides
	[82] **Schedule of the PID barrel activities for the TDR** by Mario Nicola MAZZIOTTA (BA) (Aula Seminari: 17:20 - 17:40)	slides
	[78] **Status of the barrel PID electronics** by Mr. Christophe BEIGBEDER (LAL) (Aula Seminari: 17:40 - 18:00)	slides

Contents

- TDR status
- FDIRC Test at SLAC Cosmic Ray Telescope (CRT)
- Background
- Simulation
- H-8500 Photomultiplier Tests
- FTOF-related activities

TDR Status

- For more details, see
  http://agenda.infn.it/getFile.py/access?contribId=180&sessionId=10&resId=0&materialId=slides&confId=4107

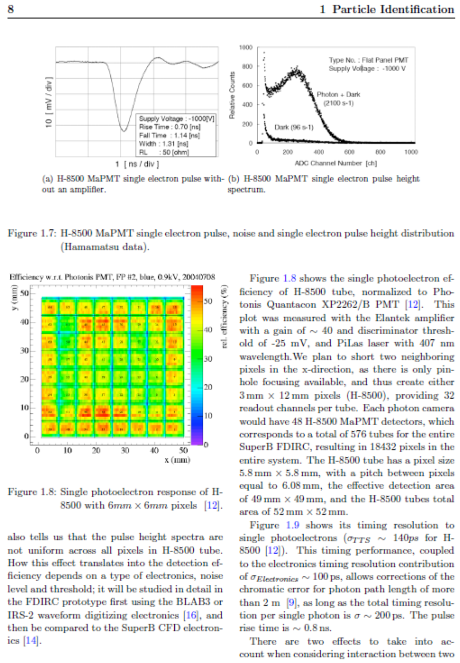
- About 60% completed – mostly detector-related sections
  → Most of the parts already written need to be reviewed and updated
  - Several sections are still empty

- All sections have been assigned to authors, detailled plan is in SVN

- Latest version of the PID chapter:
  http://www.slac.stanford.edu/~narnaud/SuperB/DTDR/dtdr-PID.pdf
  → Updated daily by a cronjob – when the compilation isn't broken ☺

A few samples

Contents



8 1 Particle Identification

(a) H-8500 MaPMT single electron pulse without an amplifier. (b) H-8500 MaPMT single electron pulse height spectrum.

Figure 1.7: H-8500 MaPMT single electron pulse, noise and single electron pulse height distribution (Hamamatsu data).

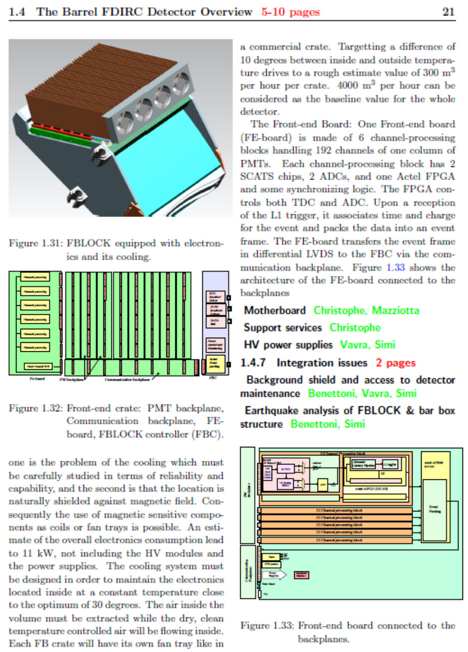
Figure 1.8: Single photoelectron response of H-8500 with $6mm \times 6mm$ pixels [12].

also tells us that the pulse height spectra are not uniform across all pixels in H-8500 tube. How this effect translates into the detection efficiency depends on a type of electronics, noise level and threshold; it will be studied in detail in the FDIRC prototype first using the BLAB3 or IRS-2 waveform digitizing electronics [16], and then be compared to the SuperB CFD electronics [14].

Figure 1.8 shows the single photoelectron efficiency of H-8500 tube, normalized to Photonis Quantacon XP2262/B PMT [12]. This plot was measured with the Elantek amplifier with a gain of ~ 40 and discriminator threshold of -25 mV, and PiLas laser with 407 nm wavelength.We plan to short two neighboring pixels in the x-direction, as there is only pinhole focusing available, and thus create either 3 mm × 12 mm pixels (H-8500), providing 32 readout channels per tube. Each photon camera would have 48 H-8500 MaPMT detectors, which corresponds to a total of 576 tubes for the entire SuperB FDIRC, resulting in 18432 pixels in the entire system. The H-8500 tube has a pixel size 5.8 mm × 5.8 mm, with a pitch between pixels equal to 6.08 mm, the effective detection area of 49 mm × 49 mm, and the H-8500 tubes total area of 52 mm × 52 mm.

Figure 1.9 shows its timing resolution to single photoelectrons ($\sigma_{TTS} \sim 140ps$ for H-8500 [12]). This timing performance, coupled to the electronics timing resolution contribution of $\sigma_{Electronics} \sim 100$ ps, allows corrections of the chromatic error for photon path length of more than 2 m [9], as long as the total timing resolution per single photon is $\sigma \sim 200$ ps. The pulse rise time is ~ 0.8 ns.

There are two effects to take into account when considering interaction between two



1.4 The Barrel FDIRC Detector Overview 5-10 pages 21

Figure 1.31: FBLOCK equipped with electronics and its cooling.

Figure 1.32: Front-end crate: PMT backplane, Communication backplane, FE-board, FBLOCK controller (FBC).

one is the problem of the cooling which must be carefully studied in terms of reliability and capability, and the second is that the location is naturally shielded against magnetic field. Consequently the use of magnetic sensitive components as coils or fan trays is possible. An estimate of the overall electronics consumption lead to 11 kW, not including the HV modules and the power supplies. The cooling system must be designed in order to maintain the electronics located inside at a constant temperature close to the optimum of 30 degrees. The air inside the volume must be extracted while the dry, clean temperature controlled air will be flowing inside. Each FB crate will have its own fan tray like in a commercial crate. Targetting a difference of 10 degrees between inside and outside temperature drives to a rough estimate value of 300 m^3 per hour per crate. 4000 m^3 per hour can be considered as the baseline value for the whole detector.

The Front-end Board: One Front-end board (FE-board) is made of 6 channel-processing blocks handling 192 channels of one column of PMTs. Each channel-processing block has 2 SCATS chips, 2 ADCs, and one Actel FPGA and some synchronizing logic. The FPGA controls both TDC and ADC. Upon a reception of the L1 trigger, it associates time and charge for the event and packs the data into an event frame. The FE-board transfers the event frame in differential LVDS to the FBC via the communication backplane. Figure 1.33 shows the architecture of the FE-board connected to the backplanes

Motherboard Christophe, Mazziotta

Support services Christophe

HV power supplies Vavra, Simi

1.4.7 Integration issues 2 pages

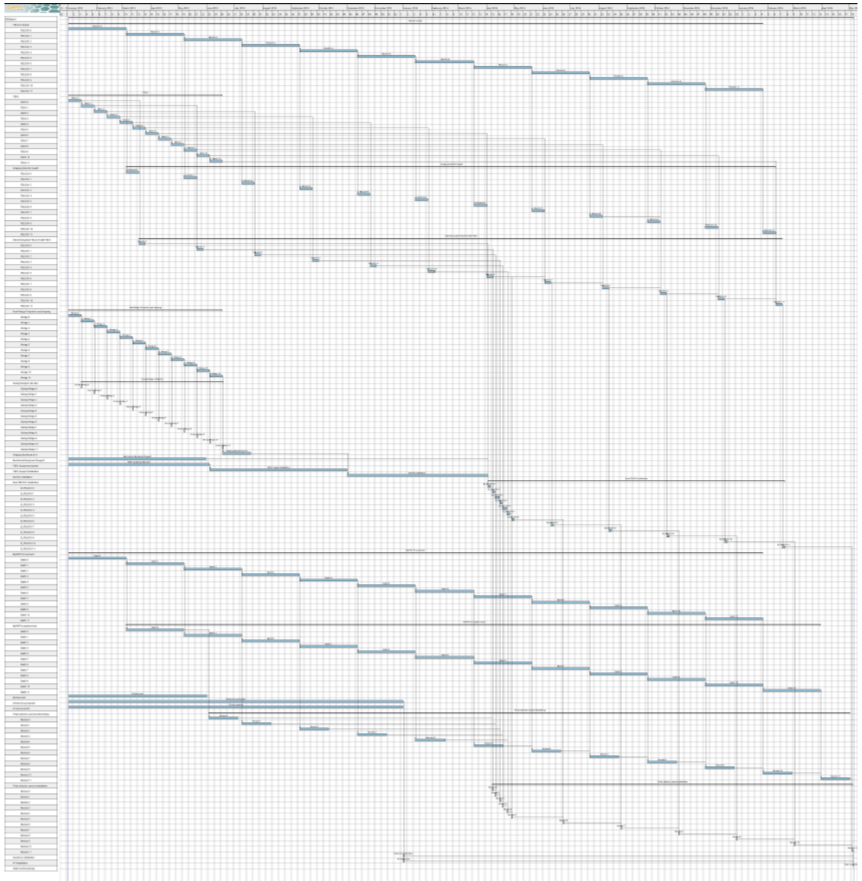
Background shield and access to detector maintenance Benettoni, Vavra, Simi

Earthquake analysis of FBLOCK & bar box structure Benettoni, Simi

Figure 1.33: Front-end board connected to the backplanes.

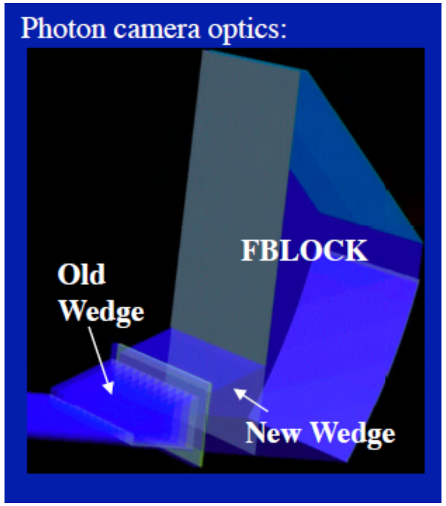
FDIRC planning

- First attempt from Bari group
- Use of free software GanttProject
  http://www.ganttproject.biz
- Good to identify items on critical paths
- Info, thoughts, etc. exist in various places
  → In particular Jerry's spreadsheets
- Need to merge all these in a consistant way
- Inputs from many sources required



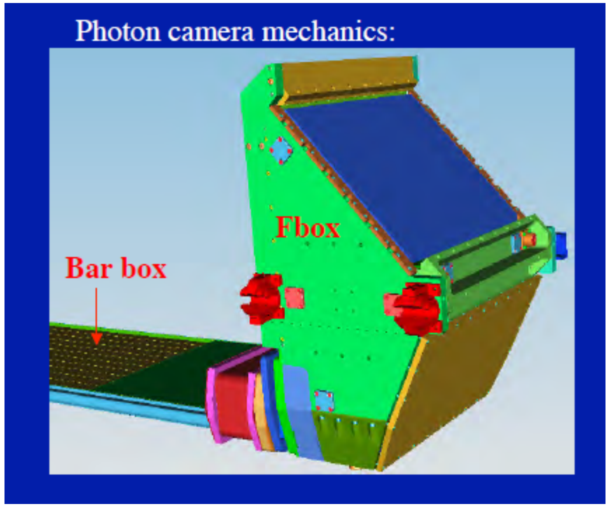
→ Will run regular meetings dedicated to this topic in 2012

FDIRC test @ SLAC CRT



- Updates on optics, Fbox & mechanics for the sector prototype
- Problem with the (temporary) Hawaii electronics
- Planning for the coming months

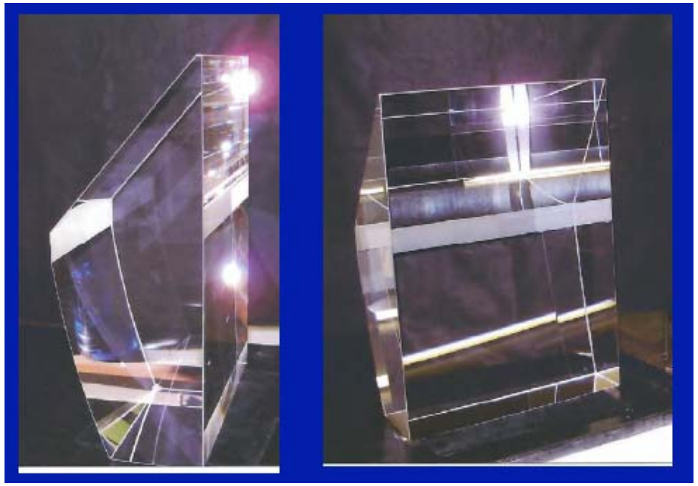
→ See Jerry's opening talk in the 1^{rst} PID parallel session for more details.



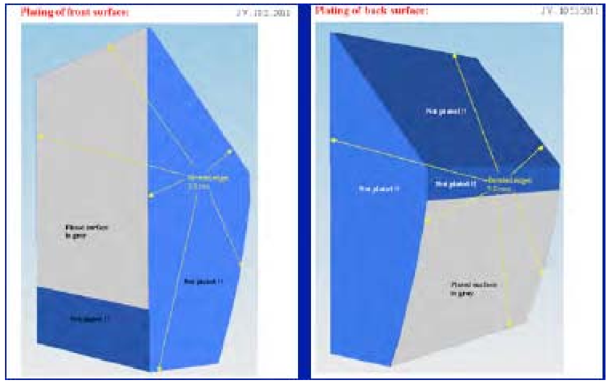
Optics

- Barbox and new wedge successfully glued together

- FLOCK polishing completed



- FBLOCK plating completed this week
  → Two mirror surfaces: 1 cylindrical,
  1 flat
  - Aluminium protected by a SiO_2 layer

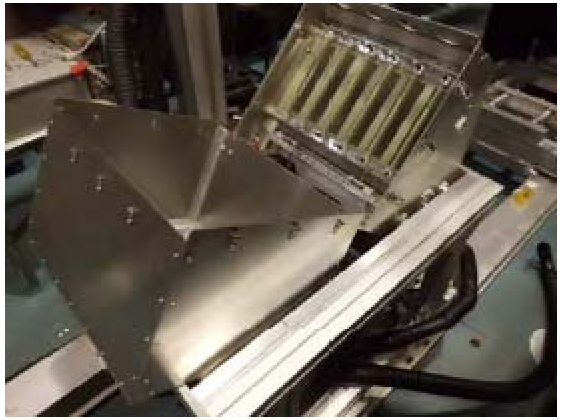


- Next challenge: to have the FBLOCK shipped safely from NY state to SLAC
  → Shipment will be done early next year once the process has been fully defined

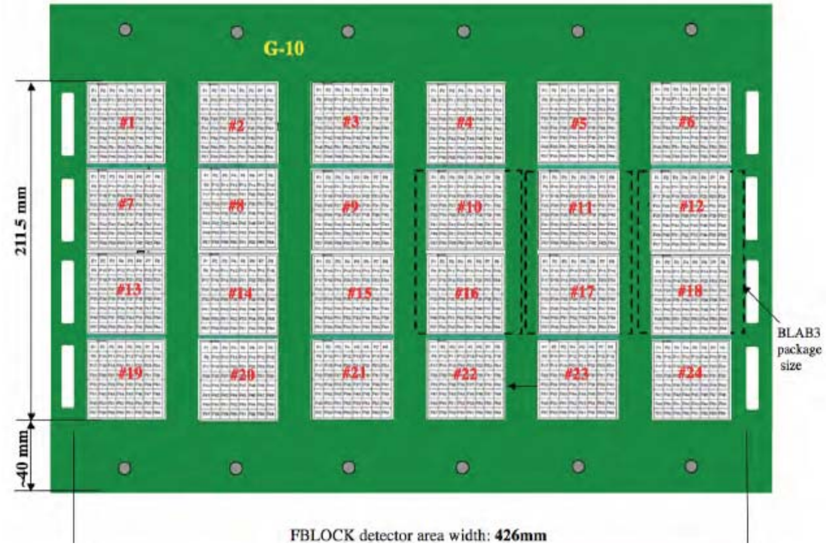
Mechanics

- Fbox preparation
  - Dismantling, cleaning in clean room and reassembly
    → Ready for assembly with FBLOCK

- Succesful mechanical trial test of Fbox in CRT support



- G-10 holder built to host electronics packages
  → Hawaii (up to 6 double packages)
     + LAL (up to 12 packages)



Electronics – hardware

- Problem with the new BLAB3 chip (Hawaii)
  → Issues with an amplifier, poor S/N ratio for H-8500 MaPMTs

- Need to make one or two steps back
  - Use ‘SLAC’ amplifiers and perhaps even BLAB2 chips

  → 1-2 months delay

- Status of Orsay electronics developments
  → See Christophe’s talk in 1^{rst} parallel session
  - SCATS chip submitted early November
    → Money issue to be able to readout all 14 PMTs of the FDIRC prototype
  - Design of the SCATS test board in progress; submission in January
  - Analog board (to test the analog part of the chip called PIF) just submitted
  - Mother board design in progress

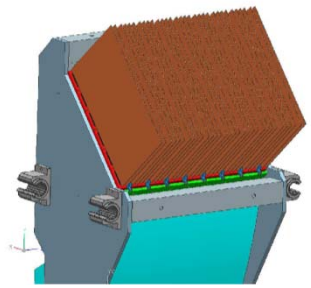
Updated planning for the FDIRC prototype

- **QC the FBLOCK in January.**
- **Assemble Fbox around the FBLOCK in January.**
- **Install the Barbox and Fbox into CRT at the end of January.**
- **Glue the New Wedge to FBLOCK in CRT using the RTV glue.**
- **Create "pixel constants" for FDIRC prototype with MC program.**
- **As a consequence of BLAB3 not working we have to:**
  - switch to IRS-2 waveform digitizer , which, however, requires adding amplifiers
  - produce 48 SLAC amplifier PC boards and components, and load components on PC boards.
  - test new amplifiers with IRS-2 digitizer in the scanning setup.
- **We may even put back in our seven BLAB2 packages.**
- **Install detectors and electronics, cooling, cables, laser calibration, etc.**
- **Start running in CRT sometimes in February-March ?**

Electronics: toward a baseline solution for TDR

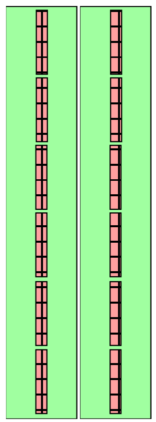
- See corresponding section in the TDR for details
  → Currently located in the PID chapter; to be moved to ETD chapter when ready

- Two design options
  1) BaBar-like: cables from PMTs to FEEs; crates on the detector sides
  2) Electronics on the FBLOCK
  → Both options have balanced pros & cons;
  cost of cables makes solution 2) the baseline for the TDR



Crate-like structure

- Many options for the backplane
  - Several factors to take into account
  → Ongoing discussion among the group

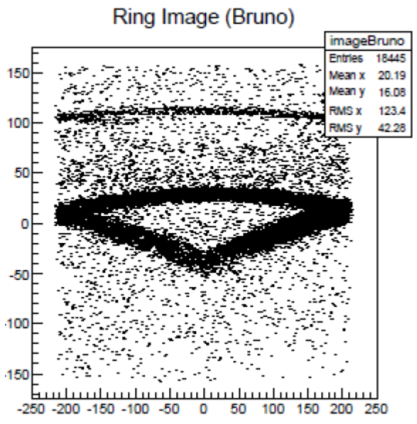


- Studies on
  - data links (numbers, data concentration, etc.)
  - cooling (dissipated power: ~500 W / sector)
  - LV power studies

Background

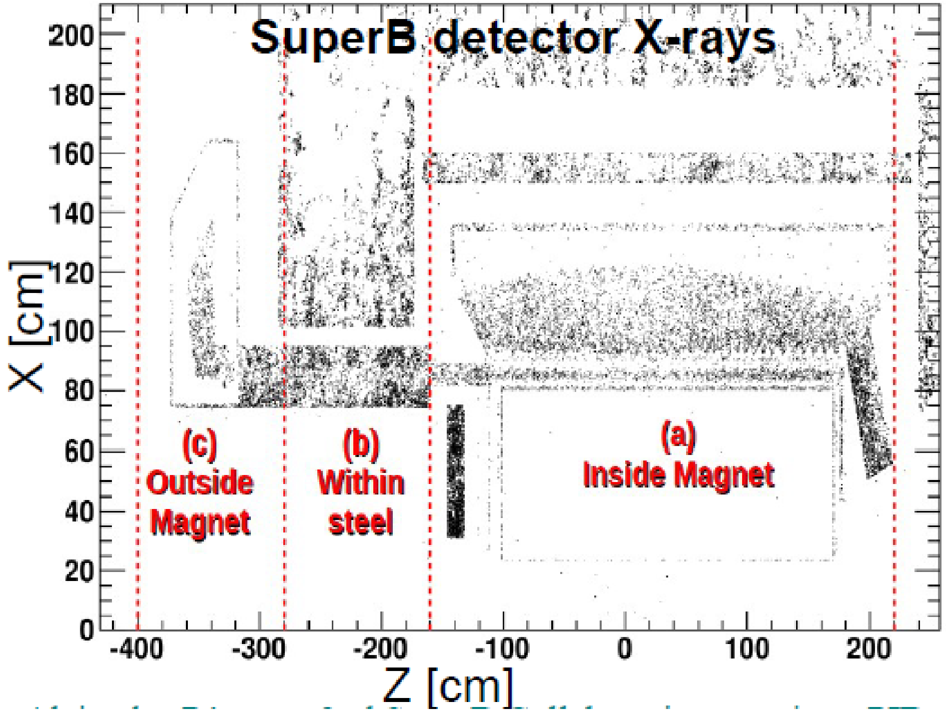
- FDIRC background is now simulated well in Bruno
- Results from the last FullSim production
- A few words about the FDIRC shieldings

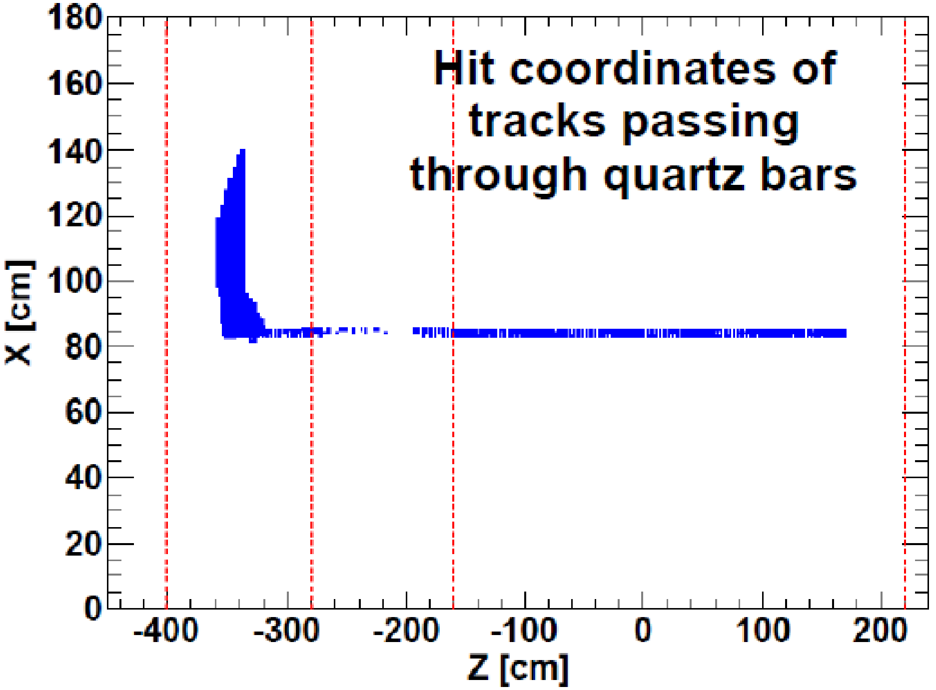
Results from the latest production



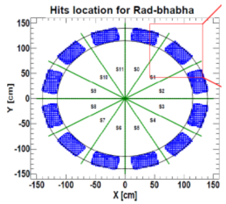
- Bruno implementation of Cherenkov optics and camera properties
  → Andrea di Simone and Doug

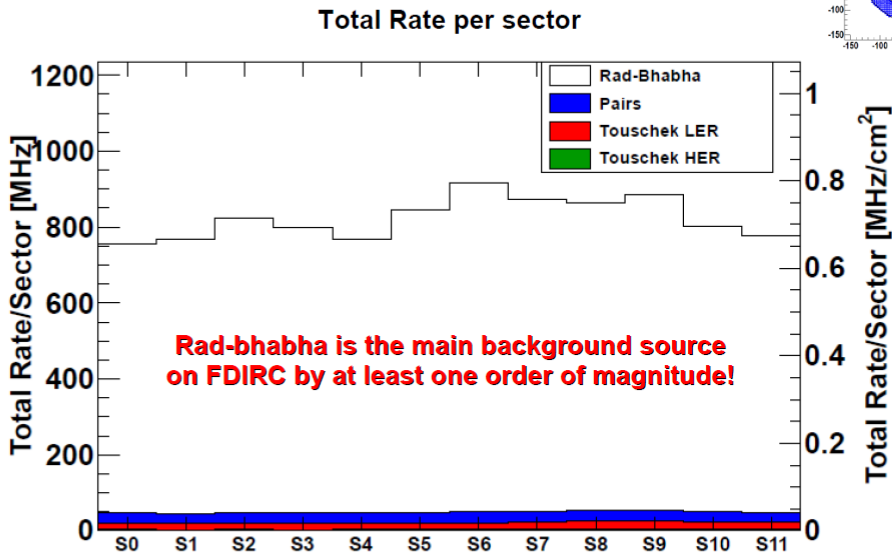
- FDIRC data analyzed by Alejandro
  → Three different z-regions analyzed separately



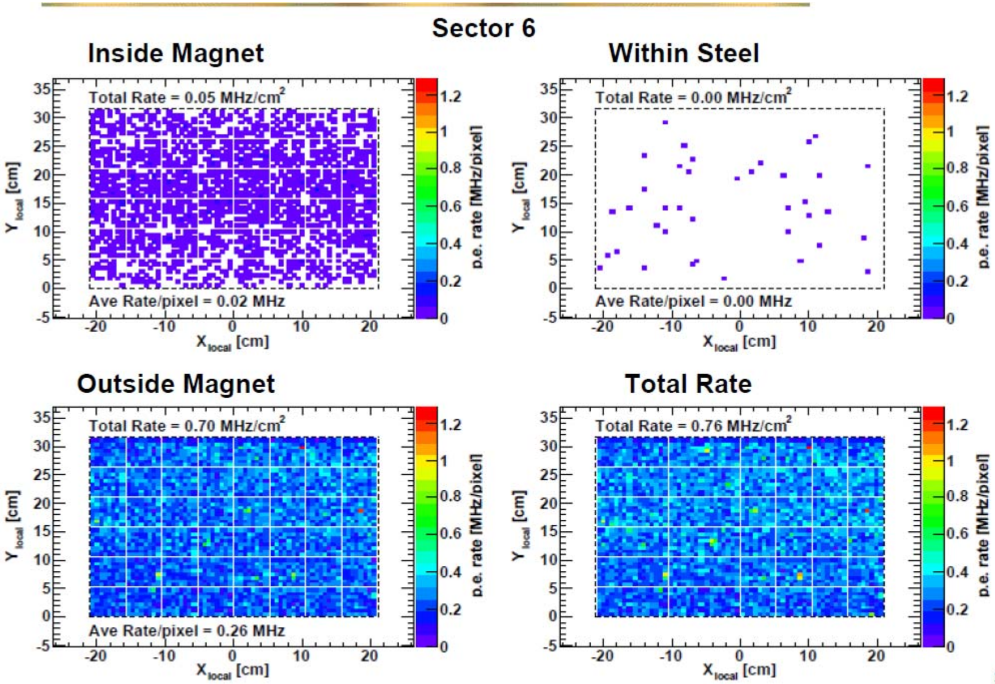


Main results





- Radiative Bhabha is the main source of background for the FDIRC



- Background is mainly coming from tracks hitting the quartz outside of the magnet
  $\Rightarrow$ Shielding will help reducing it

FDIRC background estimation: summary

- Table and conclusion/caution from Jerry's presentation in parallel session, updated in bkg parallel session

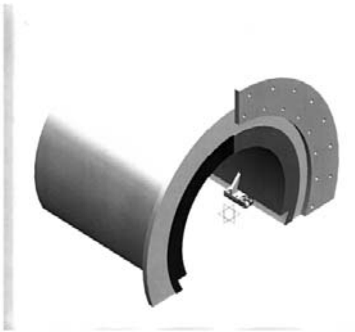
Method	Person	Rate per double-pixel from the bar box, i.e., from active volume	Rate per double-pixel from the Photon camera if not shielded
Real MC simulation using a proper treatment of optical photons	Alejandro, Doug, Andrea	~ 85 kHz	~ 550 kHz
MC simulation using a simple treatment of optical photons	Riccardo	~ 67 kHz *	~ 400 kHz *
Empirical scaling from Belle-I by quartz volume and as Lumi-term	Jerry	~ 75 kHz *	~ 120 kHz *

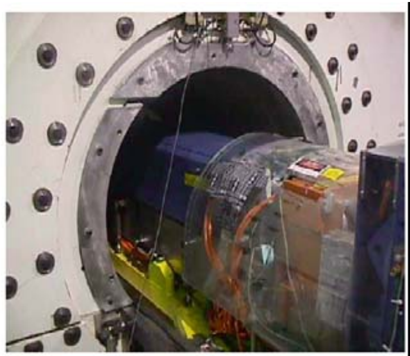
* Apply a factor of 2 reduction for a photon loss on optical surfaces

- **Impressive agreement, but may be still completely wrong !**
- **We clearly need to shield the photon camera.**

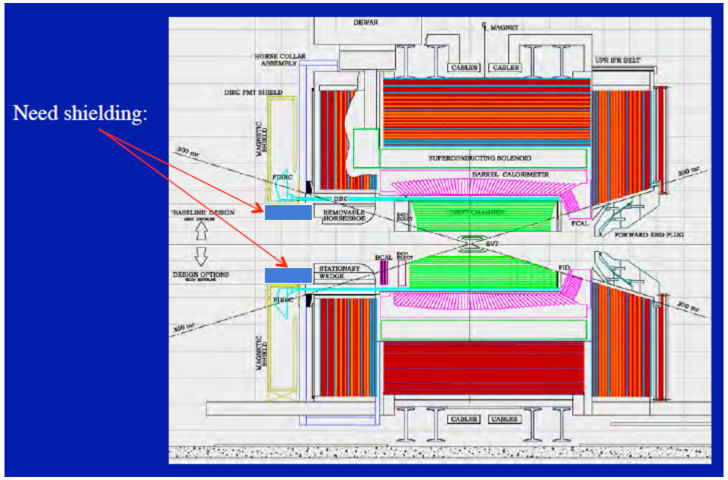
12/13/11 J. Va'vra, FDIRC status 3

- Picture of the BaBar DIRC shield inside of the camera (SOB)





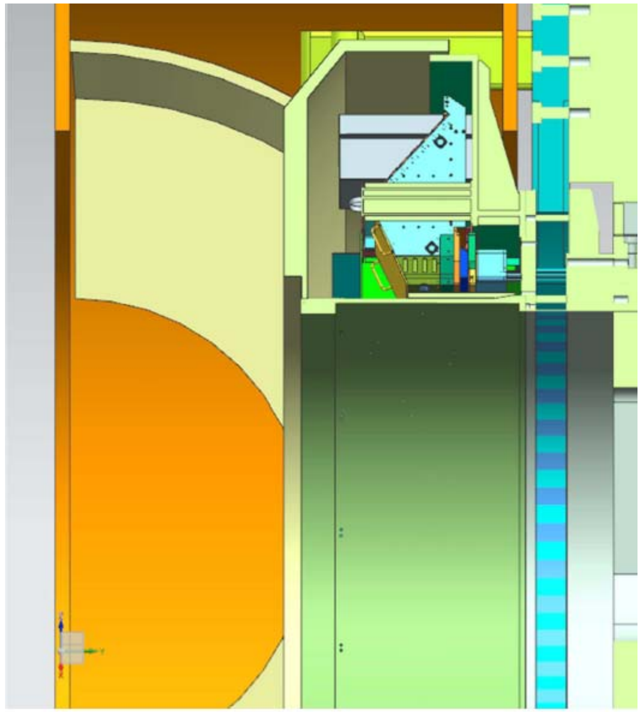
FDIRC Shielding

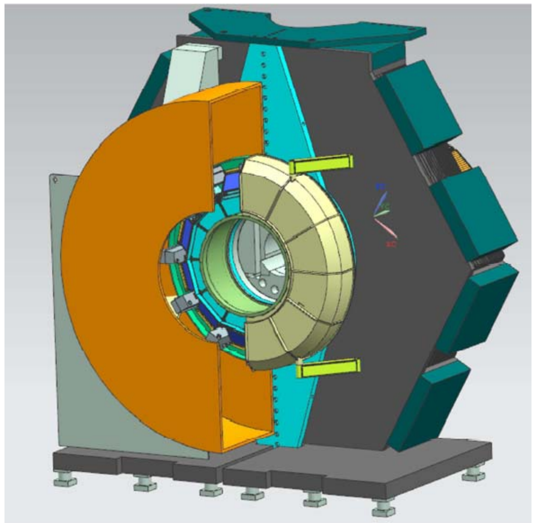


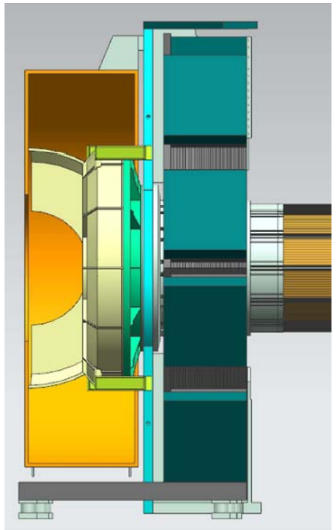
- 3 different shields:
  - optical
  - magnetic
  - background

- From BaBar experience and Bruno simulations
  → Inner shielding needed

- Initial drawings from Massimo (2 years old)
  →Iterations needed (PID, Integration, etc.)







Simulation

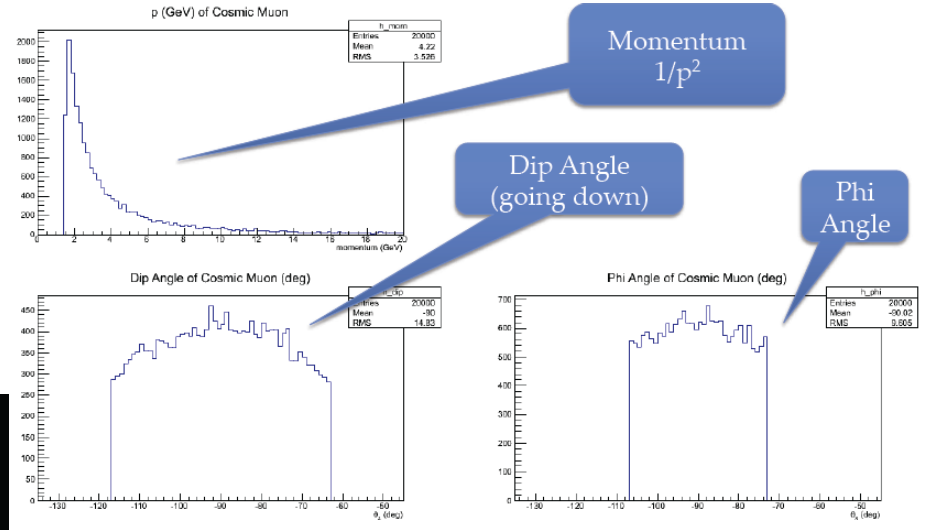
- Already reported about the progress with the FDIRC simulation in Bruno
- Focus on the simulation of the FDIRC prototype at SLAC CRT

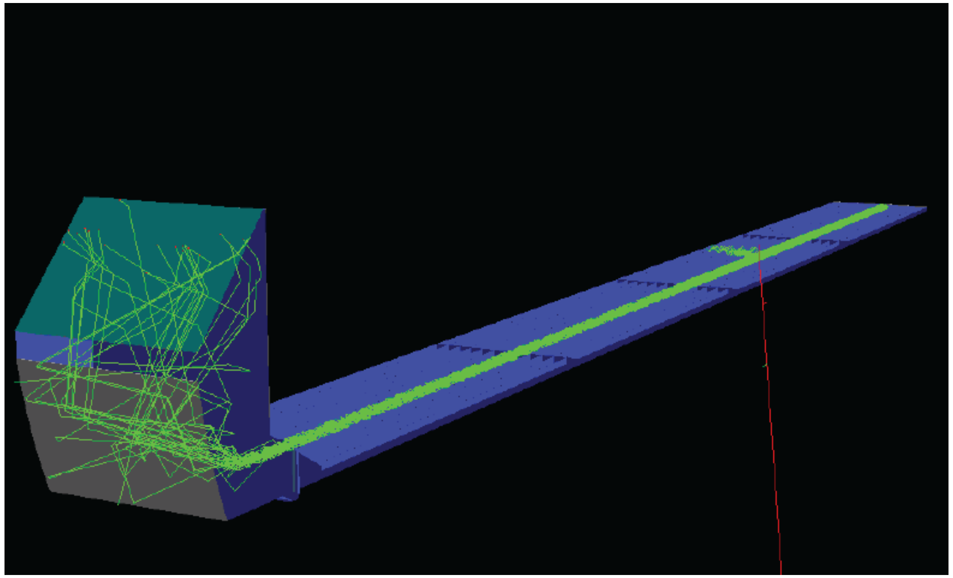
Simulating the FDIRC prototype

- Based on the FDIRC SVN repository
  - Geant4-based package developed in standalone for the FDIRC full simulation
  - Now part of Bruno and used by Alejandro for the results presented previously

- New geometry configuration

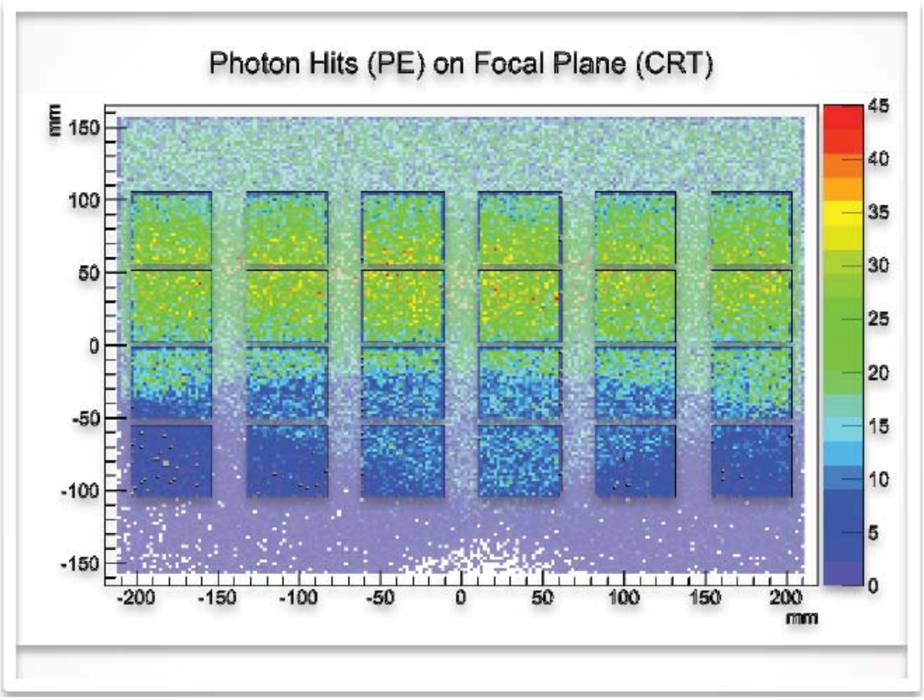
- Cosmic muon generator
  $\rightarrow$ Including CRT acceptance

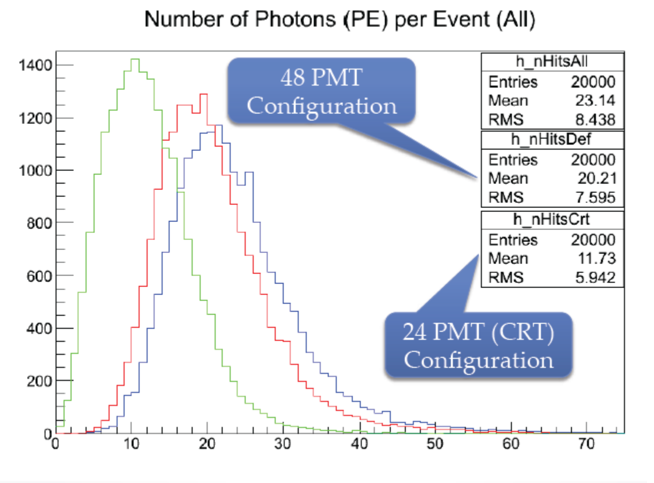




Current studies, next steps

- Test the foreseen PMT distribution on the focal plane
  → 24 PMTs at most instead of 48 (nominal)





- Geometry needs to be updated after surveys of the actual prototype

- Then: generate the (huge and geometry-dependent) single photon dictionnary

- Finally, analyze simulated or real CRT data

PMT Tests

- An important part of the PID parallel talks at each SuperB meeting

- Several groups active in this area
  → At this meeting, reports from Bari, Padova, Maryland

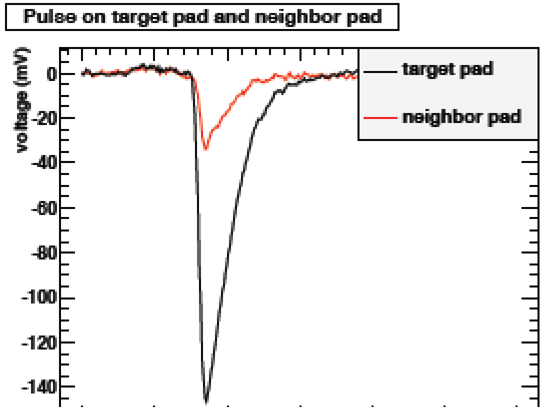
- Different and complementary studies:
  - Charge-sharing
  - Magnetic field effect – test components
  - He permeation inside the PMTs
  - PMT signal classification
  - …

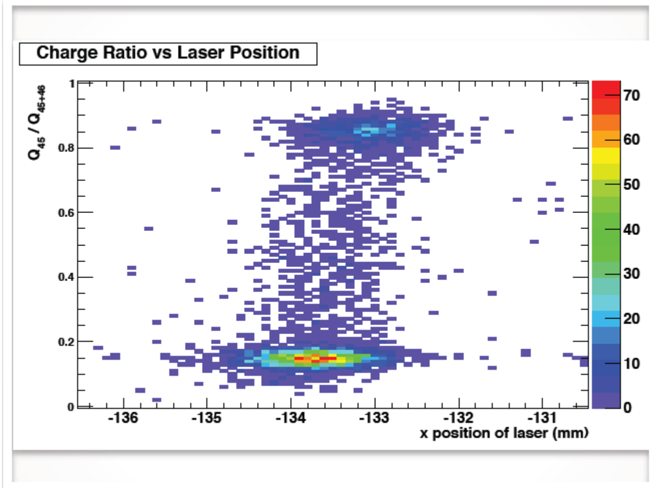
Charge sharing between pixels

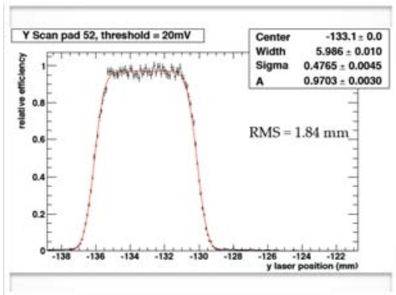
- Study at Maryland teststand (Doug)
- Main question: can it be used to improve the hit position and hence the θ_C resolution?
- The answer is probably not
  - Effect only shows up within 1-2 mm from boundary
  - Size independent of location in this area
  - In addition: pulses probably too small to be useful
  - Only seen in x-direction

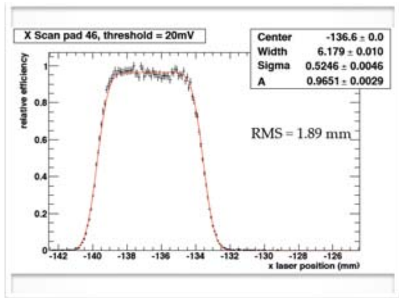
  → Overall, charge-sharing region is too small
- Study of the position resolution in x and y
  - Slightly better in y (RMS = 1.84 mm) than in x (RMS = 1.89 mm)

  → Consistent with the current tube orientation







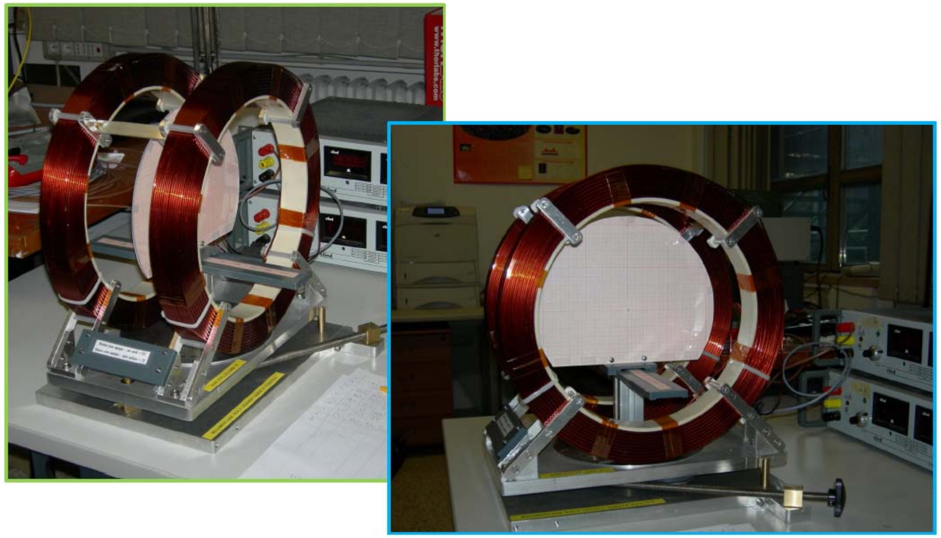


Afterpulse effect due to He permeation

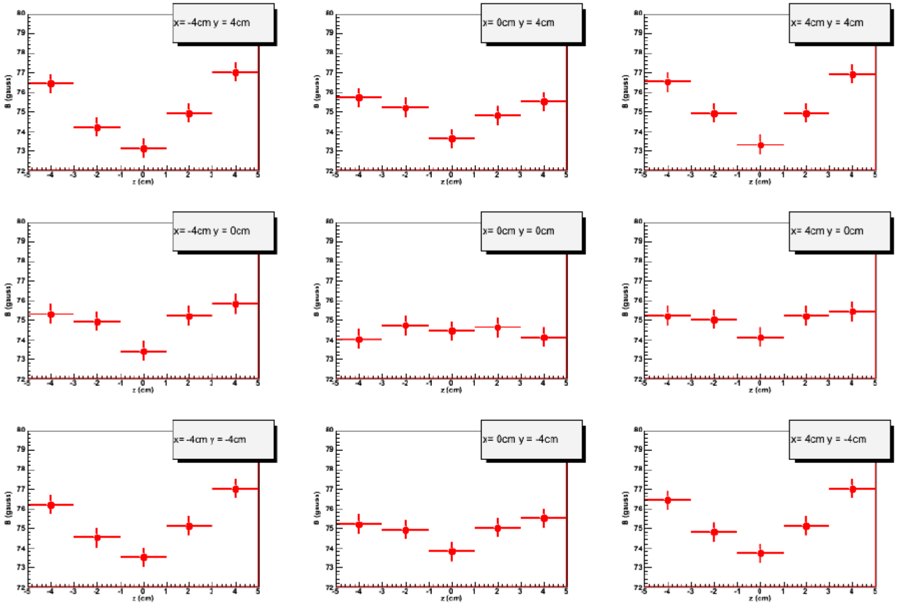
- Study by the Bari group
- Afterpulses: spurious PMT pulses delayed w.r.t. the signal output
- May be created by positive ions generated by ionization of residual gas inside PMT
  → Ion feedback: ions move back to the photocathode and produce photoelectrons
- He gas can easily leak into the PMT glass
  → Radiation damage could increase the permeability of the window
- Conclusion of the study: He is not a real concern, provided that He accumulation in the detector area is prevented.
  → Minimum airflow needed

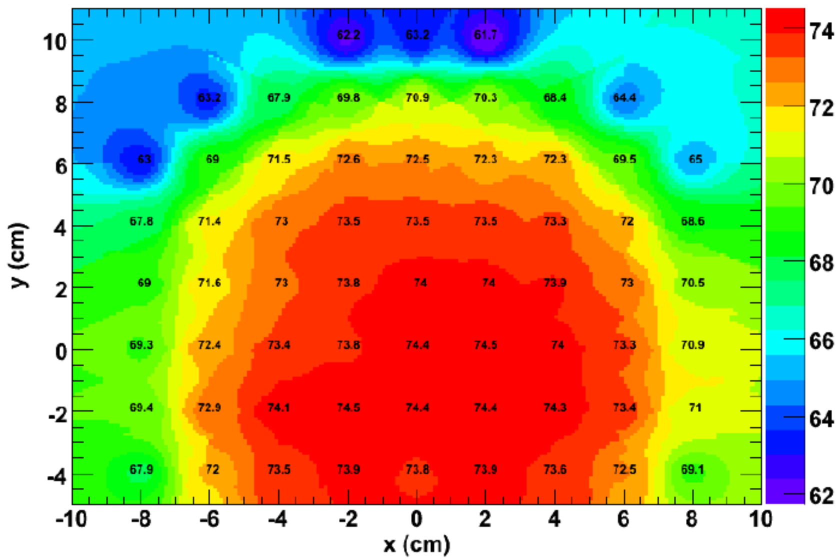
Study of magnetic field effects on MaPMT

- Bari group as well
- Design and building of Helmoltz coils
- Uniform field inside the coils
- Coils can be rotated w.r.t the MaPMT



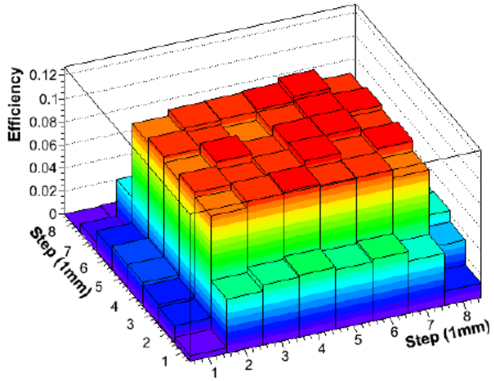
Uniformity along the z-axis

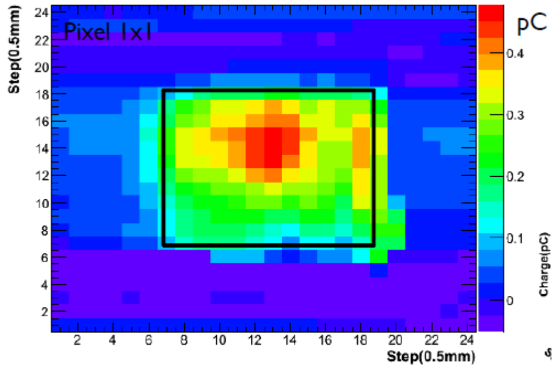




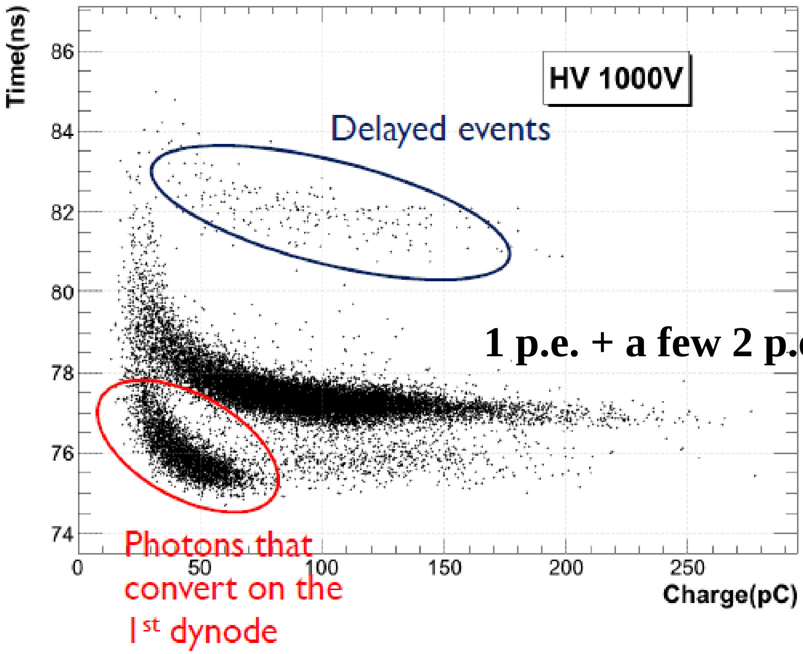
Bari H-8500 scanning setup

- Test stand setup with custom-made electronics
- Intra-pixel measurements
  - Efficiency almost uniform
  - Strong fluctuations in gain



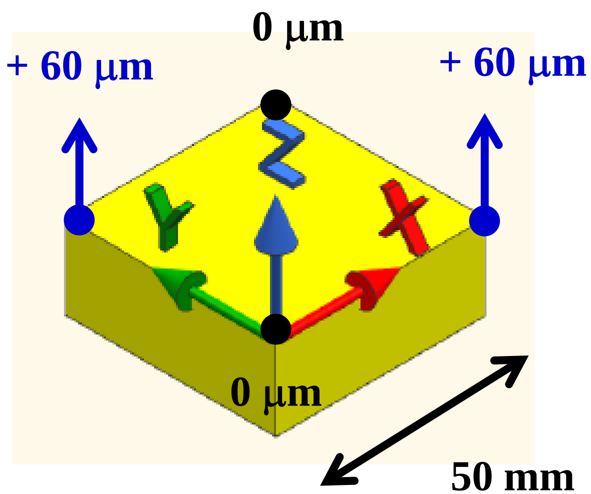


- Study of the correlation between charge and time of the signals
  - Time-walk effect clearly visible
  - ~15% of events convert on the 1rst dynode
  - ~2% of events are delayed
    → To be investigated

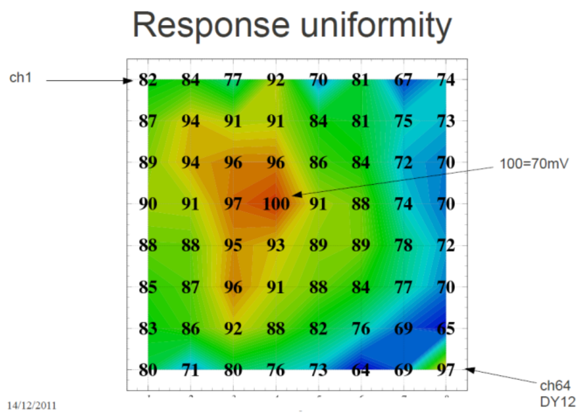


Padova studies

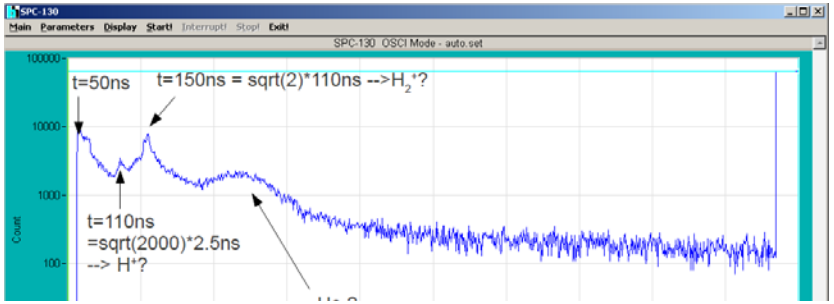
- Measurement of the front-face planarity: concave hammock shape
  → Relevant for the quartz-PMT coupling



- Test calibration scheme based on charge injection on last dynode (dy12)
  → Signals on each pixel anode



- Study pre/after pulse characteristics
  - pre-pulse ~4%
  - after-pulse ~1%
  - After pulse spectrum structures
    → Probably contributions from different ions



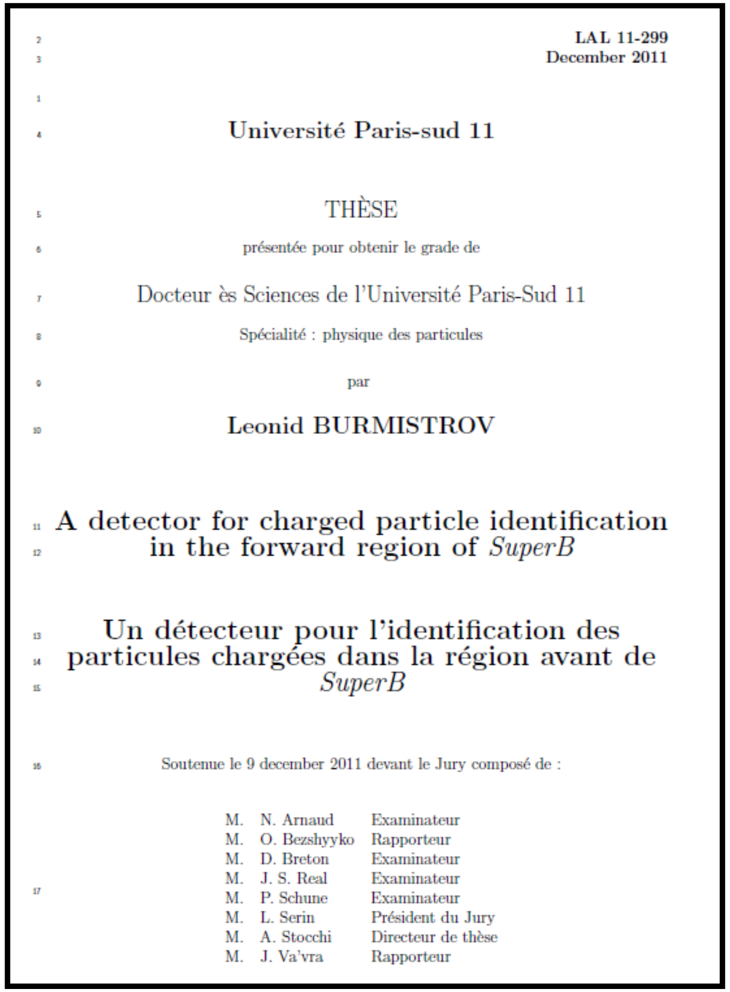
FTOF-related activities

- 2012 funding from IN2P3 (very) limited
  - Not enough to cover FTOF activities
    → Prototype of a full sector delayed

- Development of the 16-channel Wavecatcher board
  → Talk by Jihane, see next slide

- FTOF background from radiative Bhabha seems reduced by 30-40% in the latest Bruno production

- Leonid Burmistrov graduated last Friday in LAL
  → Leonid is starting a fixed-term engineer position in Dominique Breton's group
  - One of the first 100% SuperB detector PhD!?



LAL 11-299
December 2011

Université Paris-sud 11

THÈSE

présentée pour obtenir le grade de

Docteur ès Sciences de l'Université Paris-Sud 11

Spécialité : physique des particules

par

Leonid BURMISTROV

A detector for charged particle identification in the forward region of *SuperB*

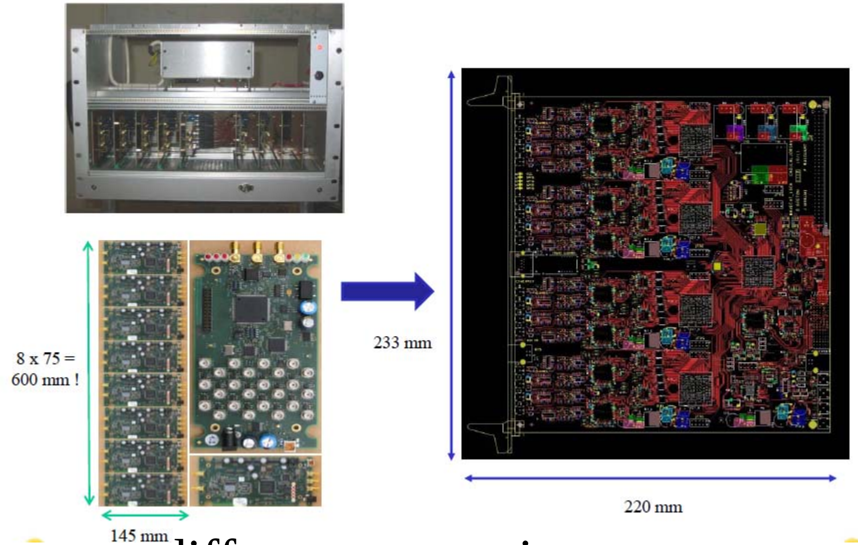
Un détecteur pour l'identification des particules chargées dans la région avant de *SuperB*

Soutenue le 9 december 2011 devant le Jury composé de :

M.	N. Arnaud	Examinateur
M.	O. Bezshyyko	Rapporteur
M.	D. Breton	Examinateur
M.	J. S. Real	Examinateur
M.	P. Schune	Examinateur
M.	L. Serin	Président du Jury
M.	A. Stocchi	Directeur de thèse
M.	J. Va'vra	Rapporteur

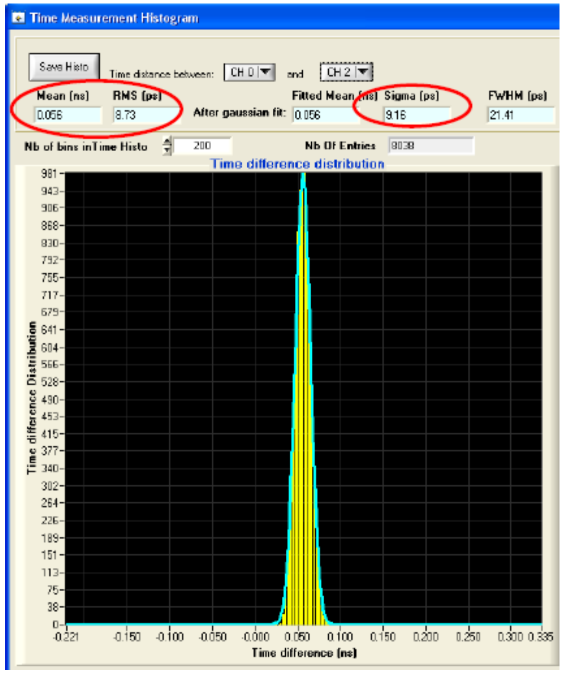
16-channel Wavecatcher board

- Goal: to replace the FTOF CRT
  test crate by a single board
  while keeping similar performances



- Four 4-channel front-end blocks
  → Validated on a mezzanine

- Precision < 10 ps RMS per channel even between different mezzanines



- First prototype board to arrive next week

- Next step: a compact 64-channel system
  - 4 synchronized 16-channel boards
  → 25×10×30 cm^3

- Then: a system up to 320 channels
  → Housed in a 6U VME crate

Conclusions

PID Outlook

- Impressive progress on the preparation of the FDIRC test @ SLAC
  - Optics and mechanics are close to being ready
  - Issue with Hawaii electronics
  - MC simulation being developed

  → Data taking to start by the end of Winter

- Studies ongoing in many areas for the FDIRC
  - Mechanics
  - Electronics
  - PMTs

  } + integration of the different components

- PID chapter of the TDR well on track
  - Drafts of many sections already commited to SVN
  - Others still need to be written

- FTOF activities slowed down due to money constraints

  → Development of the successful Wavecatcher electronics is still going on

Backup