ETD/Online Section

D. Breton, U. Marconi, S. Luitz

Summary / Frascati Meeting

December 2011

- We had three ETD sessions in this workshop:
  - Common items
  - Front-end electronics
  - Hardware trigger

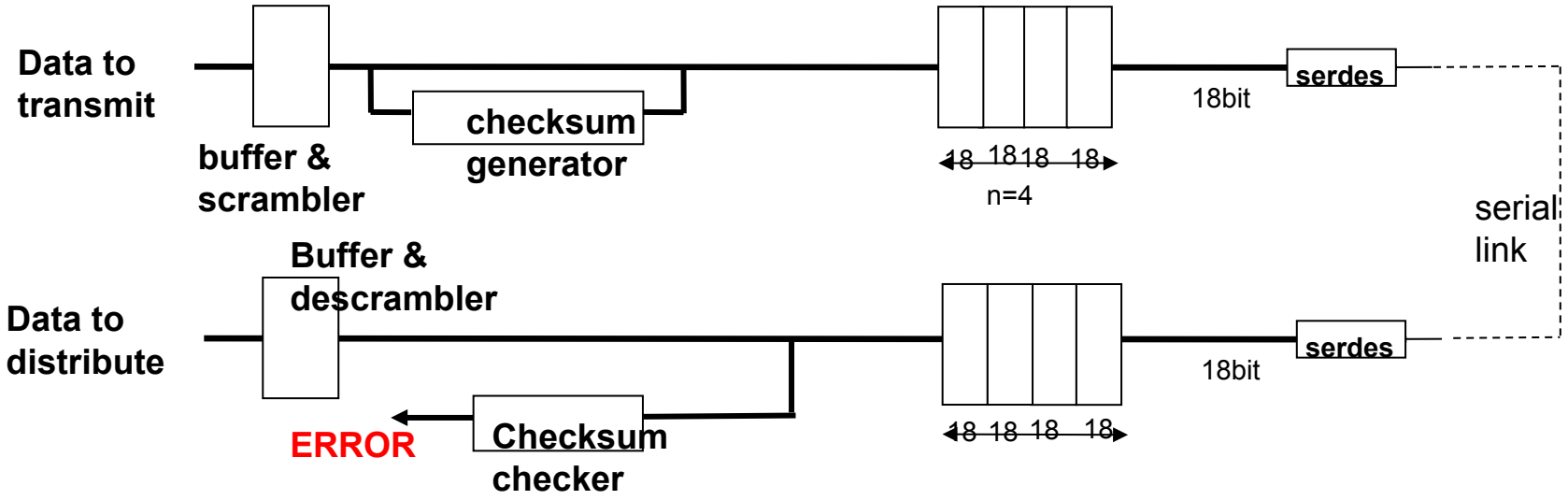
- All sessions had been very useful to refine the overall design.

- We defined almost all the baselines and the potential upgrades to describe in the TDR.

Coding analysis for the SuperB links (S.Cavaliere)

- Analysis and simulations of serial link transmission errors due to the radiation environment, affecting data integrity.
- Different possible solutions:
  - Error Correcting Coding
  - Error Detecting Coding
- The proper solution will be a light Error Detecting Coding.
- Programs, charts and various simulation and evaluation tools as well as block diagrams of the hardware organization have been set up in order to quantify the most relevant parameters to be considered:

1) Efficiency of detection 2) Undetected error probability 3) Burst errors immunity

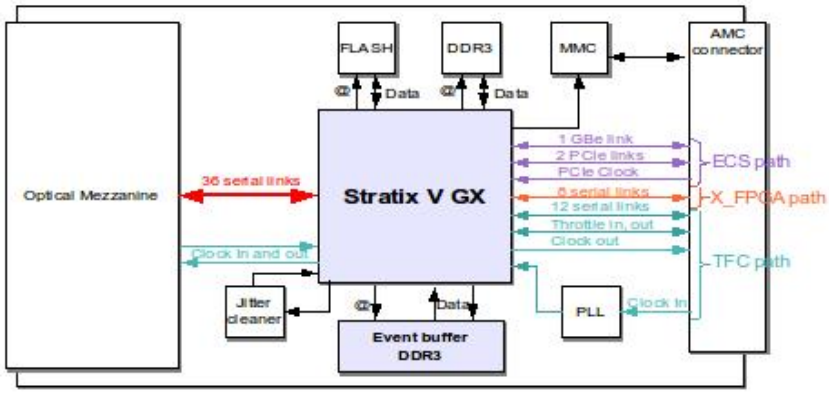


FCTS (D.Charlet)

- We propose to use uTCA standard for FCTS system.
- FCTS master board already exists: CCPM development; only the firmware needs to be developed by us.
- Due to the uTCA form factor there is not space enough to host optical mezzanine on board.
- **Decision concerning the link implementation has to be taken soon.**

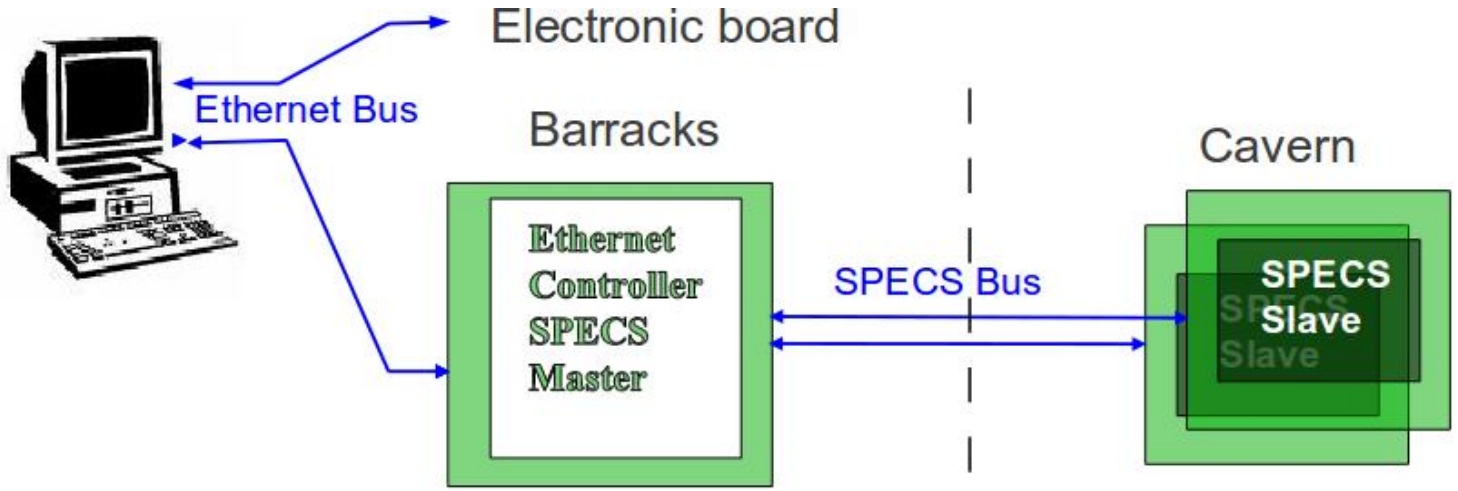
The design depend on this decision.

- Bi-directional links required between FCTS and front-end board electronics: clock and control distribution, handling throttle requests.
- Simulation have to be performed for latency evaluation.
- Choice of type of uTCA crate and number of crates have to be studied



- ECS board development for radiation environment.
  - ECS slave board functionalities match sub-detectors' requirements: it has already been confirmed during the CERN meeting in November.
  - We plan to check whether CAEN could produce and maintain the system (in long term).
  - FPGA Ethernet development is on way. TCP/IP and UDP protocol have been tested but data transmission rate remains limited with respect to 1 Gbit/s. We are working to increase this data rate.

- ECS off-detector:
  - Ethernet is the ECS standard (detector free development).



POWER SUPPLIES

- A new group, INFN Milano-Bicocca, lead by Gianluigi Pessina, is now in charge of the power supply system for the whole experiment.
- A study for a common strategy (for both LV and HV) has started.
- The first ongoing step is to collect the requirements from the different groups:

  ⇒ the questionnaire beside has been sent last week

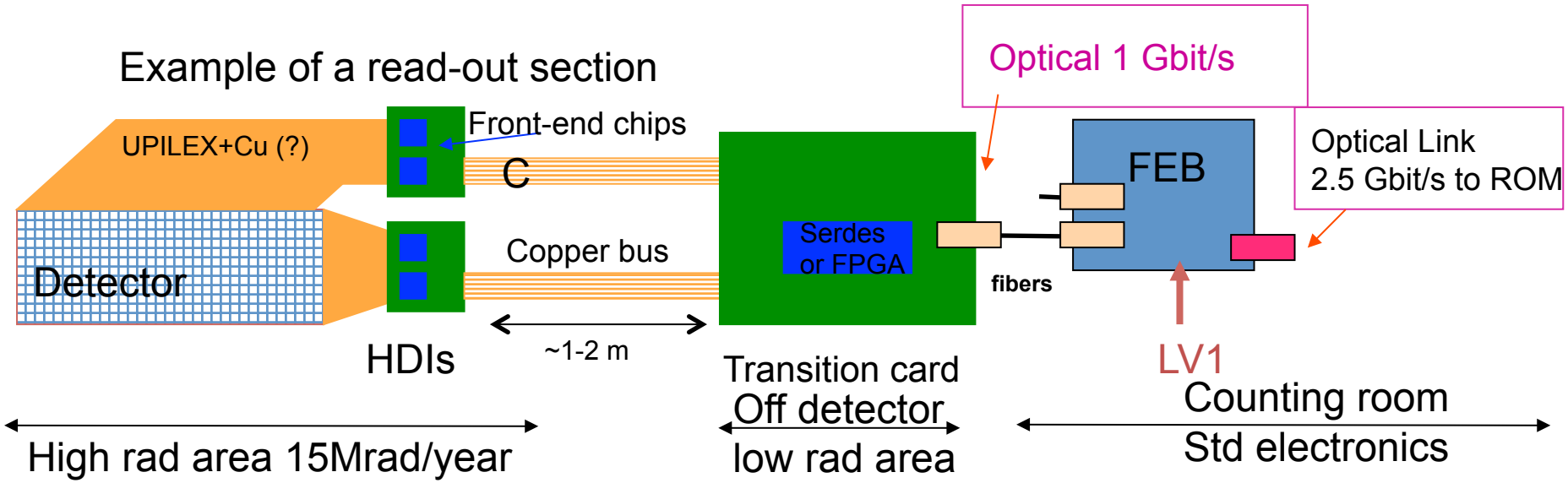
  ⇒ first feedback arrived this week

  ⇒ it will be refined on the basis of the remarks gotten during the sessions

DC/DC power Supply						
	V1	V2	V3	V4	V5	Comment, if any
Required Voltage level (V)						
Total power (W)						
Number of input connections/cables						
Current absorption per input cable						
Number of output connections/cables						
Current absorption per ouput cable						
Purpose (pre-regulation followed by linear regulator, final value, etc.)						
Power supply location (detector area, outside detecotr area)						
Maximum ripple (mV), or						
Maximum ripple (%)						

HV for detectors bias						
	V1	V2	V3	V4	V5	Comment, if any
Required Voltage level (V)						
Total power (W)						
Number of input connections/cables						
Number of output connections/cables						
Power supply location (detector area, outside detecotr area)						
pp noise (mV), or						
pp noise (%)						

SVT – Summary: DAQ readout chain (M. Villa)

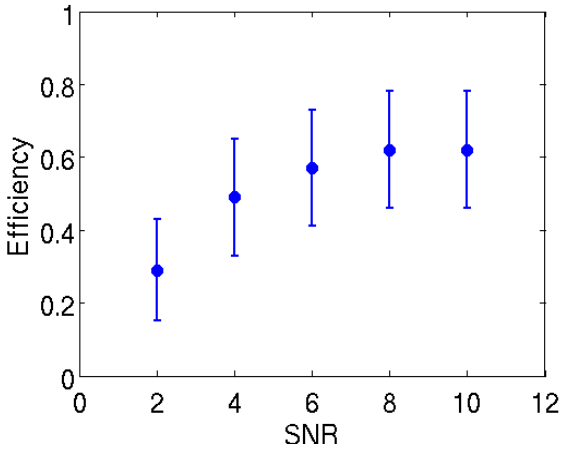


FE chip prototypes to be submitted in 2012 (in the design phase now)
Fan-Outs under design HDI card design is ongoing
Transition cards with open options: which optical link? Which serdes?
Rad-hard Ics to be tested FEB to be designed in 2012

DAQ Chain data & volumes:
240 Read-out sections; 172 1-Gbps optical link; 18 Front-end Boards
About 24 kB average event size (according to the last-1 MC simulations)

- *Design goals have been defined*

- *Two different implementation of dE/dx measurements have been evaluated and will be reported in TDR.*
  - *Truncated mean method has already been used by other experiments and, according to BaBar experience, should provide a σ_E around 7-8 %*
  - *Cluster Counting is under study and measurements both at LNF and TRIUMF are going on. Simulations using GARFIELD data have been carried out as well by using real preamplifier response convolution and different SNR.*



Impact parameter = 0 mm

% of Detected Cluster = (Rnc-Mnc)/Rnc *100

Rnc = Real Number of Clusters

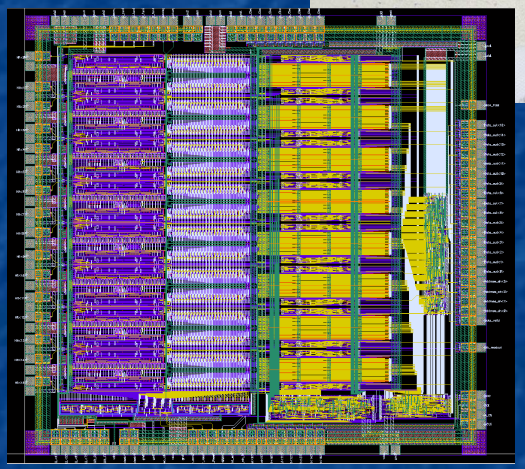
Mnc = Measured Number of Cluster after convolution and noise addition

Threshold = 1.5*σ

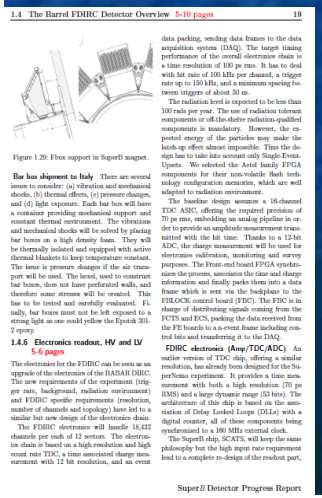
- *HV distribution system has been defined and modularity will be finalized as soon as chamber final design will be available. HV distribution boards should be located on FORWARD end-plate.*
- *On-Detector electronics (preamplifier boards) will be located on BACKWARD end-plate. We are investigating the possibility of exiting the cables from the outer layer of the chamber*
- *We are also investigating the possibility of using the top of the detector to locate off-detector electronics then simplifying setup and maintenance of the system*

PID

- FTOF : A 16-channel board and 4-channel daughter board based on 3.2GHz-1024 sample analog memory are under test . Preliminary results showed better than 10 ps resolution between channels and between boards in the CAEN desktop digitizer.
- Barrel. There were 4 presentations dedicated to the H8500 MaPMT tests with many very interesting results on cross talk, timing performances, He sensitivity and dyn12 triggering method.
- TDC chip arriving soon. Test board and module for CRT are under design. Policy for setup and test bench software has been agreed.
- A first version of the TDR has been presented. Integration and Power questionnaires are also ready.



SCATS TDC ~25 mm2



1.4 The Barrel FDIRC Detector Overview 5-10 pages 19

Figure 1.29: Fbox support in SuperB magnet.

Bar box shipment to Italy There are several issues to consider: (a) vibration and mechanical shocks, (b) thermal efforts, (c) pressure changes, and (d) light exposure. Each bar box will have a container providing mechanical support and constant thermal environment. The vibrations and mechanical shocks will be solved by placing bar boxes on a high density foam. They will be thermally isolated and equipped with active thermal blankets to keep temperature constant. The issue is pressure changes if the air transport will be used. The hotel, used to construct bar boxes, does not have perforated walls, and therefore some stresses will be created. This has to be tested and carefully evaluated. Finally, bar boxes must not be left exposed to a strong light as one could yellow the Epotek 301-2 epoxy.

1.4.6 Electronics readout, HV and LV 5-6 pages

The electronics for the FDIRC can be seen as an upgrade of the electronics of the BABAR DIRC. The new requirements of the experiment (trigger rate, background, radiation environment) and FDIRC specific requirements (resolution, number of channels and topology) have led to a similar but new design of the electronics chain.

The FDIRC electronics will handle 18,432 channels per each of 12 sectors. The electronics chain is based on a high resolution and high count rate TDC, a time associated charge measurement with 12 bit resolution, and an event data packing, sending data frames to the data acquisition system (DAQ). The target timing performance of the overall electronics chain is a time resolution of 100 ps rms. It has to deal with hit rate of 100 kHz per channel, a trigger rate up to 150 kHz, and a minimum spacing between triggers of about 30 ns.

The radiation level is expected to be less than 100 rads per year. The use of radiation tolerant components or off-the-shelve radiation-qualified components is mandatory. However, the expected energy of the particles may make the latch-up effect almost impossible. Thus the design has to take into account only Single-Event-Upsets. We selected the Actel family FPGA components for their non-volatile flash technology configuration memories, which are well adapted to radiation environment.

The baseline design assumes a 16-channel TDC ASIC, offering the required precision of 70 ps rms, embedding an analog pipeline in order to provide an amplitude measurement transmitted with the hit time. Thanks to a 12-bit ADC, the charge measurement will be used for electronics calibration, monitoring and survey purposes. The Front-end board FPGA synchronizes the process, associates the time and charge information and finally packs them into a data frame which is sent via the backplane to the FILOCK control board (FBC). The FBC is in charge of distributing signals coming from the FCTS and ECS, packing the data received from the FE boards to a n-event frame including control bits and transferring it to the DAQ.

FDIRC electronics (Amp/TDC/ADC) An earlier version of TDC chip, offering a similar resolution, has already been designed for the SuperNemo experiment. It provides a time measurement with both a high resolution (70 ps RMS) and a large dynamic range (32 bits). The architecture of this chip is based on the association of Delay Locked Loops (DLLs) with a digital counter, all of these components being synchronized to a 160 MHz external clock.

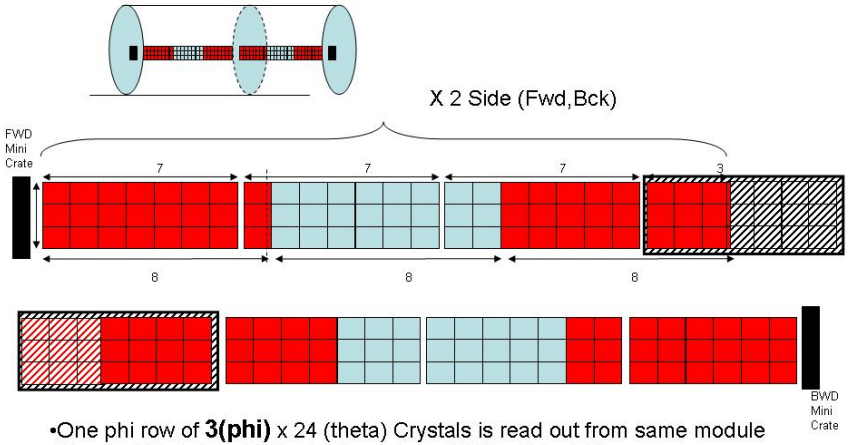
The SuperB chip, SCATS, will keep the same philosophy but the high input rate requirement lead to a complete re-design of the readout part,

SuperB Detector Progress Report

- A base line design has been chosen for the global architecture.
- We are pretty confident about the different elements of the electronics chain including the integration inside the shield.
- More iteration on the coupling between PM and Front end electronics is necessary including optical coupling, mechanics cooling and power issues but collaboration is well on tracks.

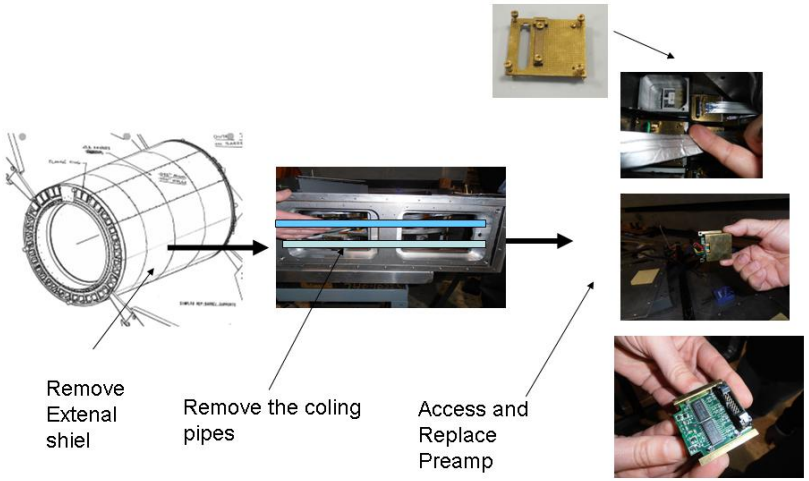
EMC Calorimeter

EMC Barrel readout granularity



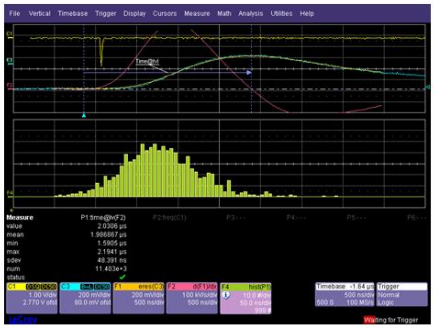
- One phi row of **3(phi)** x 24 (theta) Crystals is read out from same module
- Physical Module = 3 * 7 =21 Crystals and 3*6 =18 last bkw
- Trigger Tower =3*8=24 Crystals in Babar →proposed 3*4=12 in SuperB
- One optical fiber for two trigger module (3 optical fiber)

Way to replace Preamps



Crystals Test Box

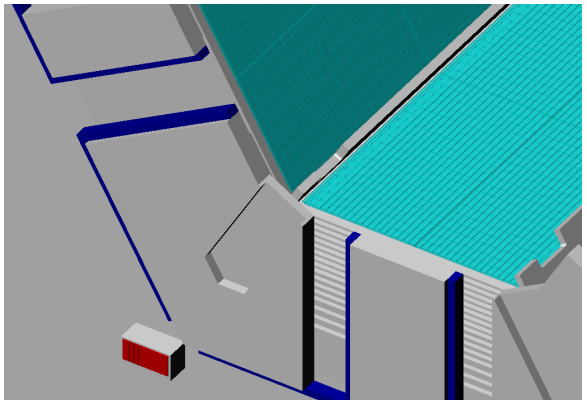
Time jitter of the APD signals from CsI(Tl) crystal



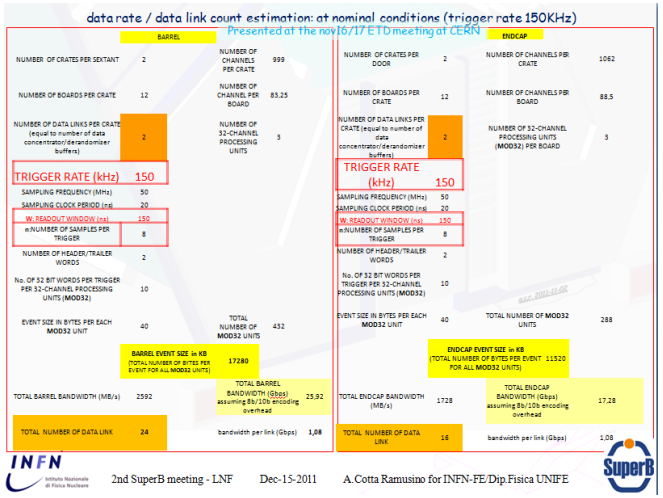
1) Signal from external scintillator (PM readout)
2) Signal from CsI(Tl) (PM readout)
3) Signal froma CsI(Tl) (APD readout)
4) DSP d(apd)/dt to found the maximum
5) Jitter measurements 48 ns RMS

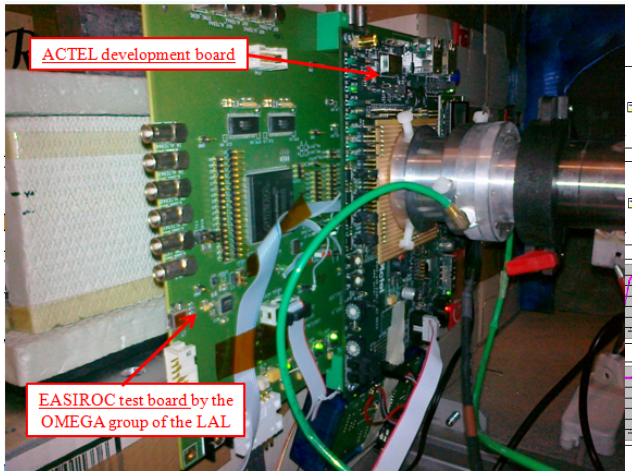
SuperB IFR electronics update: summary slide

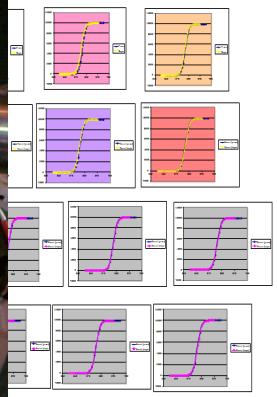
- the current baseline design for the IFR detector and electronics has been presented, with some detail, at this meeting



- the current estimates of DAQ related quantities (number of channels, data bandwidth, event size) have been given for the IFR detector according to the premises outlined at the previous point







- the results of neutron irradiation tests of an FPGA and an ASIC (possible candidate as building block of the front end electronics for the IFR) at the INFN-Laboratori di Legnaro CN accelerator have been presented

- the second draft of the replies to the integration questionnaire has been prepared and it has been summarily described
- the replies to the power supplies questionnaire have been prepared and summarily described

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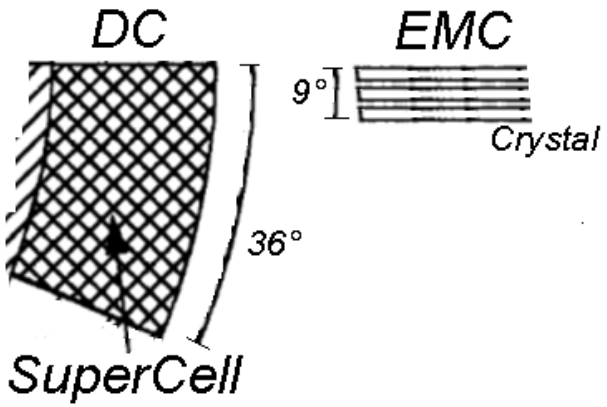
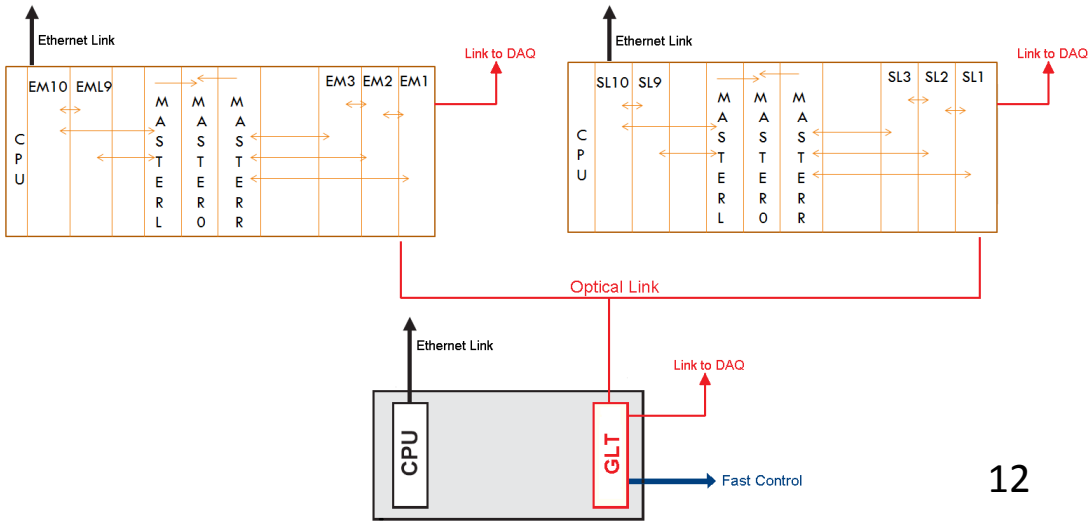
TRIGGER

The minimum distance between triggers is ~50ns.
This requirement pushes for a very good
trigger time resolution that it should be reachable.



There are several mechanical constraints from barrel EMC, inducing a 9 degree modularity for the EMC (3 crystals in ϕ). The ϕ at the calorimeter covered by each card reading the DC had better match with the calorimeter ϕ granularity. 48 channels reading a supercell would imply a coverage of 36 degrees.

DC and EMC trigger crates have a common interface (LVDS or optical) with pertaining sub-detectors. EMC (i) and DC(i) boards share a common HV platform and only differ in firmware.



Conclusion

- During all ETD sessions, we could notice that the designs really got refined in view of the TDR:
    - the CERN meeting from November was very useful to this end

- Main source of worry the pin diodes of the EMC, which do not seem to be sufficiently performing, both for energy resolution and trigger time precision.

- The writing of the TDR ETD sections in ongoing.
    - In some cases (like barrel PID), a draft is already available
    - The answers to the integration questionnaire are almost ready and should be sent very soon

- We now have a responsible for power supplies (LV & HV):
    - He will take care of these elements for the whole experiment
    - The goal is to standardize the supply system as much as possible
    - A power supply dedicated questionnaire has been sent last week