



SuperB Timing Specification

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2nd SuperB Collaboration Meeting

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Preliminary Consideration

This talk tries only to start a partial analysis of the problems connected to the Superb timing system specification.

The real design and implementation could be implemented by technologies to be evaluated and that will be studied more in depth in the following talk by Marco Bellato.



A starting
point for discussion
can be the last
version of CDR

Looking in particular
at the par. 12.6,
a list of requested
items are described
for the Timing
System
specification

Super*B* **Progress Report**

The Collider

<http://agenda.infn.it/conferenceDisplay.py?confId=3828>

<http://arxiv.org/abs/1009.6178v3>

12.6 Synchronization and timing

The goal of the synchronization and timing system is to assure that all the RF systems and the other timed devices will be able to work with signal and frequencies locked in phase within the ranges defined by the specifications. A master sinusoidal oscillator at the RF frequency (476 MHz) including a phase continuity feature must be considered, and it must be able to provide a 10^{-11} short term stability. Small change of frequency in a range <100 KHz (by steps of 1 or 5 kHz) must be accepted without loose of signal phase. The distribution of the RF main signal must be assured with a peak-peak jitter < 0.5 ps. Very low jitter phase shifters must be implemented to synchronize, separately for each ring, beam collisions and bunch injections. The synchronization and timing system must also provide sinusoidal frequencies for the LINAC cavities, typically 6 and/or 12 times the main RF sinusoidal signal. Generation of other $(m/n)*\text{RF}$ frequencies, with m and n integer, could be considered if necessary. The utmost peak-peak jitter for these devices can be within 2 ps. The injection triggers have to be locked to the main RF frequency and to the 50 Hz of the main power supplies. Diagnostics and injection triggers must include at least the “Fiducial” (a reference revolution frequency given by main RF frequency divided by the harmonic number) and bunch number triggers, all locked in phase with the RF main frequency within a 2 ps peak-peak jitter.

Timing possible main blocks

- 1) Master RF oscillator (fixed reference)
- 2) HER main ring triggers, linked to HER radio frequency phase shifter and every bucket must be labeled with a number (from 1 to harmonic number)
- 3) LER main ring (linked to HER radio frequency phase shifter+bucket label): both MR phase shifters must obey to control room “manual shift” operations or to the luminosity feedback (automatic shift)
- 4) 50 Hz frequency from main power supplies (by a PLL)
- 5) HER injector must inject in the “right” bucket, the bunch that in every second has less current between those included in the bunch pattern chosen for collision
- 6) LER injector as the previous 5)

A first example: clock & triggers for bunch-by-bunch feedback systems / 1

- sampling clock 476 or 238 MHz locked to the radio-frequency of the ring (LER, HER, DR), max peak-peak jitter (or dephasing): 2ps
- injection trigger of the ring (LER, HER, DR)
- fiducial (= revolution frequency)
- electrical levels:
 - ac 7-10 dBm for sampling clock
 - NIM levels for the other triggers

A first example: clock & triggers for bunch-by-bunch feedback systems / 2

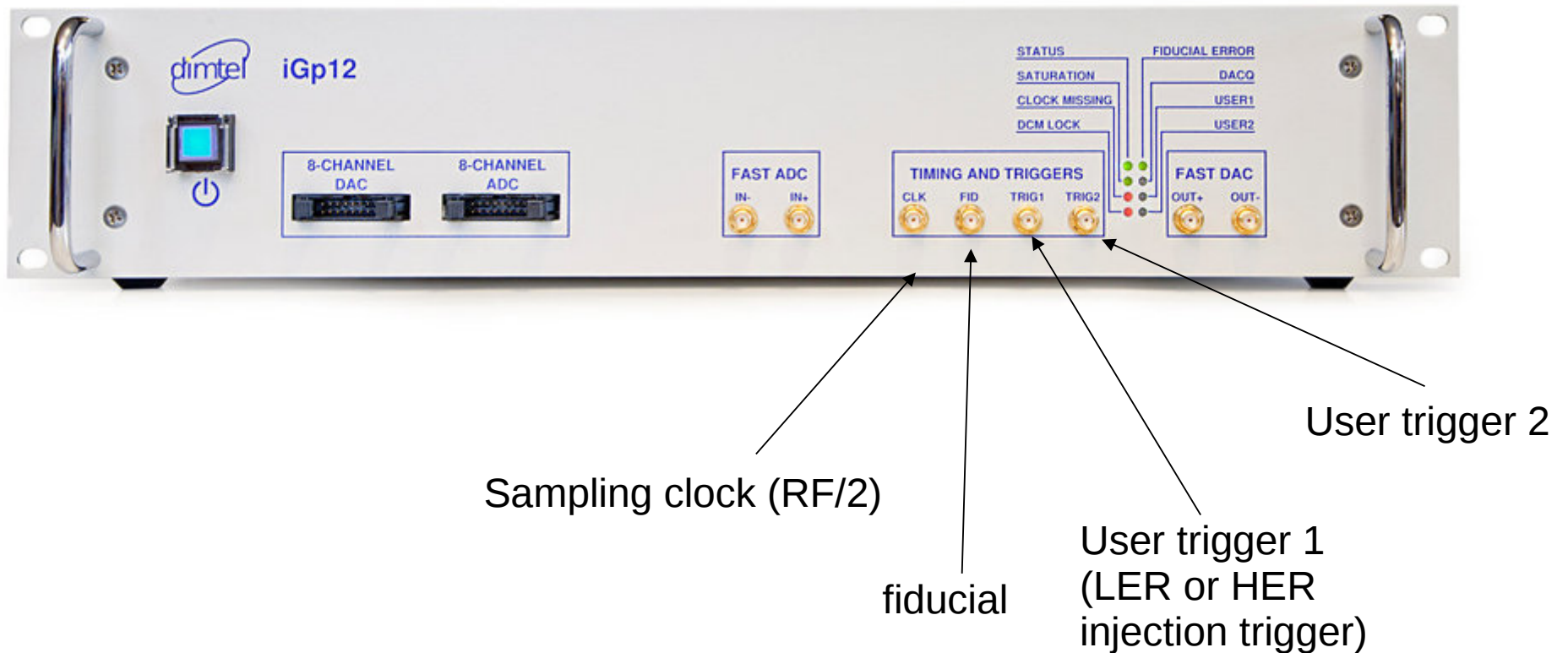
The screenshot shows the 'iGp12: Control Panel' window. The title bar includes 'ID=IGPF:VerPos', 'HELP', and 'EXIT' buttons. The interface is divided into several sections:

- FEEDBACK SETTINGS:** Includes 'COEFFICIENT SET' (Set 0), 'SHIFT GAIN' (1), 'DOWNSAMPLING' (1), and 'SAT. THRESHOLD' (20.00 %).
- DATA ACQUISITION:** Includes 'GROW/DAMP ENABLE' (OFF), 'REC. DOWNSAMPLE' (1), 'RECORD LENGTH' (10.0 ms), 'GROW LENGTH' (1.0 ms), and 'HOLD-OFF' (0.0 ms).
- TRIGGER:** Includes 'INT' and 'EXT' buttons, 'TRIG1' and 'TRIG2' buttons, 'Acquire' (OFF), 'Arm' (OFF), 'Auto re-arm' (OFF), and an 'ARM' button (red text).
- ACQ MEMORY:** Includes 'BLOCK', 'SRAM', and 'MEMORY' (read) buttons.
- STATUS:** Includes 'Clock missing' (0), 'DCM1 unlocked' (0), 'DCM2 unlocked' (0), 'FIR saturation' (0), 'Fiducial error' (0), 'Interval (sec)' (14), and a 'COUNT' button.

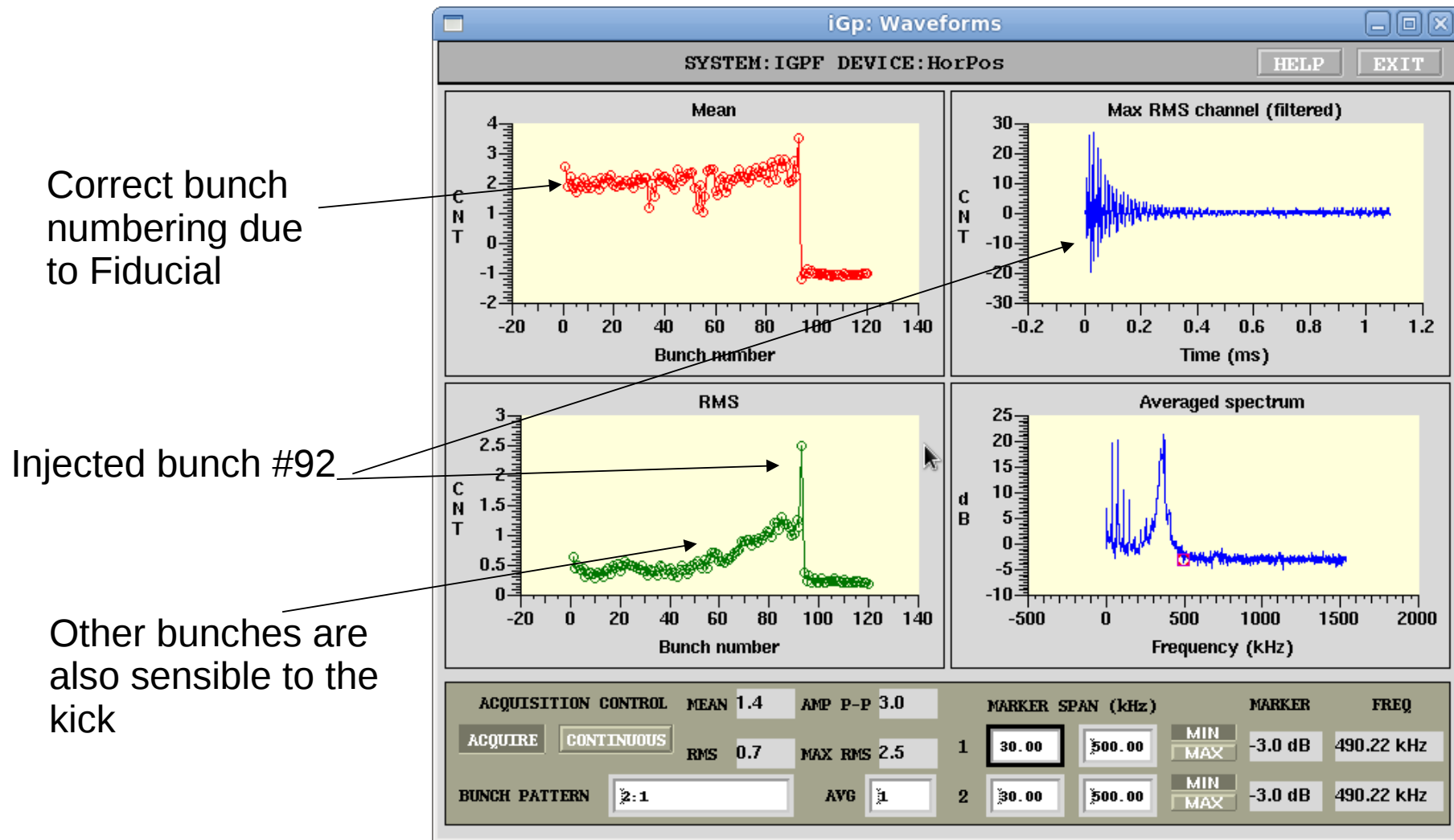
Annotations with arrows point to specific elements:

- 'Internal or external trigger' points to the 'DOWNSAMPLING' field.
- 'External trigger1 or trigger 2' points to the 'TRIG1' and 'TRIG2' buttons.
- 'RF clock check' points to the 'Clock missing' status indicator.
- 'Fiducial trigger check by a comparison with RF clock' points to the 'Fiducial error' status indicator.

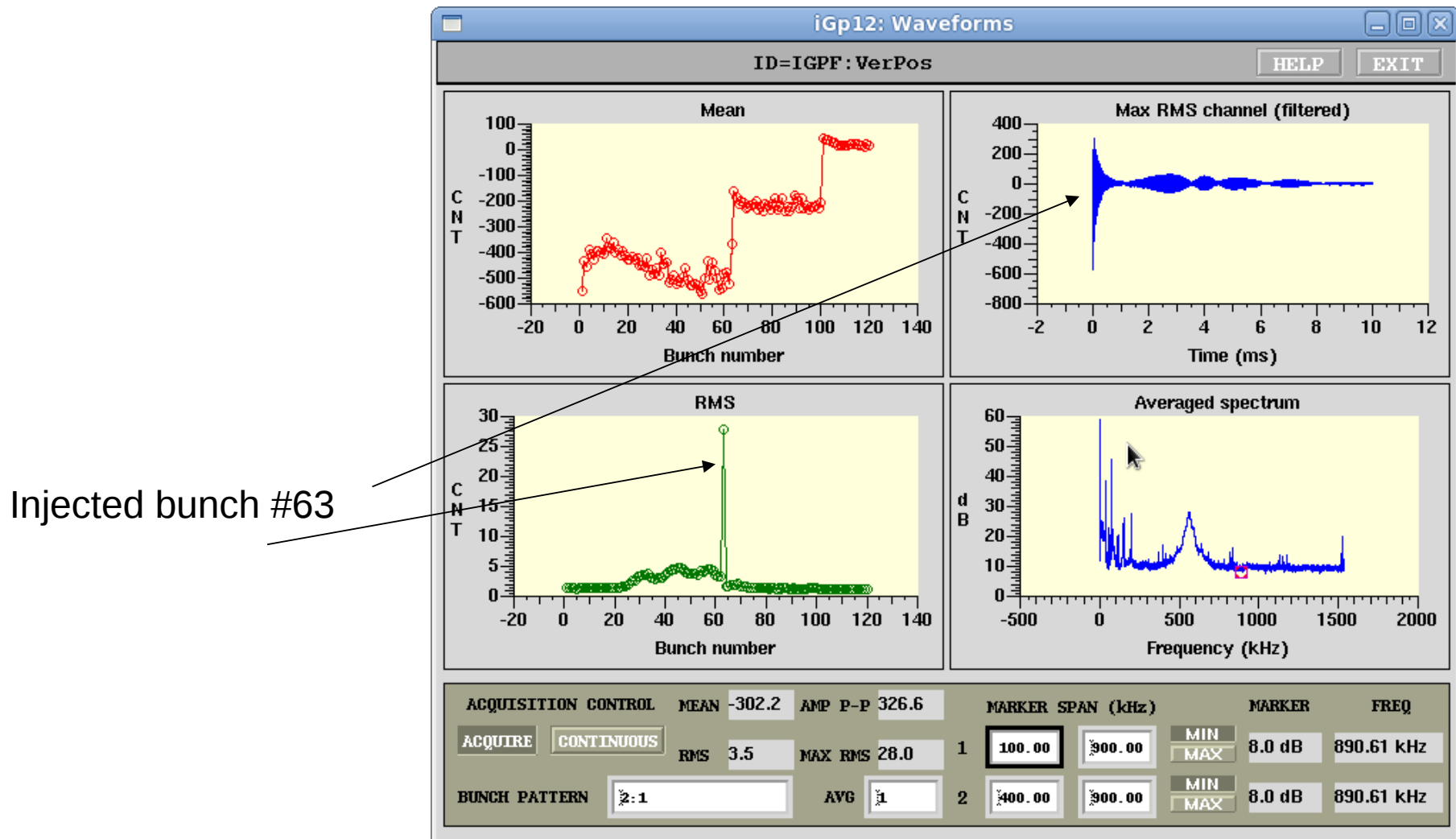
A first example: clock & triggers for bunch-by-bunch feedback systems / 3



Effect of injection kicker on the horizontal plane: data taken by using the injection trigger for diagnostics



We can see also an effect on the vertical planes !!!
also these data taken by using the injection trigger
for diagnostics



Fiducial

Fiducial must be generated dividing RF by the harmonic number.

Fiducial phase is fixed and cannot be modified.

It is a fundamental frequency to lock the bucket numbers for both main rings, considering that (of course) LER bunch number 1 must collide with HER bunch number 1.

All the bucket counters must obey to the fiducial signal, typically a ~ 20 ns pulse that in many accelerators has NIM levels.

Fiducial

Question :

- Fiducial should be locked to one of the two rings radiofrequency or to the master oscillator ?

Taking in mind as example the DAFNE Timing :

- 1) one master RF generator at Main Ring frequency (i.e. $\sim 476\text{MHz}$)
- 2) Main Ring clocks for distribution to diagnostics locked with radio-frequency phase shifters
- 3) gun + linac + damping ring + kicker must be also synchronized with the bunch that have to be injected in the selected main ring
- 4) machine state word at 50 Hz (SuperB 200Hz ?):
 - DAFNE ==> 32 bit
 - SuperB ==> 256 or 512 bit
- 5) bunch-by-bunch current monitor for both MR

Taking in mind DAFNE Timing:

Machine State Word at 50 Hz (SuperB \geq 200 Hz ?):

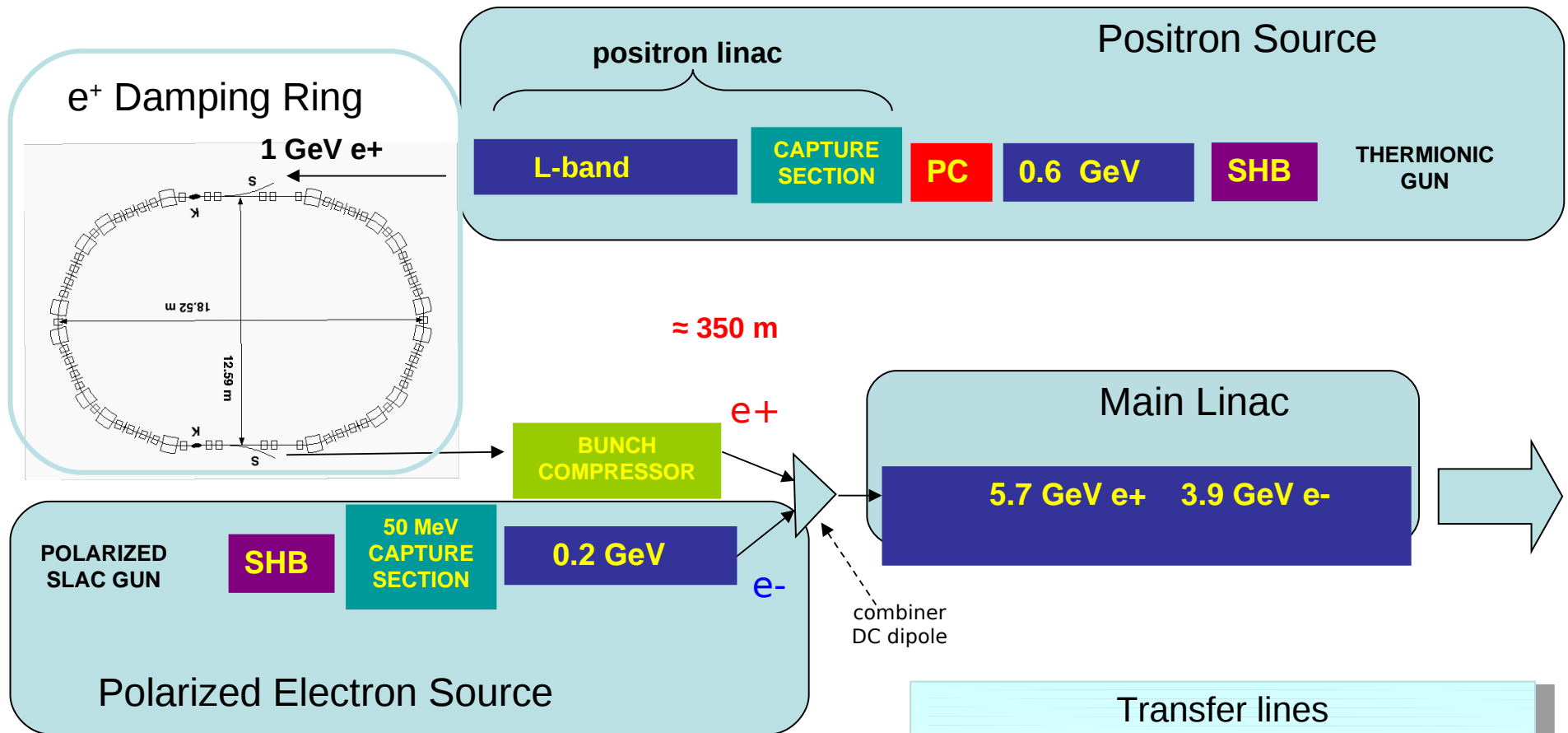
DAFNE \Rightarrow 32 bit (in reality 31 bit + 1 bit toggle)

SuperB \Rightarrow 256 or 512 bit

- 32 bit time stamp
- 16 bit LER bunch # to be injected
- 16 bit LER bunch # selected for diagnostics
- 16 bit HER bunch # to be injected
- 16 bit HER bunch # selected for diagnostics
- 32 bit Linac
- 32 bit damping ring including 16 bit bucket #
- 32 transfer lines
- 4 bit toggle
- Other bits: reserved for future upgrading

Injection system layout

From Guiducci's talk



Details:

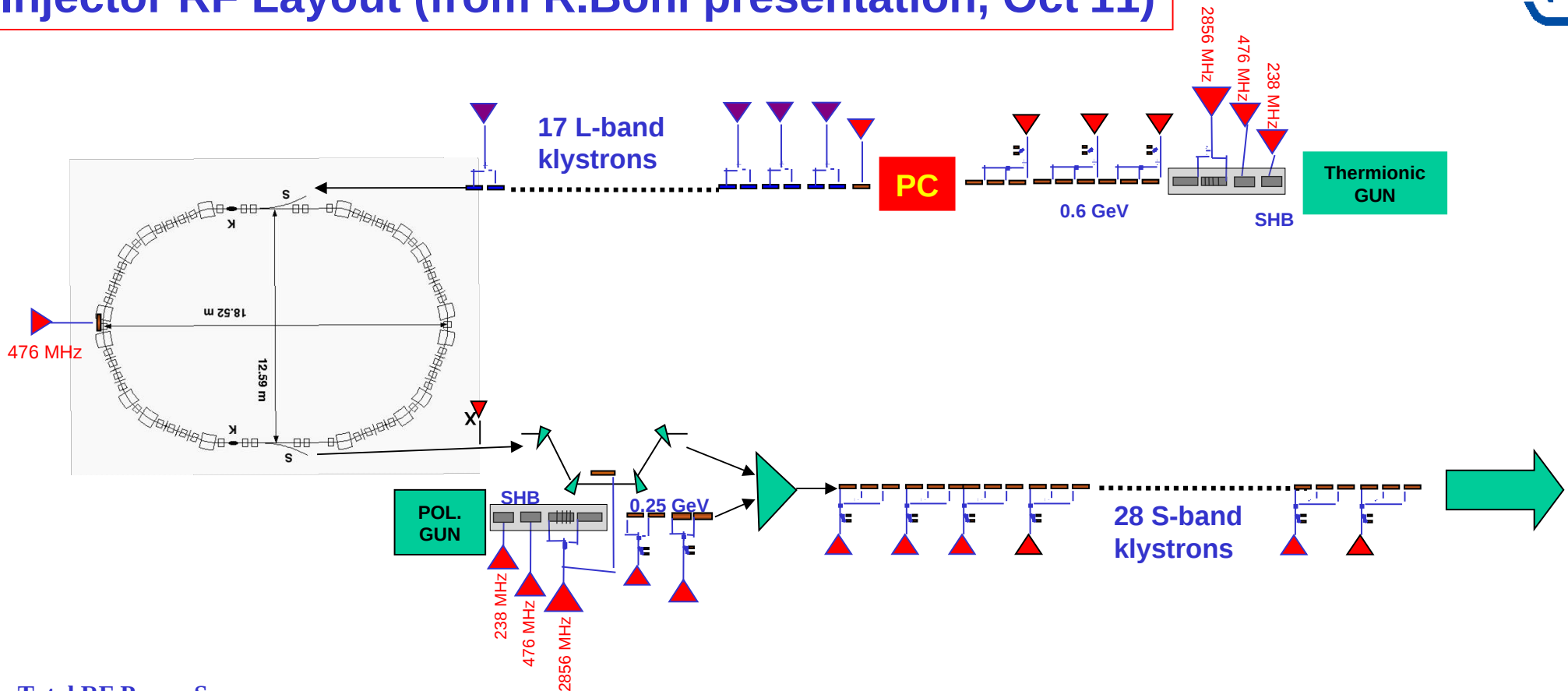
"SuperB Progress Reports - Accelerator", (Dec. 2010) - Chapter 15 <http://arxiv.org/abs/1009.6178v3>.

"Updated Design of the Italian SuperB Factory Injection System", IPAC'11

Transfer lines

- Positron Source to Damping Ring
- Damping Ring to Main Linac
- Electron Source to Main Linac
- Main Linac to HER
- Main Linac to LER

Injector RF Layout (from R.Boni presentation, Oct'11)



Total RF Power Sources

S-band 36

L-band 17

UHF 5

X-band 1

Things are even more complicated !!!
Many frequencies have to be generated
(synchronously)

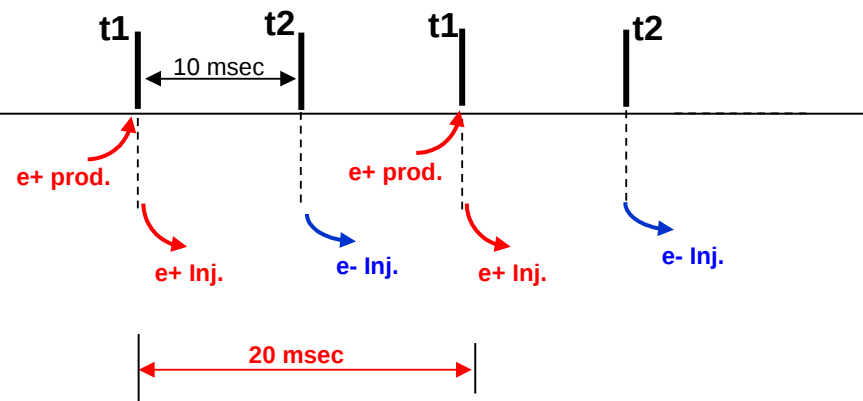
TL Synch. or timed device list

- e- Linac gun (50Hz synchronized to MR bucket #)
- e- Linac radiofrequency (2854MHz=476 x 6 MHz)
- e- damping ring (476 MHz)
- Damping ring injection and extraction kickers (2+2 ?)
- Common (e+/e-) linac @ 2856MHz
- Polarized gun → laser : (50 Hz synchronized to MR bucket #)

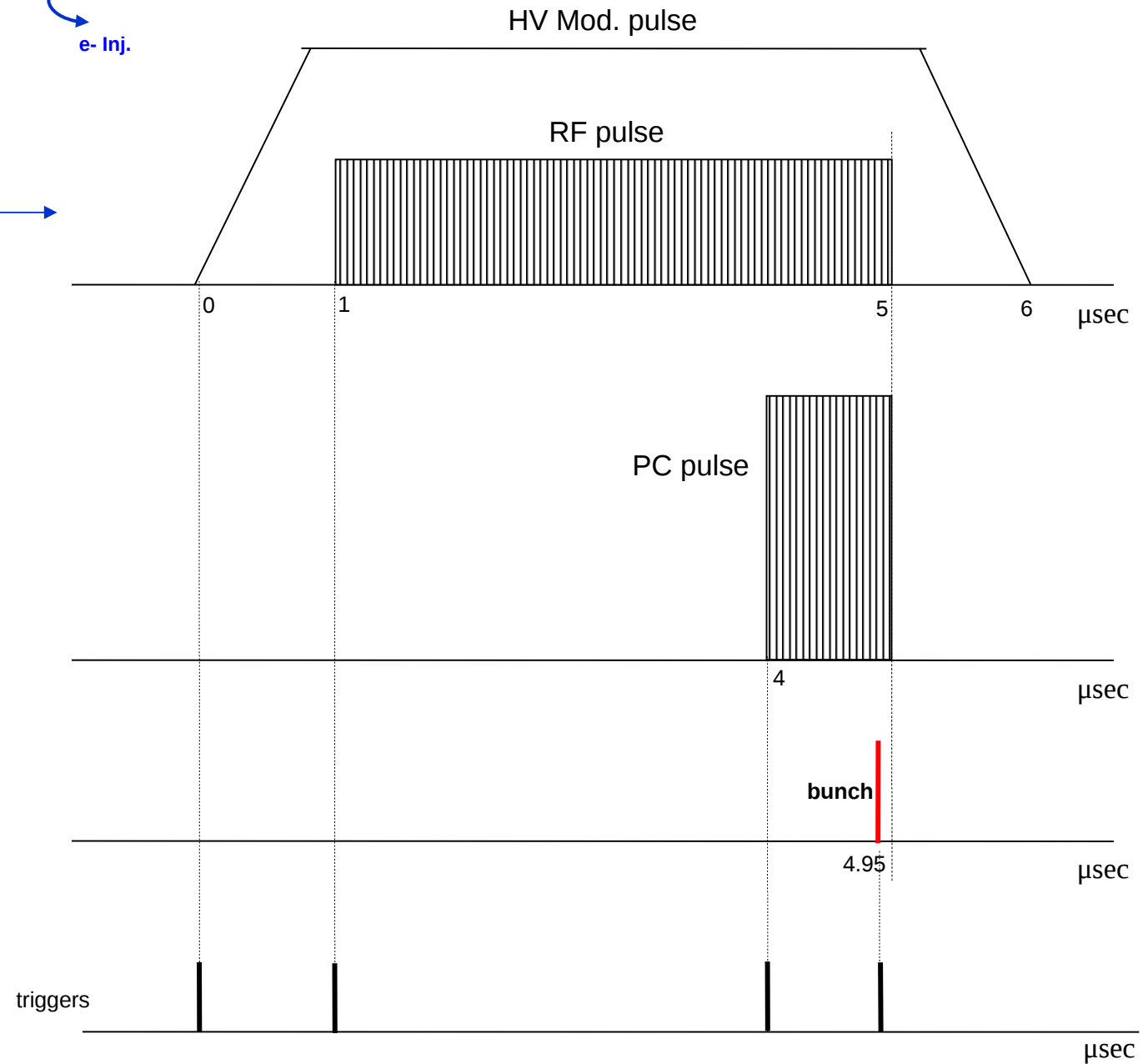
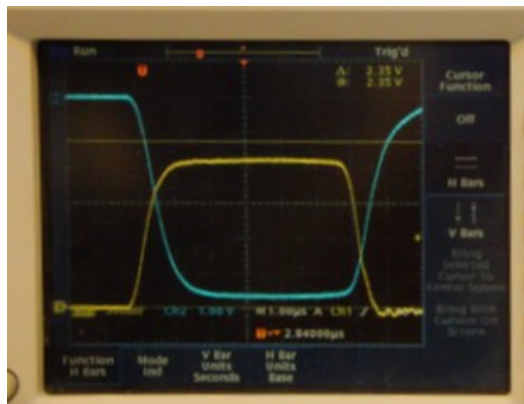
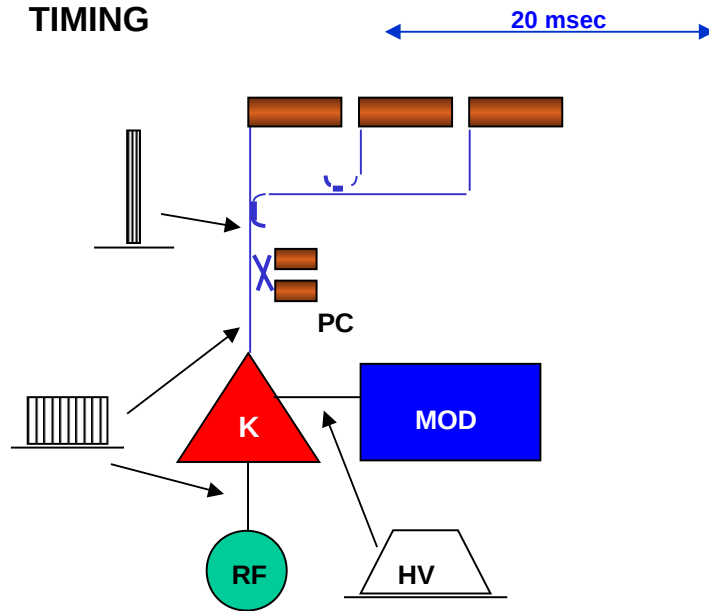
Damping ring

We suppose that the damping ring RF frequency and plant shall be the identical to the main ring RF systems.

This means that the DR frequency signal should not need to be shifted following the bucket # phase shifting but it should have just a dedicated rf phase shifter to be adapted to the “right” phase to accept the bunches coming from the linac.



TIMING



Diagnostics

SuperB need timed main ring diagnostics and transfer line diagnostics.

Main rings diagnostics could ask for RF/2, RF/4, RF/6, RF/h or other frequencies locked to each main ring as well “RF/h + selected bunch phase advance”.

RF x n/m (n and m integer) frequencies are also necessary for Linac, diagnostics and feedback systems.

Signal versus jitter list

Gun	2ps rms	50 Hz synch bucket #
Kickers	1ns peak-peak	50 Hz synch bucket #
RF modulators	100 ns peak-peak	
Laser	2ps rms	50 Hz synch bucket #
MR feedback	1ps peak-peak	RF
Sampler(s)	1ps peak-peak	RF
MR triggers	2 ps rms	fiducial+bucket #
Fiducial	2 ps rms	RF/harmonic number
Gated camera	.5 ns	depending on the experiment
Streak camera	.1 ns	depending on the experiment

Dear participant/speaker of the SuperB meeting, in view of the planning of work needed for the TDR, we'd like to ask you to answer in your talk as much as possible to the following questions:

- (1) Clear list of the describing system components.
- (2) Is the system ready to start the technical design?
- (3) If "not", what kind of activity (calculation, simulation, etc.) should be done before? Please estimate time, specialists and schedule necessary for that.
- (4) If "yes", could you estimate manpower (engineers, designers, etc.) and time schedule for the technical design?
- (5) What are according to you the critical points, which may influence performances of the system?
- (6) What kind of prototyping work should be done before the mass production? Time schedule for that?
- (7) Rough estimate of resources and time schedule for the whole system manufacture.

We will have a dedicated session on Thursday 15th at 5pm to discuss in detail all these plans, so those of you attending but not giving a talk will have a chance to participate and contribute actively.

Thank you very much for your collaboration!

We are looking forward to meet you in Frascati.

Best regards

Eugene Levichev and Marica Biagini

Many questions from project management to be carefully evaluated...
in base at what we mean for TDR:
just a “brief” description of the goals and strategies of each subsystem
or a true detailed technical design that looks adequate budget ?

Conclusion

The timing system should have a flexible design to be able to solve foreseen and also not foreseen technical problems.

Signal distribution must assure to maintain jitter levels.

To start a real TDR phase more information on specification are necessary.