Timing Studies for SuperB

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2nd Collaboration Meeting
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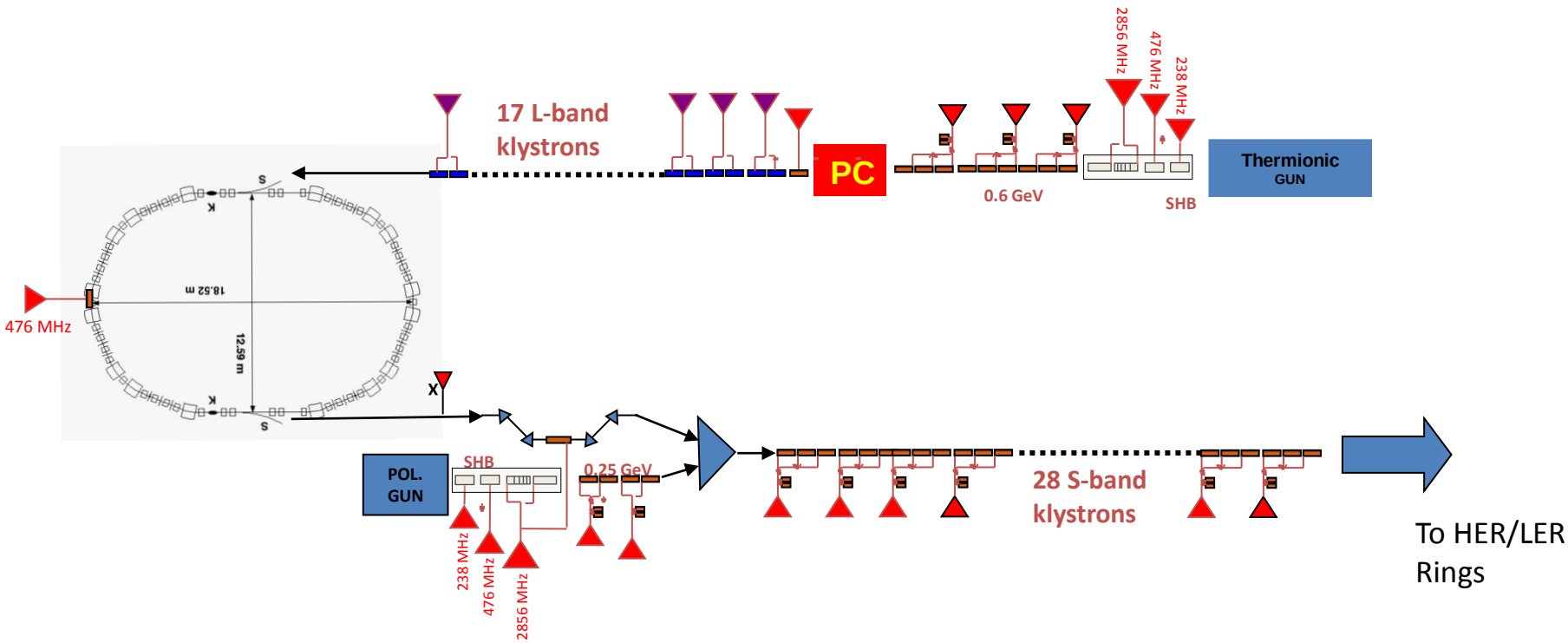
SuperB Schematic View (Injector)



Timing and Synchronization Definitions

- Accelerator Timing
  - Eg. : triggers for acceleration & diagnostics
  - ‘Triggers’ are signals from the timing system used by hardware to accelerate & measure the beam
- Synchronization
  - 476 MHz RF phase reference distribution (Master Local Oscillator)
    - 2856 MHz and fractional frequencies derived from MLO
    - 500 fs p-p jitter max. (source: SuperB Progress Report)

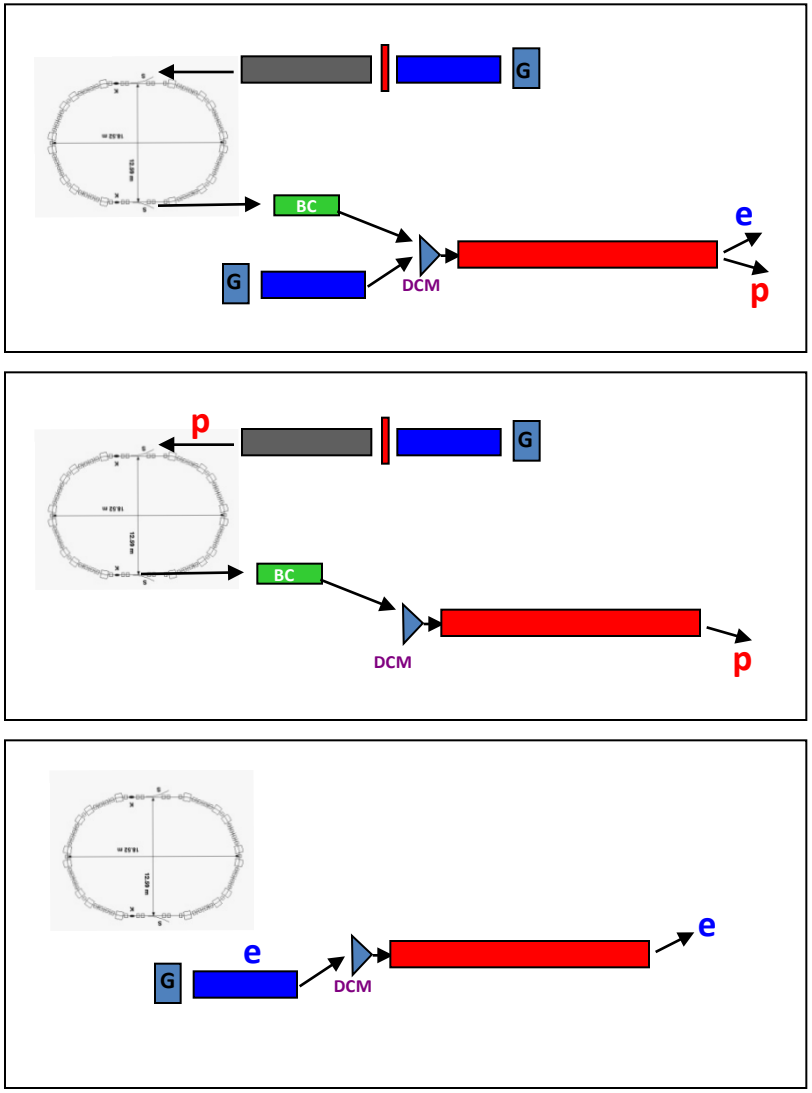
Timing and Synchronization Domains

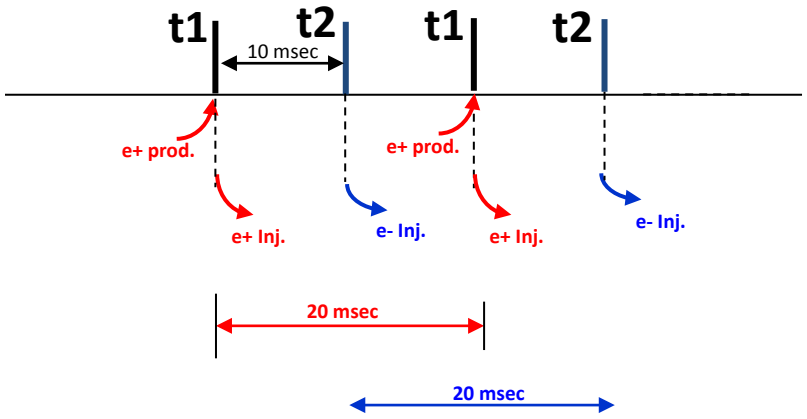
- 20ms - Pulse-to-pulse, Beam mode flavors
- us - pulsed power supplies
- ns - Shape of pulses for pulsed microwave
- ps - Beam timing, instrumentation
- fs - Microwave phases

Timing Performance Requirements

Parameter	Value
Maximum trigger rate	100 Hz (50Hz overlapped op. for e^+ / e^-)
Min trigger duration	420 ps
Clock Frequency	476 MHz
Lock-in Bandwidth	+/- 50 KHz
Delay coarse step size	2.1 ns
Delay fine step size	5 ps
Delay range	> 1 s
Max timing jitter w.r.t clock	2 ps rms
Long term stability	< 10 ps
Signal level	NIM, CML, TTL

Injector operation

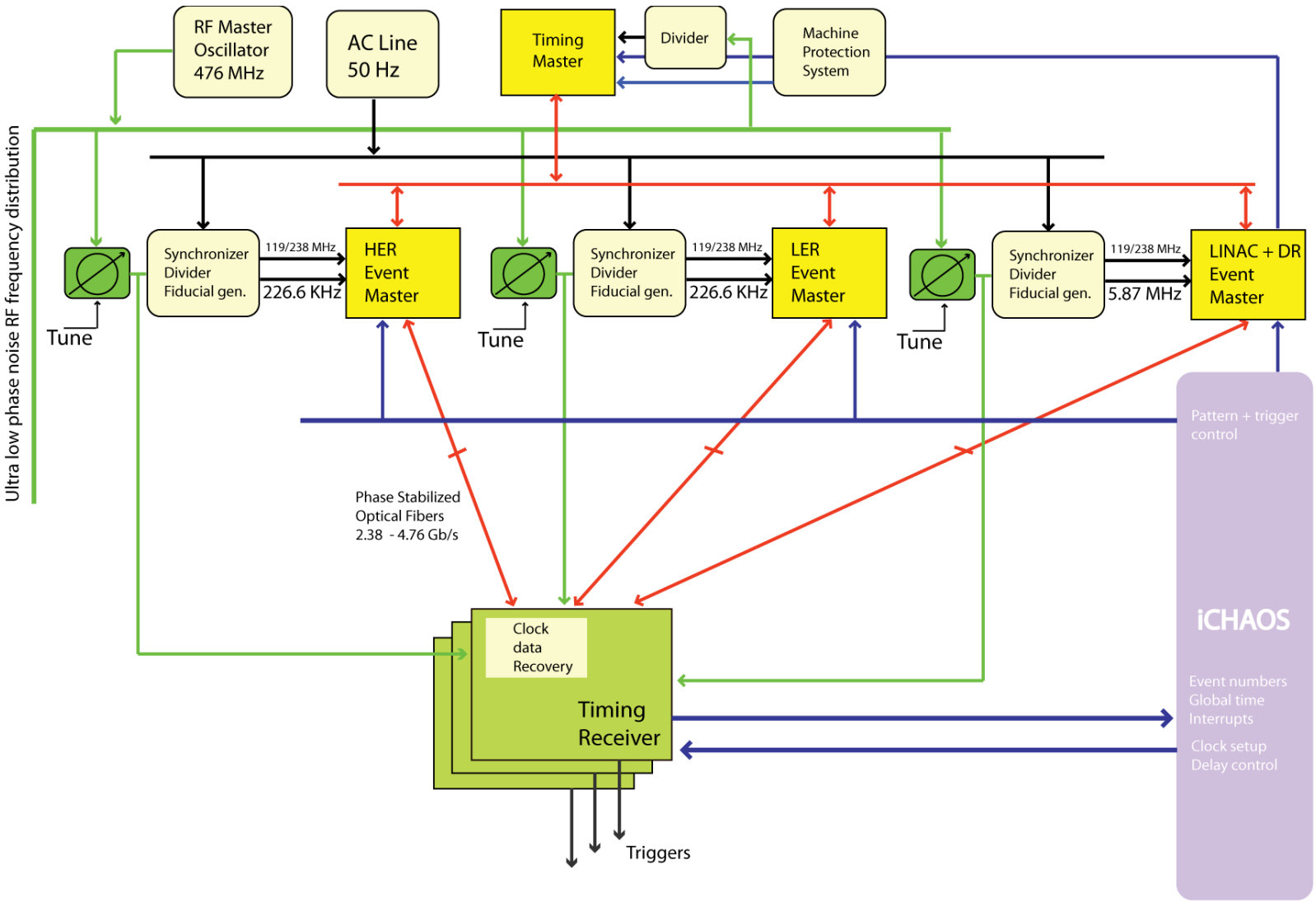




Timing system functional requirements

- Coordinate operation of
  - HER/LER injection
  - e- / e+ (with DR) extraction
  - Bucket selection
  - Guns & pulsed magnets triggering
  - Diagnostic measurements
  - LLRF triggers and delays
- Potentially hundreds of parameters to be switched within 10 ms

Timing system block diagram

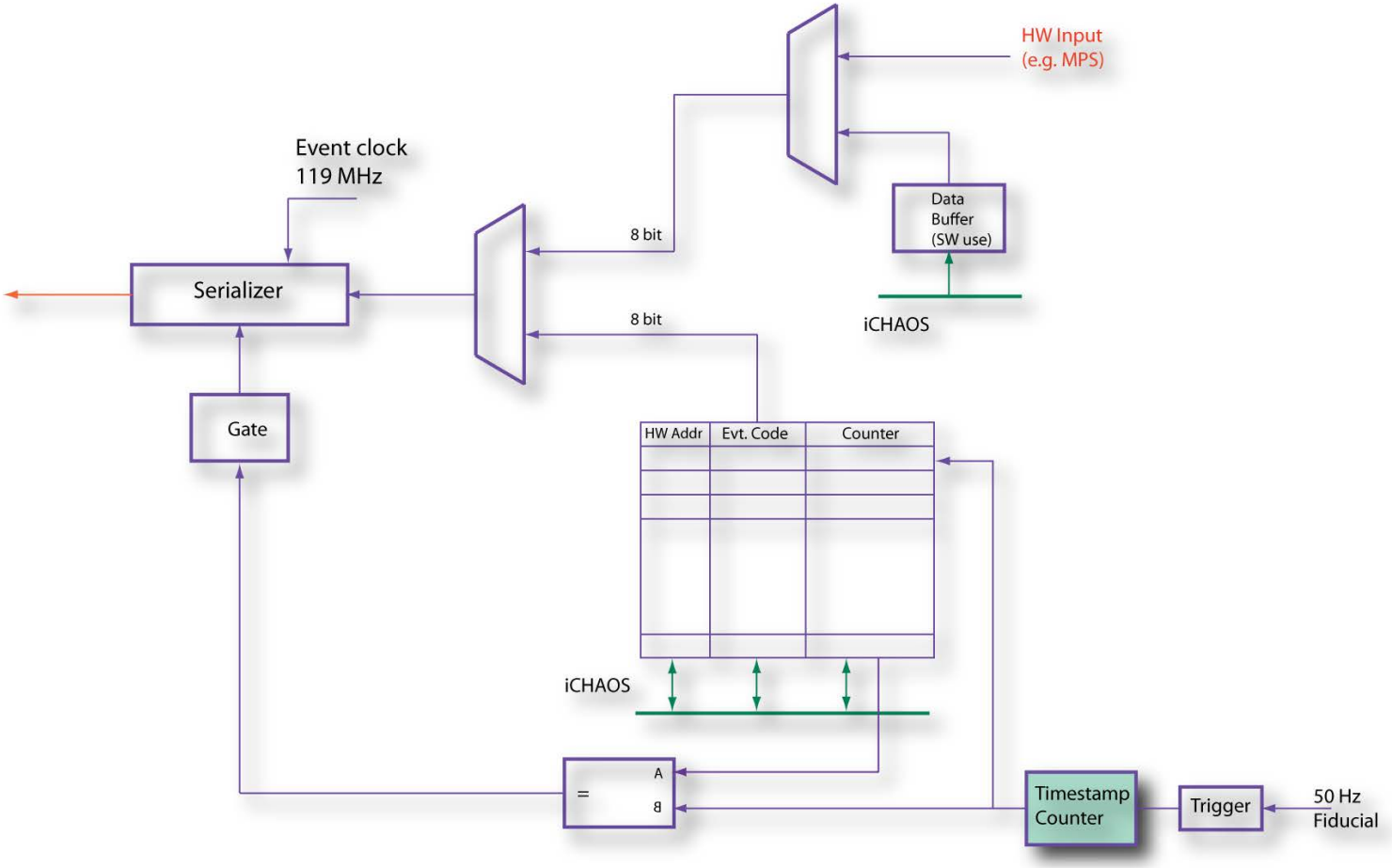


Event based timing system

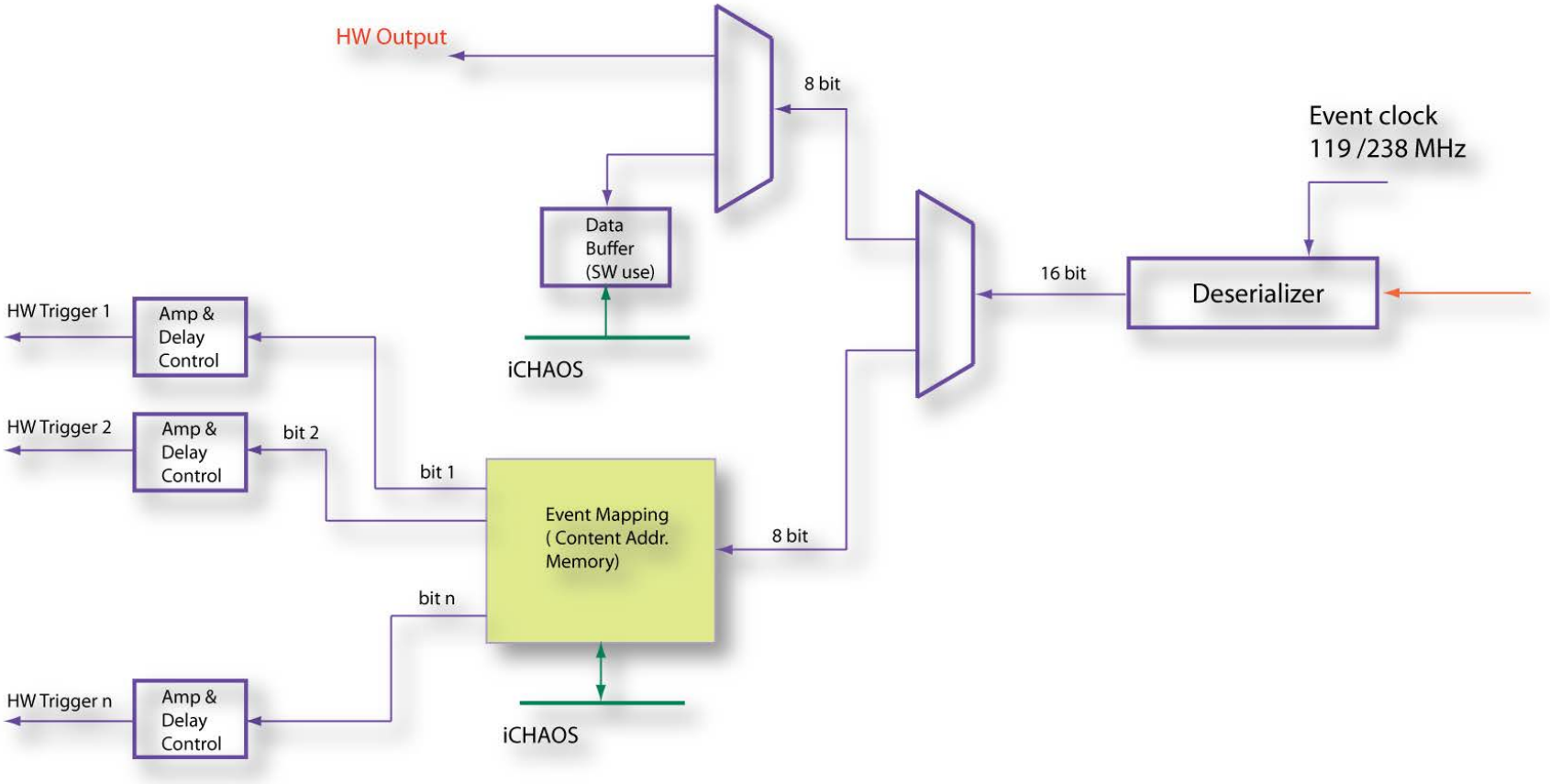
- Tree-like structure
- Interconnect via high speed serial transceivers at 2.38/4.76 Gb/s and single mode fibers
- All timing functions in FPGA
- 16bit word of time code + trigger info at 119/238 MHz between master and all receivers
- Enough bandwidth to close loops between receivers and master (e.g. automatic luminosity feedback*)
- Embedded microprocessor can host iCHAOS interface

***A PROPOSED FAST LUMINOSITY FEEDBACK FOR THE SUPER-B ACCELERATOR**
Kirk Bertsche et al, 2009

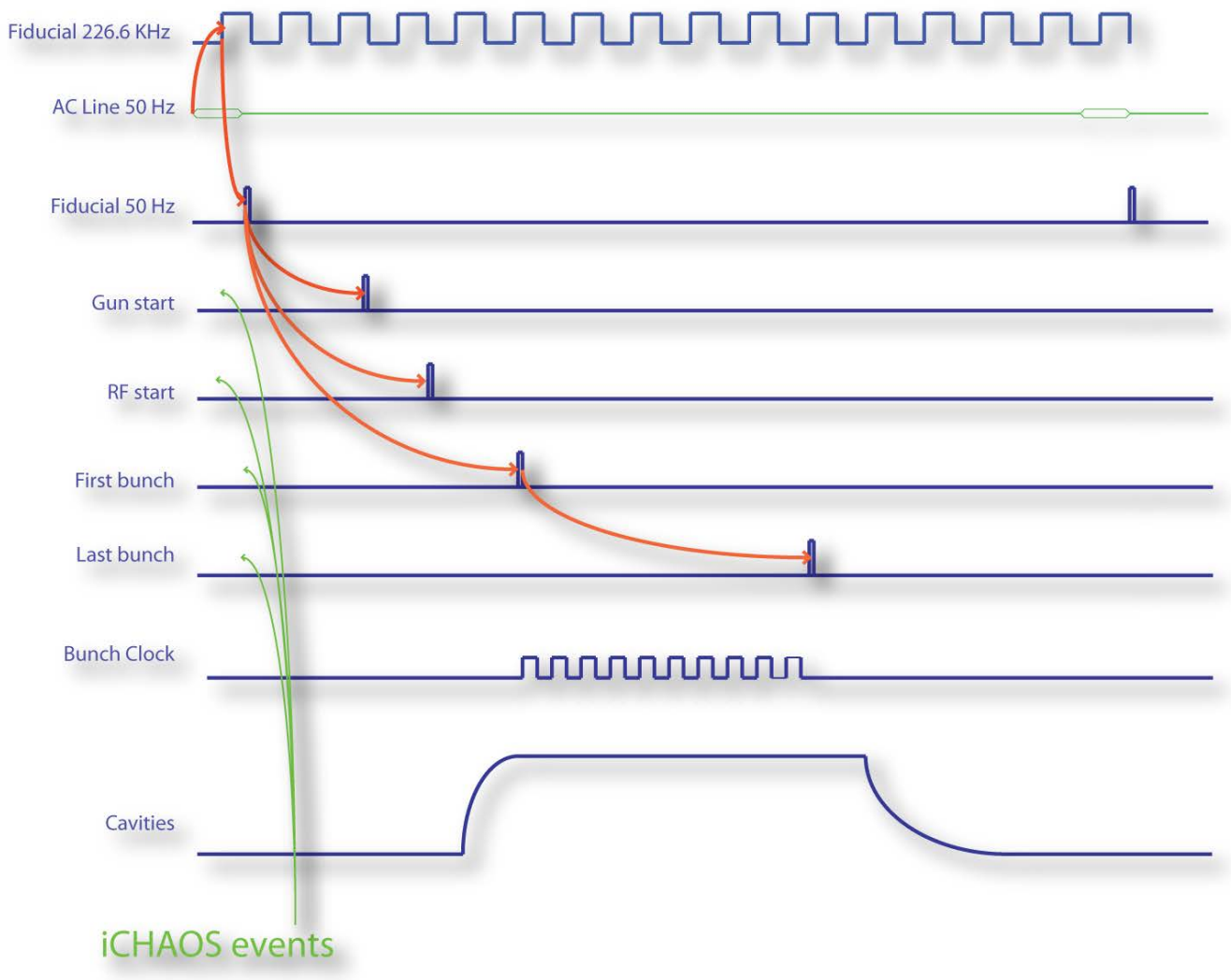
Event broadcast concept



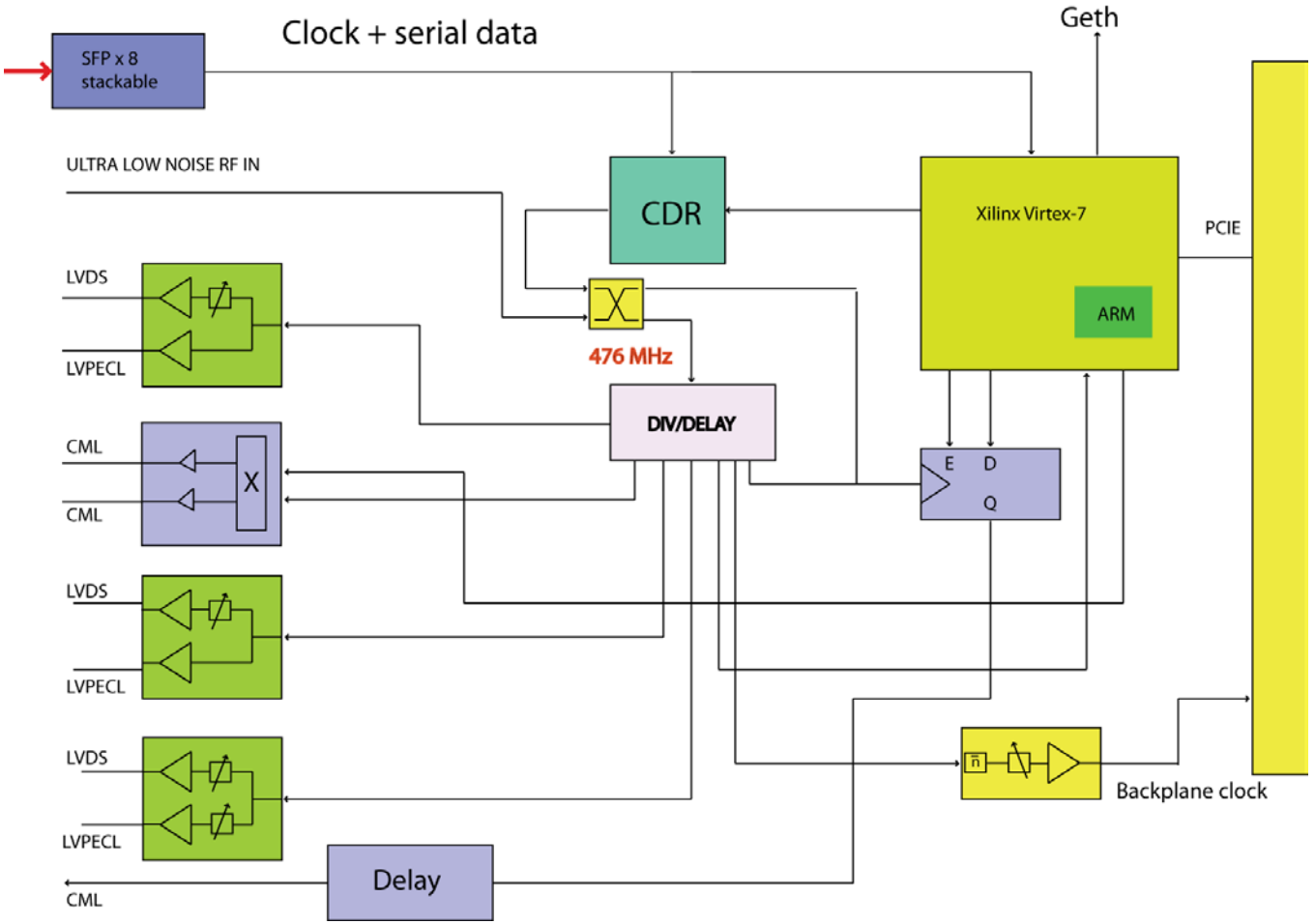
Event Reception



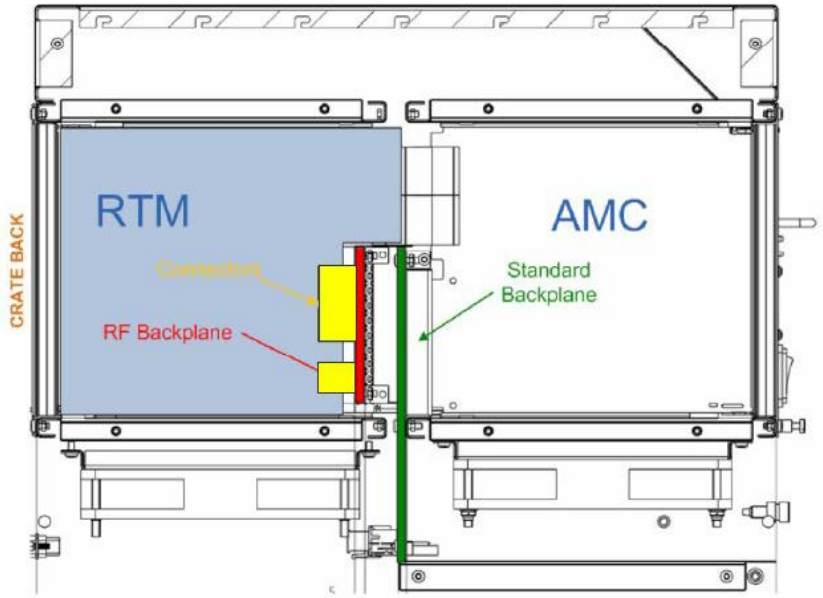
A Trigger “Timing Diagram” Example

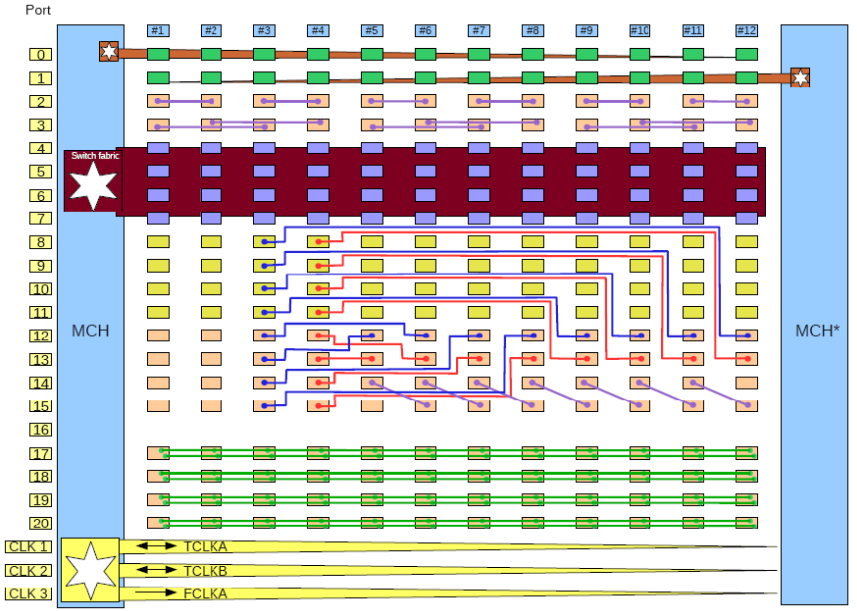


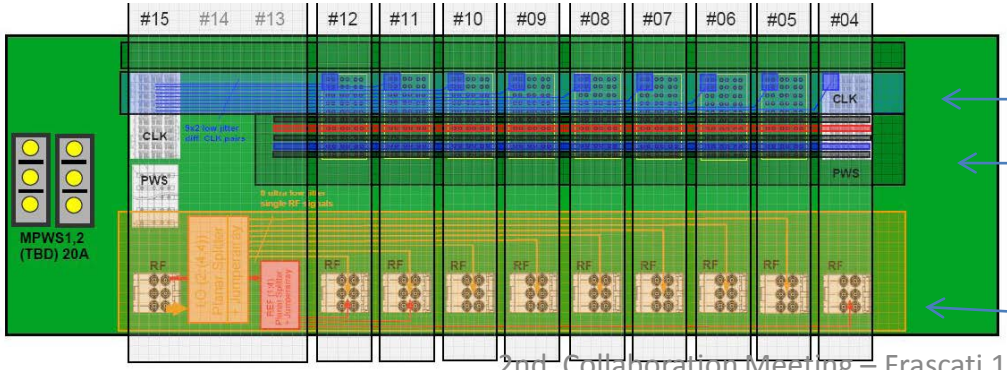
Transmitter/Receiver Block Diagram



uTCA for Physics







Low Jitter clock distribution < 200fs

Independent redundant power supplies

Ultra Low jitter RF signals < 70fs

uTCA for Physics

Commercial timing systems

- Micro Research Finland
  - (EVG,EVR) VME, cPCI, PMC
  - Widely deployed (APS, PSI, KEKB,SLAC, ..)
- White Rabbit
  - Not truly commercial (yet)
  - CERN, GSI + National Instruments.
  - Real implementations exist ?
- …more may exist !

Open Issues

- Technical
  - AC Line 50Hz synchronization
  - Fractional frequencies generation
  - Temperature drift compensation
  - Field bus standard
  - “Hands-on” review of commercial timing systems
- … less “technical”
  - Manpower (for the event distribution system)
    - For custom solution
      - HW + firmware : 3 FTE - 4 years
      - SW : 1 FTE – 2 years
    - For other trigger modules : ?
  - R&D phase duration + prototyping
    - 1 year
  - Integration : ?
  - Commissioning : ?

Conclusions

- An event based timing system may fulfill SuperB requirements
- The system is complex
  - 3 virtual (HER,LER, DR+Linac) systems to coordinate
  - Must be open to future changes / requirements
  - Has tight jitter requirements
- More discussion with machine and RF designers is needed to iron out all the issues that may impact the timing system (and viceversa)