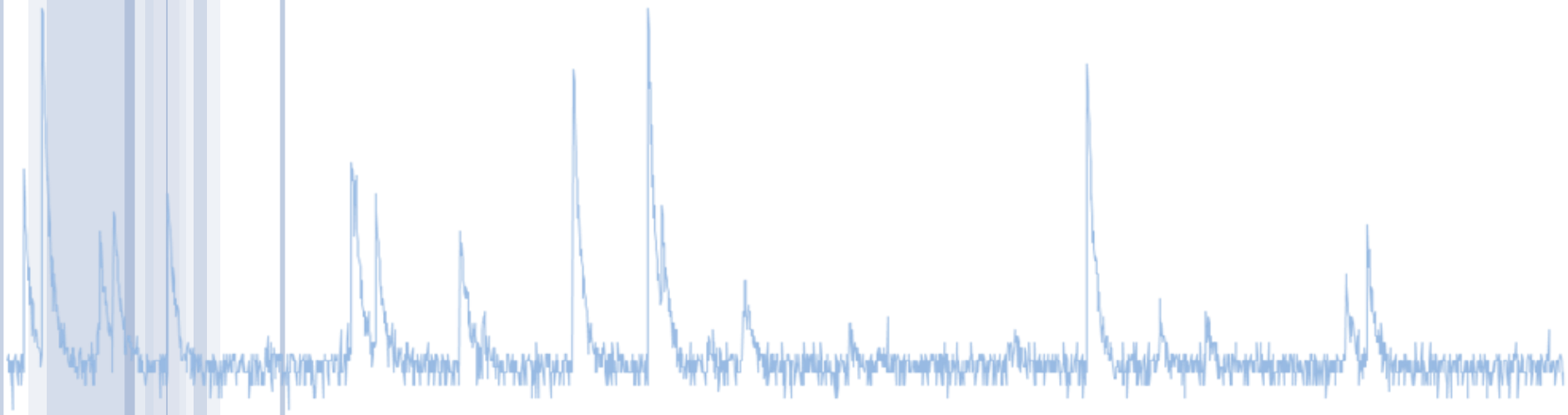


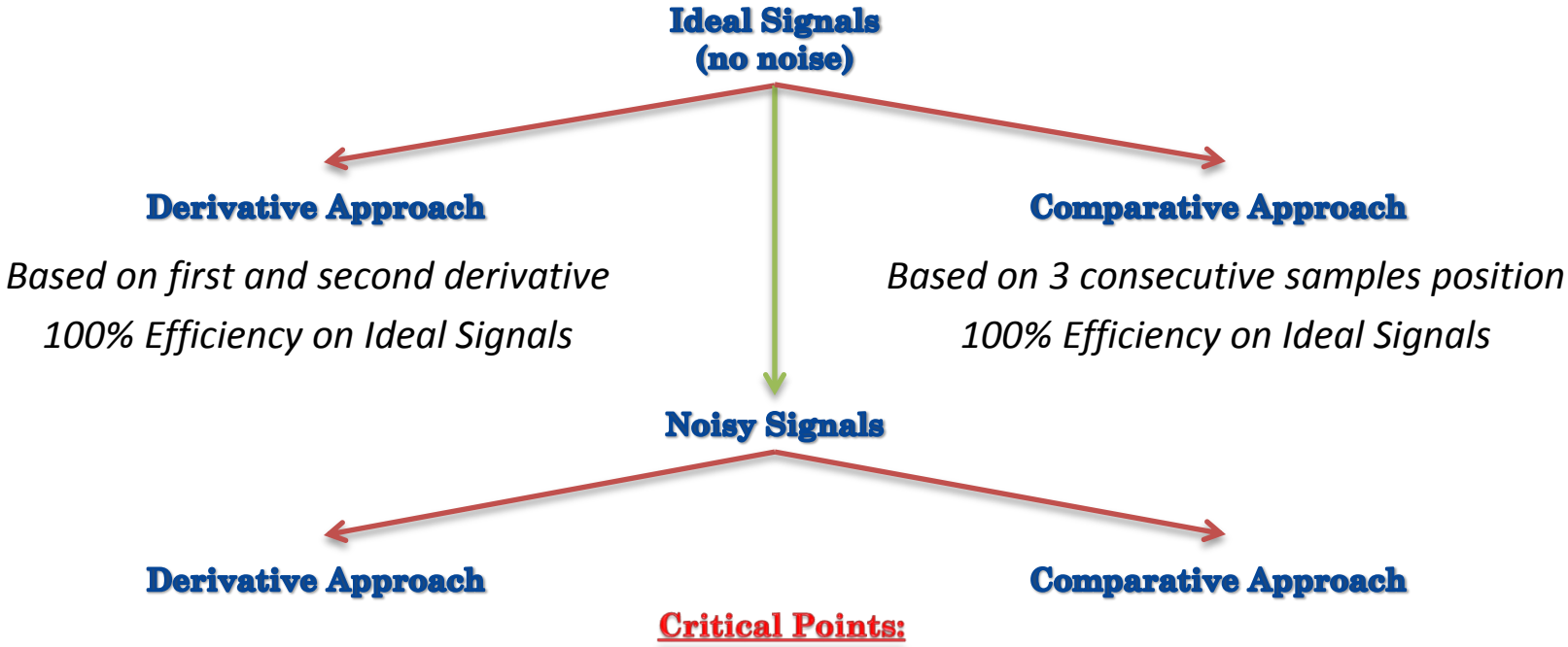
CluTim Algorithm for Drift Chambers Readout Electronics

Luigi Cappelli

Outline

1. **CluTim Approaches**
2. **Sigma Approach**
3. **Efficiency Evaluation**
4. **Simulation Results**
5. **State of the art and future steps**
6. **Conclusions**

CluTim Approaches



Critical Points:

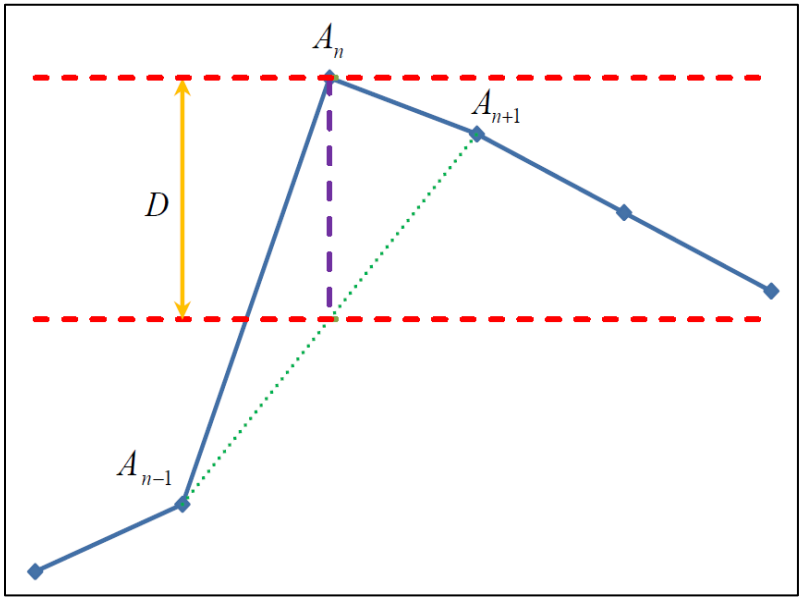
1. **Smoothing**
2. **Good Efficiency but too many fakes**

New Approach

Focusing on noise characterization

Sigma Approach

Noisy Signals → **Sigma Approach** → **Efficiency Evaluation**



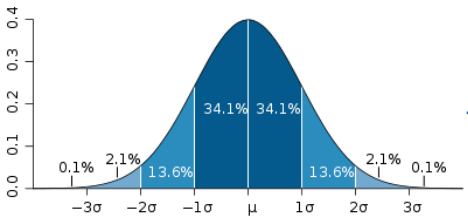
$$\varepsilon = \frac{\text{Algorithm Identified Peaks}}{\text{Ideal Peaks}}$$

Absolute Efficiency **Relative Efficiency**

$$D = A_n - \left(\frac{A_{n-1} + A_{n+1}}{2}\right) \geq 3\sigma_d$$ **Peak Found Condition**

$$\sigma_d{}^2 = \sigma_{A_n}{}^2 + \frac{1}{4}\sigma_{A_{n-1}}{}^2 + \frac{1}{4}\sigma_{A_{n+1}}{}^2 = \frac{3}{2}\sigma^2$$ **Set Threshold**

Example:
σ = 3 → D ≥ 11.02 ≈ 11



→ 3σ = cutting 99.7% of noise

Efficiency Evaluation - Noisy Signals

Ideal Signal →

Number of peaks is well known

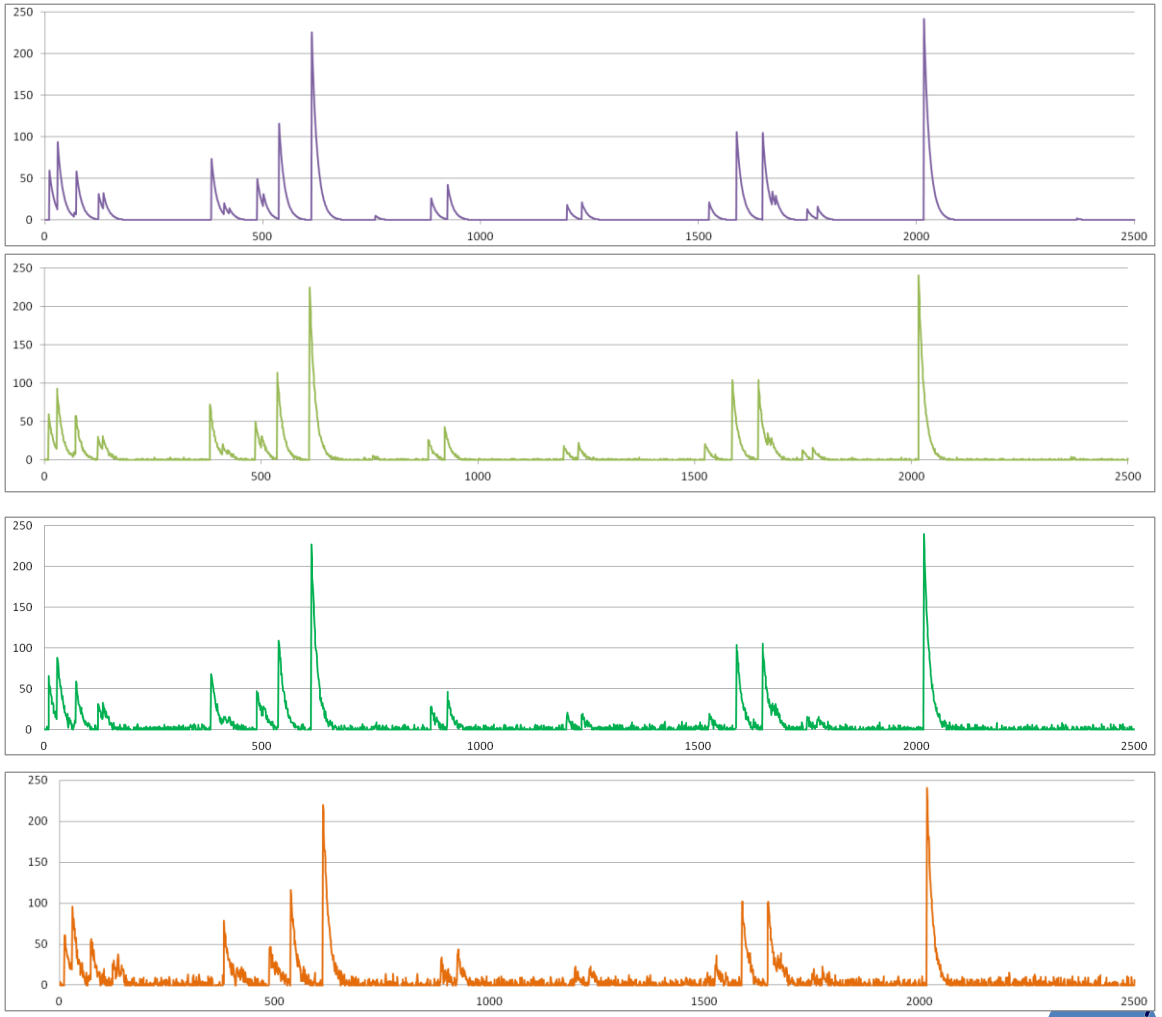
NOISE

$[6-30\ mV_{pp}]$

σ = 1

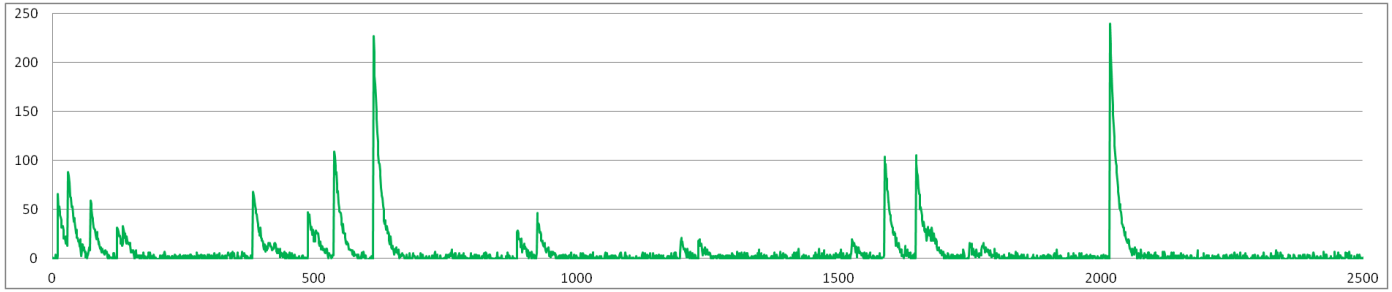
σ = 3

σ = 5



Study of efficiency and fakes as function of noise amplitude has been carried out.

Efficiency evaluation – Absolute Efficiency



TOT PEAKS 22

AMPL AVERAGE 54

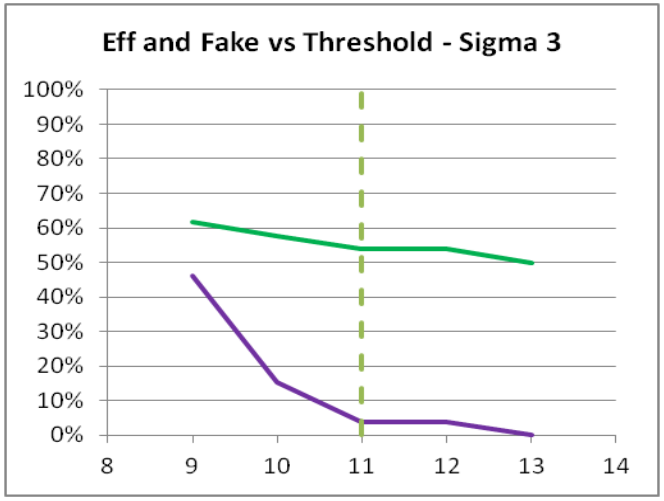
$$\mathrm{SNR} = \frac{\mu}{\sigma}$$

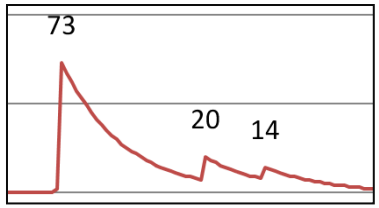
Book8_sig2 – SNR: 27			
THR	EFF	FAKE	MAX
7	84.62%	11.54%	25
8	69.23%	3.85%	19
9	61.54%	0.00%	16
10	61.54%	0.00%	16
11	53.85%	0.00%	14

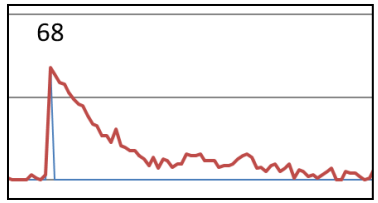
Book8_sig3 – SNR: 18			
THR	EFF	FAKE	MAX
9	61.54%	46.15%	28
10	57.69%	15.38%	19
11	53.85%	3.85%	15
12	53.85%	3.85%	15
13	50.00%	0.00%	13

Book8_sig4 – SNR: 13.5			
THR	EFF	FAKE	MAX
11	65.38%	34.62%	26
12	57.69%	15.38%	19
13	57.69%	3.85%	16
14	50.00%	0.00%	13
15	42.31%	0.00%	11

Book8_sig5 – SNR: 10.8			
THR	EFF	FAKE	MAX
14	57.69%	15.38%	19
15	53.85%	3.85%	15
16	50.00%	3.85%	14
17	42.31%	3.85%	12
18	42%	3.85%	12





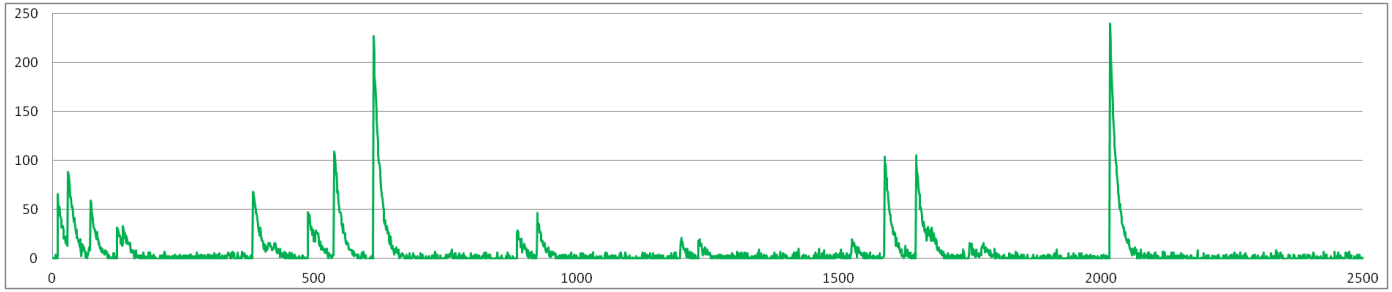


Ideal Signal **Noisy Signal**

Depending on the peak amplitude, it could be comparable to noise and no algorithm could identify it.

RELATIVE EFFICIENCY EVALUATION

Efficiency evaluation – Relative Efficiency

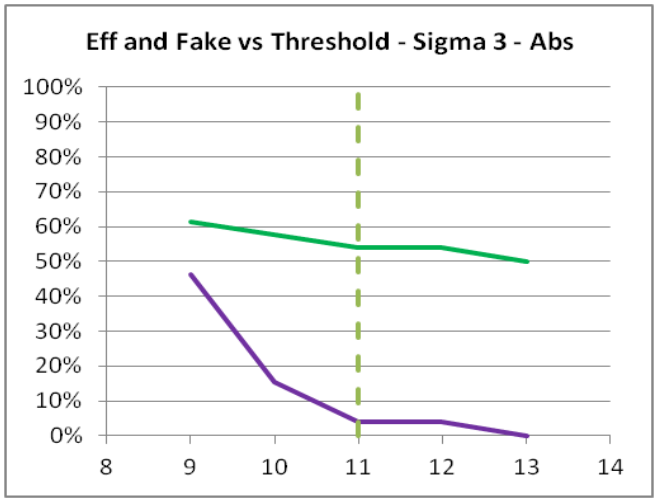


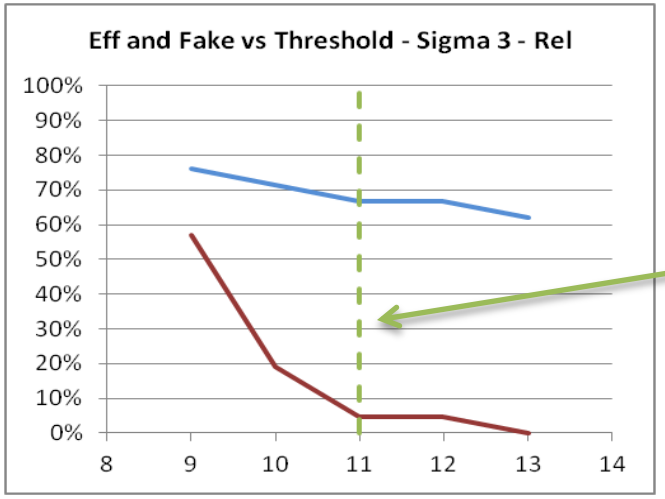
TOT PEAKS	22
AMPL AVERAGE	57

Book8_sig3_abs			
THR	EFF	FAKE	MAX
9	61.54%	46.15%	28
10	57.69%	15.38%	19
11	53.85%	3.85%	15
12	53.85%	3.85%	15
13	50.00%	0.00%	13

Book8_sig3_rel			
THR	EFF	FAKE	MAX
9	76.19%	57.14%	28
10	71.43%	19.05%	19
11	66.67%	4.76%	15
12	66.67%	4.76%	15
13	61.90%	0.00%	13

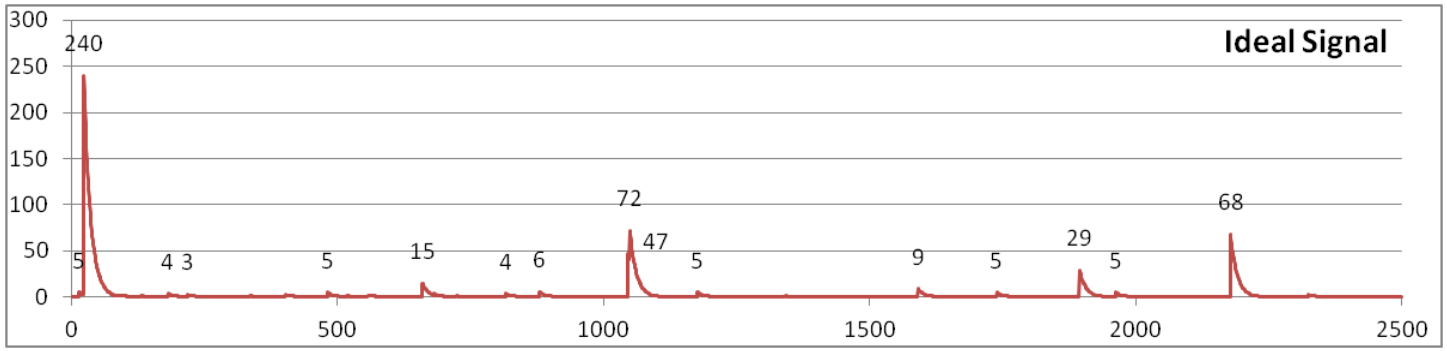
Taking into account just potential identifying peaks. (in this case 5 are covered by noise)



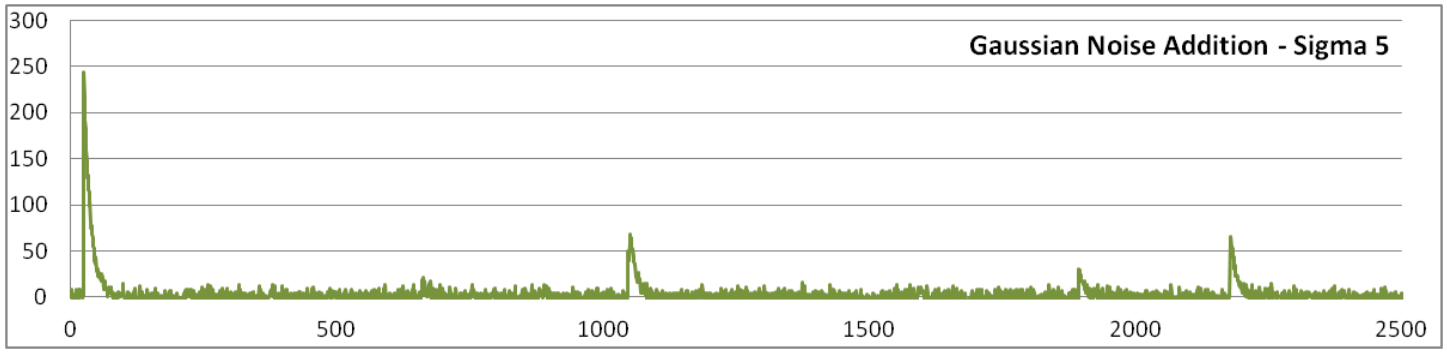


Reference level for the threshold with σ = 3

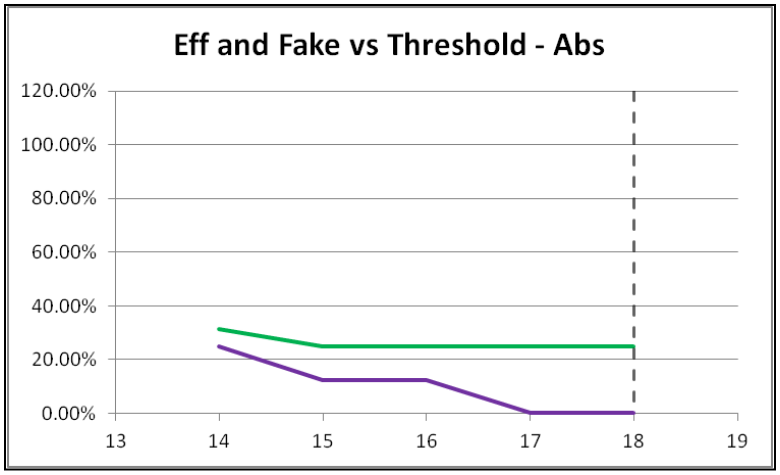
Relative Efficiency - Example

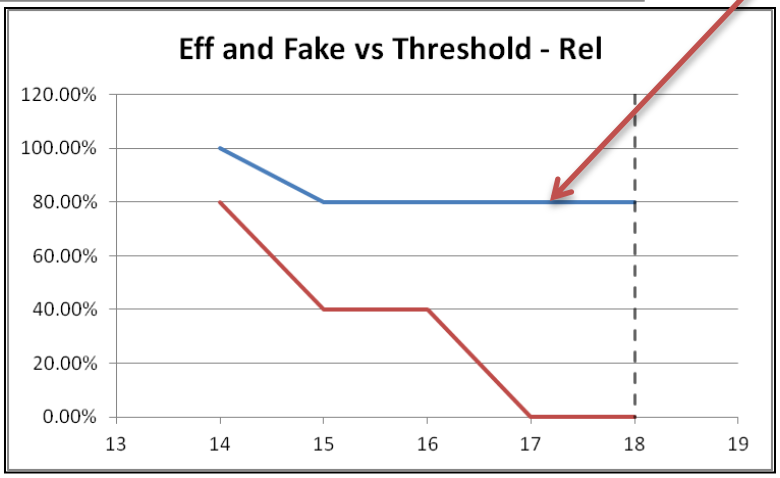


TOT PEAKS 16
AMPL AVERAGE 33

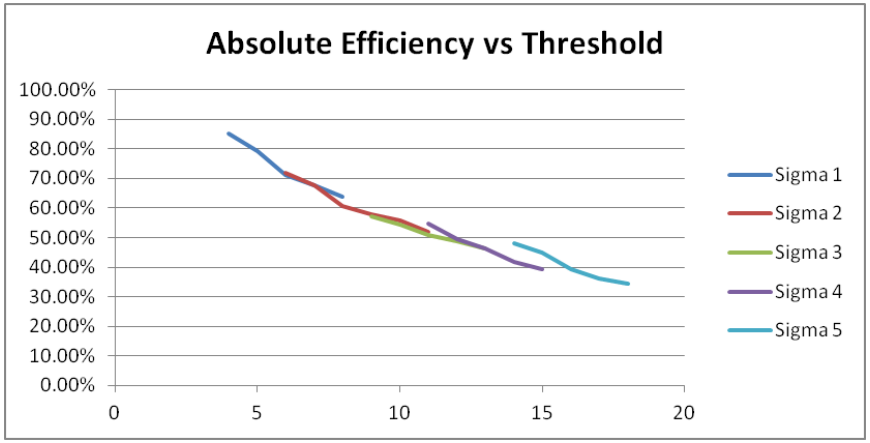


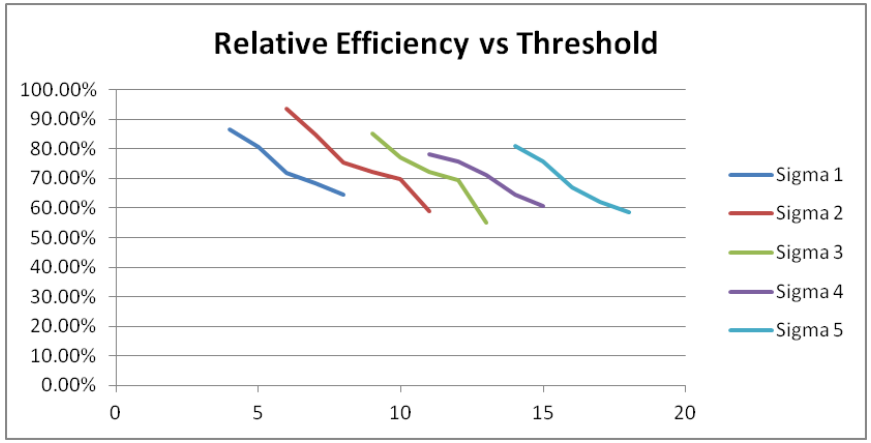
TOT PEAKS 16
COVERED BY NOISE 11

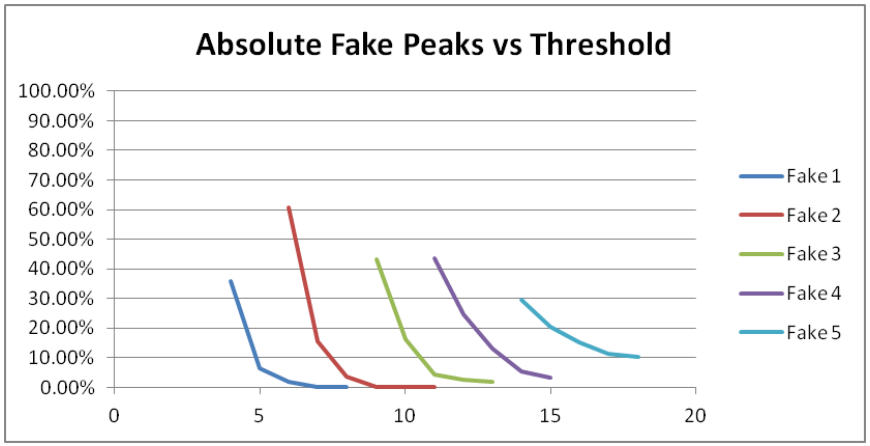


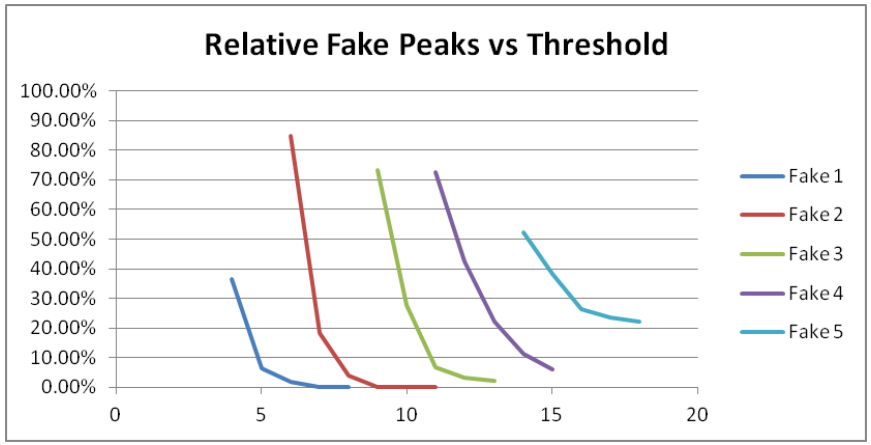


Efficiency – Simulation Results



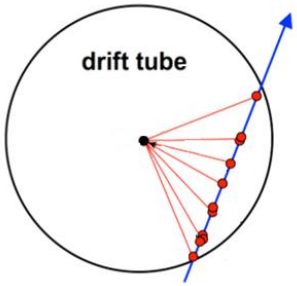




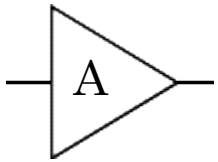


- **Absolute Efficiency scales down proportionally increasing the noise**
- **Relative Efficiency is confined within 60 – 90% depending on threshold**
- **Fake peaks obviously increase increasing the noise**
- **Unrevealed peaks are generally part of the same cluster, it means the efficiency could increase referring to clusters, not to single electrons.**

Next Step – Parallel paths



Drift Tube



Amplifier

ADC08D1500DEV with Virtex 4 from National Semiconductor

Hittite HMCAD1511
8-Bit 1 GSPS A/D Converter
710 mW – SNR: 49.8 dBFS

Xilinx ML605 Virtex 6

Conclusions and Future Plans

- **Cluster Timing algorithms have been developed with three different approaches;**
- **Sigma Approach Algorithm Efficiency has been evaluated and it meets the requirements;**
- **Efficiency as function of noise has been evaluated;**
- **Upgrades of the Cluster Timing Electronics:**
  - **Use of an ADC – FPGA integrated board from National Semiconductor, (ADC08D1500) are underway;**
  - **New Flash ADC interfacing Xilinx ML605**
- **VHDL Code improvements:**
  - **Timing performance improvement by pipelining**
  - **Mapping Strategies**
- **Final Target: Readout Board with, at least, 4 channels.**

THANK YOU