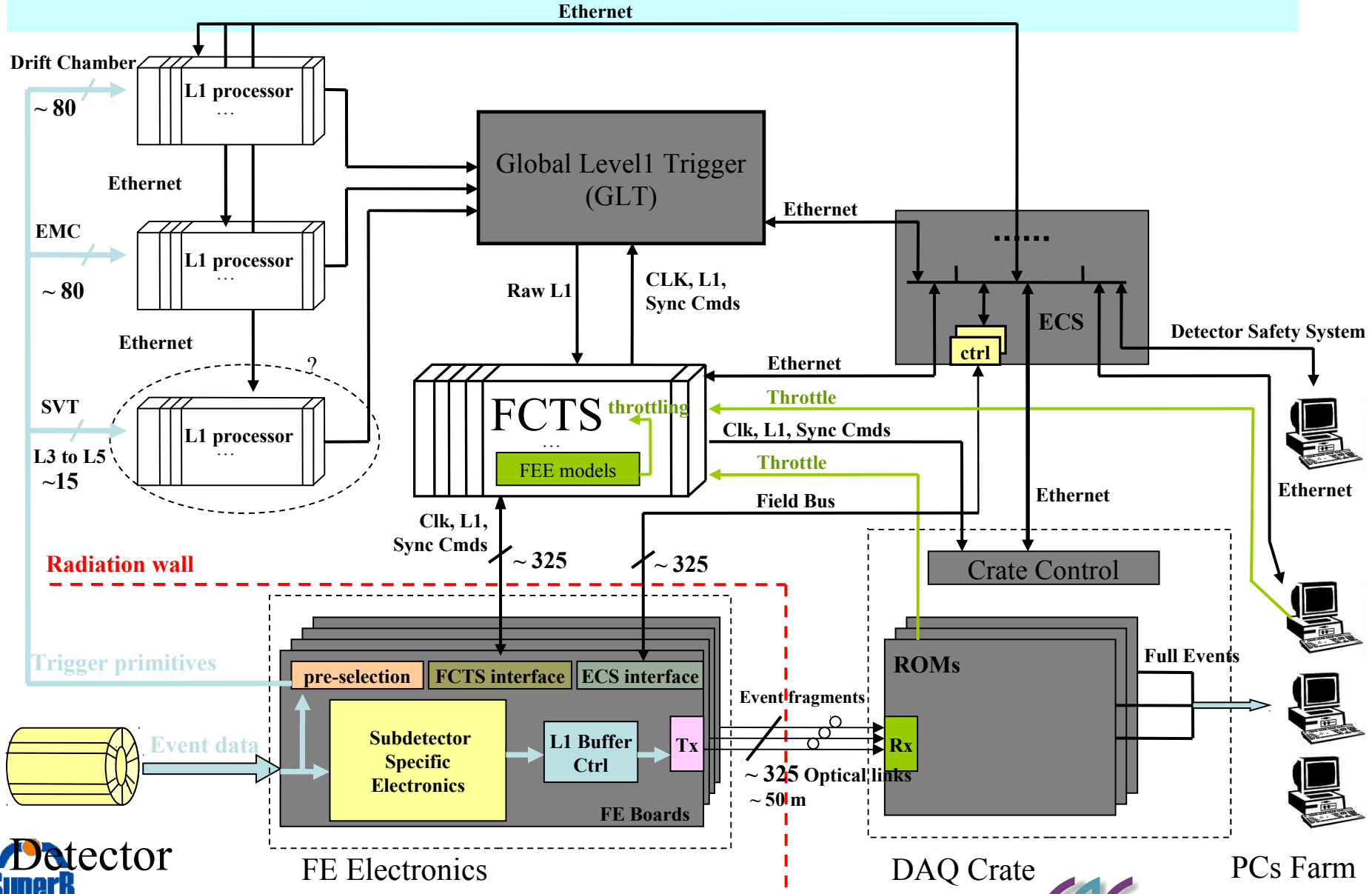
PROPOSAL FOR FTCS & ECS

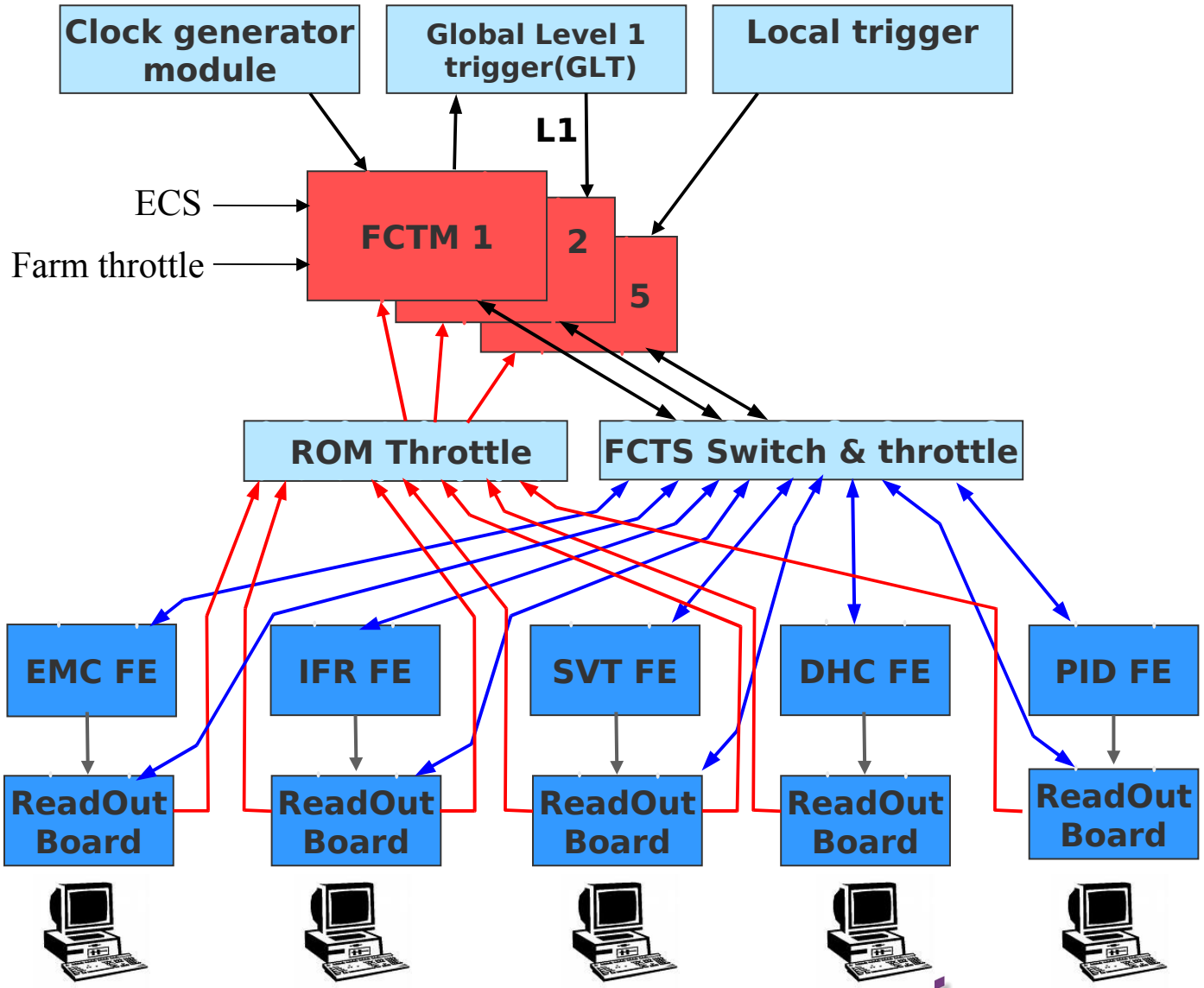
FCTS requirements

- Synchronizing the experiment with the machine.
- Delivering and buffering the reference clock (56 MHz) to the experiment.
- Dealing with the raw L1 trigger decision.
- Throttling the latter and tagging it with respect to the machine clock and to the slowest divided clock.
- Permitting the partitioning of the system into independent subsystems or groups of subsystems.
- Generating programmable local trigger for calibration and commissioning.
- Generating different commands (calibration pulse, reset, BxID and event ID).
- Managing the stack of IP addresses for PC farm.
- Keeping trace of all event-linked data to put in the event readout

Overall system achitecture



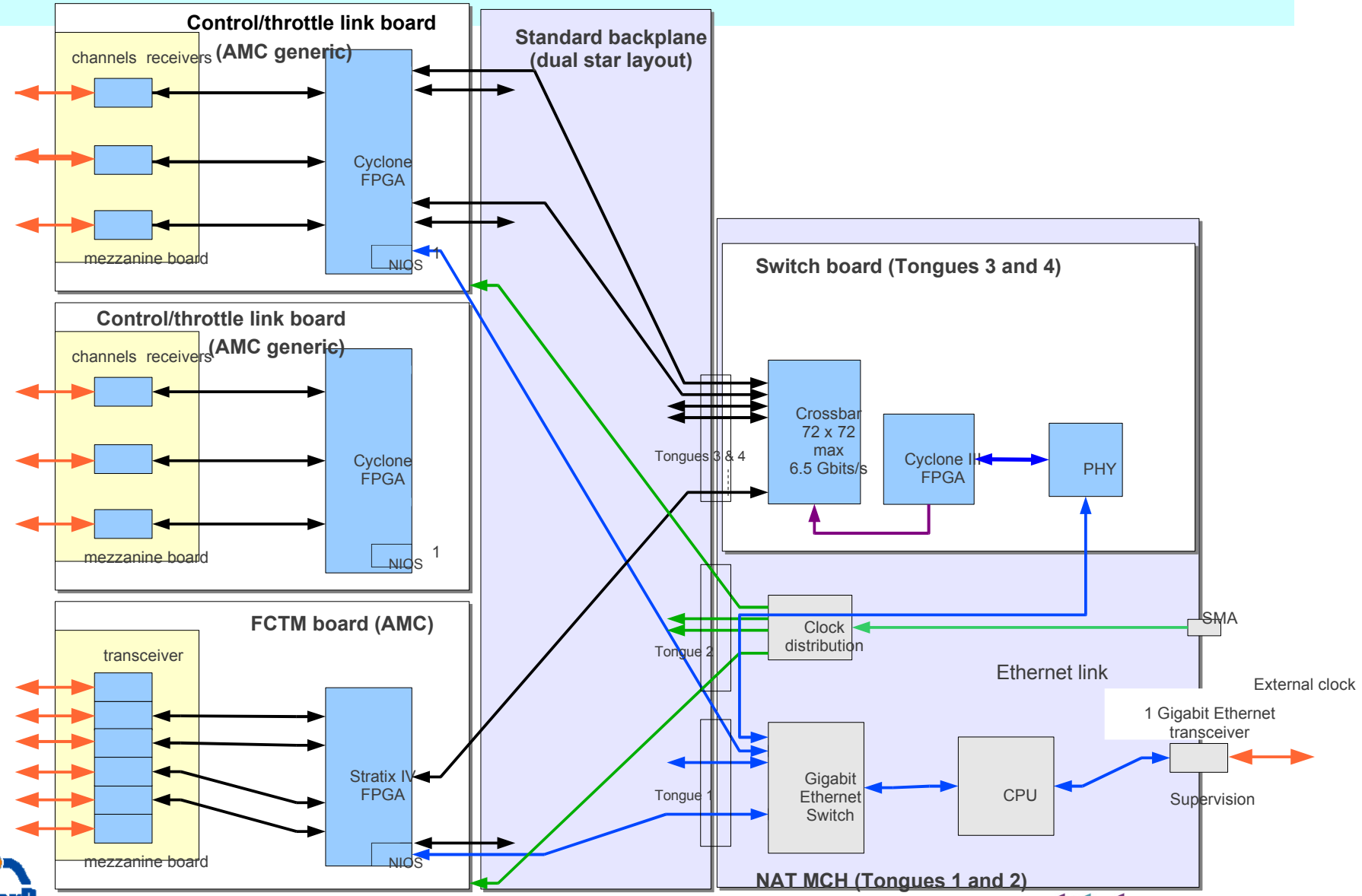
FCTS Architecture



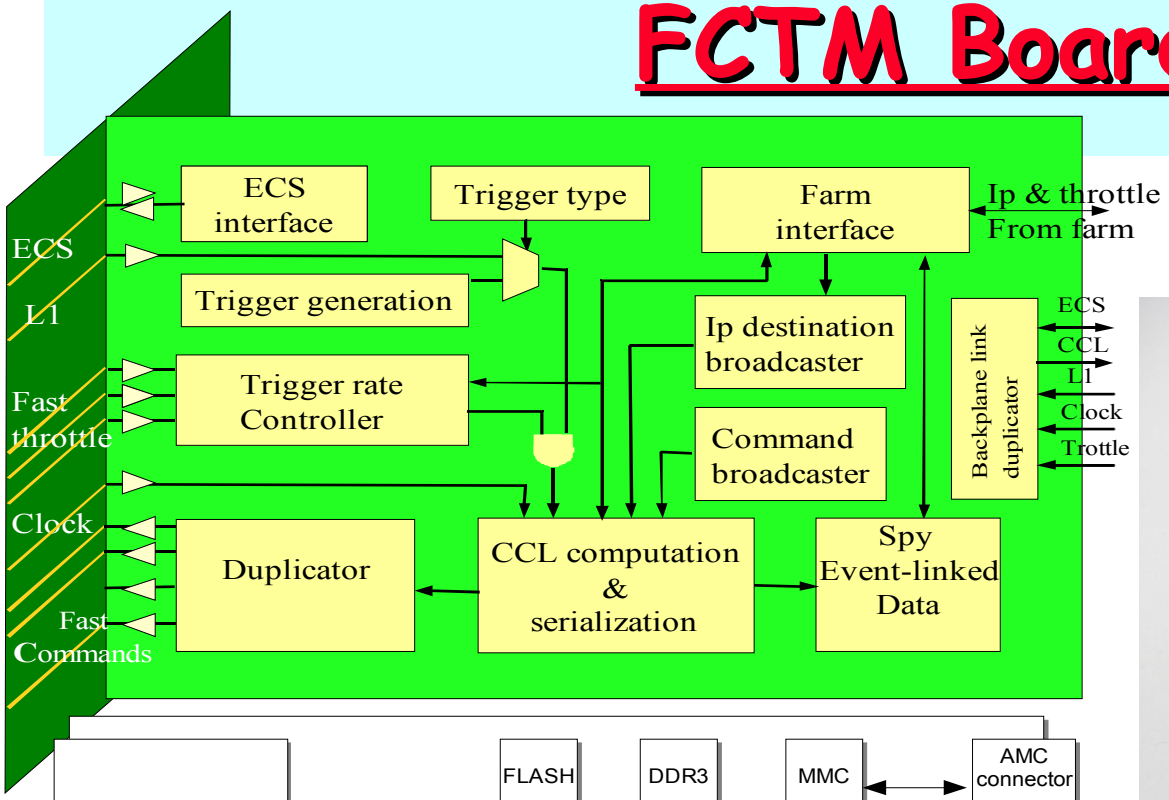
FCTS connections

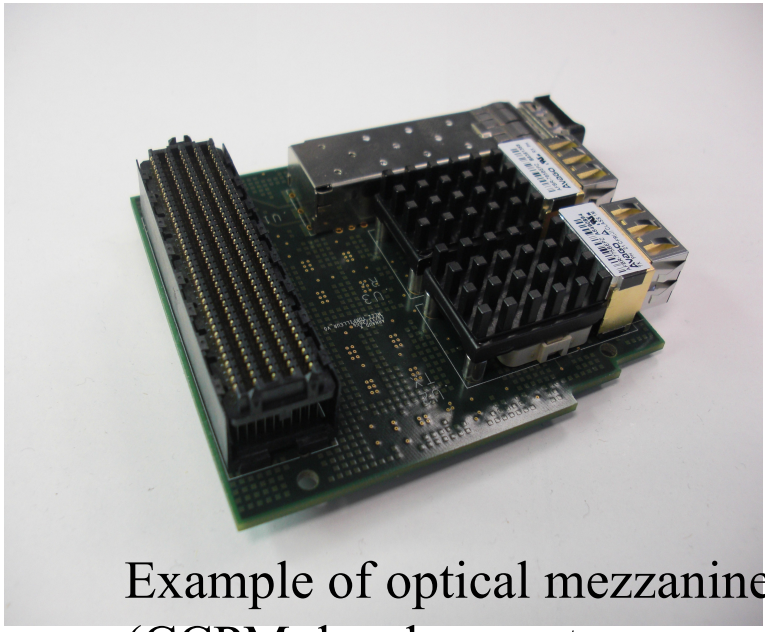
- Throttle:
  1. Front end electronics on detector: Bi-directional rad-hard link (~325links).
  2. Read Out Module: dedicated link (~50), ethernet link by UDP protocol (~1). **TEST and choice have to be done in coordination with Bologna group.**
  3. Slow throttle PC-farm: Ethernet link (~1).
- Clock and trigger command distribution.
  - Bi-directional rad-hard link .
- Clock machine input: Dedicated link (must be defined).
- Trigger link: Dedicated link (must be defined).

FCTS uTCA architecture

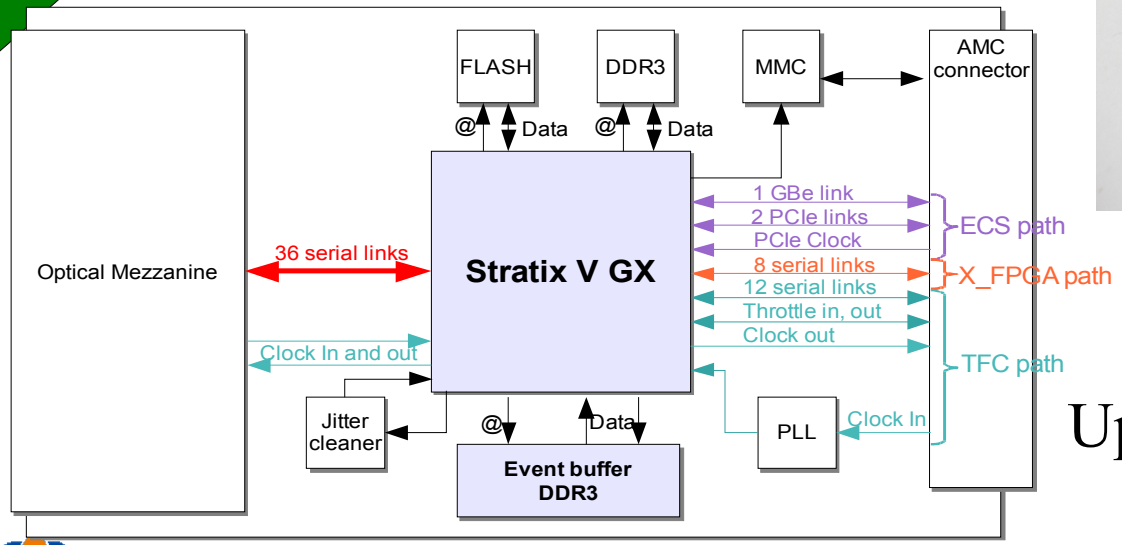


FCTM Board





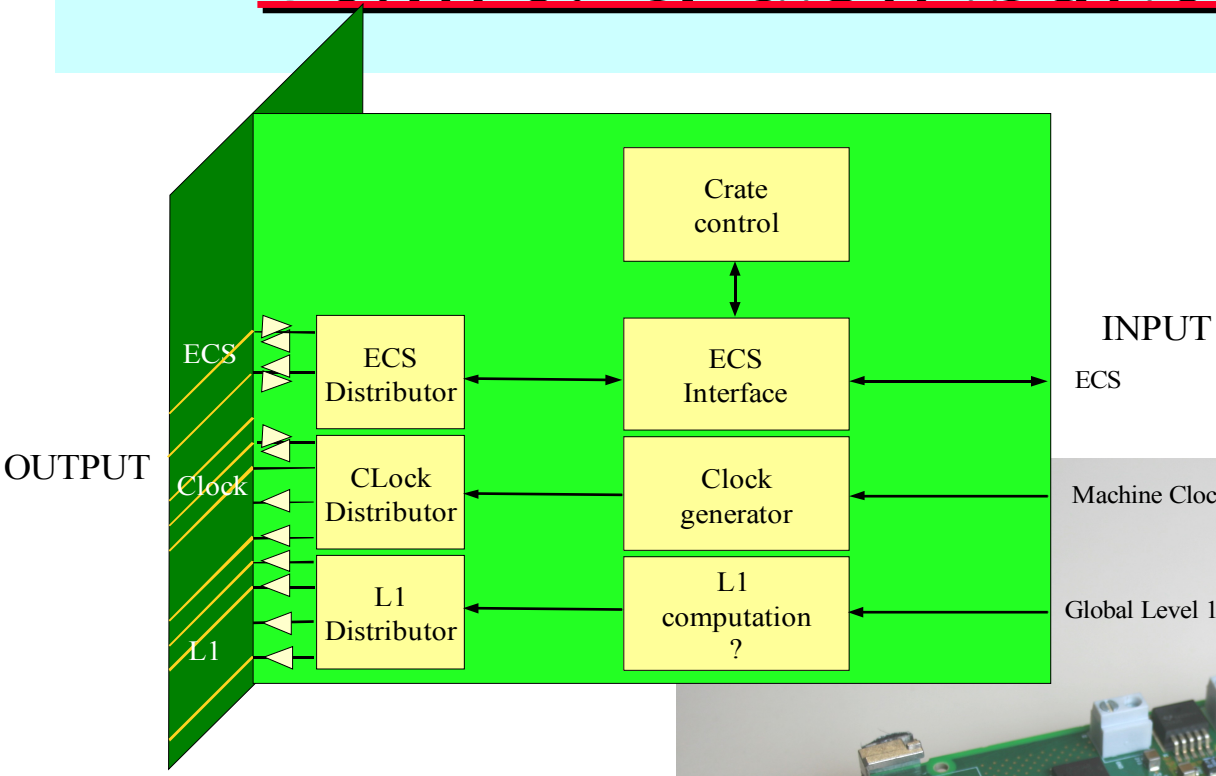
Example of optical mezzanine (CCPM development



Up to 36 link with MicroPOD

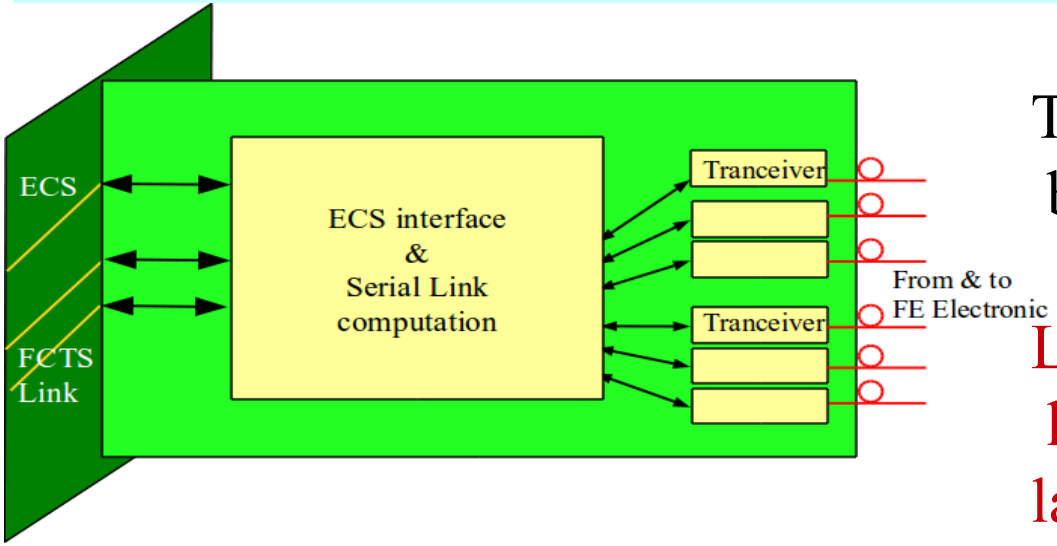
AMC mezzanine board (CCPM development)

Control & distribution module



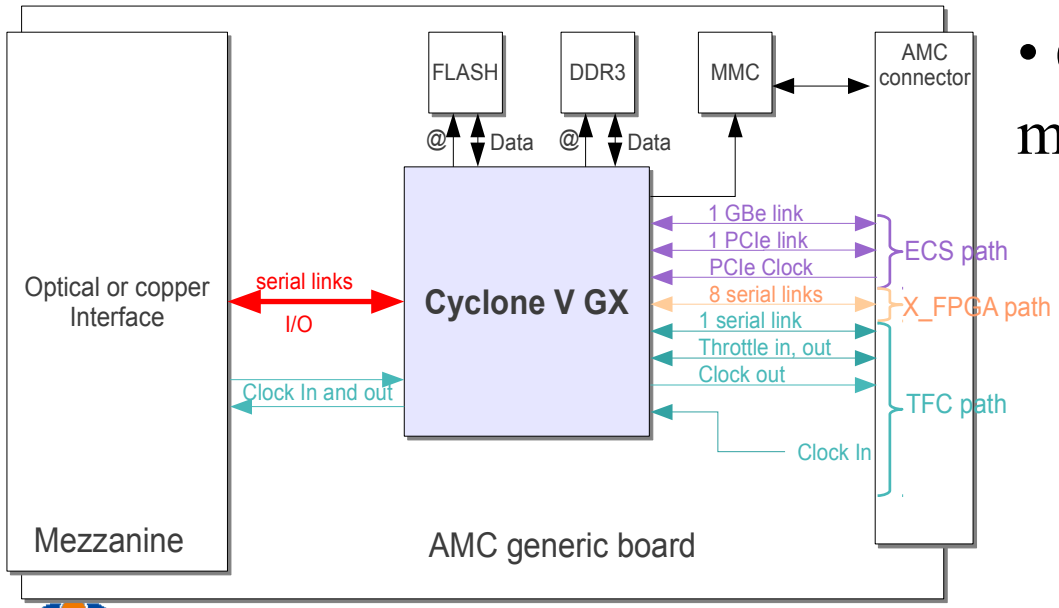
MCH board
Tongue 1: Off the shelf industrial board.
Tongue 2 : CCPM board

Distribution & trottle



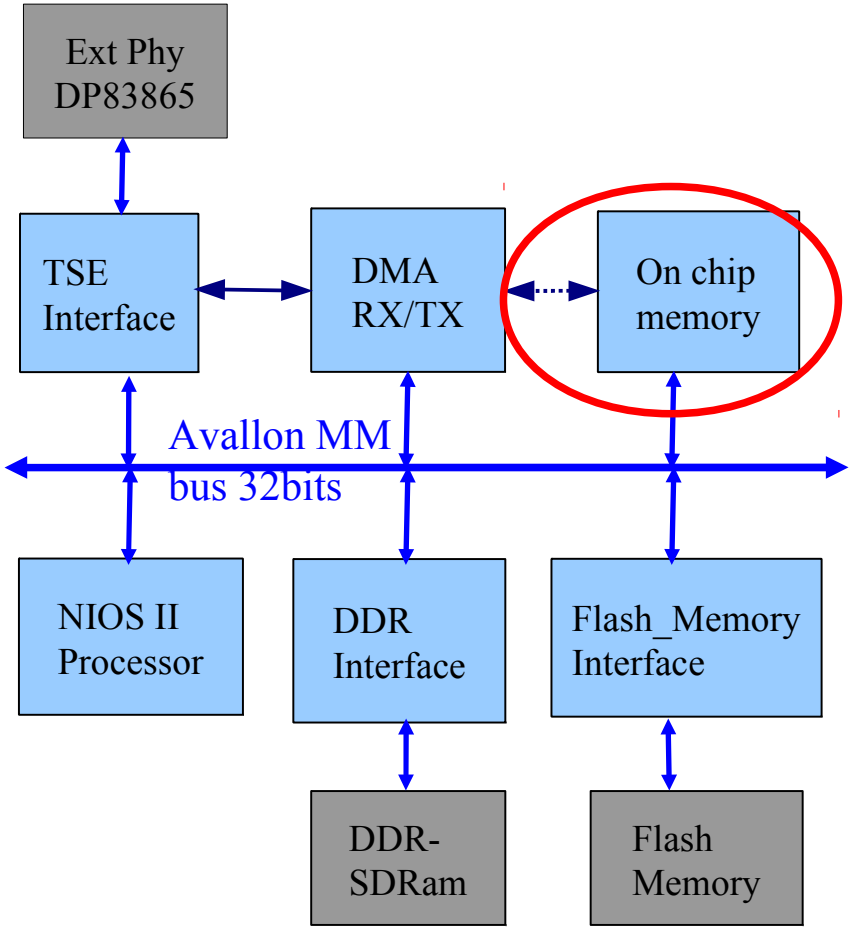
Those 2 functionalities must be integrated in the same board

Link modeling and simulation have to be performed for latency evaluation



- One FCTS uTCA crate cant manage all links (~325 links)
  1. Dedicated crate for switch and throttle links.
  2. Further crates
  3. uTCA for physics 2u size.

Ethernet development



- Mandatory for ECS and FCTS.
  - Full TCP/IP and UDP protocol have been tested.
  - Custom uCLinux have been implemented.
  - Tested on Cyclone III Neek design kit.
  - Performance improvement is on way (increase niosII frequency, hardware check sum, memory access.....

FCTS Conclusion

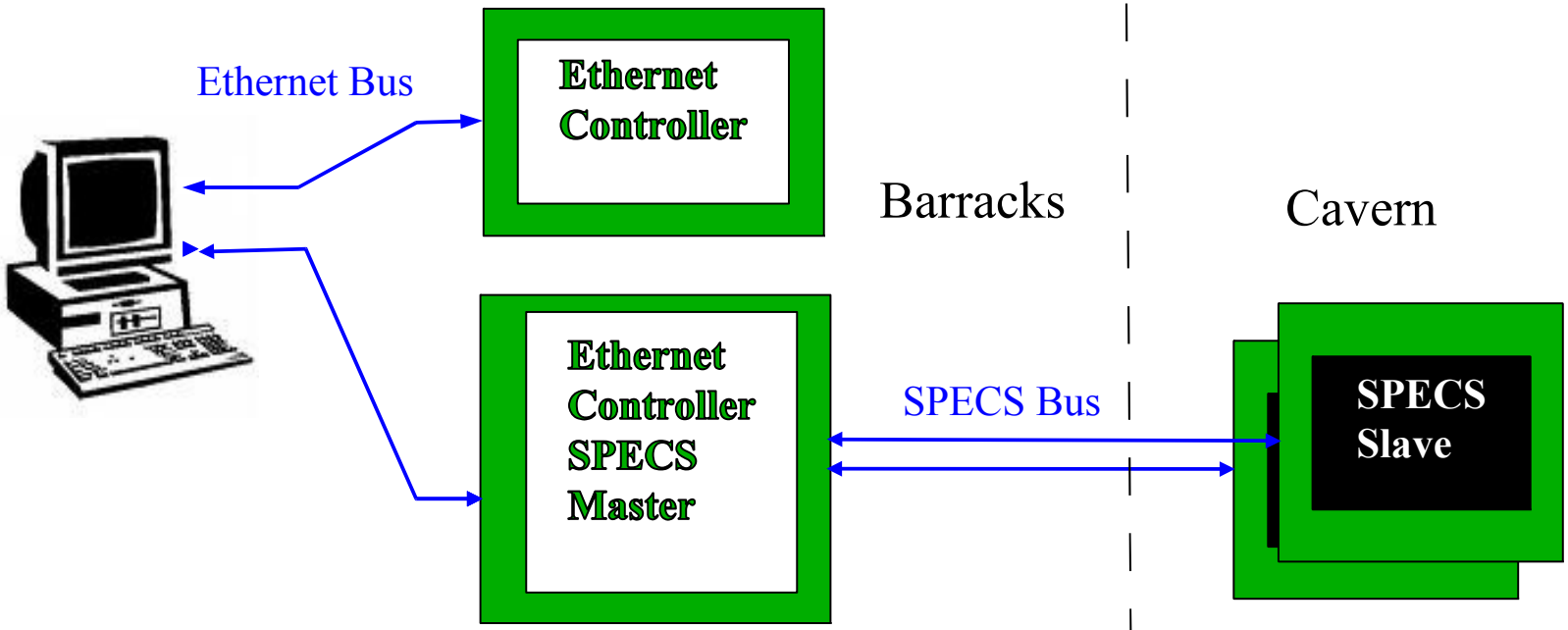
- We would like to use uTCA standard for FCTS system:
  - AMC board standardization: throttle, switch, SPECS master (only custom transceivers mezzanines).
  - Industrial board for “crate controller” (MCH tong 1).
  - FCTS board already developed (CCPM development)
    - Consequence => CONTROL LINK SERIALIZERS MUST BE IMPLEMENTED IN FPGA (due to the uTCA form factor).

Bi-directional link on front-end board electronics (control & throttle) make the FCTS system much more complex.

Decision concerning the link implementation must be taken soon. (FCTS implementation is dependent on this decision and delays the TDR writing).

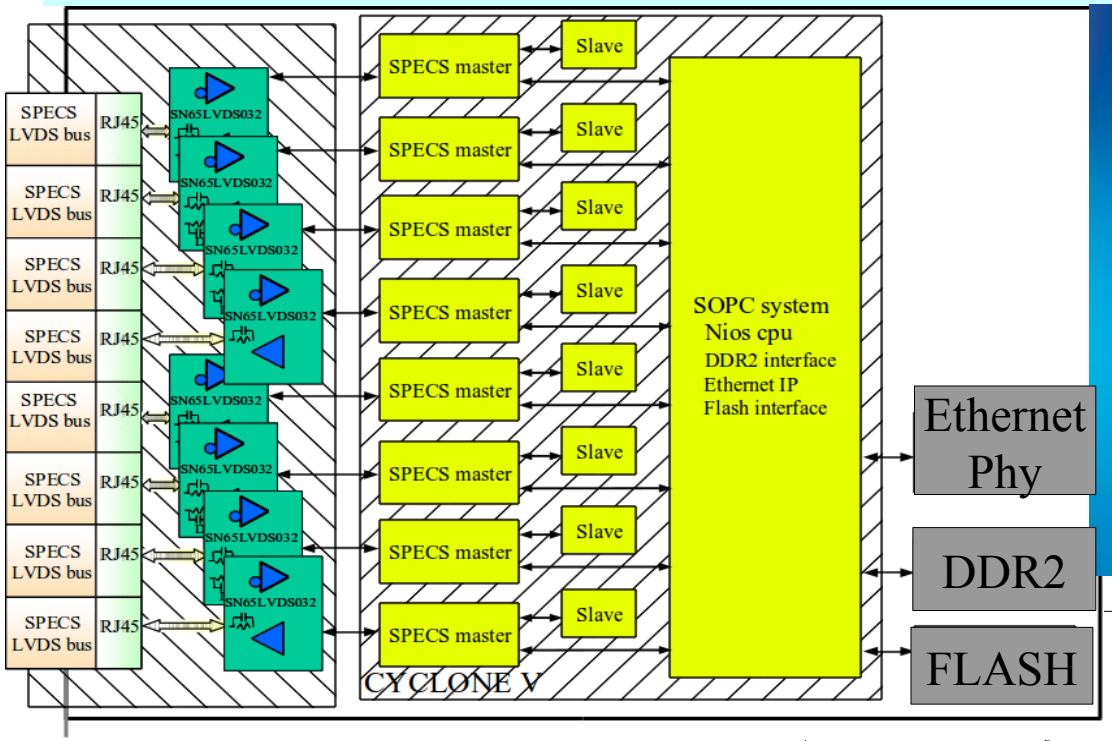
ECS requirement

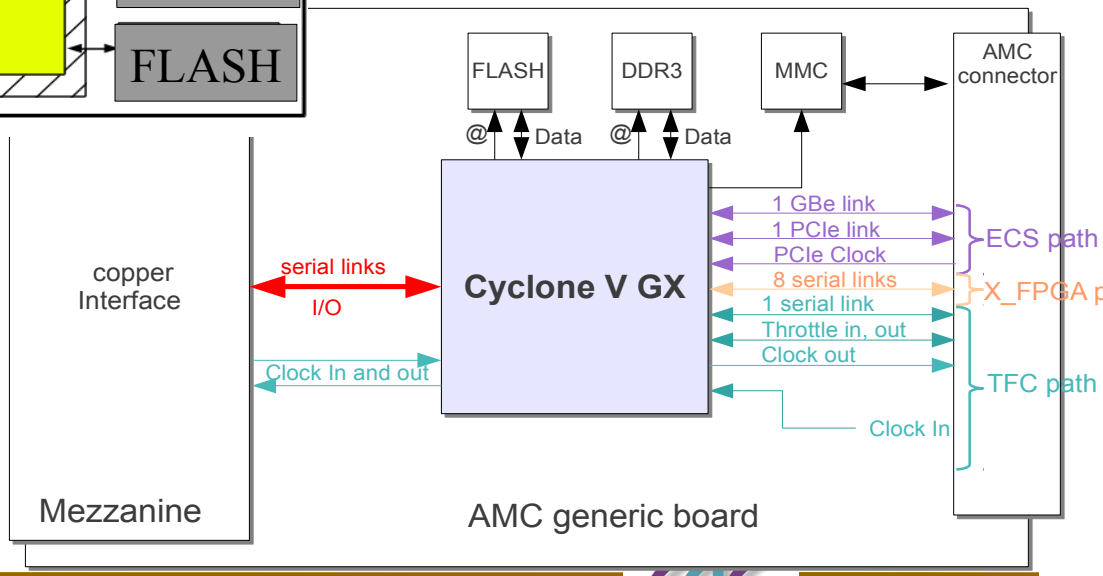
- Configuration system for individual boards located on the detector or crate located in the cavern.
  - Located in radiation sensitive environment, up to 20KRads.
  - Long distance link, up to 100m.
  - Multi configuration (multi-drop bus, point to point).
  - Multi standard interfaces (JTAG, I2C, parallel bus, ctrl I/O).



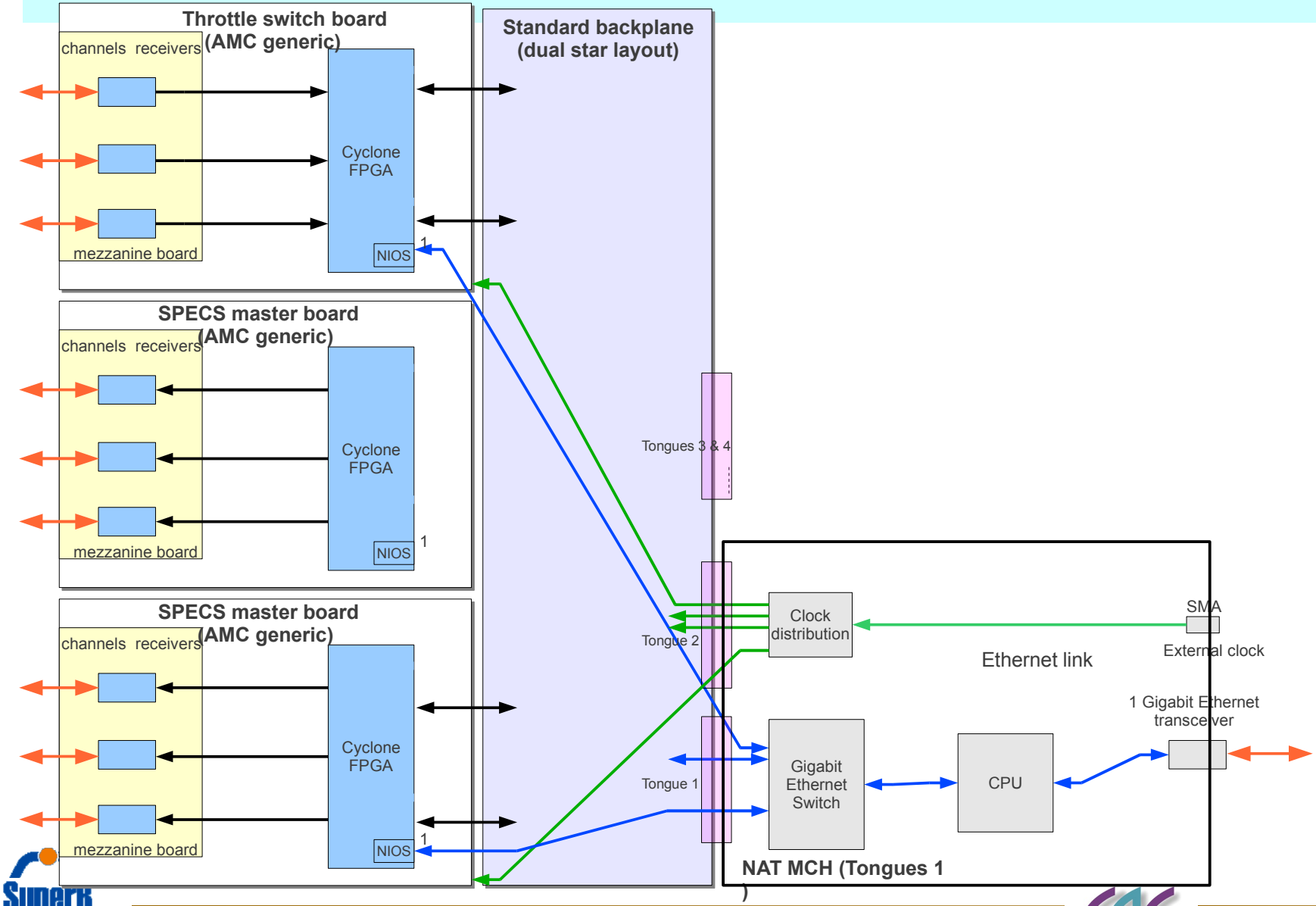
A Serial Protocol for Experiment Control System SPECS

Ethernet SPECS master





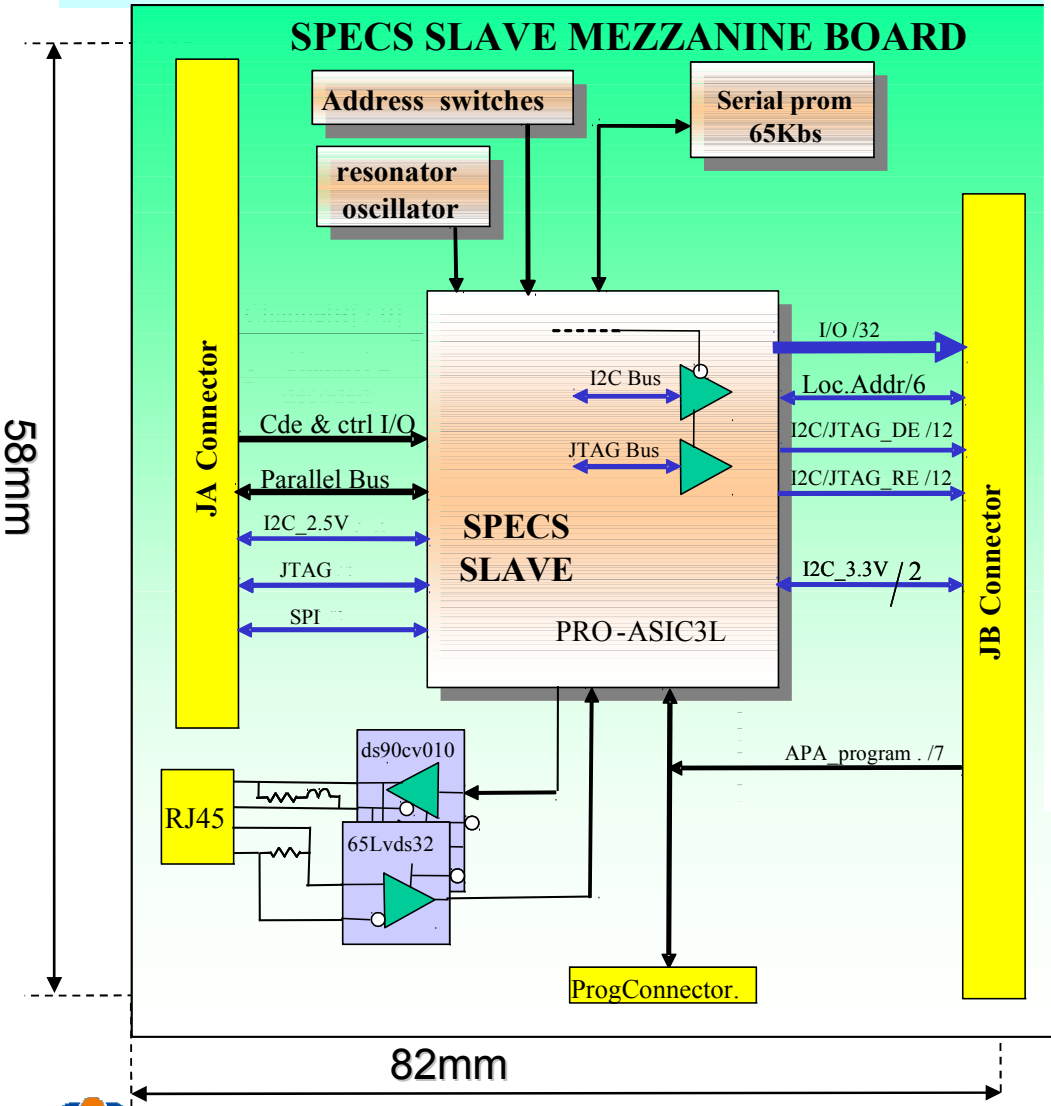
ECS uTCA architecture



ECS Conclusion

- ECS board development.
  - All ECS slaves' functionalities cover the sub-detectors' requirements, confirmed during the CERN meeting in November.
  - We feel like asking CAEN to produce and maintain the system (in long term).
  - ECS TDR is on its way.

SuperB SPECS slave implementation



FPGA ProASIC3L from ACTEL. Triple voting register.

Transfer rate: ~ 14Mbits/s

Address: Local address switch. Broadcast address capability.

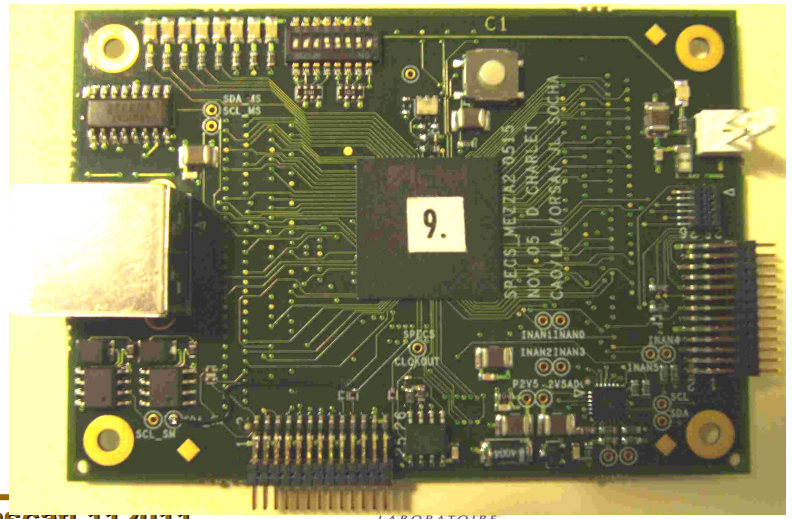
On board clock: Crystal resonator

Programmable clock for SPECS read back:

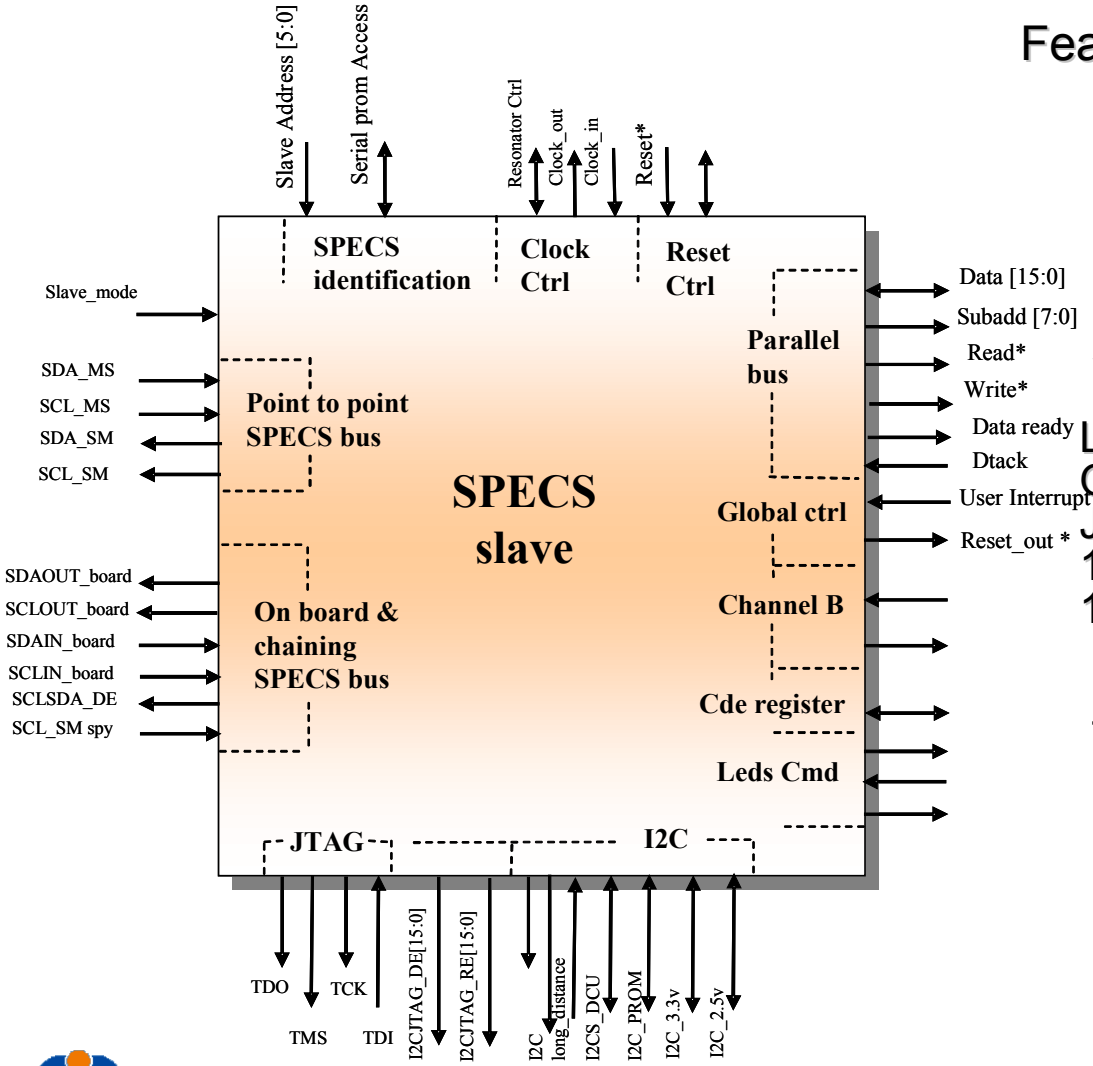
Long distance capability: 100m cat6 cable

User Serial EEPROM: 65Kbits capacity

JTAG bus, I2C bus, SPI Bus



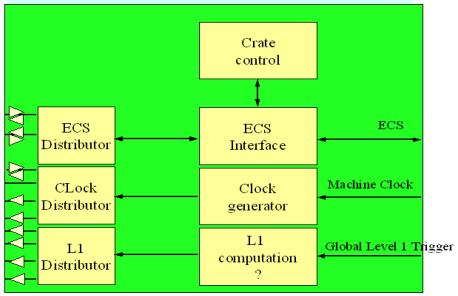
SPECS slave functions

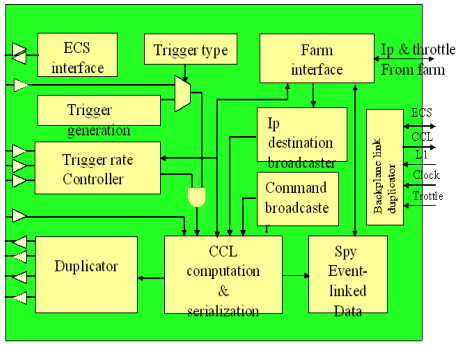


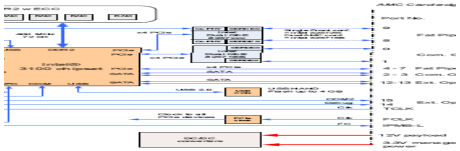
Features of slave:

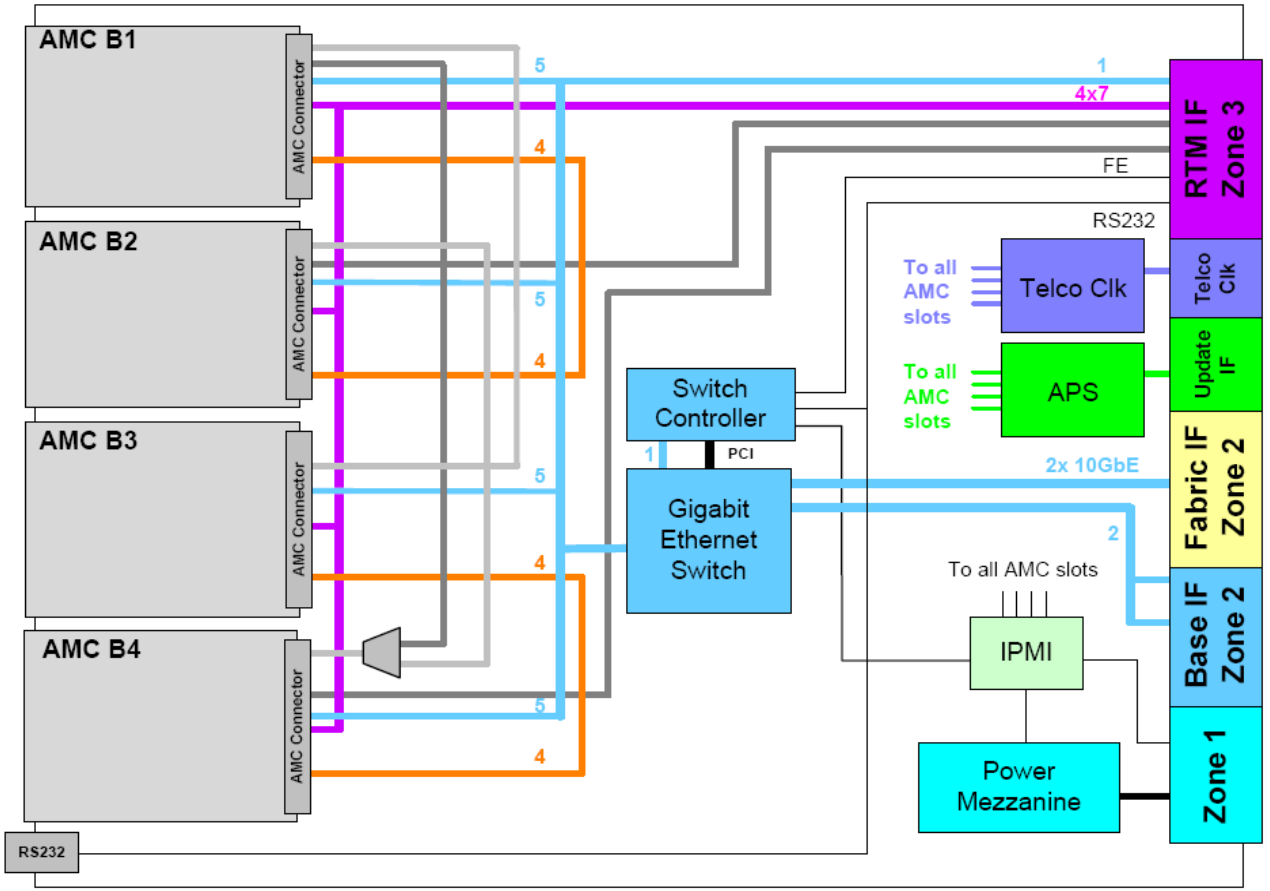
- SPECS bus:
  Point to point slave interface
  Multi drop
- Parallel interface:
  Parallel bus (16data, 8address)
  32 configurable I/O lines
- Serial interface:
  Long distance I2C bus
  On board I2C bus
  JTAG bus
  12 receiver enable
  12 driver enable
- Interrupt:
  User interrupt
  Transmission error
- Serial EEPROM interface:
  Identification register
  Users register

Kontron carrier board AT8404







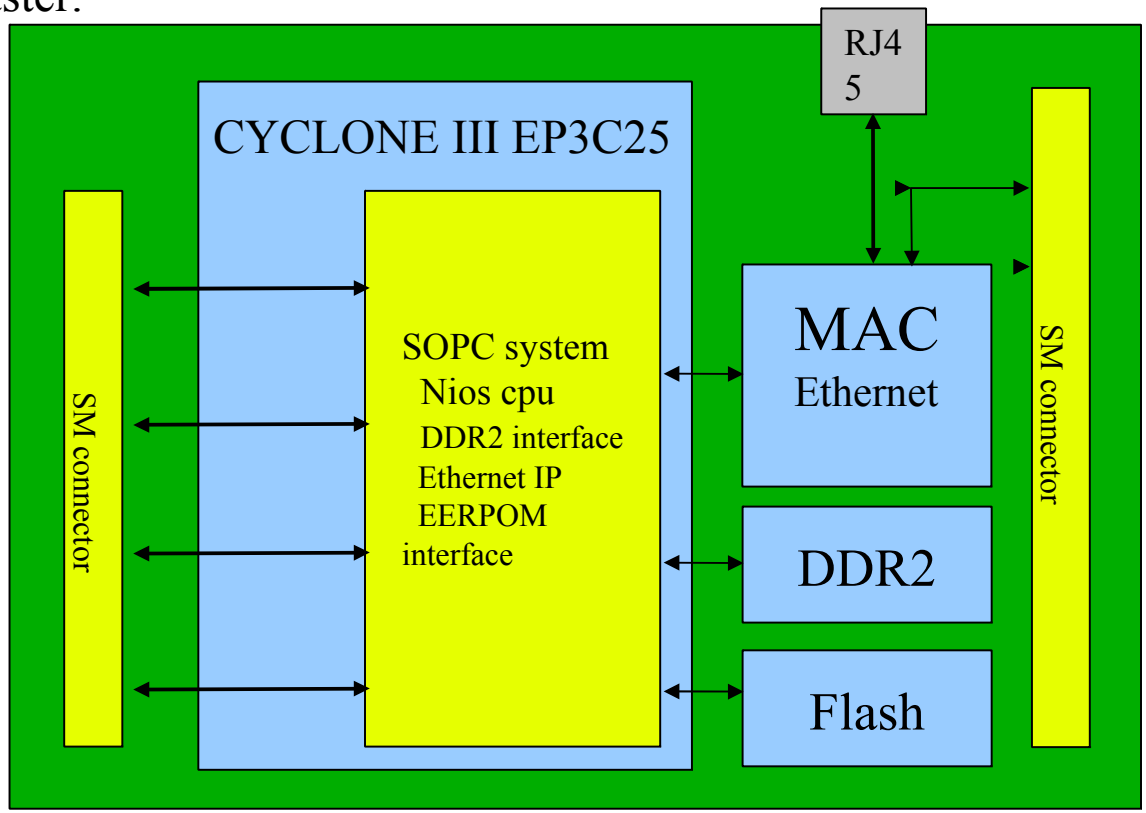


Gigabit Ethernet
Storage Interconnect
AMC Fabric P2P Interconnect
AMC/RTM Extension Ports

Possible solution for off-detector area

Hardware

- Based on Ethernet SPECS master.
- SM connector.
  Parallel bus,Configurable.
  I/O ligne, I2C bus, SPI bus.
  JTAG bus.
- 32MBytes DDR2 memory.
- 16MBytes Flash memory.



Firmware

- Ethernet reconfiguration.
- Cyclone III EP3C25F324.
- Base on NIOS II processor.

Soft

- OS µclinux.
- DIM server.
- SPECS library.
- SPECS users library.

Throttle Switch Module