An introduction to
CLARO
A fast Front-End ASIC for Photomultipliers

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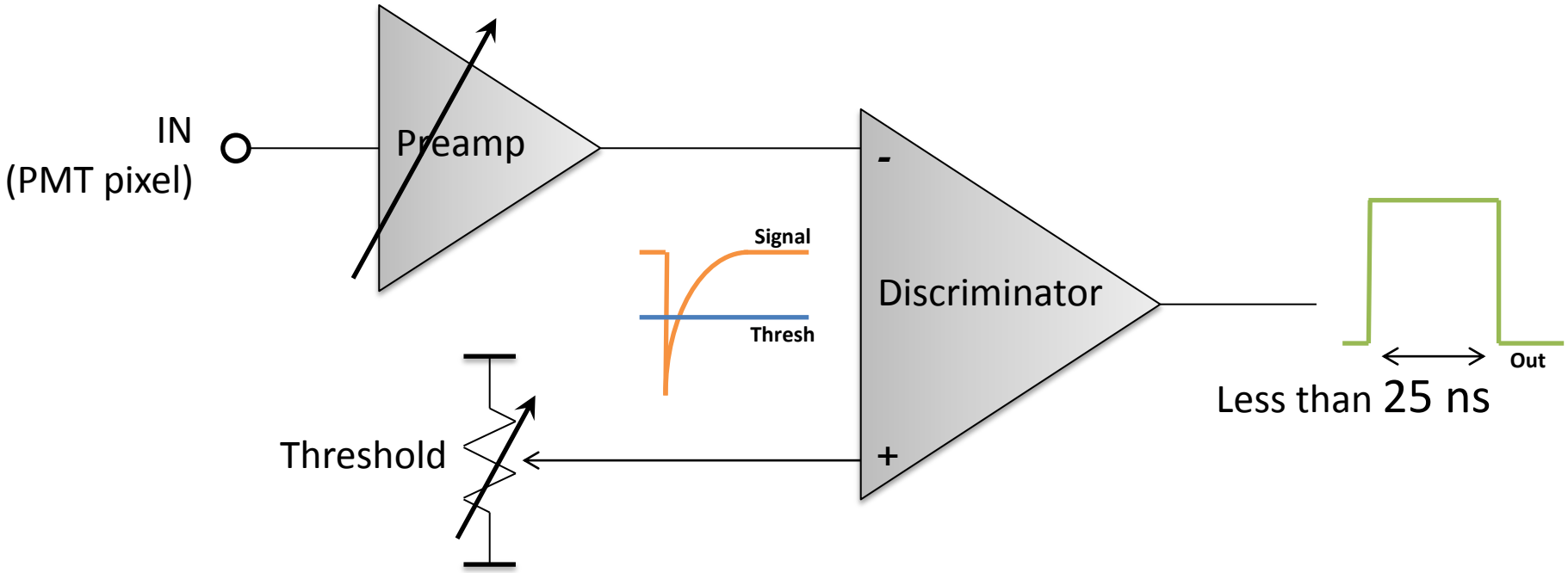
The CLARO Concept (1)

CLARO is a monolithic front-end chip for Multi-anode PMTs (or MCPs).
It is meant to readout Ma-PMTs in the upgraded LHCb RICH detector.

Each channel is made of:

- A charge preamplifier with adjustable gain
- A discriminator with adjustable threshold

The circuit is optimized for 100 ke$^-$ (16 fC) to 10 Me$^-$ (1600 fC) pulses from a 1 pF source.

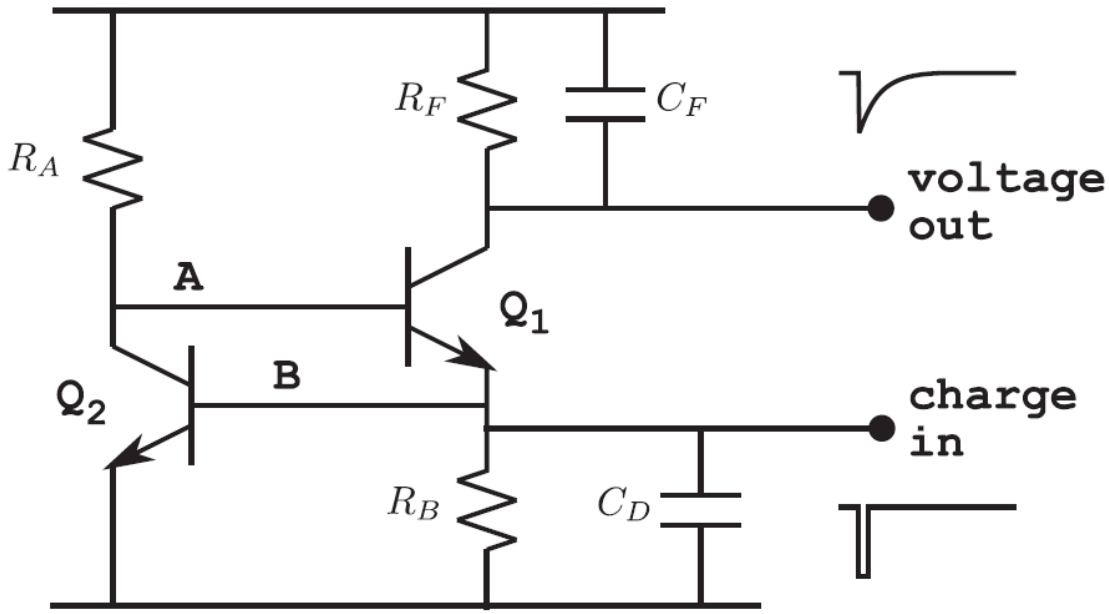


The main features are:

- Power consumption below 1 mW / channel
- No dead time at 40 MHz hit rate

The CLARO Concept (2)

The input stage is an "active cascode" (a.k.a."super common base"), with low input impedance up to high frequency.



In 2010, a prototype built with discrete components was realized.

More details here:

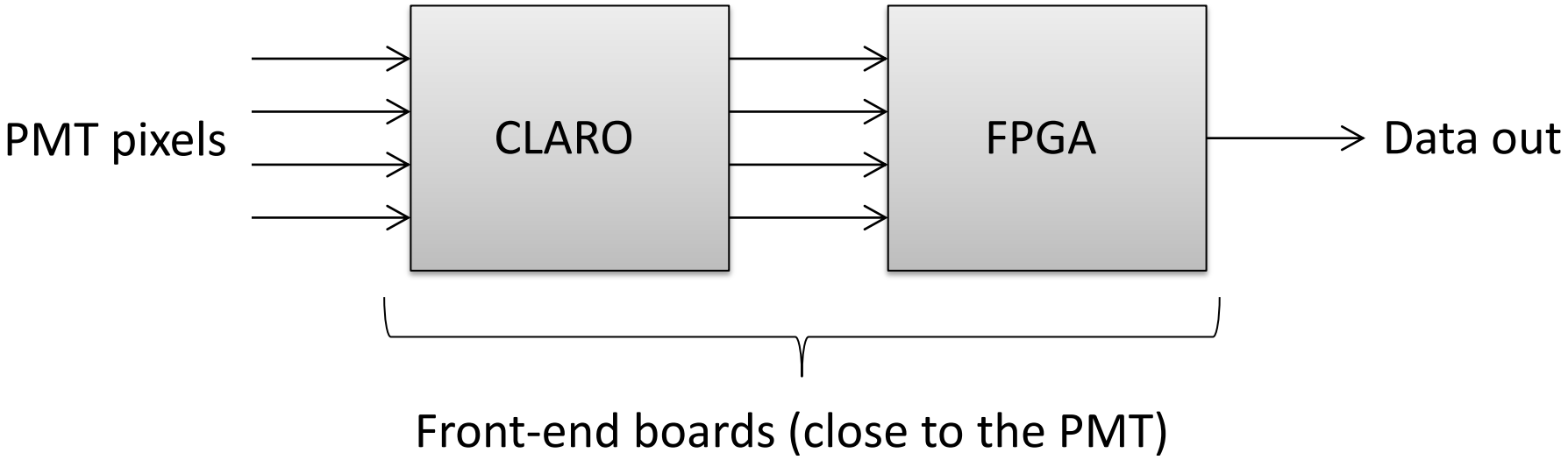
C.Arnaboldi, A.Giachero, C.Gotti, M.Maino, G.Pessina
An ultra fast, low power readout chain for single photon sensitivity with multi-anode photomultiplier tubes for the RICH upgrade at LHCb
Nuclear Instruments and Methods in Physics Research Section A, Vol. 652, Issue 1, pp. 487-490, Oct 2011
DOI: 10.1016/j.nima.2010.10.051

The CLARO Concept (3)

Small chips of 4 or 8 channels are foreseen.

The outputs will feed into a commercial FPGA to perform all fast digital functions (counting, time over threshold, …).

This separation allows to:
- Minimize coupling (noise) between analog and digital
- Reduce time/manpower/cost needed



The CLARO Concept (4)

Two technologies where considered for CLARO:
- 0.35 um CMOS (cheaper)
- 0.35 um SiGe-CMOS (about 30% more expensive; faster)

Both from Austriamicrosystems (AMS).

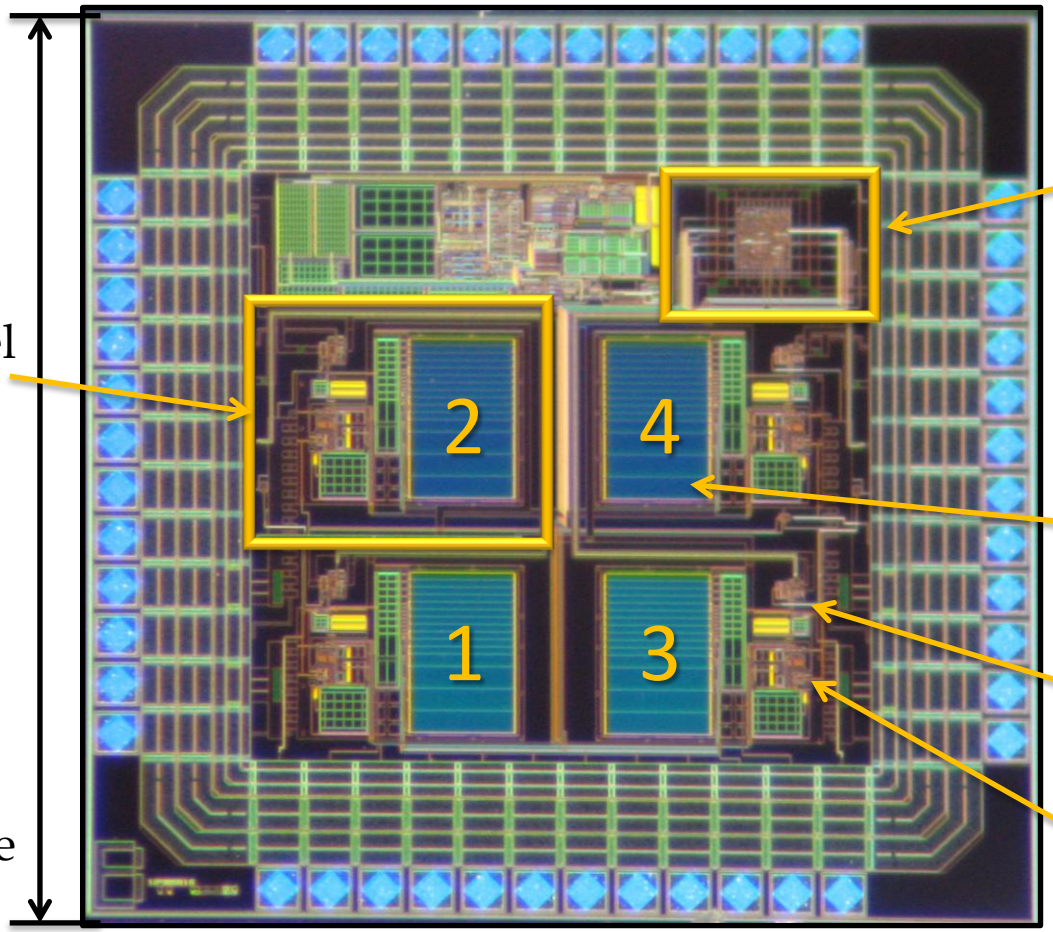
- The first CLARO-CMOS (2+2 channels) was submitted to the foundry in July and received in October; testing is in progress.
- The first CLARO-SiGe (2 channels) was submitted to the foundry at the end of November, and is expected for testing in January 2012.

Both versions are expected to show very low jitter, of the order of a few tenths of ps (lower for the SiGe version than for the CMOS version); it may be used for Time Of Flight (TOF) applications.
The Timewalk can be compensated using Time Over Threshold (TOT) measurement.

The design approach (simple chip + FPGA) allows flexibility to adapt the readout scheme to other similar applications.
- Modified/custom versions of the chip can be realized on the timescale of a few months
- The FPGA can be reprogrammed to fit the application

The first CLARO-CMOS prototype (1)

The first CLARO-CMOS prototype is a "2+2" channel chip.
(Minor differences between channels 1,2 and 3,4)
There are 3 bits for gain and 5 bits for threshold per channel.
Gain and threshold setting is the same for 1 and 3, and for 2 and 4.



One channel

2 mm side

Shift register for gain and threshold setting (16 bits total)

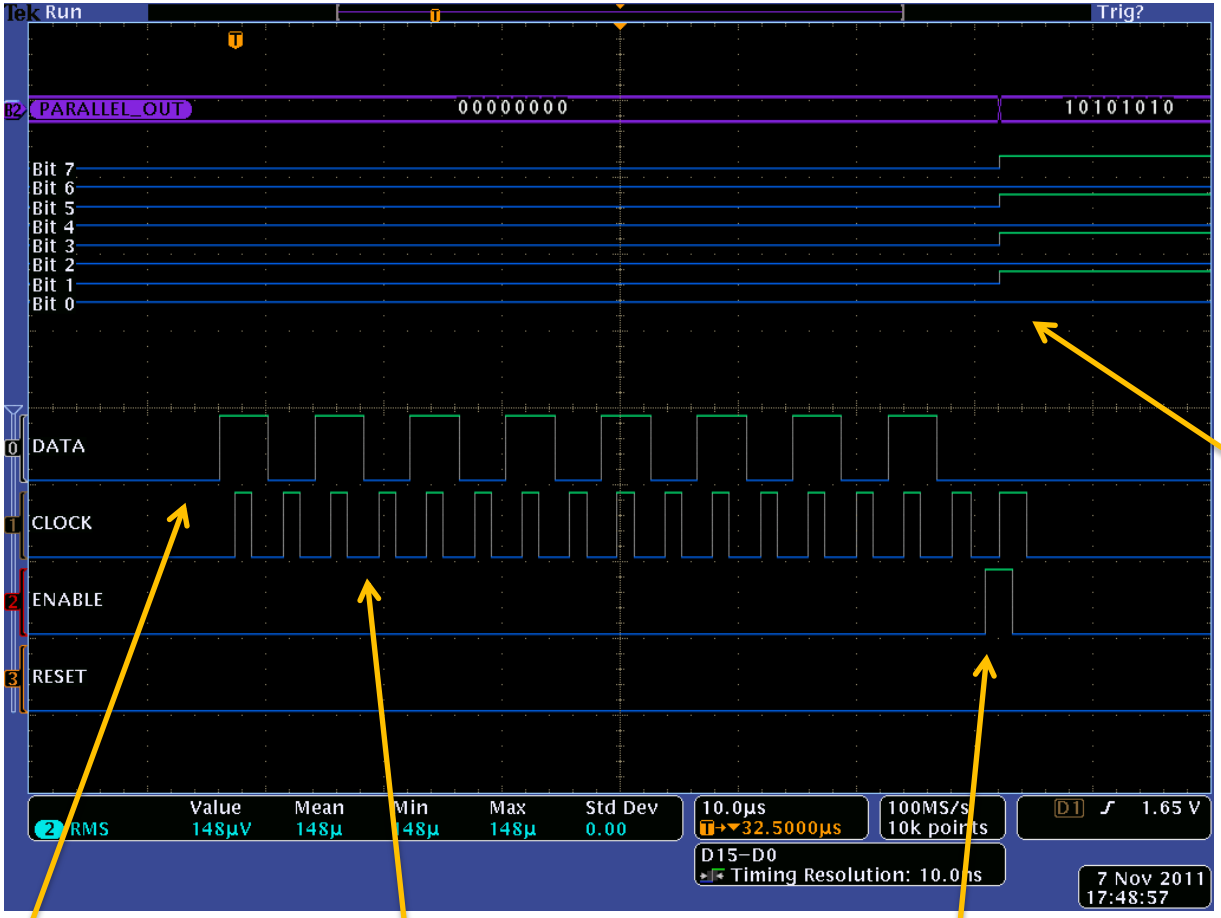
Array of resistors for threshold setting

Discriminator

Preamp

The first CLARO-CMOS prototype (2)

The shift register for gain and threshold setting works fine:



Parallel signals to gain and threshold switches (only 8 of 16 bits are displayed)

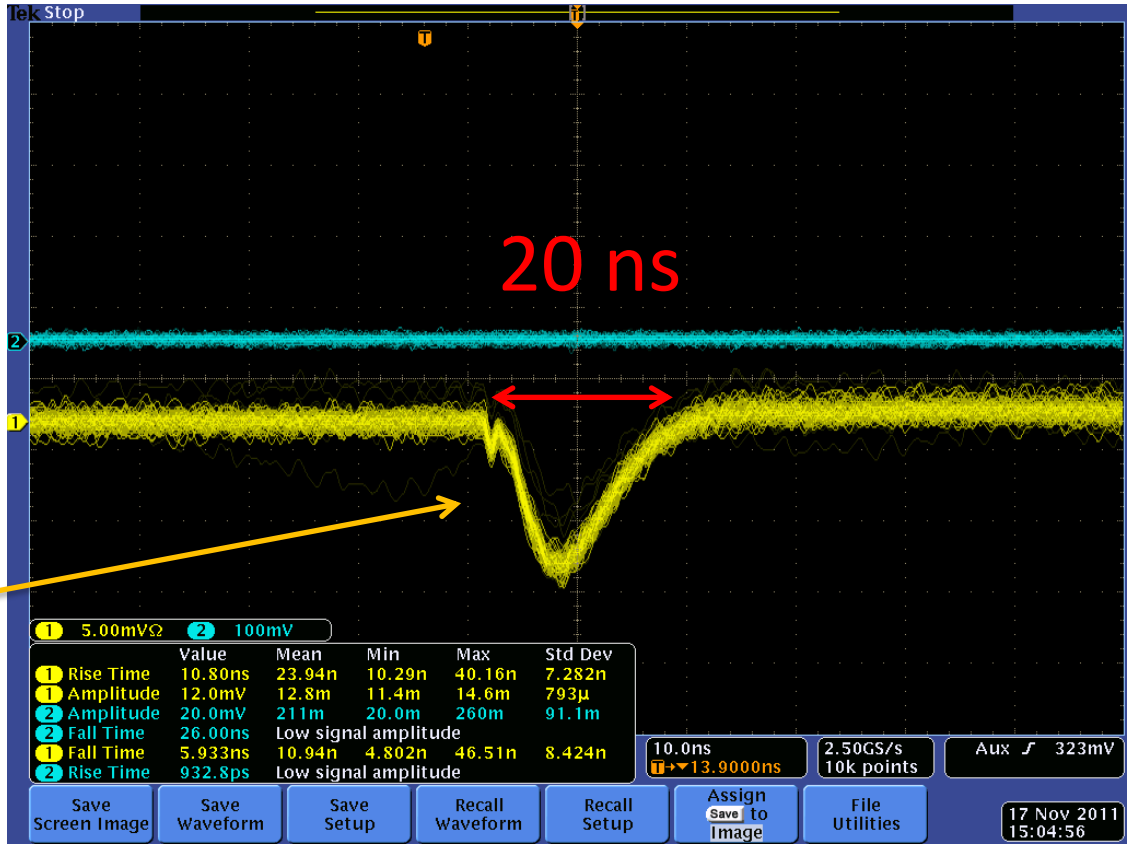
Serial data in (SPI-like)

Slow clock

Enable signal

The first CLARO-CMOS prototype (3)

The output of the preamplifier is buffered to the outside, and the buffer is slower than the preamplifier.
This is the buffered signal in response to charge pulses of about 1 Me:



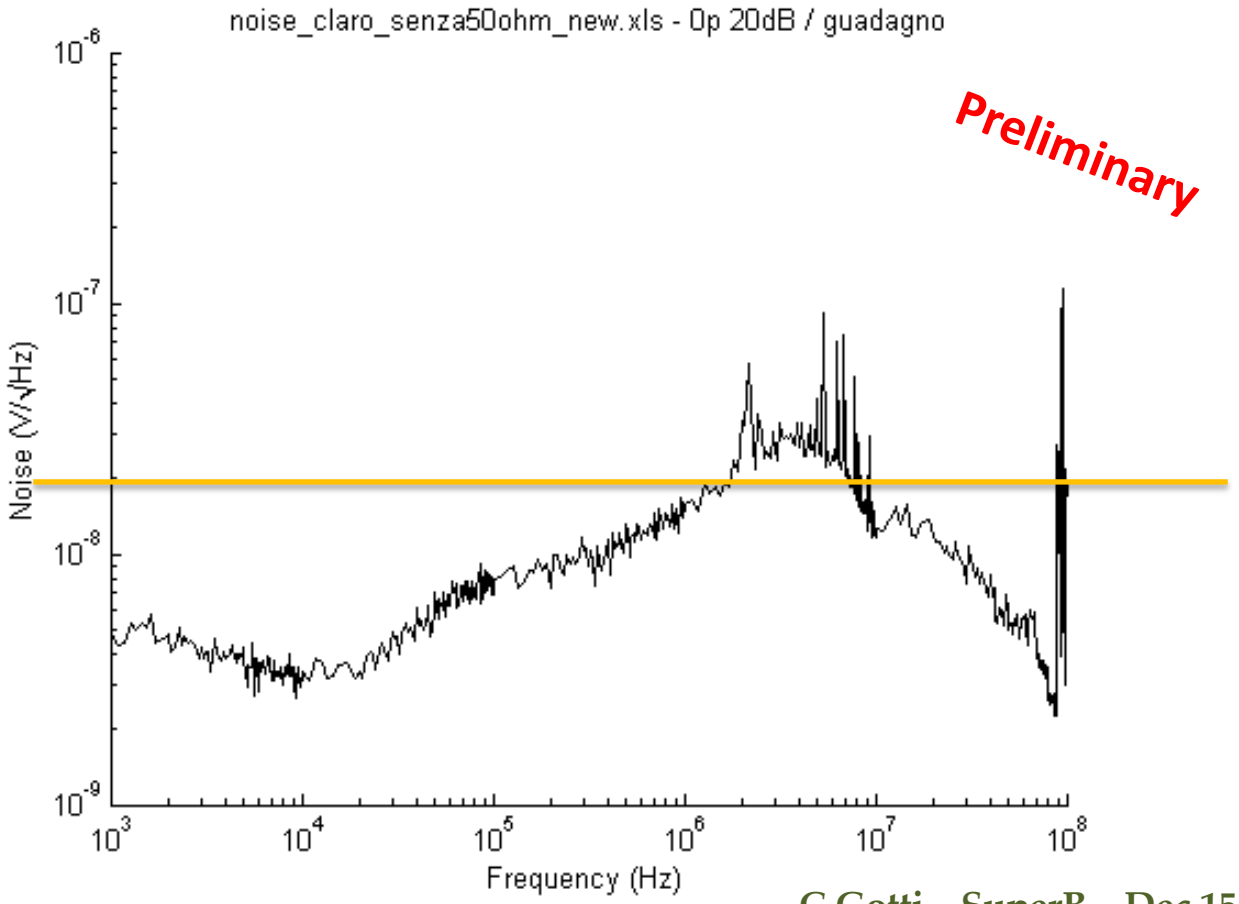
8 ns
peaking time

(We cannot see the output of the preamplifier before the buffer, where the signal is faster and higher.)

The first CLARO-CMOS prototype (4)

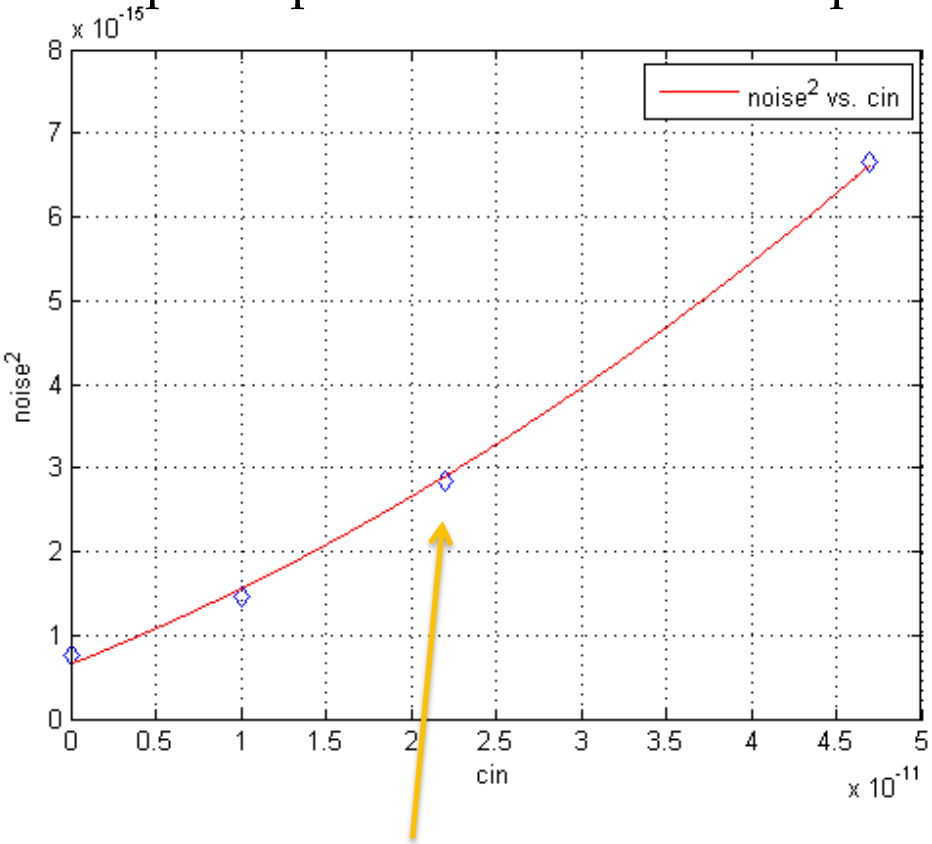
Noise at the output of the preamplifier (at the input of the discriminator) is about 20 nV/ √Hz.
This corresponds to about 300 uV RMS at the output; or about 1000 e^- at the input, matching simulations.

20 nV/ √Hz



The first CLARO-CMOS prototype (5)

Noise of the preamplifier was measured vs capacitance at the input.
The curve of noise^2 vs input capacitance shows the expected behaviour.



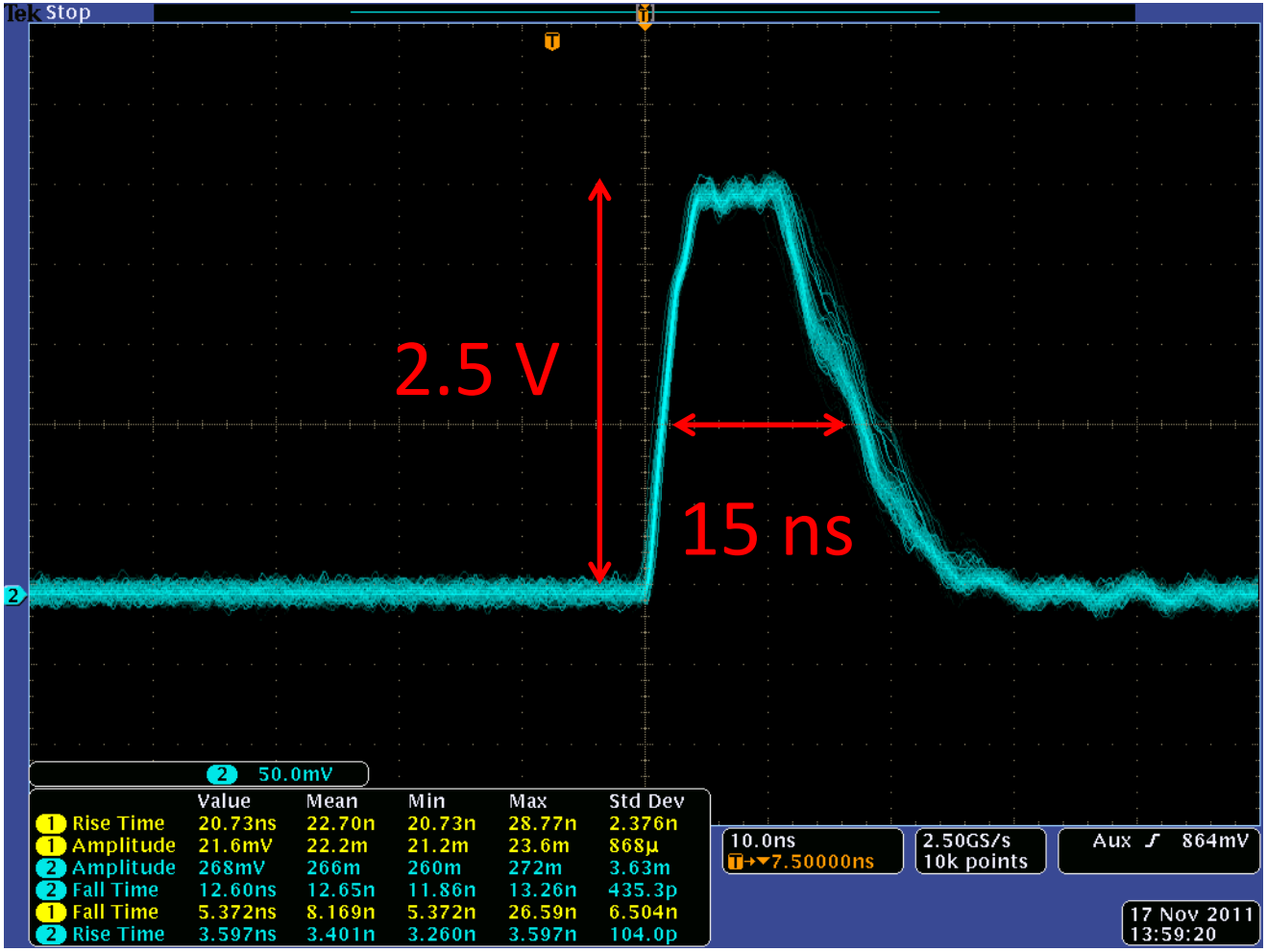
Preliminary

Squared max of noise spectrum (nV^2 / Hz)

At 25 pF input capacitance, noise is about 900 uV RMS at the output, or about 3000 electrons (0.5 fC) at the input, although the circuit is not optimized for such capacitance (being intended for 1 pF pixels).

The first CLARO-CMOS prototype (6)

This is the output of the discriminator for 1 Me^- test pulses:



- Threshold: 300 ke^-
- Power: 1 mW
- Rise time: 3 ns
- Fall time: 10 ns
- Pulse width: 15 ns
- Pulse height: 2.5 V

The first CLARO-CMOS prototype (7)

We believe the performance (speed, noise) is limited by the package parasitics.

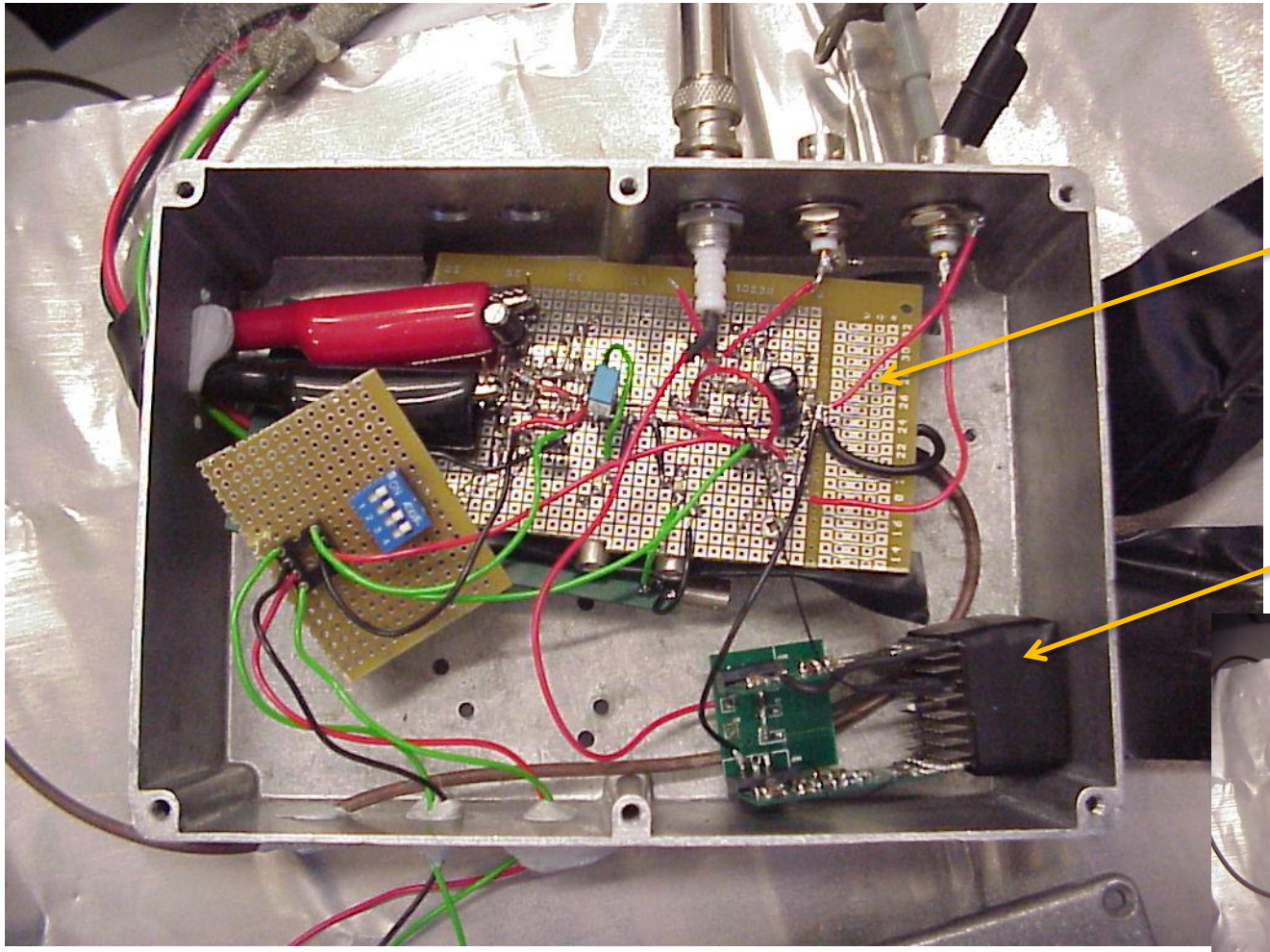
DIL48

(Parasitics of about 3 to 5 pF capacitance, 5 to 10 nH inductance on inputs and outputs)

This package was the cheapest, and was meant for early testing.
We already placed and order to have more chips in a much smaller QFN48 package.

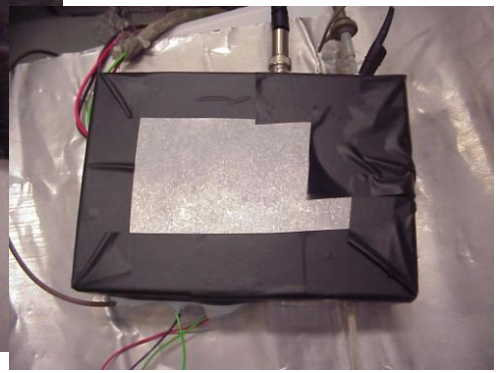
The first CLARO-CMOS prototype (8)

We coupled the chip to the new R11265 Multi-anode PMT (the baseline for the LHCb RICH upgrade).



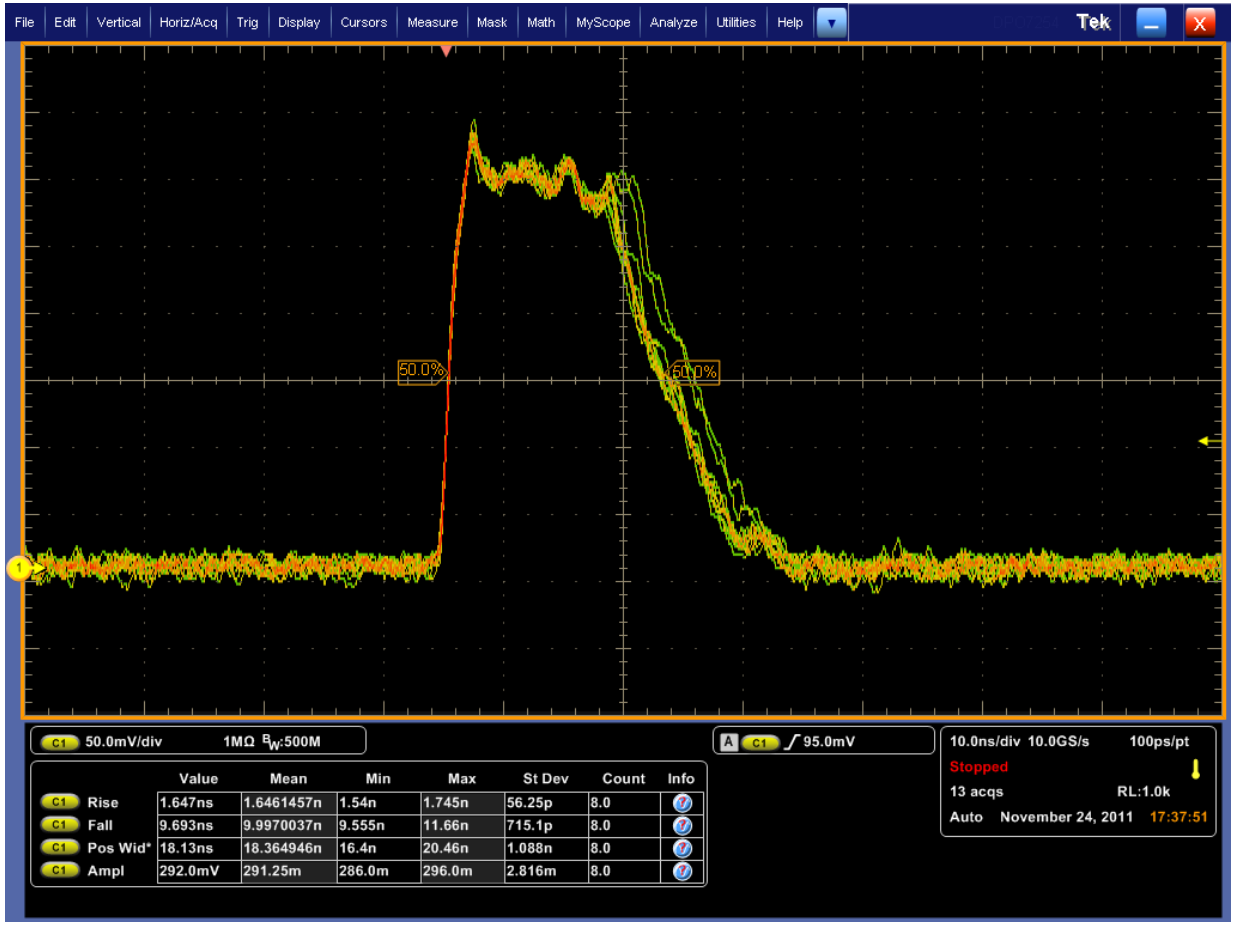
CLARO test board
(the chip is on the back)

R11265 PMT



The first CLARO-CMOS prototype (9)

Discriminator output for single photons on the R11265 Ma-PMT:



R11265 PMT
Biased at 900 V

The power supply was increased to 3.3 V: rise time dropped to 2 ns.
(Power consumption is still about 1 mW / channel.)

Conclusions/Open issues

The first prototype of the CLARO-CMOS chip works, reading signals from the new R11265 PMT in 25 ns, with 1 mW power consumption per channel.

Results are very close to simulations; discrepancies seem to be related to parasitics on inputs and outputs.

Deep characterization is in progress.

- Jitter of this CMOS version will be measured in the next days
- A smaller package (QFN) was ordered, and is expected in about 1 month
- Radiation hardness tests will be planned
- The SiGe version (2 channels) was submitted to the foundry a few weeks ago; it is expected for testing in January 2012

A CLARO-based ASIC for SuperB

The CLARO chip "as is" is not optimized for an application in SuperB.

But the design can be modified, and dedicated versions can be made.

The key point is that for simple chips as the CLARO, with only a few tenths of transistors per channel, customizations of the design can be performed on a short (months, and not years) timescale.

• Already spoke with Giulietto Felici to probe a possible application in the DCH.

• If others groups are interested, we can talk and see if the design can fit the requirements of other SuperB subdetectors.

- Thank you! -