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SuperB meeting
Frascati

Update on Strasbourg activities

on CMOS pixel sensor developments for the SuperB SVT

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current work plan: chip design

Migration to 0.18 µm technology to improve ionising radiation tolerance.

- Focus on optimising performances of the charge collection system and the in-pixel pre-amplification (S/N, noise reduction).
- In synergy with INFN groups.

1) MISTRAL sensor:
Translation of MIMOSA chip from 0.35 µm to 0.18 µm technology.
First real scale prototype for ALICE and CBM in 2013, with **read-out time 20-40 µs**
➔ MIMOSA-32 in 0.18 µm **has been submitted in October 2011**.

2) Design of a new chip with faster read-out time **2-3 µs** foreseen for 2016:

- Optimisation of the rolling shutter read-out.
- Sparsification: sophisticated sampling.
- Simultaneously addressing 2 rows.
- Elongated pixels. ⟶ need to compensate for the resolution loss: cf. PLUME (next slides)
- In-pixel discrimination.

Expected power dissipation: 300-500 mW.cm^{-2}

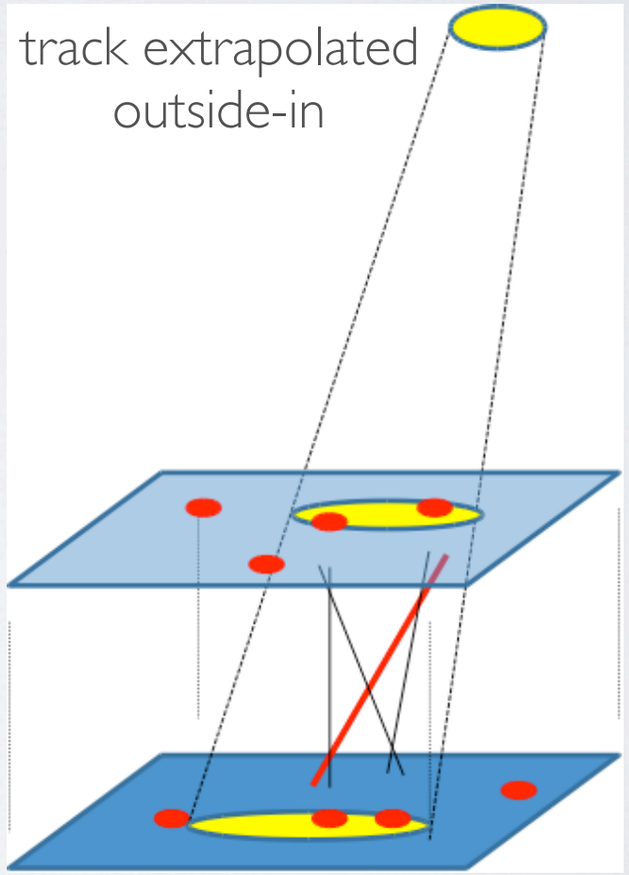
current work plan: system integration

- Evaluation of the asset of a double-sided layer of CMOS pixel sensors:
  - Better association to the extrapolated track thanks to the mini-vector approach.
  - Need to do global studies of the tracking performances of this approach because of the interplay between the different layer performances: the quality of the extrapolated track is a key parameter!
  - Both sides of the ladder can be equipped with CMOS pixel sensors differently optimised

➔ **combination of time stamping on one side and spatial resolution on the other side.**

- Pixelated ladder development with ultra-low material embedding: the PLUME project (see recent results on next slide).

- Design of the low mass flex cable (Sernwiete) with total material budget < 0.15 % X_0.



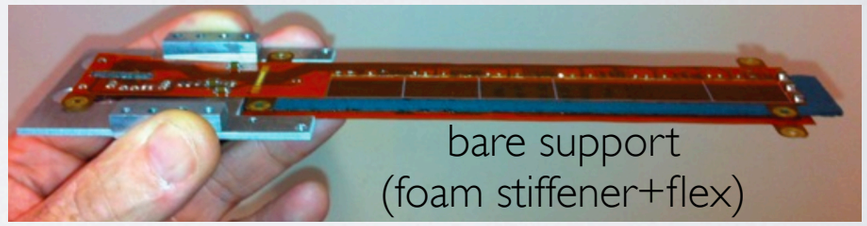
the PLUME project

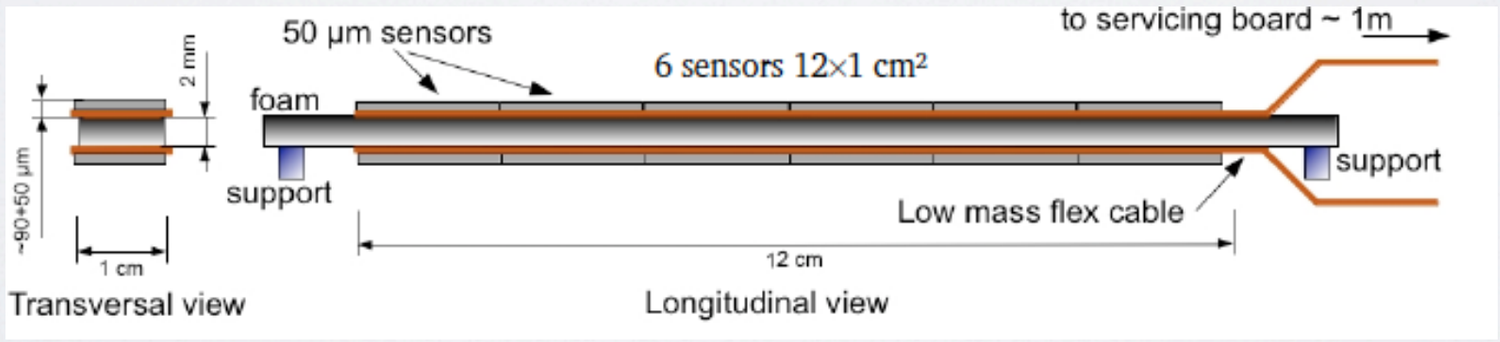
Pixelated Ladder with Ultra-low Material Embedding
collaboration between IPHC Strasbourg, DESY, Oxford and Bristol
see: http://www.iphc.cnrs.fr/CMOSILCPLUME.html

- Motivation: ILD vertex detector at the ILC.
- Goal: to achieve by ≥ 2012 a prototype double-sided ladder equipped with CMOS pixel sensors with material budget ≤ 0.3 % X_0

➛ added value of a double-sided layer w.r.t. a single-sided layer?

- Design: sensitive area 2x12x1 cm^2
  2x6 MIMOSA-26 thinned down to 50 µm
  binary read-out
  air cooling



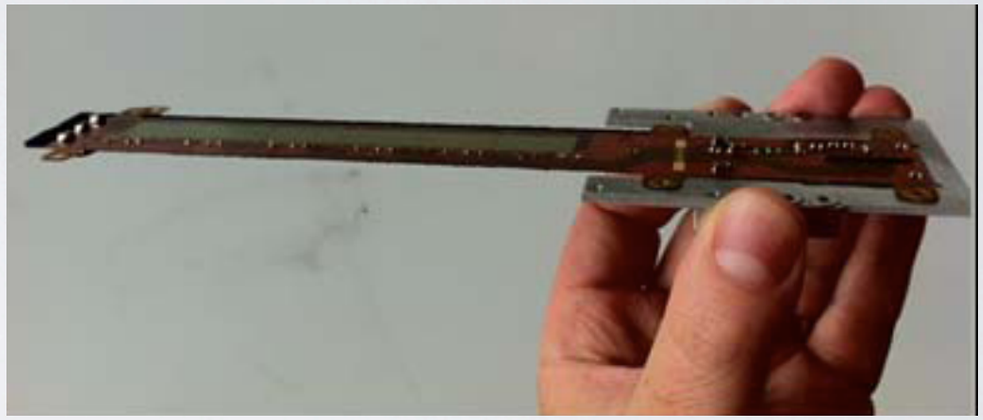


latest PLUME results (1)

- 2011 prototype:

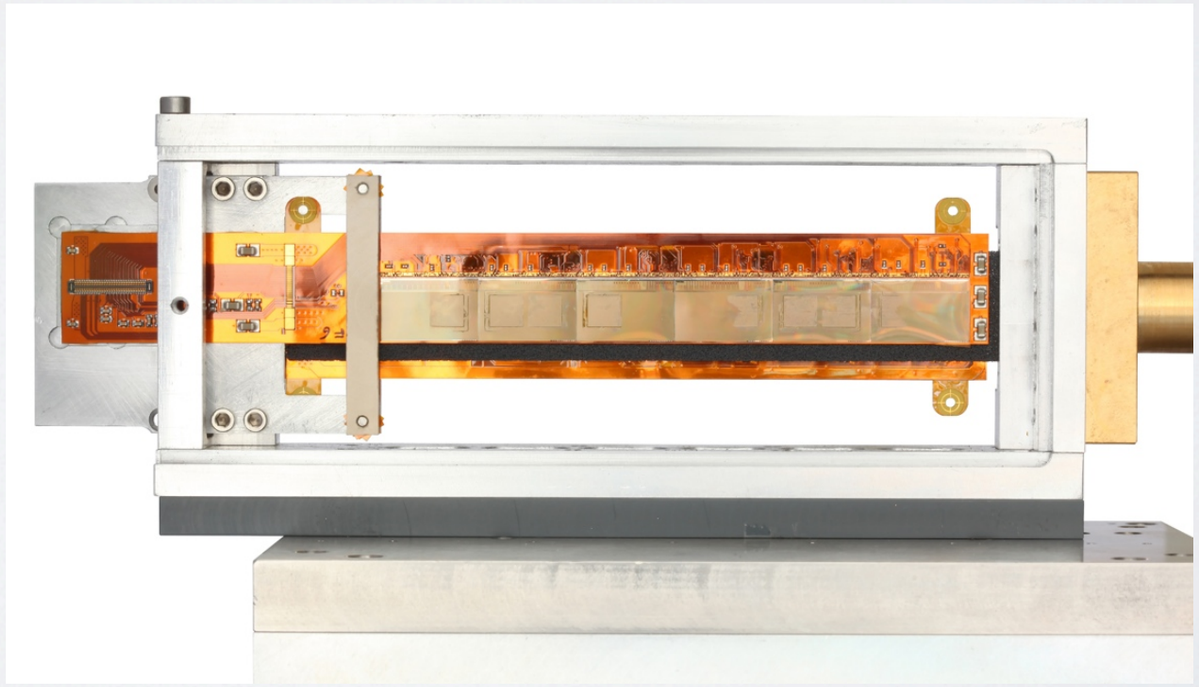
First double-layers ladders equipped with 12 EUDET sensors (0.35 µm) have been constructed and **tested on beam at SPS in November 2011**:

- 2x6 MIMOSA-26,
- sensitive area 2x12x1 cm^2, 2x4x10^6 pixels,
- digital read-out,
- resolution 3 µm,
- **total power consumption 6 W**,
- **total material budget 0.6 % X_0**,
- air cooling 3 $m.s^{-1}$.



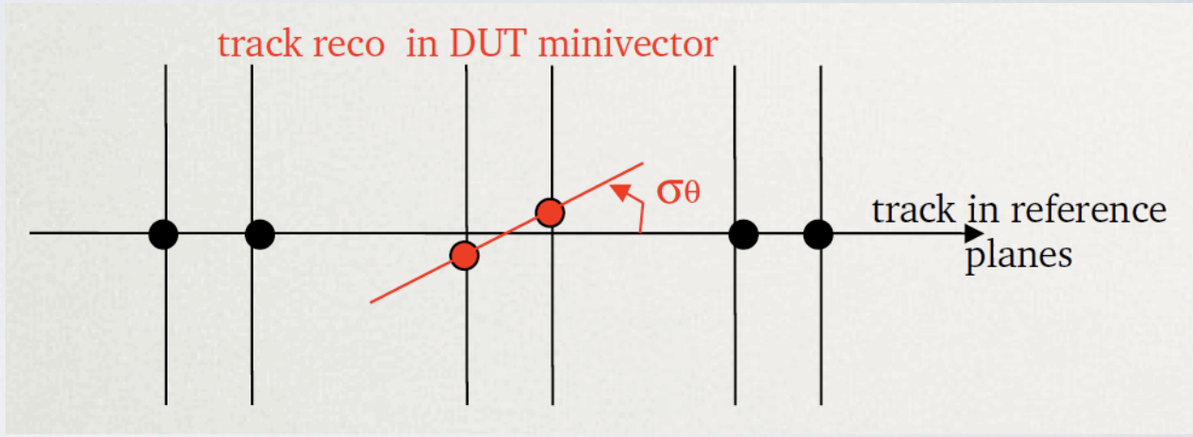
- Next step: 2012 prototype

Optimised for material budget: **0.35 % X_0 for a complete double layer**.



latest PLUME results (2)

The track reconstructed in the telescope is extrapolated to the double-sided ladder equipped with CMOS pixel sensors.
Hits from each side of the ladder are paired to build mini-vectors.
These mini-vectors are matched to the extrapolated track.



preliminary result on vertical residual

preliminary result on angular residual