



Istituto Nazionale di Fisica Nucleare

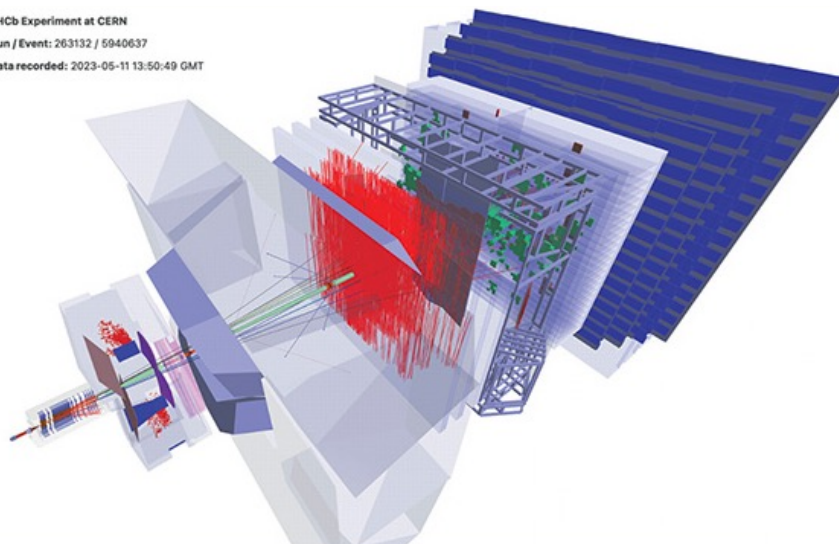


The LHCb Upstream Tracker: Operations and Performance in Run3



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 LHCb Experiment at CERN
Run / Event: 263132 / 5940637
Data recorded: 2023-05-11 13:50:49 GMT



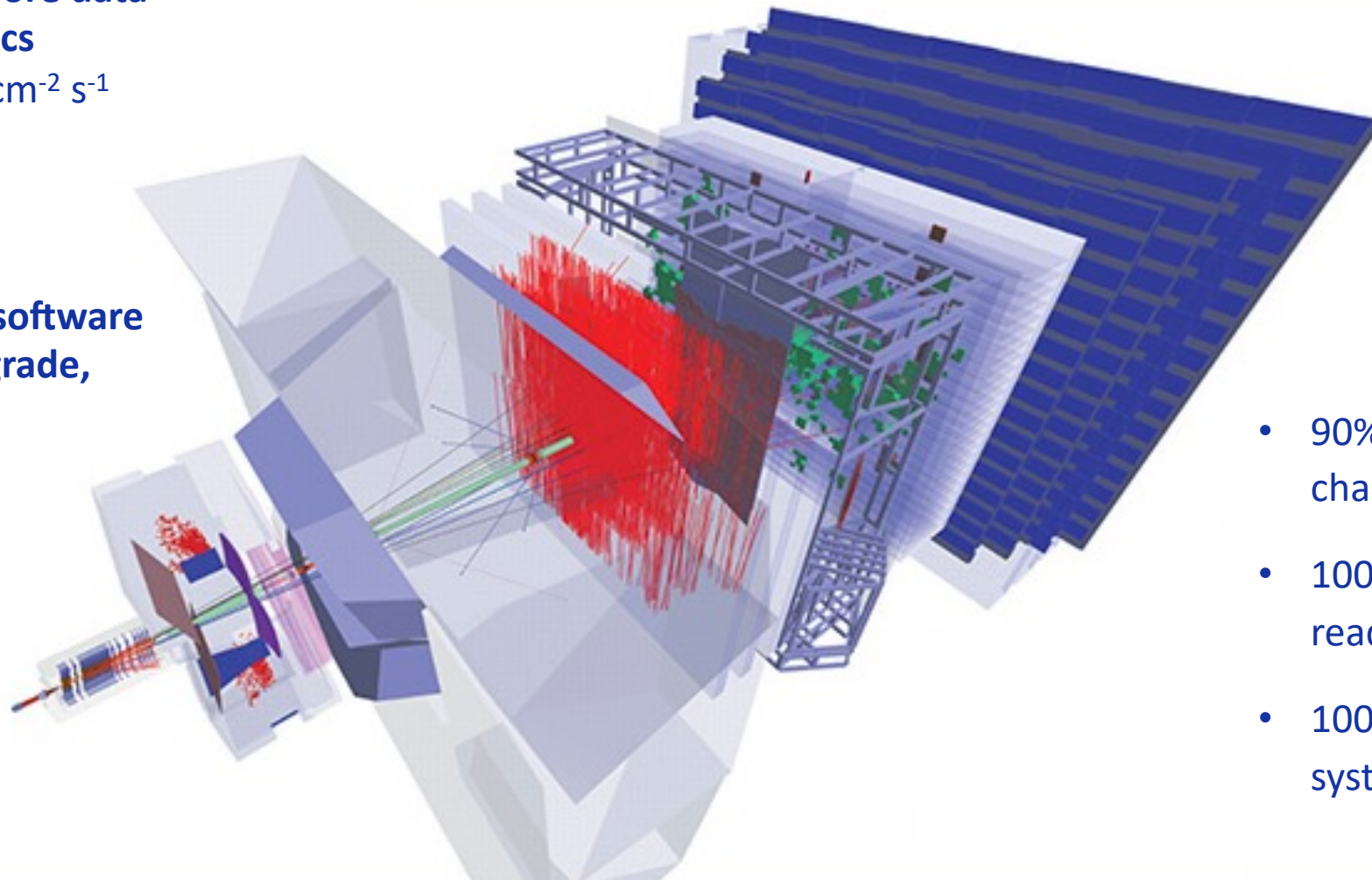
The LHCb experiment



Run 3 goal: collect **more data**
to improve the **physics**
results $\rightarrow L = 2 \cdot 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$

Main limitation:
L0 hardware trigger

BRAND NEW LHCb: software
trigger, detector upgrade,
change of readout
electronics



- 90% of the detector channels upgraded
- 100% replacement of readout electronics
- 100% new DAQ & online system @ collision rate

The LHCb experiment

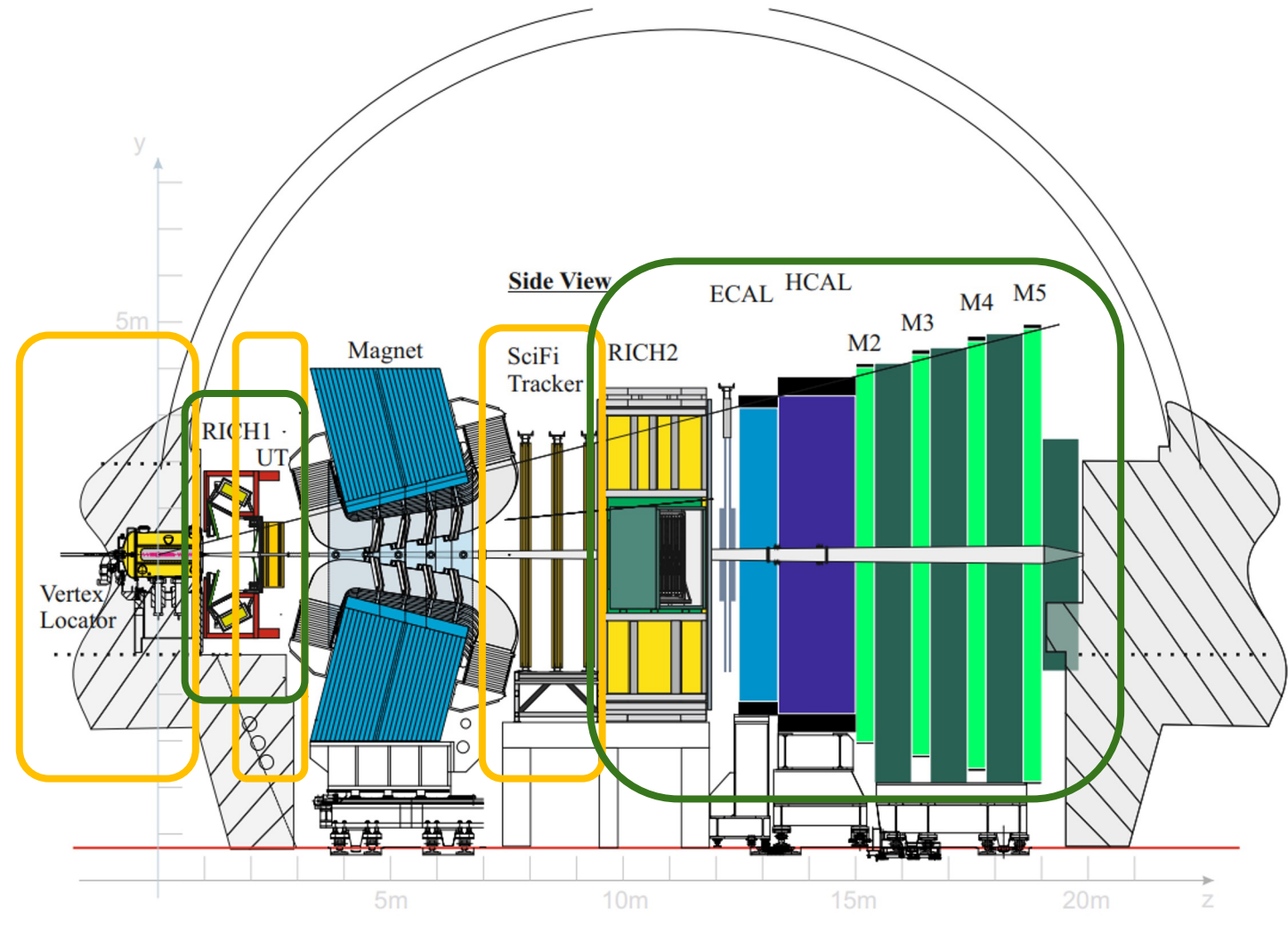


Single-arm
forward
spectrometer

Pseudorapidity
range: $2 < \eta < 5$

Tracking system

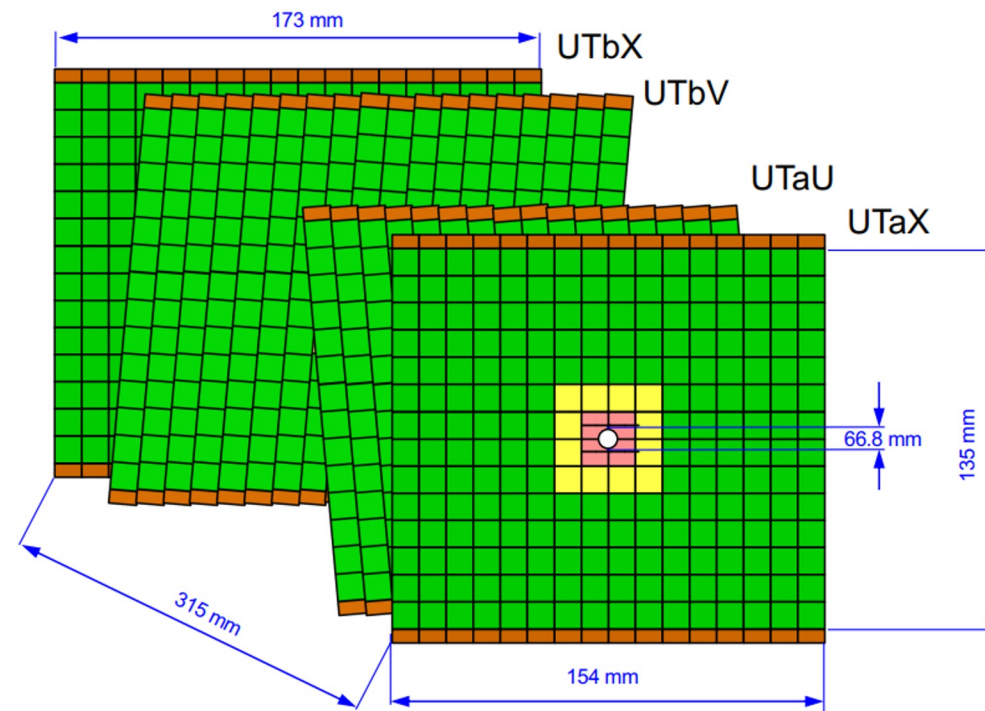
Particle identification
system



Upstream Tracker (UT)



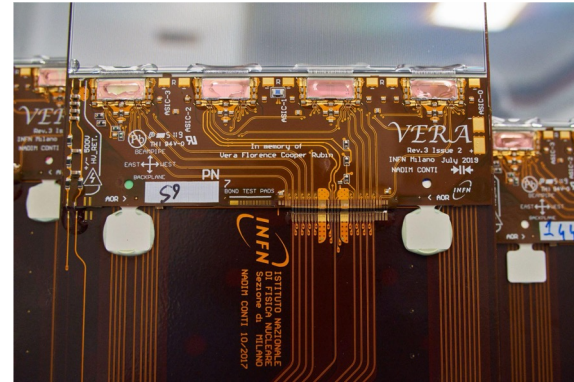
- Silicon strip detector
- 4 layers with vertical and stereo (± 5 deg) orientation
- divided in 2 sides: A-side and C-side
- organized in 68 staves



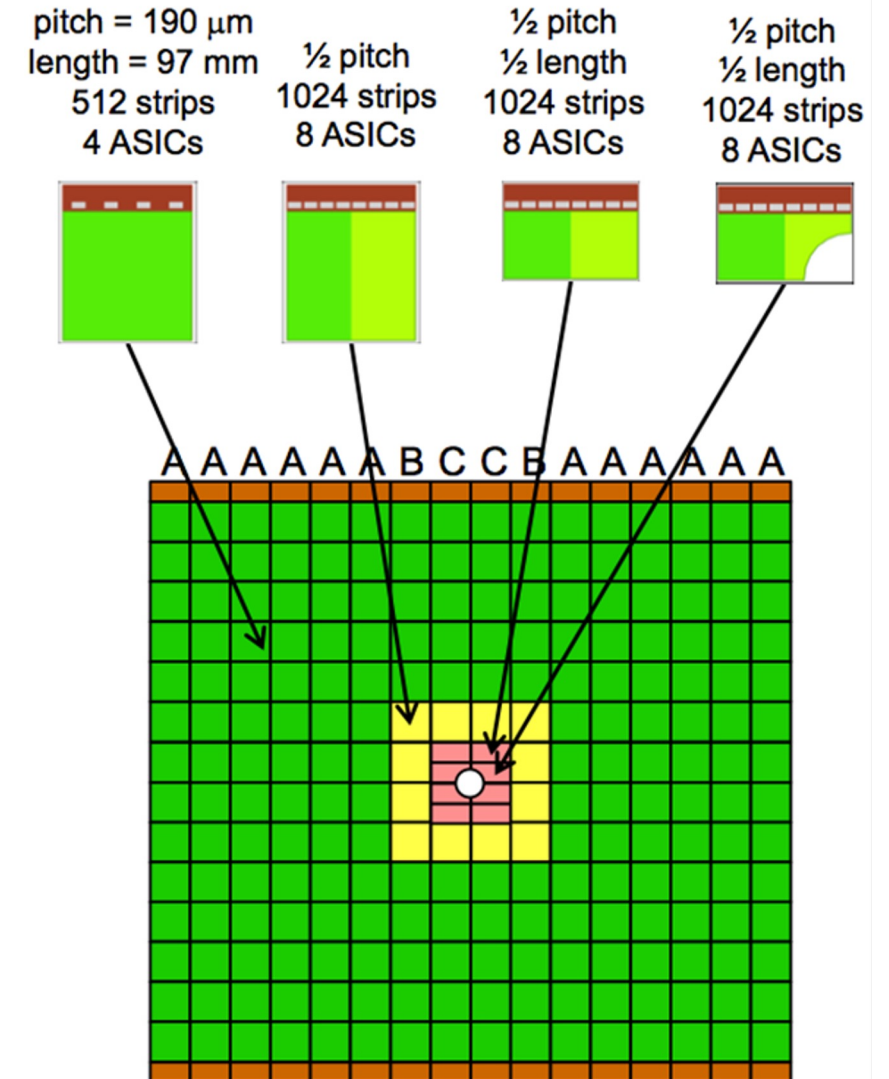
Upstream Tracker (UT)



Modules



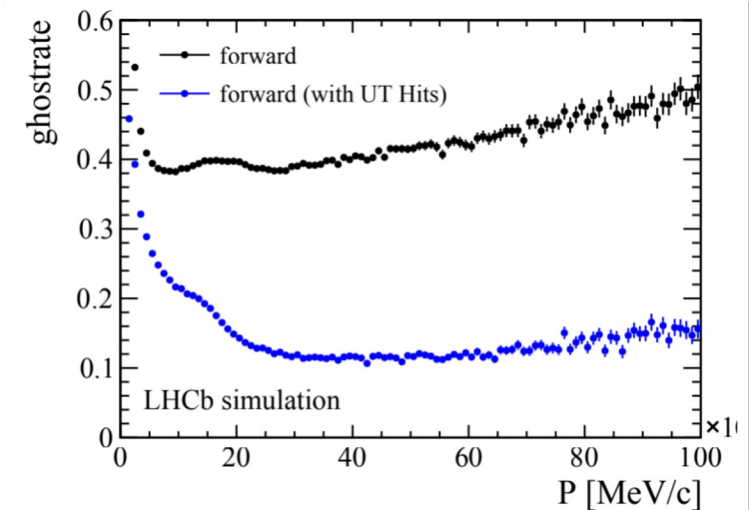
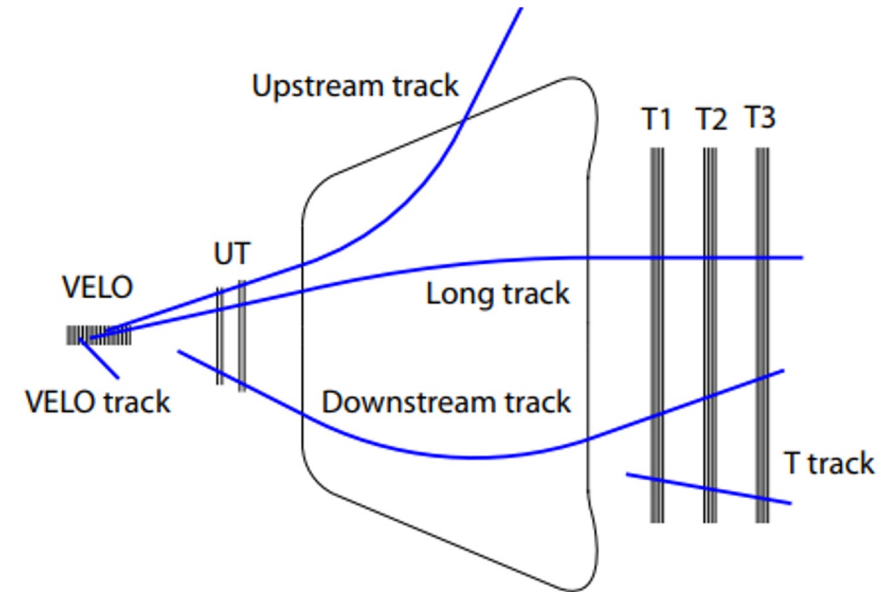
- **silicon micro strip sensors (A-Type: p-in-n; B-, C-, D-type: n-in-p)**
- Hybrids: VERA (4 ASICs), SUSI (8 ASICs)
- Front-end ASIC (**SALT**) glued and bonded to hybrid flex
- Ceramic stiffener (PBN): good thermal conductivity and electrical insulation



Importance of UT in LHCb



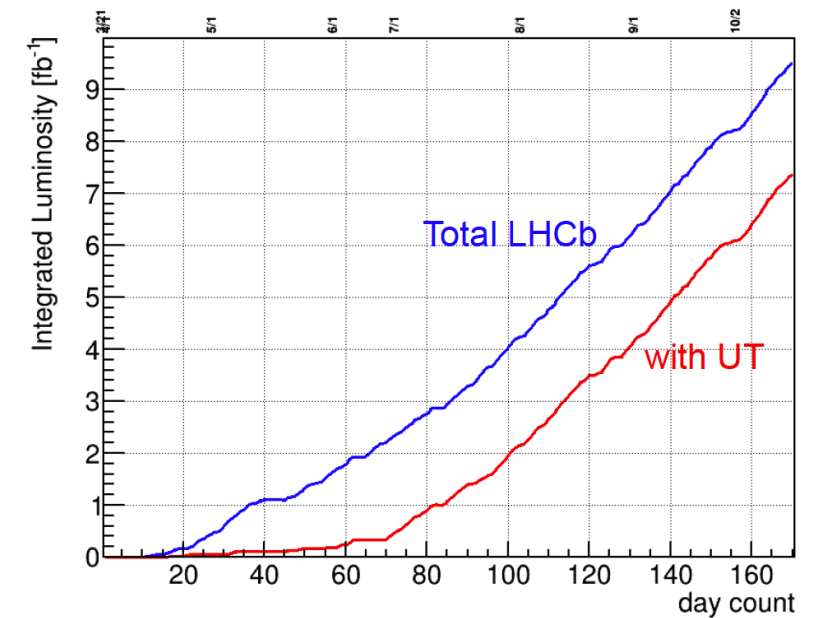
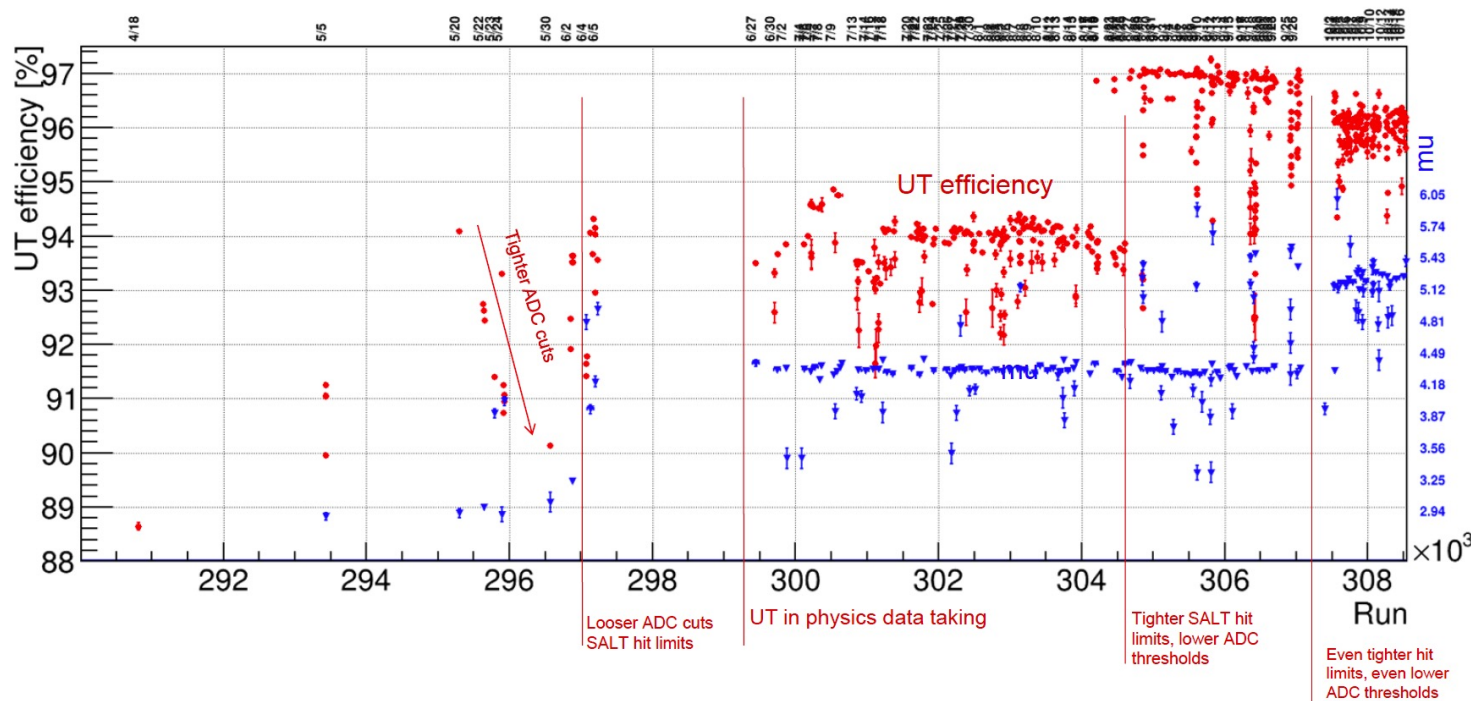
- **Ghost rate** reduction: factor 2 improvement, essential for the software trigger
- **Long lived particles reconstruction** decaying after the VELO (e.g. Λ , K^0_S)
- Track reconstruction: UT fundamental to improve the **momentum resolution** of Long tracks



Run 3 timeline



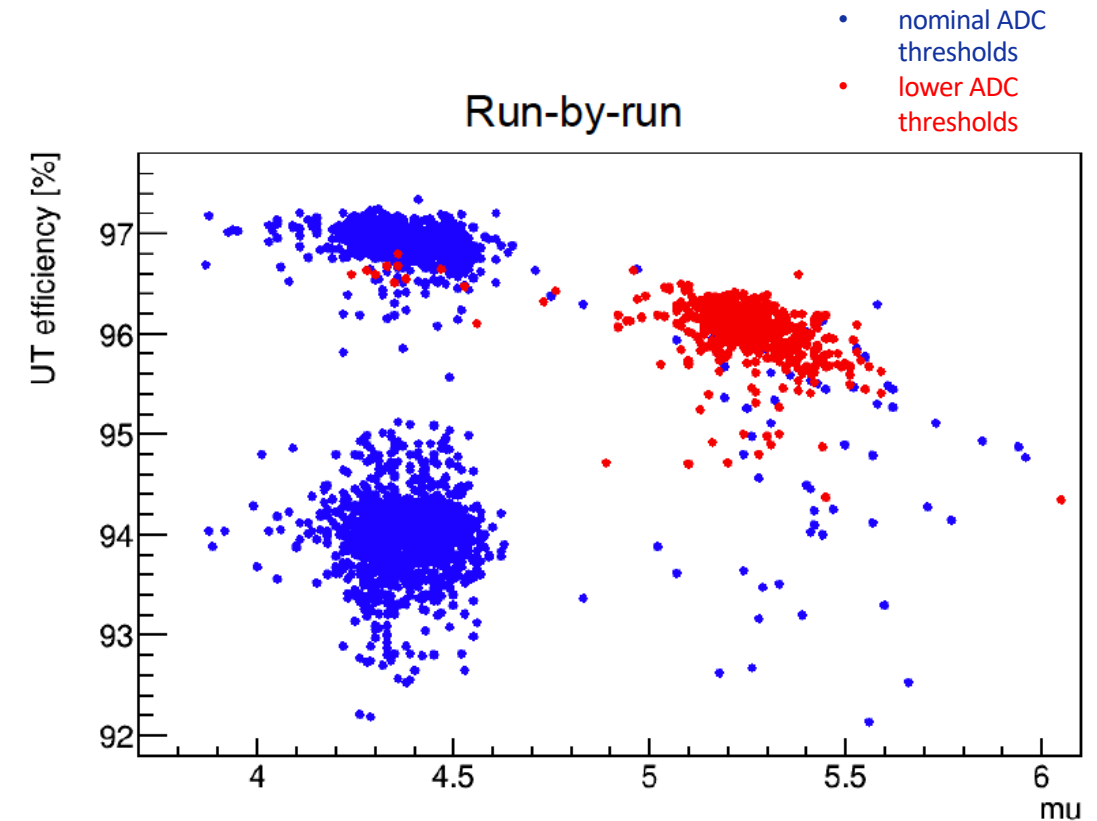
- November 2023: first data collected in the Global LHCb data taking during the Ions run (Pb-Pb collisions).
- Spring 2024: commissioning of the settings for the Global data taking.
- Summer 2024: the UT detector has been included in both HTL1 and HLT2.
- Now: reached stable and efficient data taking with both proton and ion collisions.



DAQ performance



- Stable data taking was achieved, including the highest collision rates (μ).
- Firmware adjustments and FE parameter tuning were necessary to achieve this result.
- Looser ADC thresholds increase the overall efficiency but are a challenge for the data acquisition at high luminosity.

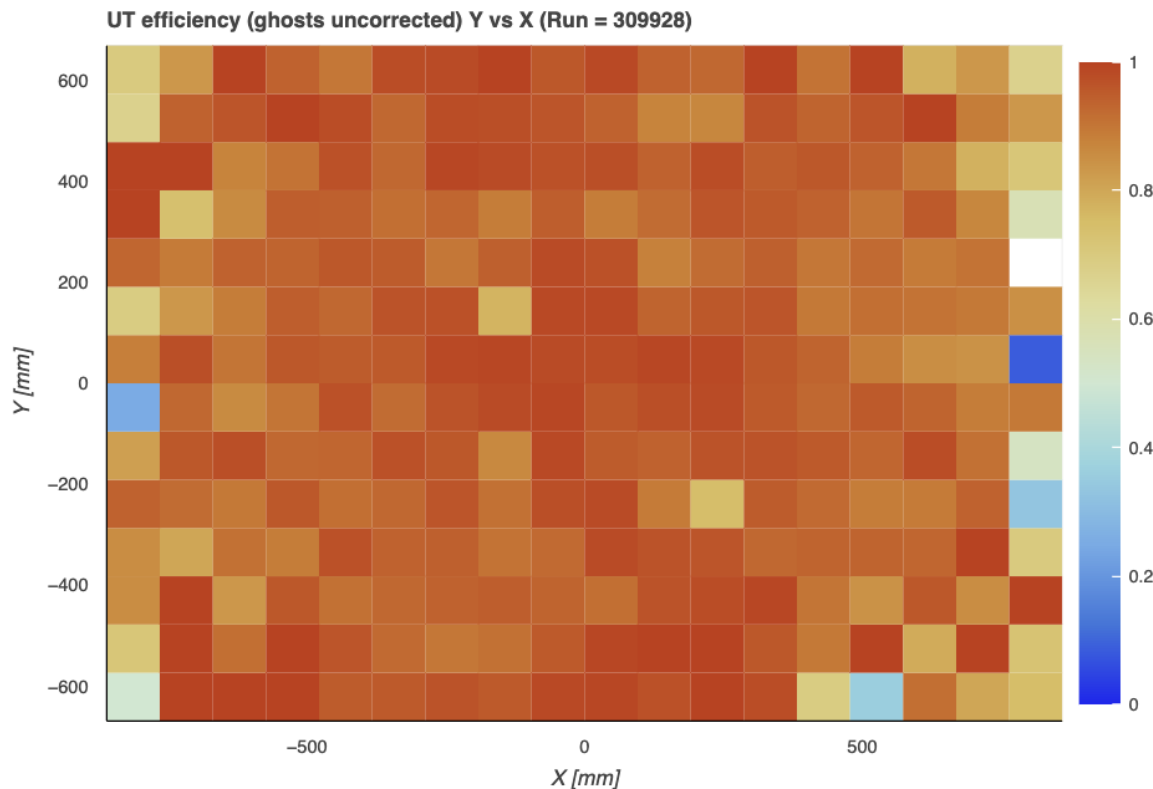


pp reference run

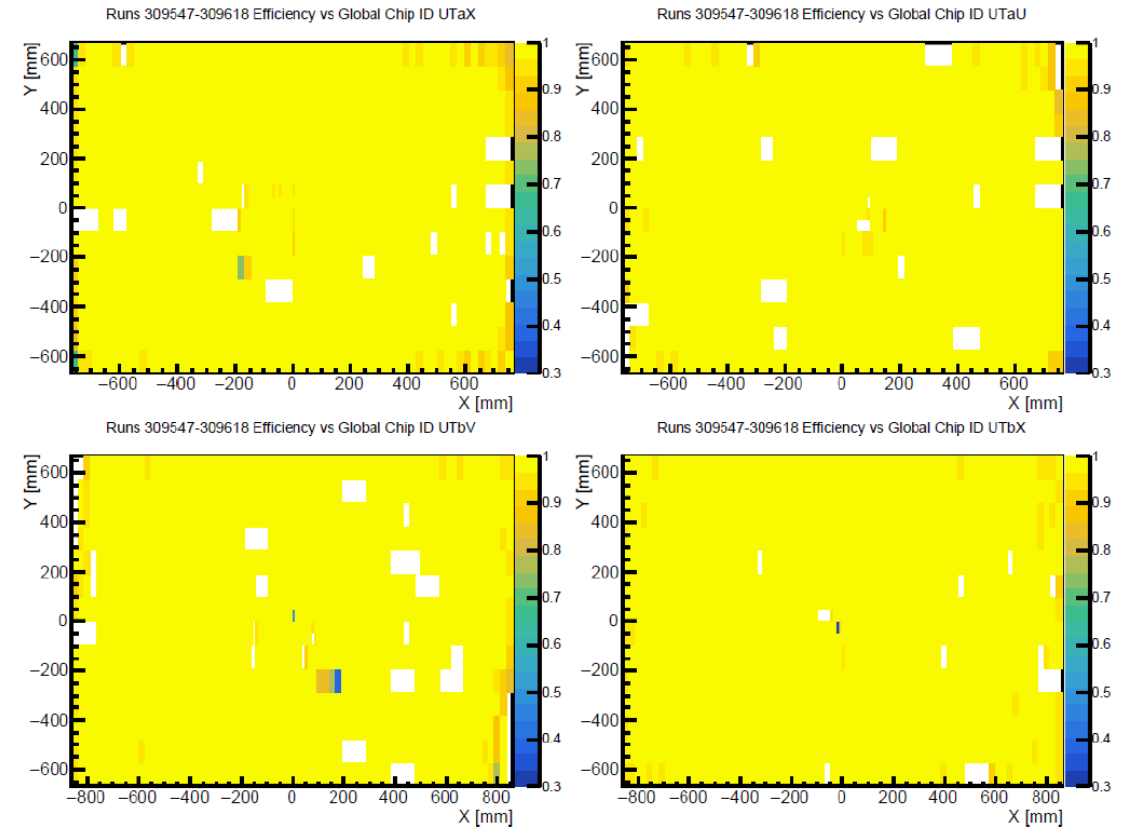


Very stable data taking and good efficiency during Run 3 pp reference run performed the last week of October 2024.

- Overall Tracking efficiency



- Monitoring plots of DAQ efficiency vs Chip ID during the pp reference run at low energy and low luminosity.



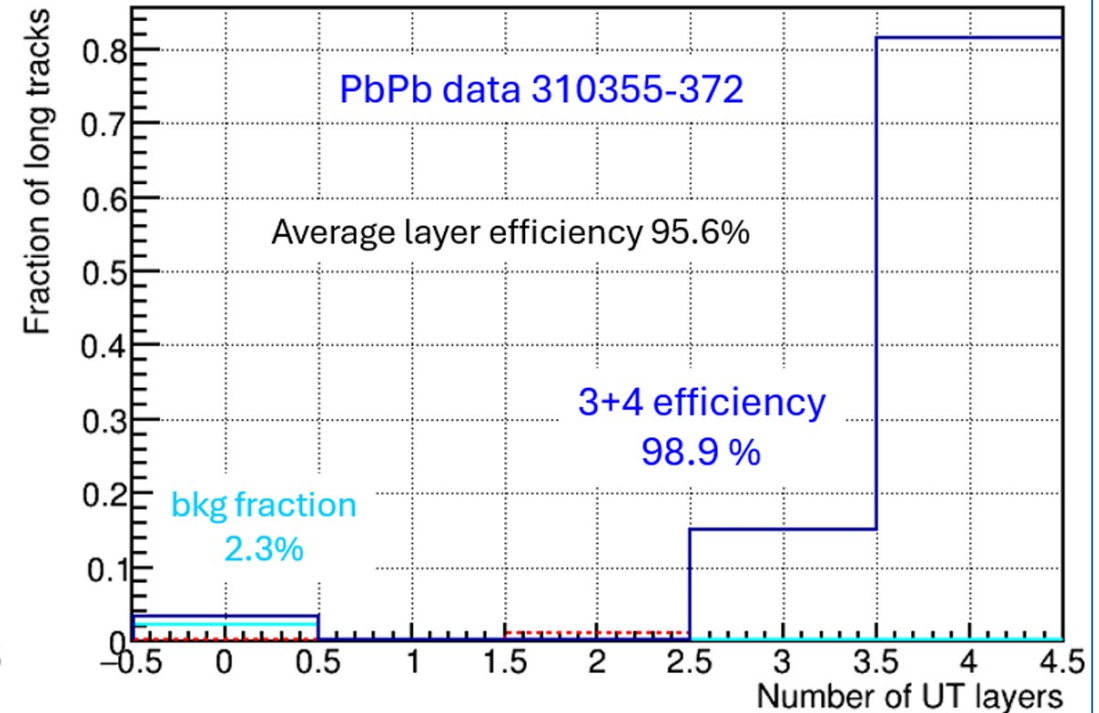
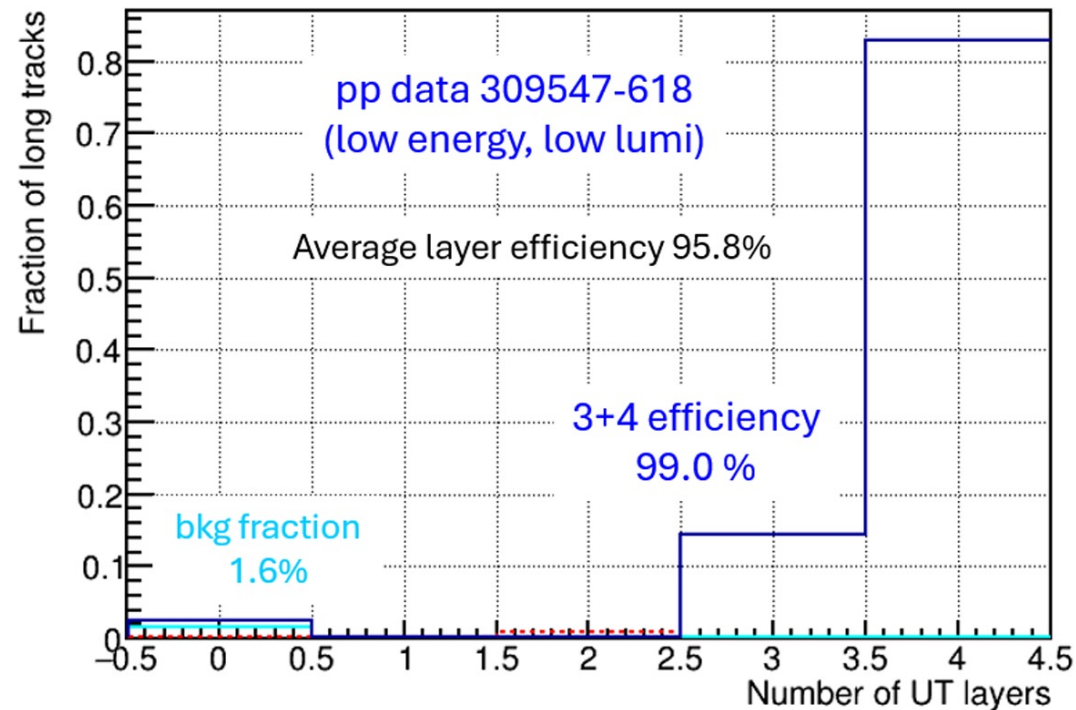
UT tracking efficiency



Heavy Ion run

- Extremely stable data taking
- Very low rate of DAQ errors

Number of UT layers matched to a long track and the relative tracking efficiency

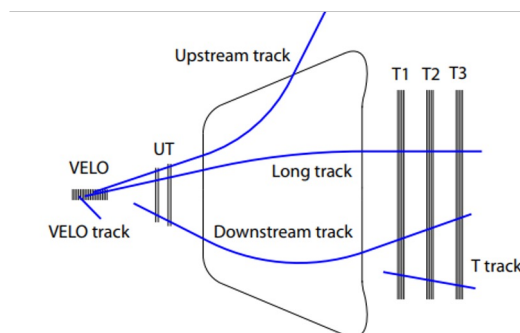
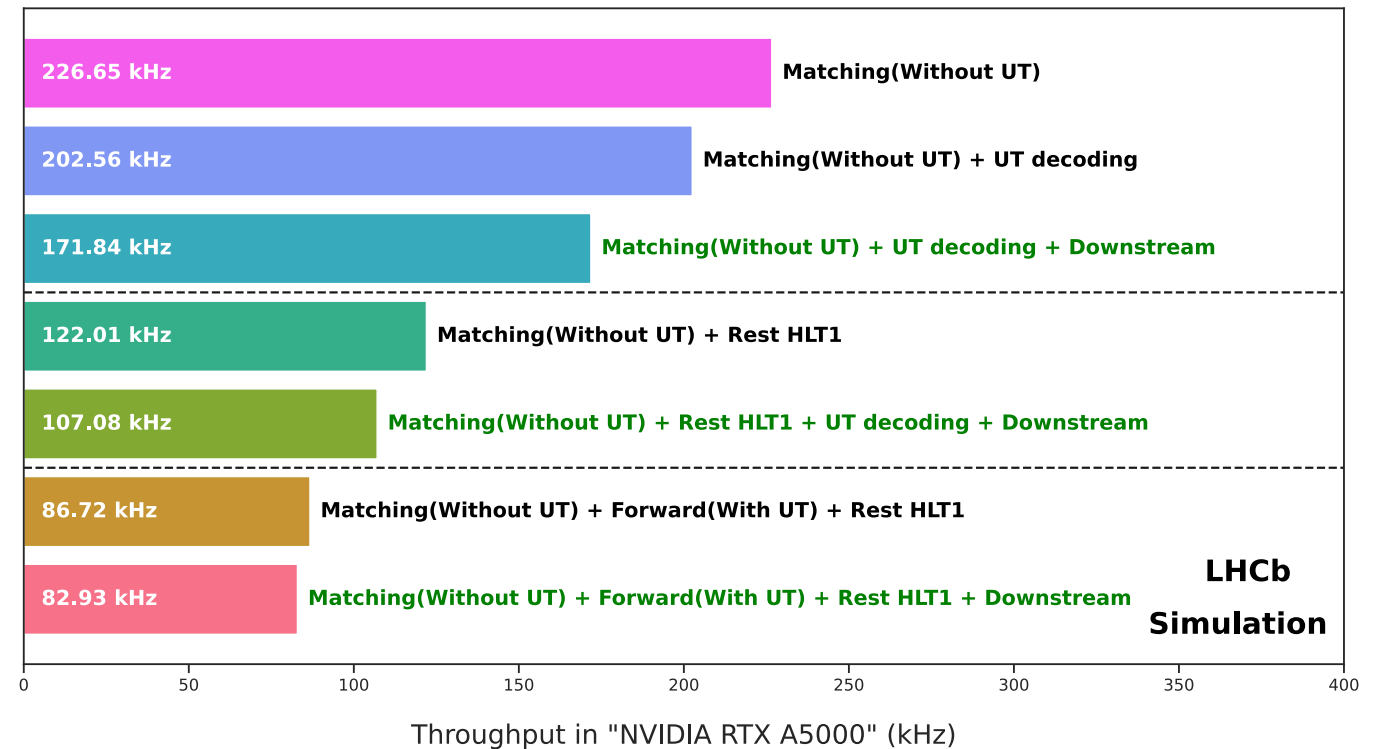


UT in HLT1 – Downstream tracks



- The new HLT1 downstream tracking is designed to reconstruct decays outside the VELO in HLT1 and has been running in Run 3 data-taking since October 2024.
- Downstream tracking will not be possible without UT in HLT1
- The algorithm reduces HLT1 throughput by approximately 9%, achieving 67.50 kHz per GPU, which meets the HLT1 requirement of over 60 kHz per GPU.

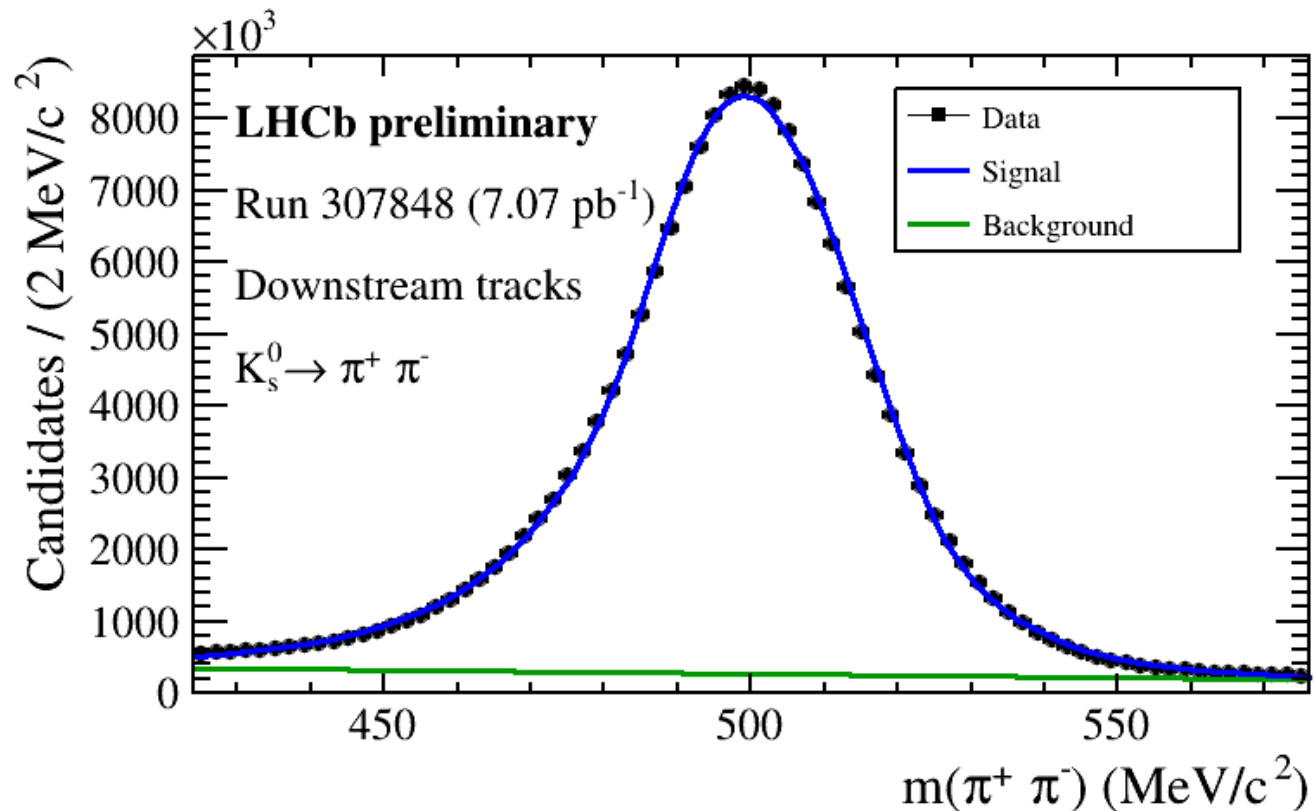
[LHCb-FIGURE-2023-028]



UT in HLT1 – Downstream tracks



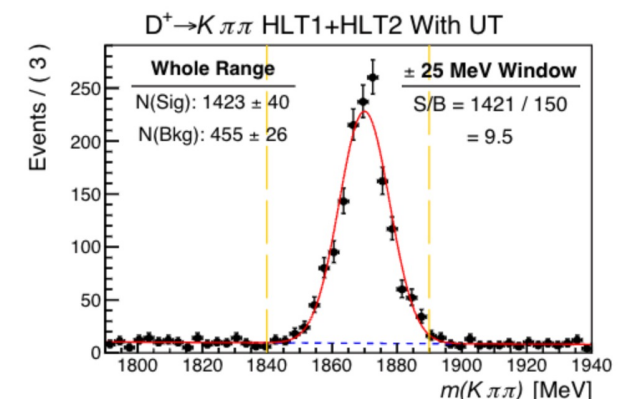
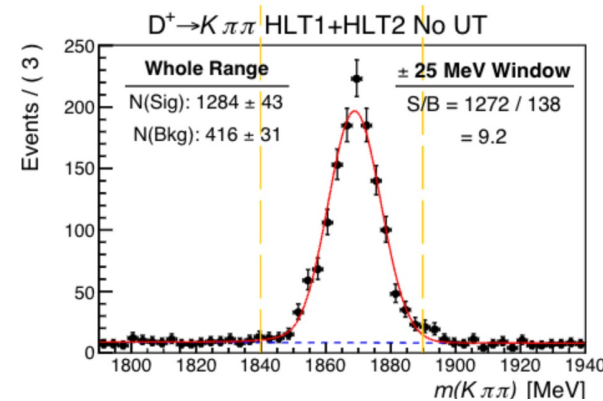
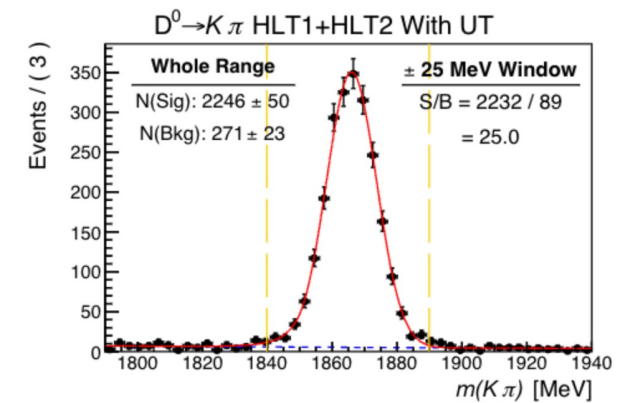
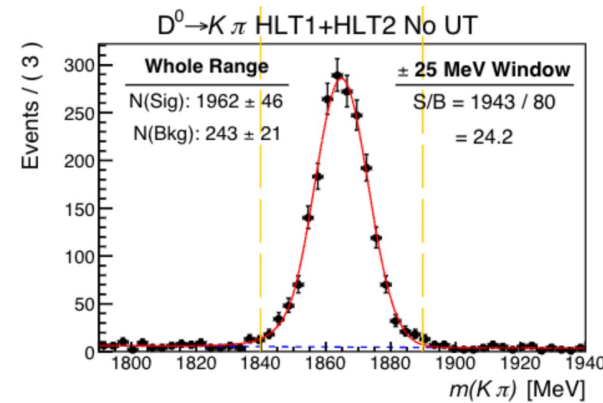
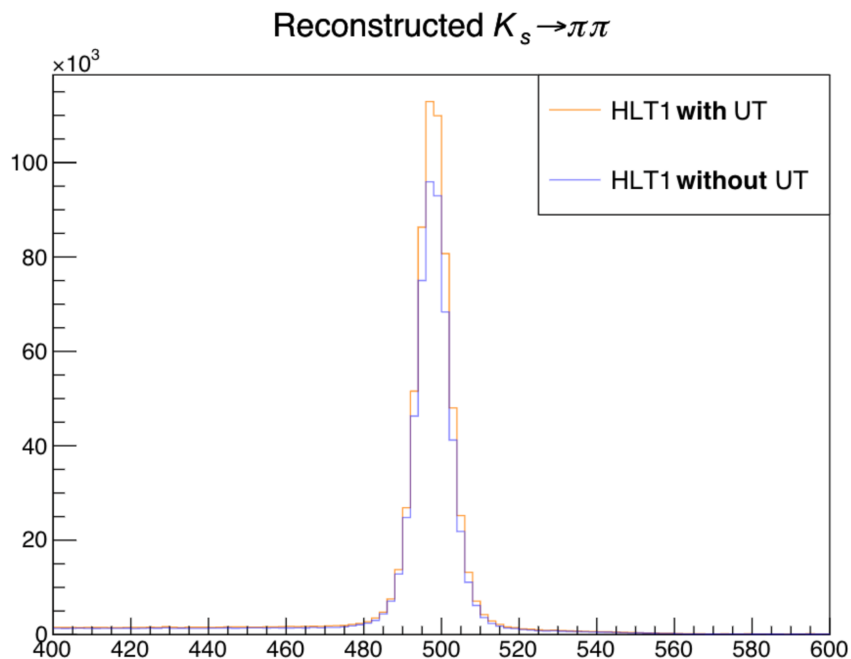
- Checking the mass distributions of the $\Lambda^0 \rightarrow p\pi^-$ and $K_S^0 \rightarrow \pi^+\pi^-$ decays can be used to benchmark the performance of Downstream tracking



Matching with UT in HLT1 + HLT2



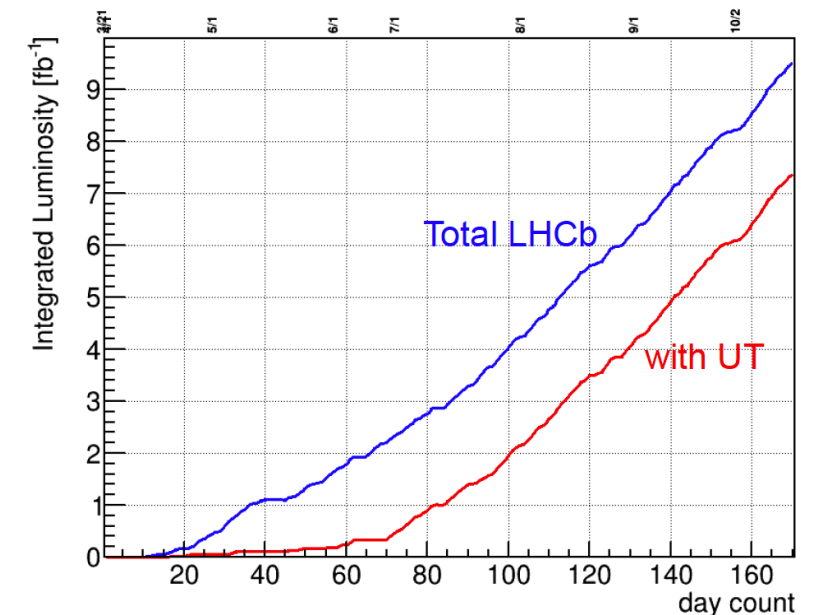
- The inclusion of UT in HLT1 and HLT2 has improved the physics performance of the LHCb experiment since it is important to improve the **momentum resolution** of Long tracks



Conclusions



- After commissioning in spring 2024, UT detector joined physics data taking in summer and improved LHCb physics performance.
- Efficiency of UT detector was improved during 2024 data taking. Suitable UT configuration was found for the design luminosity ($\mu=5.3$)
- The best UT performance was achieved for heavy ion physics and in related low-energy pp reference run.
- The presence of UT in the software trigger has highly improved the physics performance of the LHCb experiment.





Thanks for the attention!

Backups



PP collisions

- Very stable data taking and good efficiency during Run 3 pp reference run performed the last week of October 2024.
- Data acquisition stable even with tighter ADC threshold

Heavy Ion run

- Extremely stable data taking
- Very low rate of DAQ errors

Backups

Silicon ASIC for LHCb Tracking

(SALT):

- CMOS 130 nm

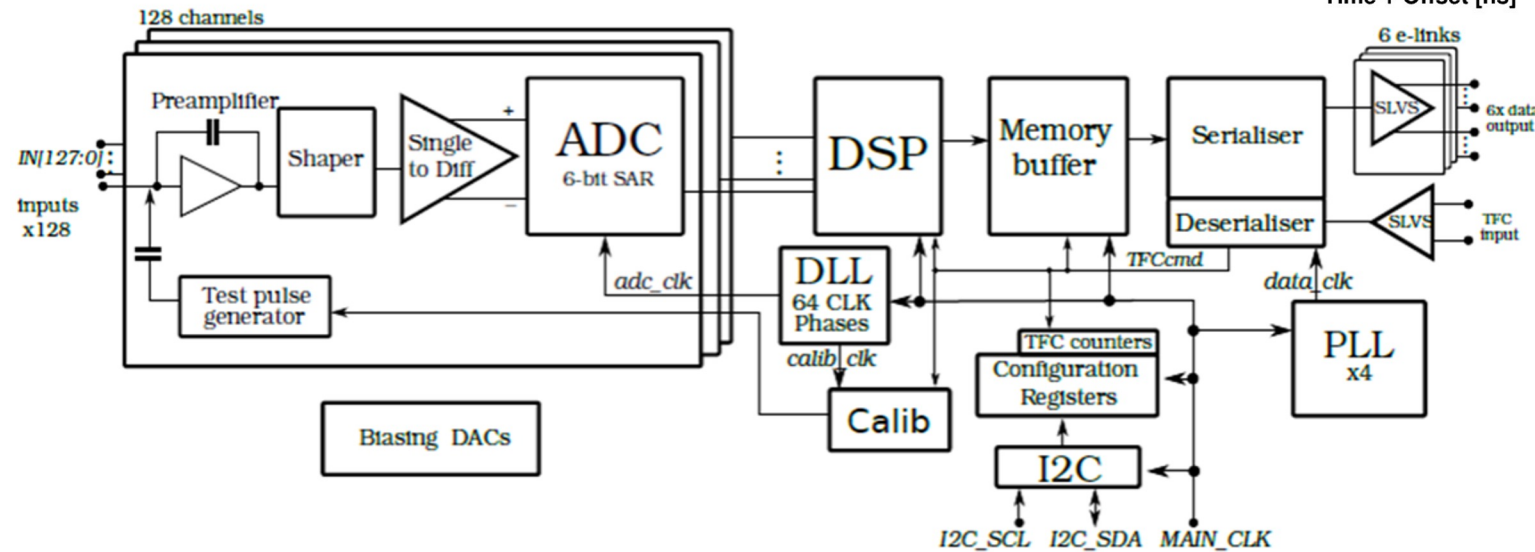
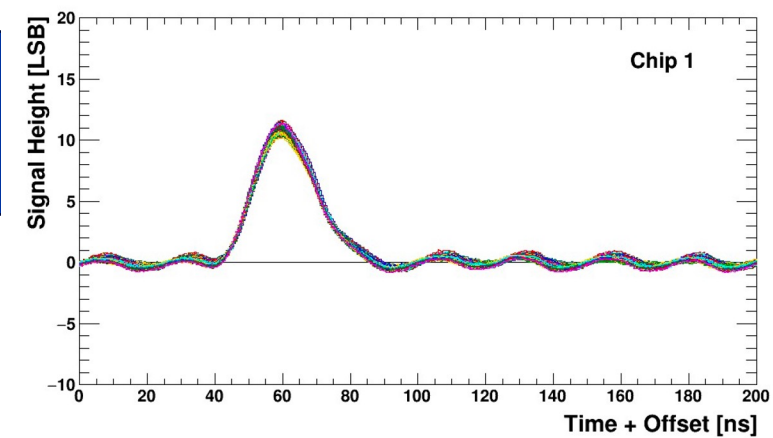
technology

- 128 channels / ASIC

- 6 bit ADC / channel

- Digital Signal Processing (DSP): pedestal and common mode noise subtraction, zero-suppression, data formatting, spillover correction

- peaking time \sim 25 ns, S/N \sim 20, input C=12 pF, power dissipation/channel $<$ 6mW

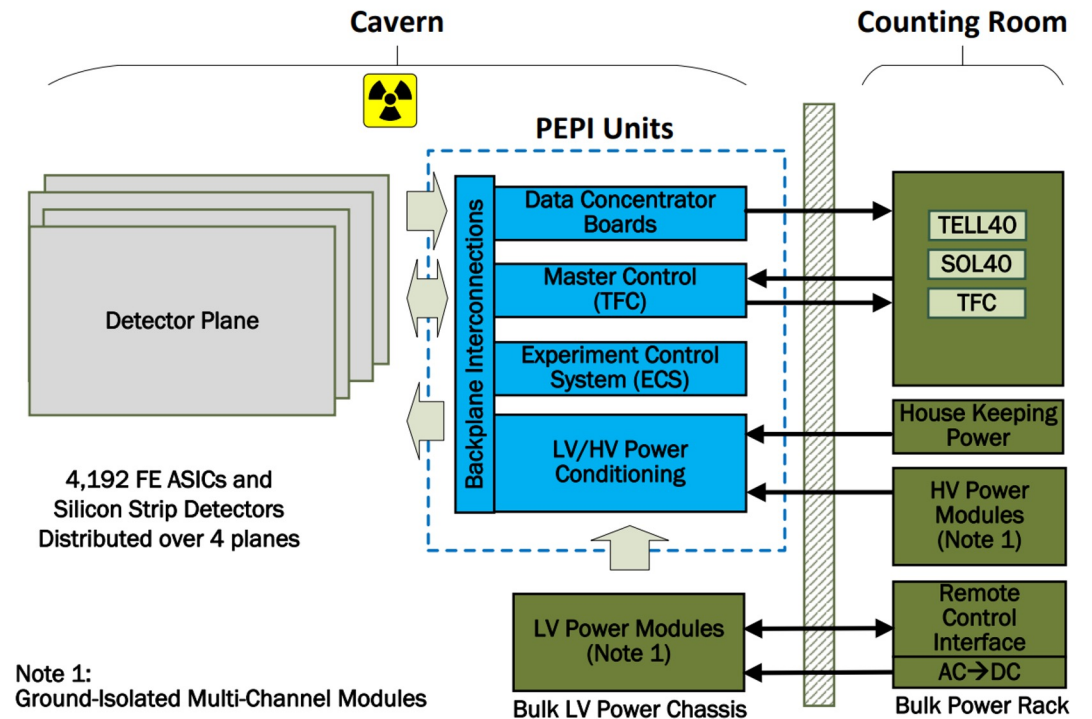


Backups



Periphery electronics processing interface (PEPI) to read out and control the detector:

- 24 backplanes
- 24 pigtail power breakout boards (P2B2s)
- 248 data and control boards (DCBs)



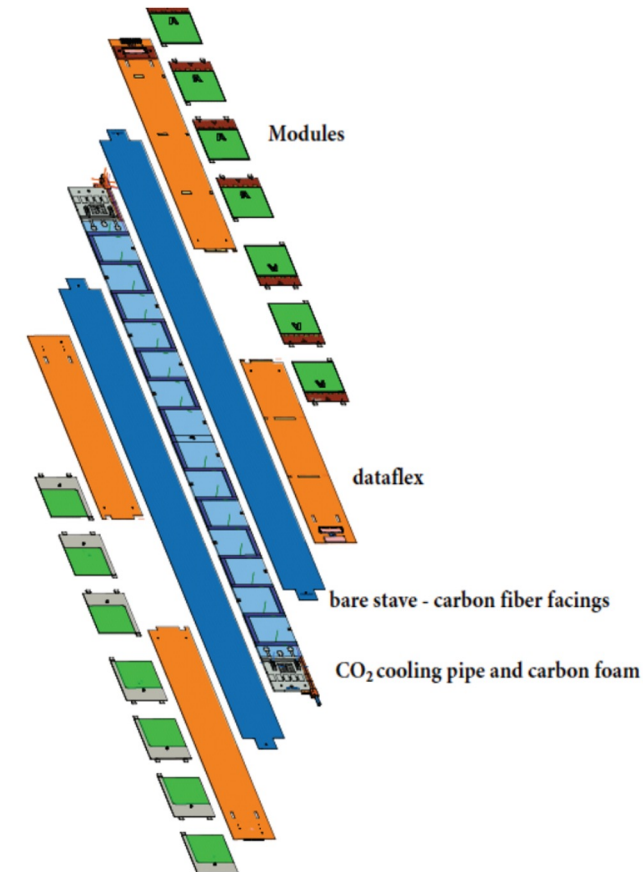
The **GBTx**, mounted on the DCBs, implements bidirectional **links** between the **detector** and the **counting room**

Backups



Stave:

- 99.5mm x 1640mm (width x length)
- **carbon fiber structure** with thermal and structural foam in between
- S-shaped titanium **cooling pipe**
- 4 Flex Cu- Kapton cables, power and data distribution
- Single stave can host 14 or 16 **modules**, on both sides



Backups

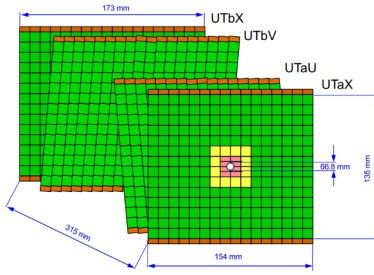


to make UT work..

DETECTOR SAFETY

DETECTOR
MONITORING

UT



to take data..

FIRMWARE

ECS

Software

to take good quality data for physics..

Time alignment

Space alignment

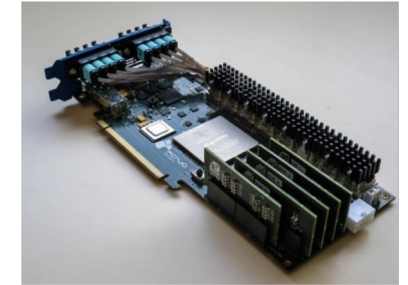
Calibration

Data quality
monitoring

Backups

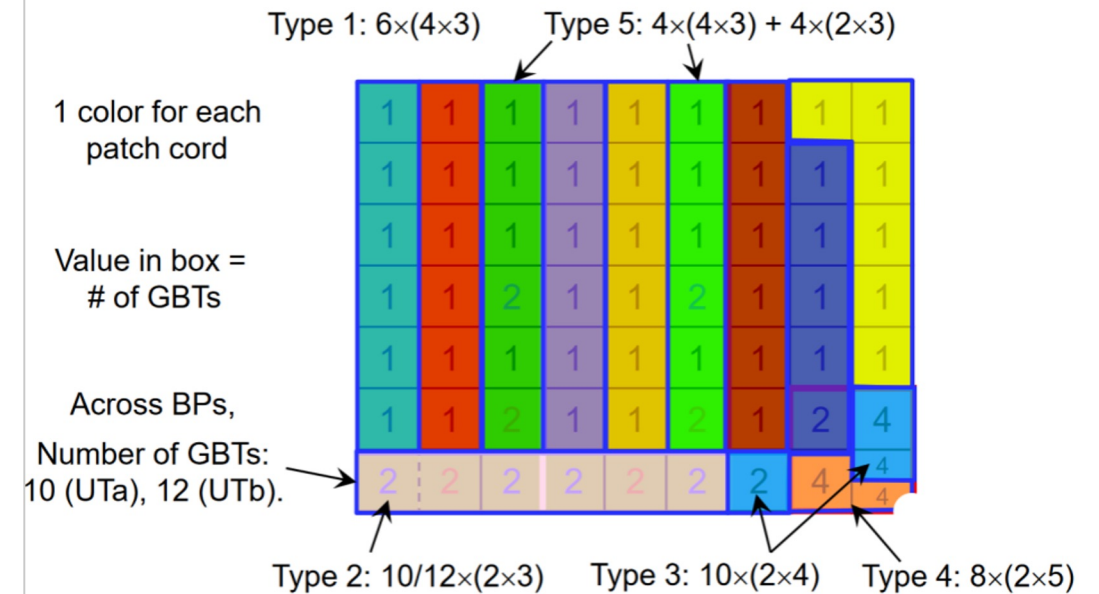


- **Readout of the detector** possible with PCIe40 cards hosting
Intel Arria 10 **FPGA**: transforms the data from ASIC to PCIe format
- **5 flavours**, design to cope with different occupancies and to minimize the cost



flavour= (#ASICs x #e-links)

GBT frame byte	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4 x 3-eports			24-bit		24-bit		24-bit		24-bit					
2 x 3-eports			24-bit				24-bit							
2 x 4-eports			32-bit				32-bit							
2 x 5-eports			40-bit				40-bit							



Implemented to work in Non-zero-suppressed (NZS) and in Zero-suppressed (ZS) mode

Backups

