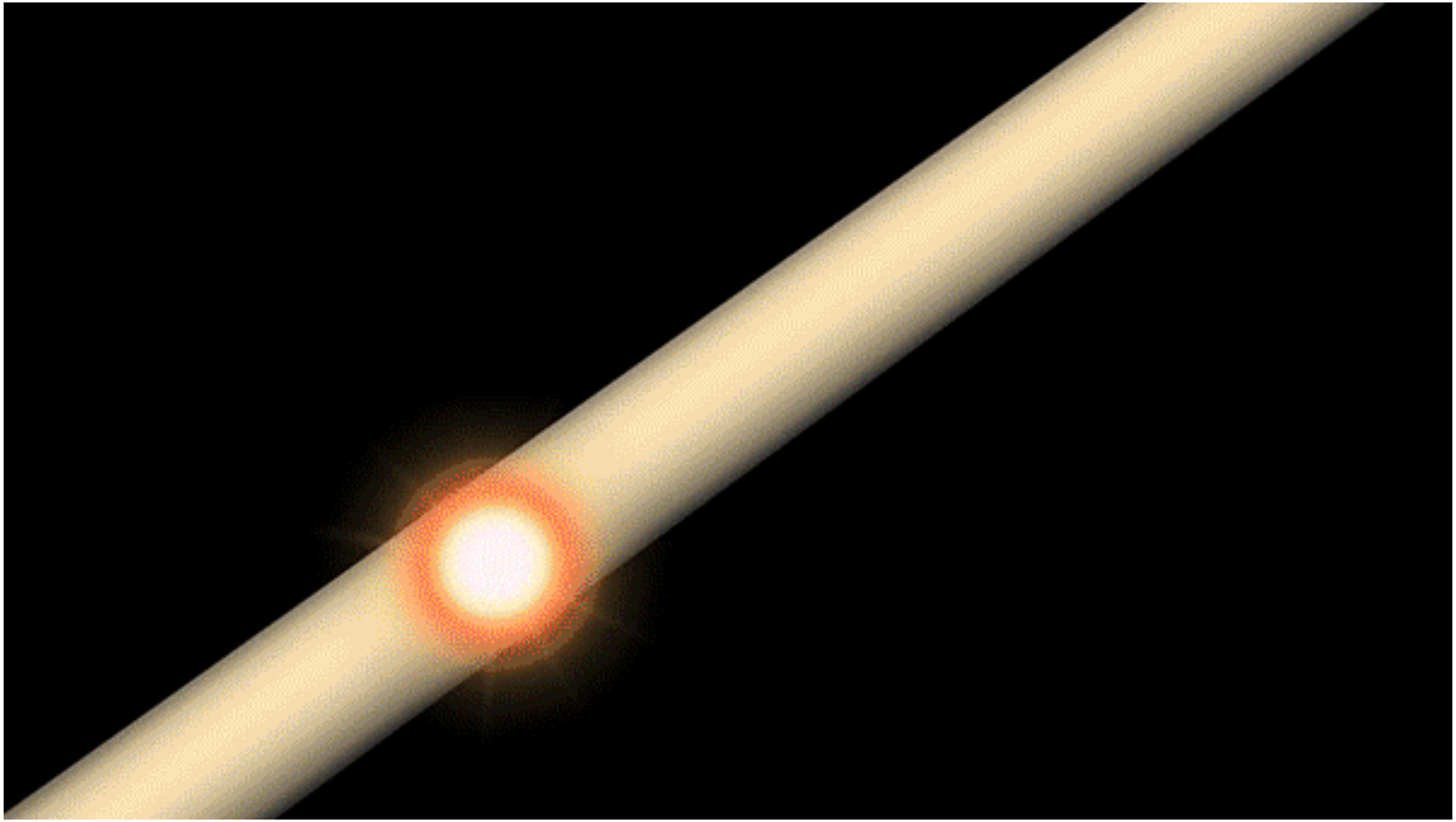
Monolithic Pixel Sensors for charged particle tracking at colliders and on satellites

Stefania Maria Beolé

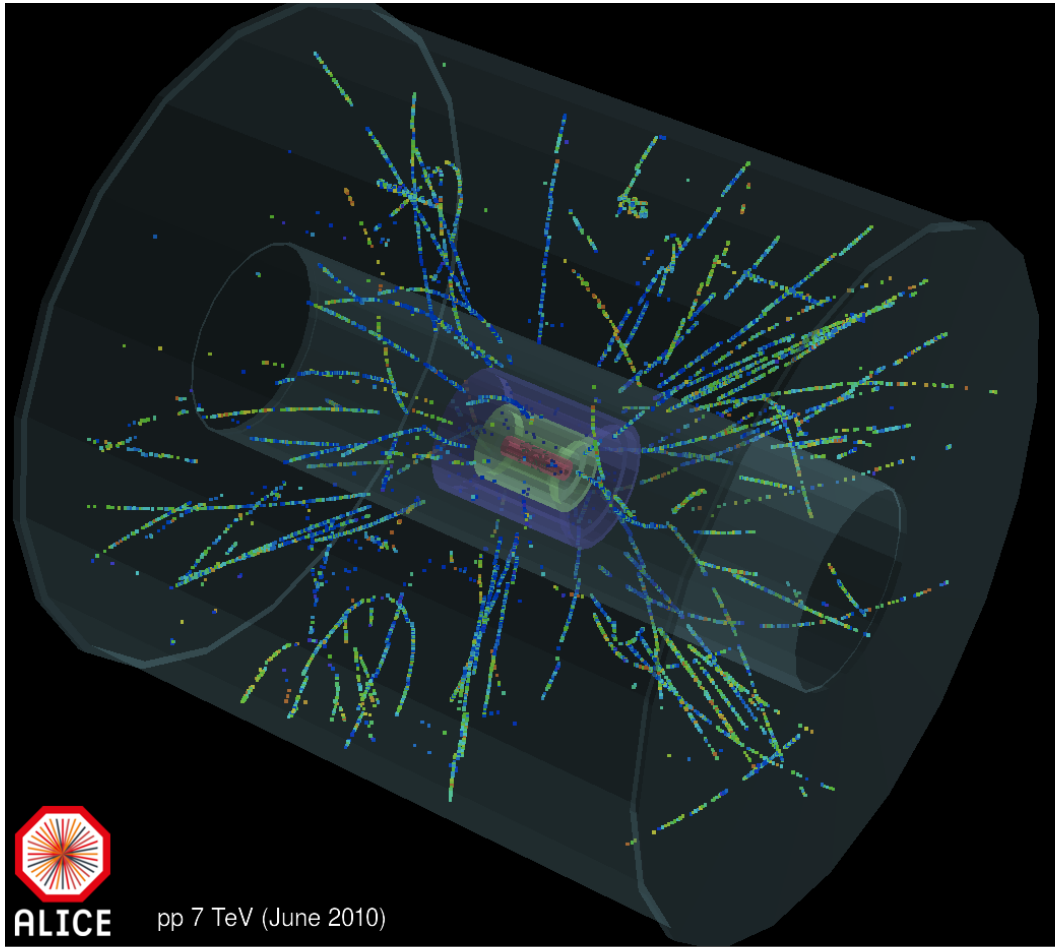
Hadron-hadron collisions at LHC



Source: https://youtu.be/NhXMXiXOWAA

Charged particle tracker: goals

- **Measure trajectory of charged particles**
  - Measure several points along the track and fit curves to the points (helix in a magnetic field)



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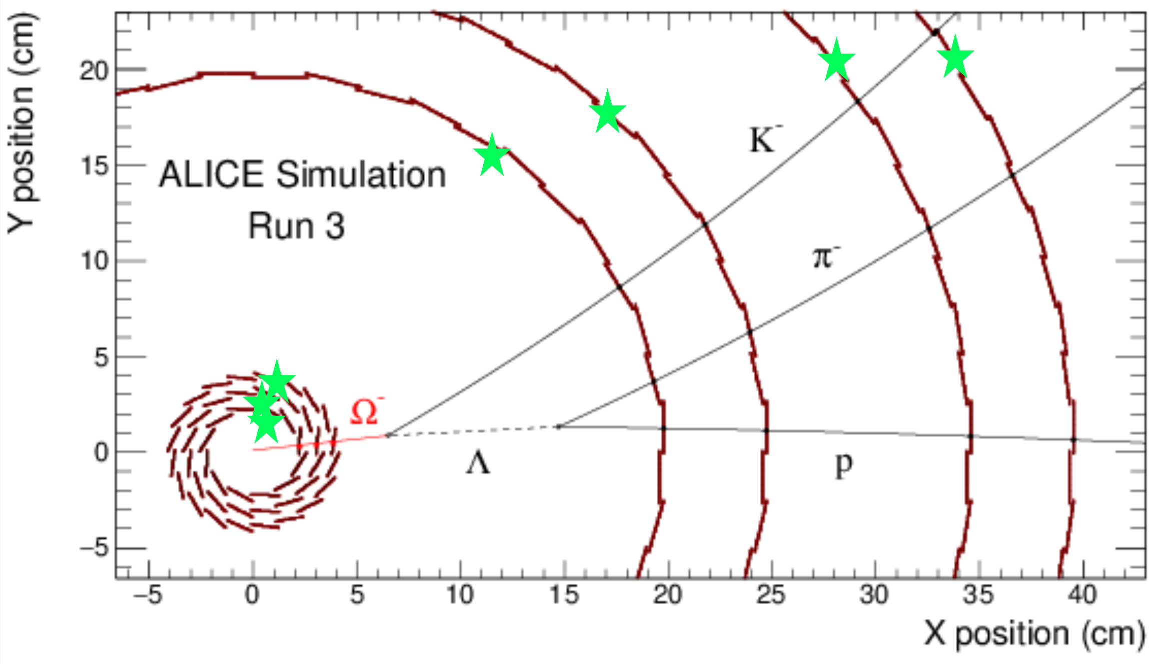

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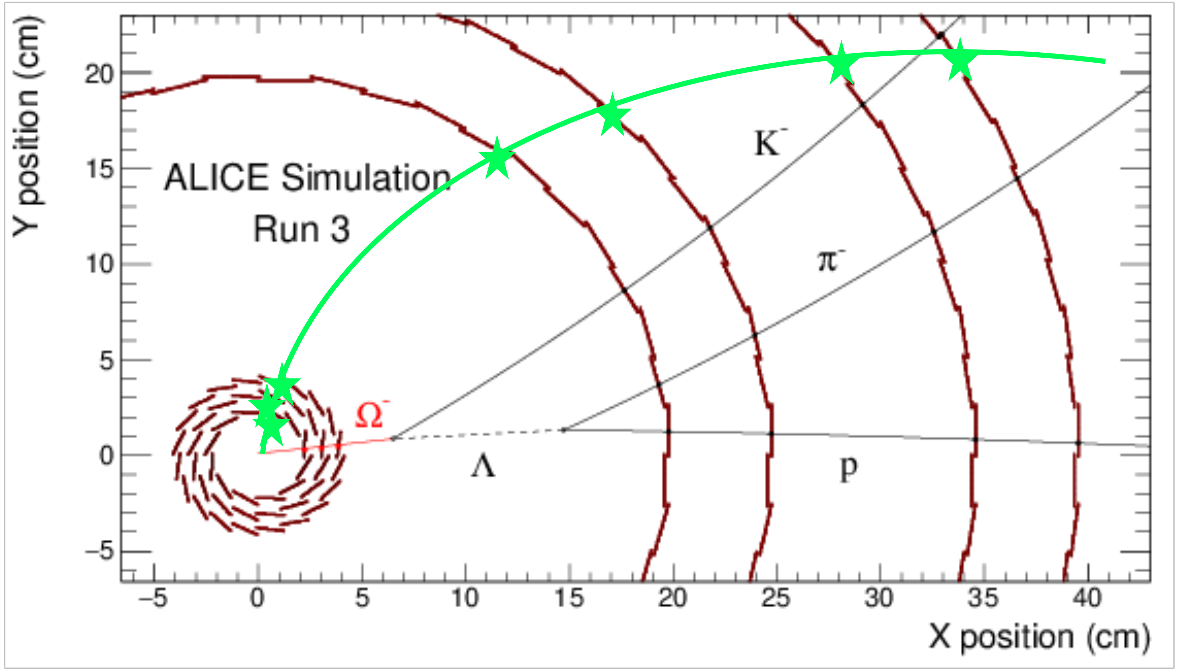
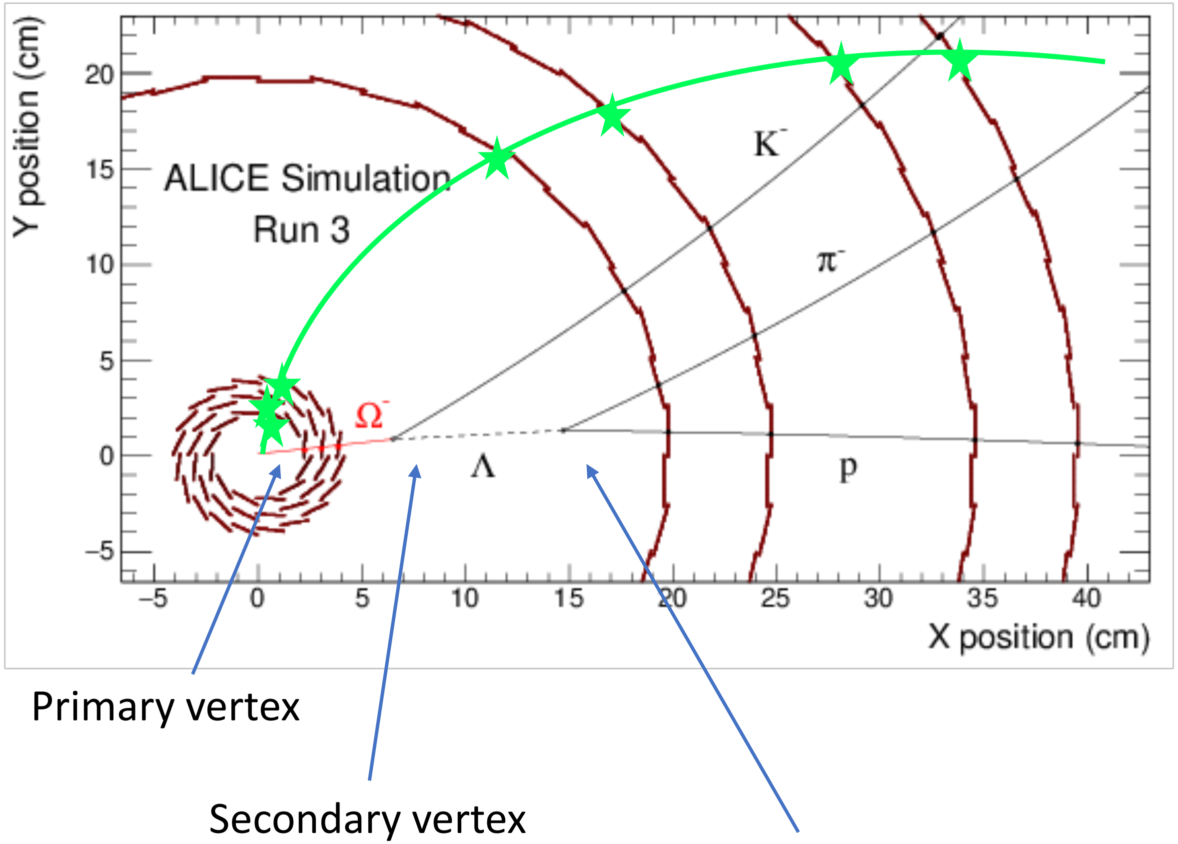


Charged particle tracker: goals

- **Measure trajectory of charged particles**
  - Measure several points along the track and fit curves to the points (helix in a magnetic field)
- **Extrapolate tracks to the point of origin**
  - Determine positions of primary vertices and identify interesting collision vertex: **VERTEXING**
  - Find **secondary vertices** from decay of long-lived particles
- **Use the track curvature to determine the particle momentum: PID**

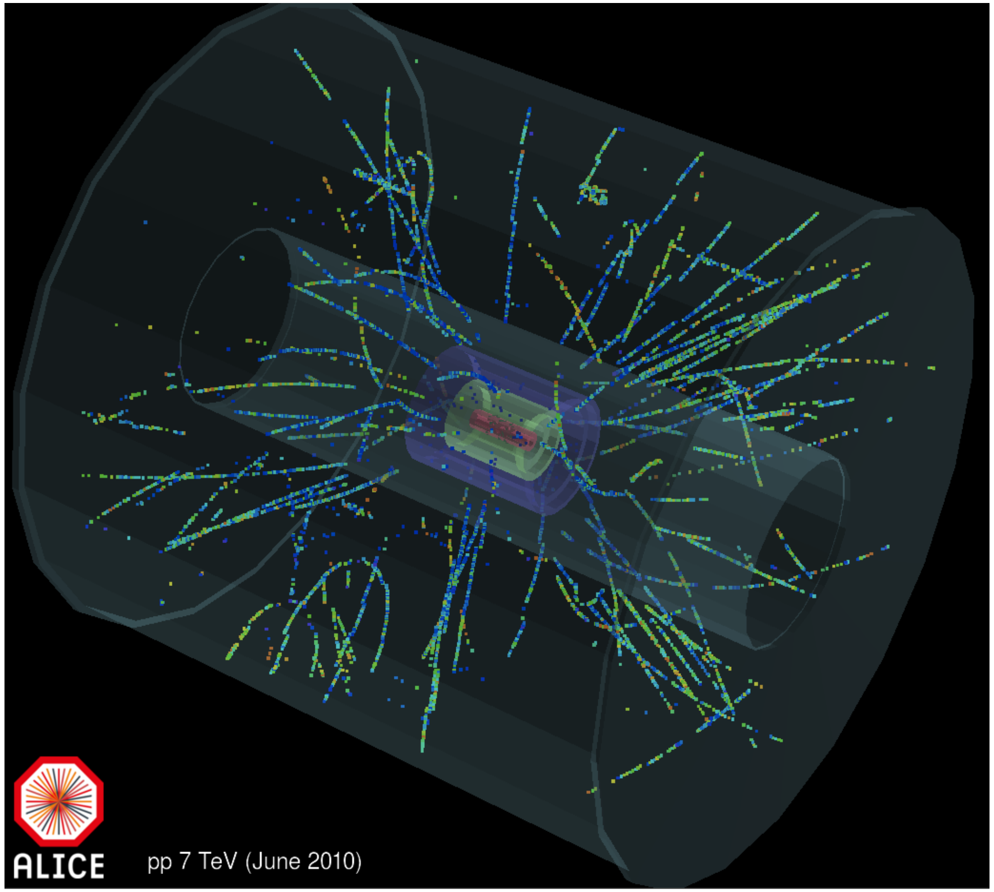


Primary vertex

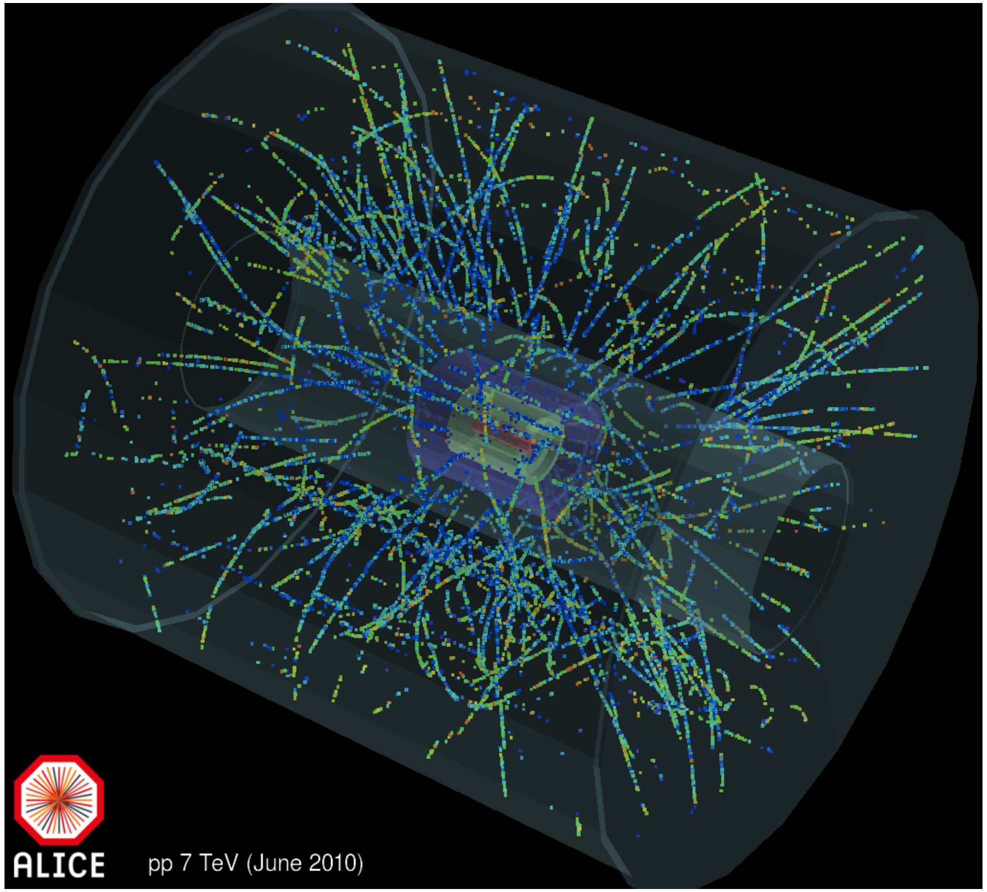
Secondary vertex

Tertiary vertex

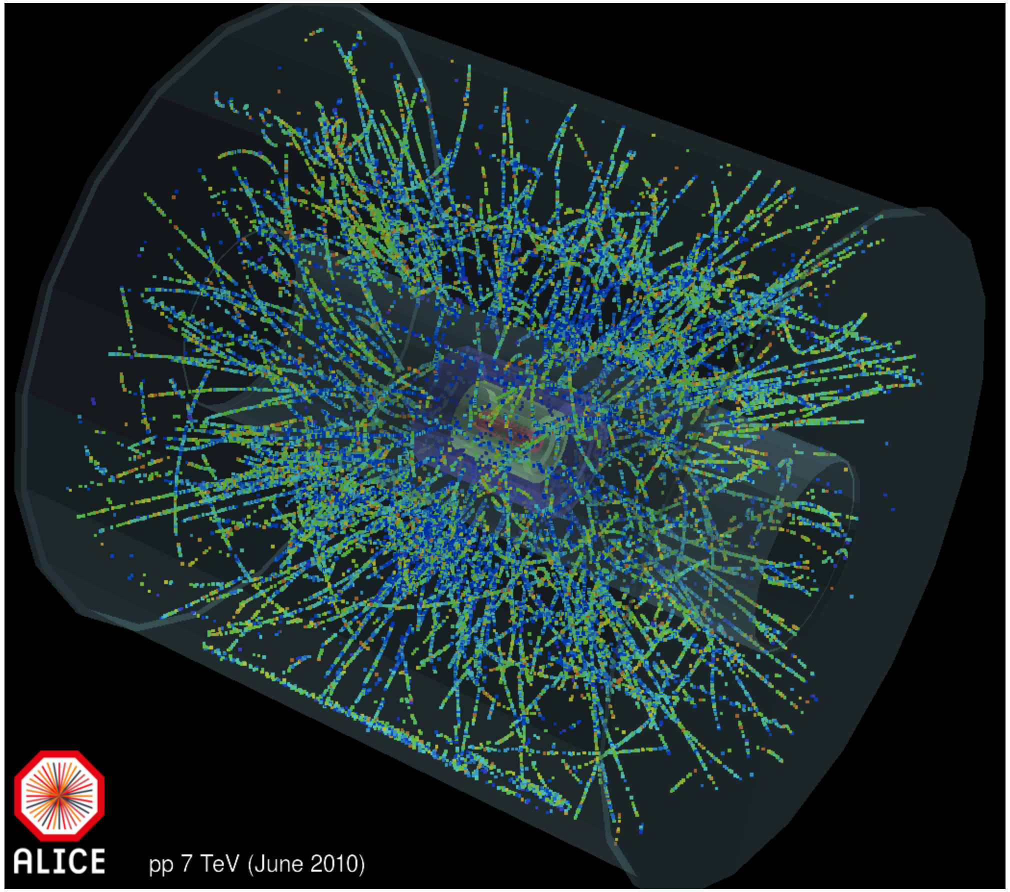
Tracking in pp collisions @LHC: low multiplicity



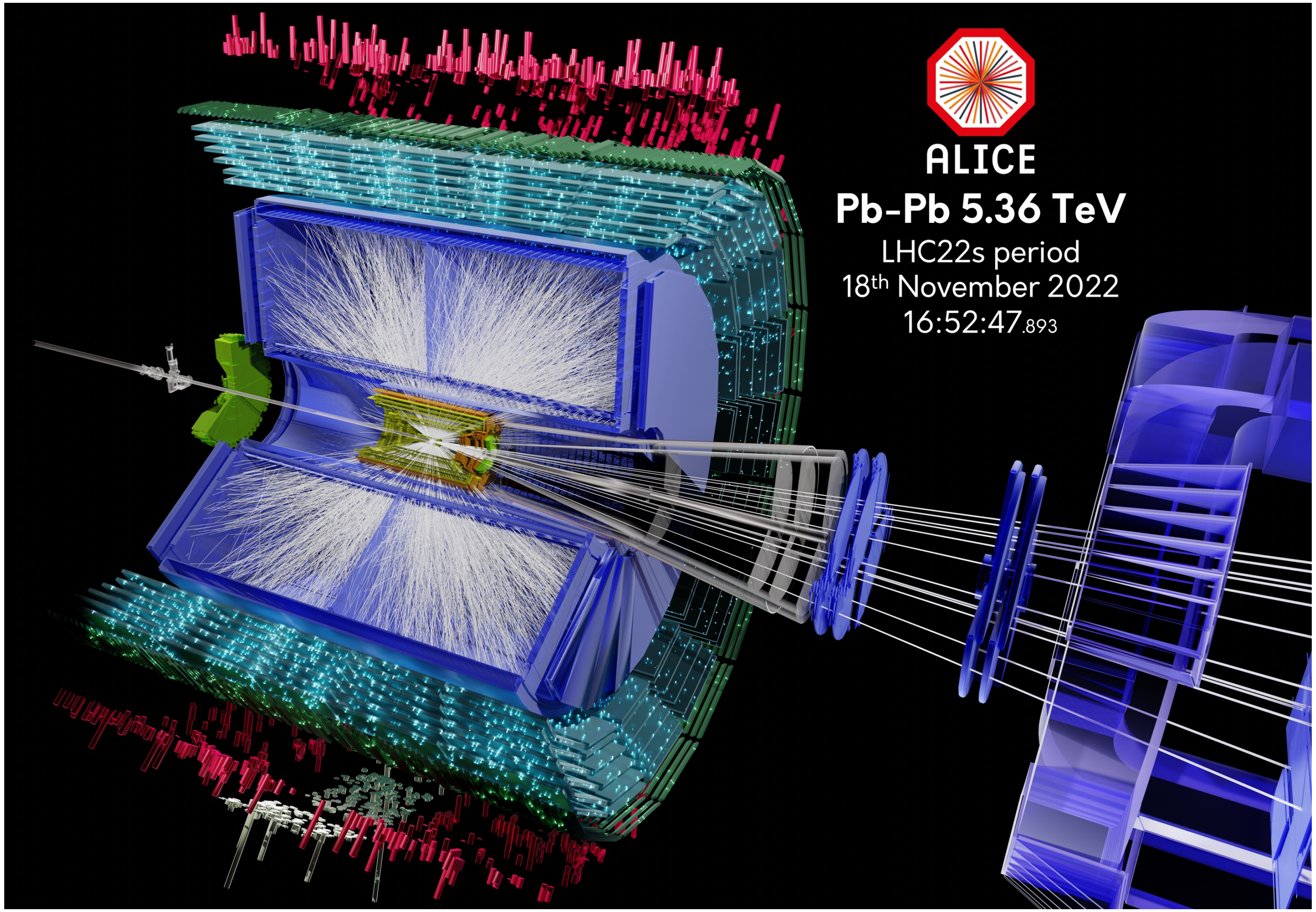
Tracking in pp collisions @LHC: medium multiplicity



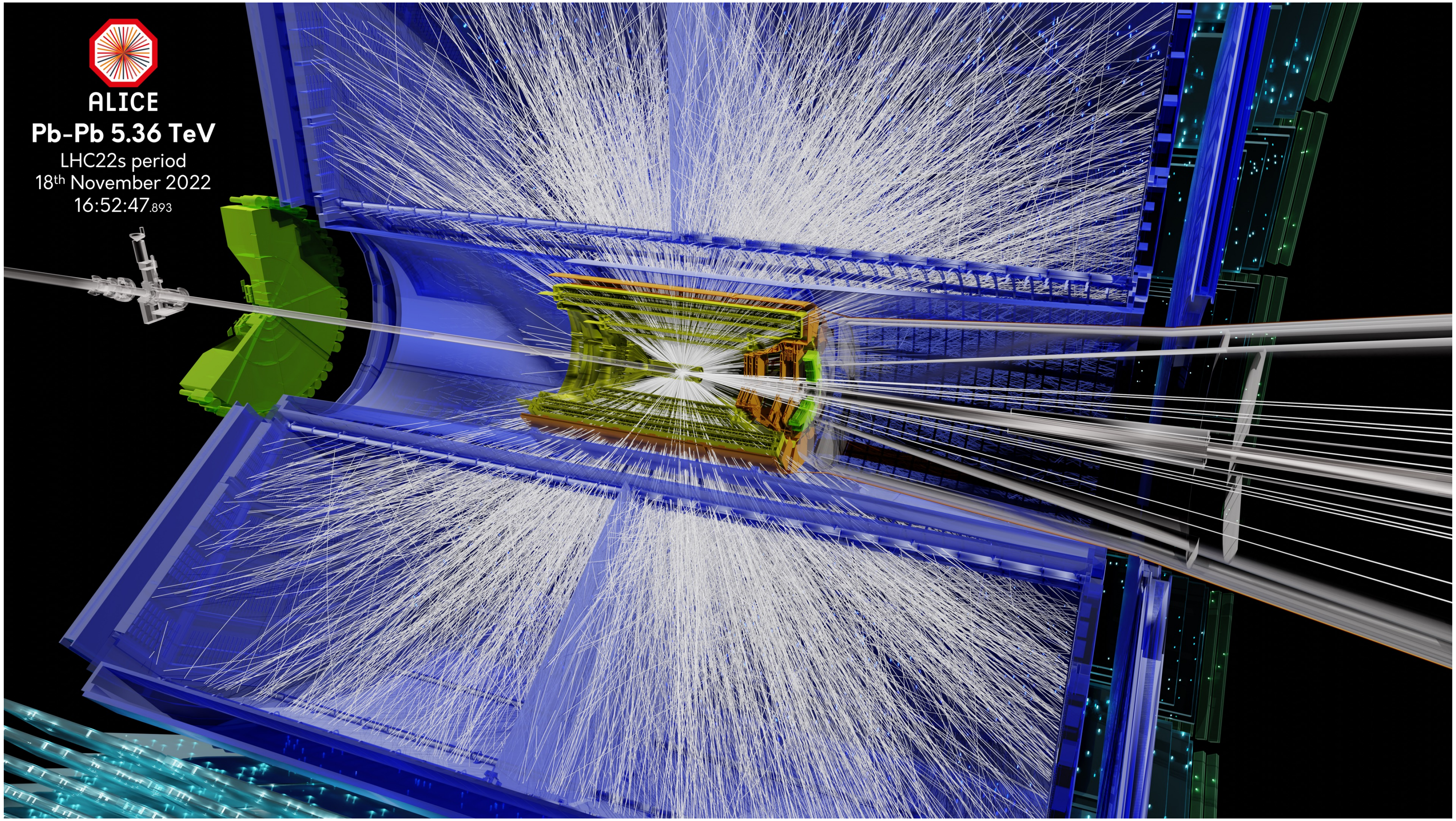
Tracking in pp collisions @LHC : high multiplicity



Tracking in lead-lead collisions at LHC

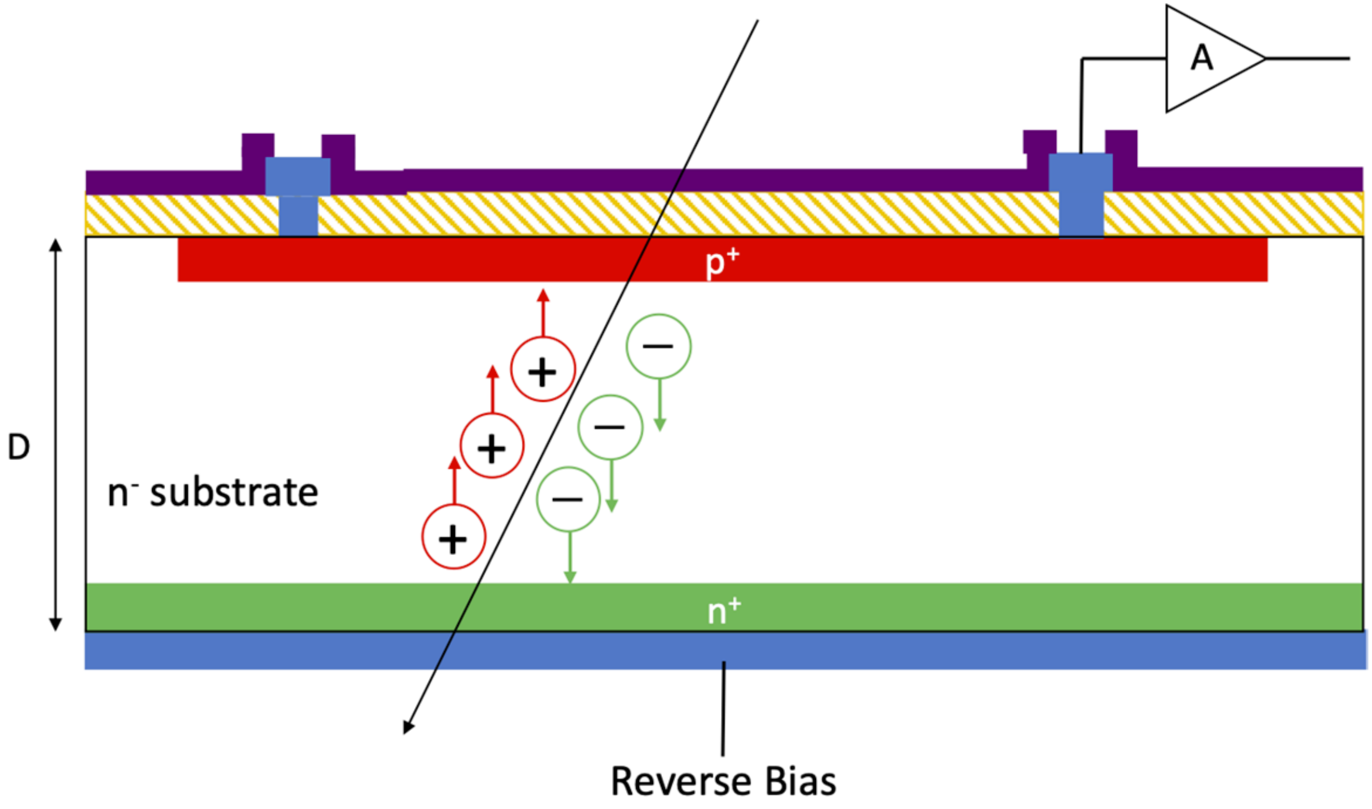


Tracking in lead-lead collisions at LHC



Tracking devices

Position sensitive silicon detector: working principle



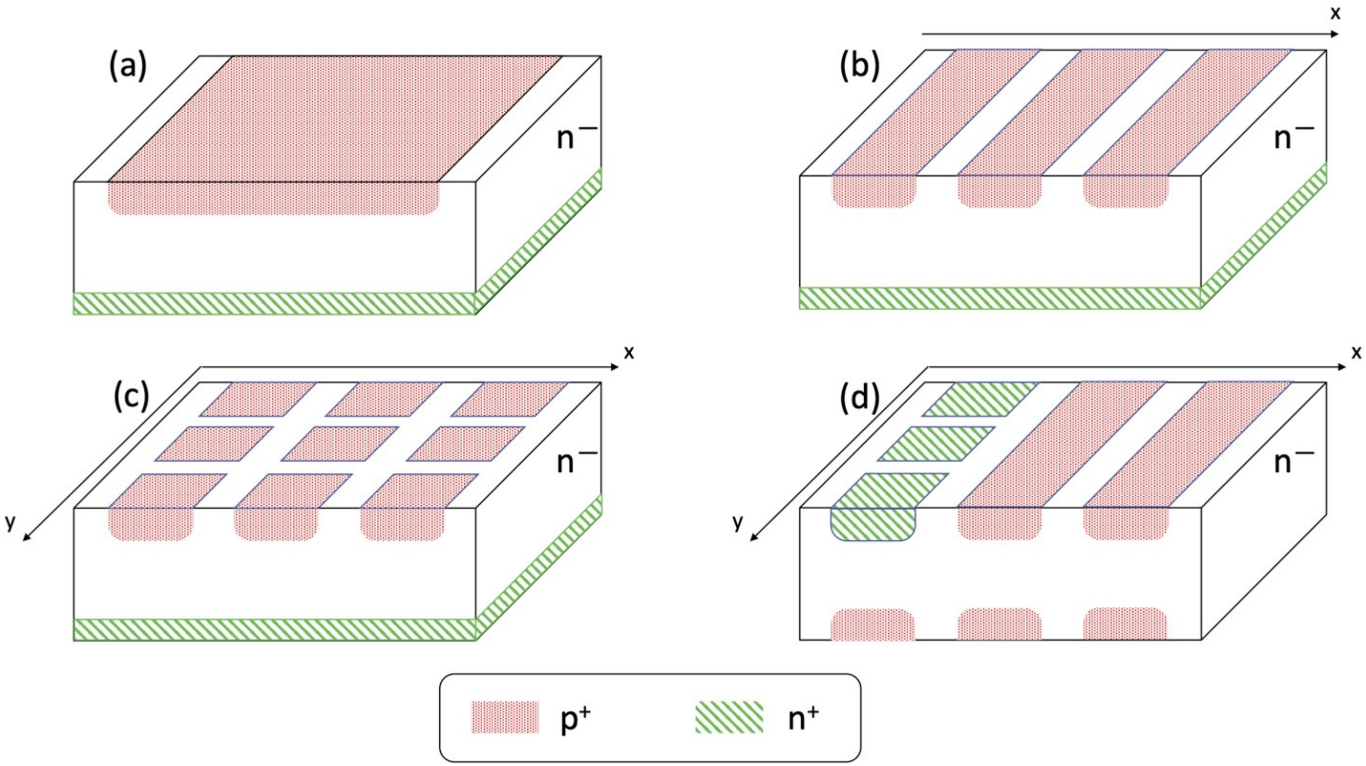
Strip, pixel, drift detectors

a) diode

b) strip (single side): 1D

c) pixel: 2D

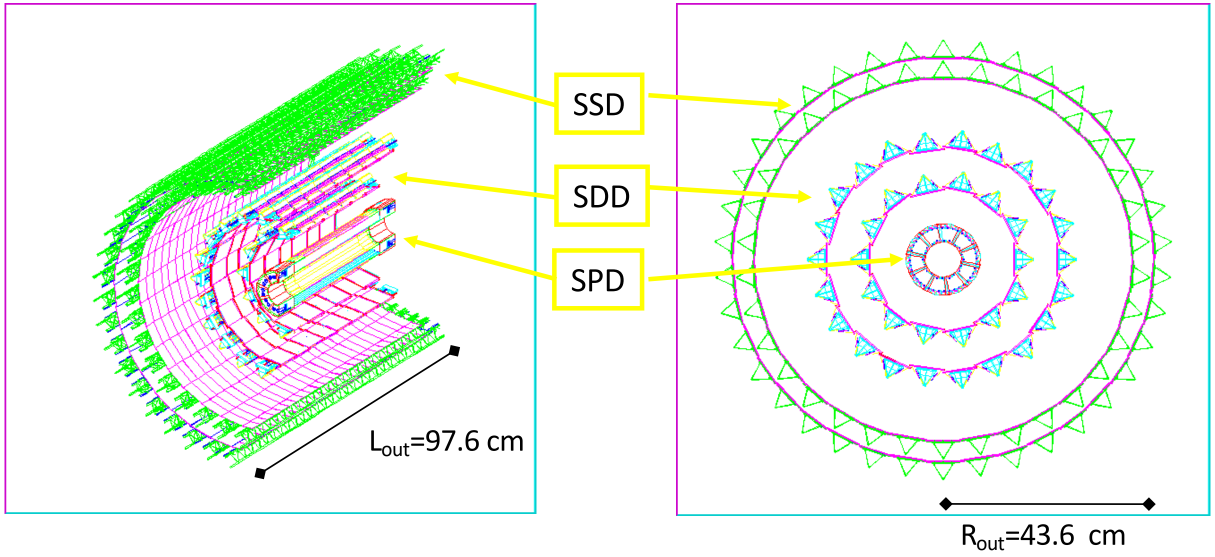
d) drift: 2D



Tracker requirements

- Excellent spatial resolution
- Efficiency (100%)
- As little material as possible
- Time resolution (4D tracking)
- Radiation hardness

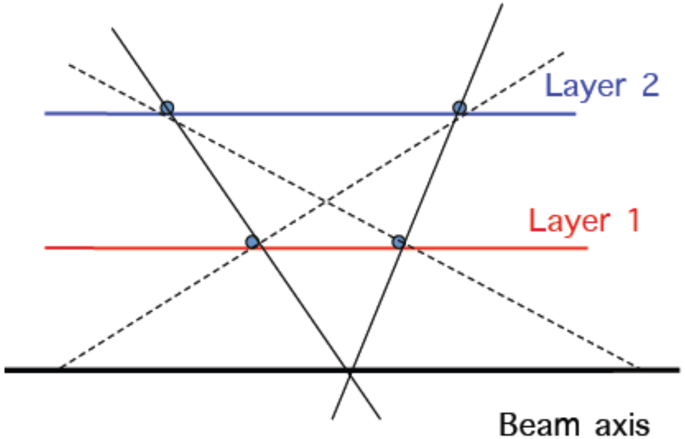
ALICE ITS1



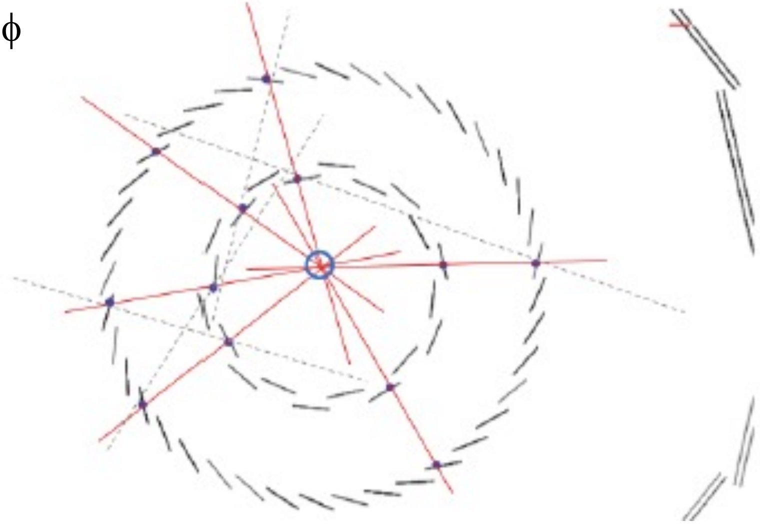
- 6 Layers, three technologies
  - **SPD: Silicon Pixels (0.2 m^2, 9.8 Mchannels)**
  - SDD: Silicon Drift (1.3 m^2, 133 kchannels)
  - SSD: Double-sided Strip Strip (4.9 m^2, 2.6 Mchannels)

Vertexing

Side view: Z position



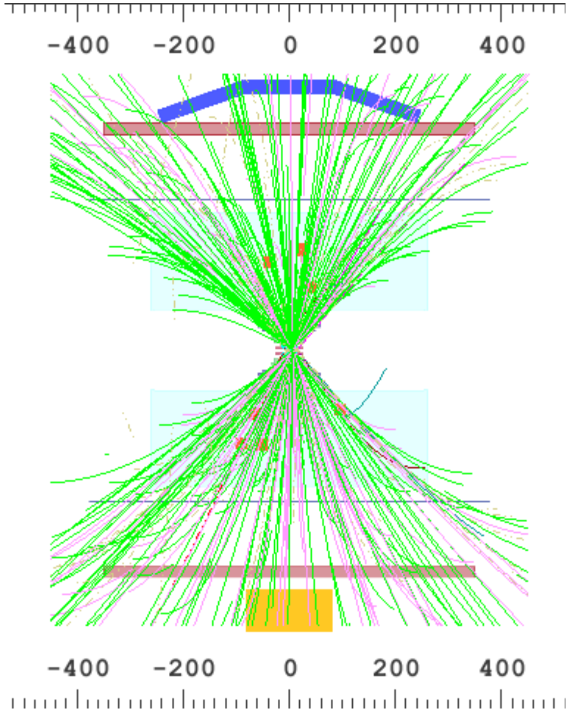
Front view: rϕ



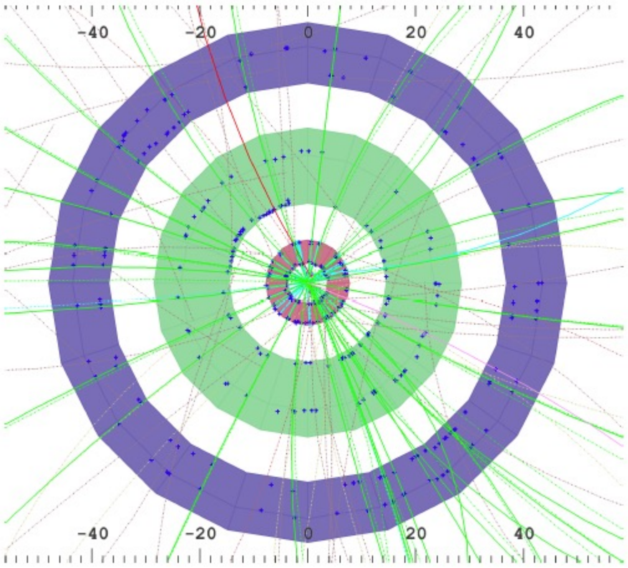
- Pixel detector are used to provide vertex position (fast response – online determination)
  - Tracklets instead of tracks
- Vertex is used as seed for tracking
- Tracks are used to refine vertex position measurement after tracking

Vertexing

Side view: Z position



Front view: rϕ



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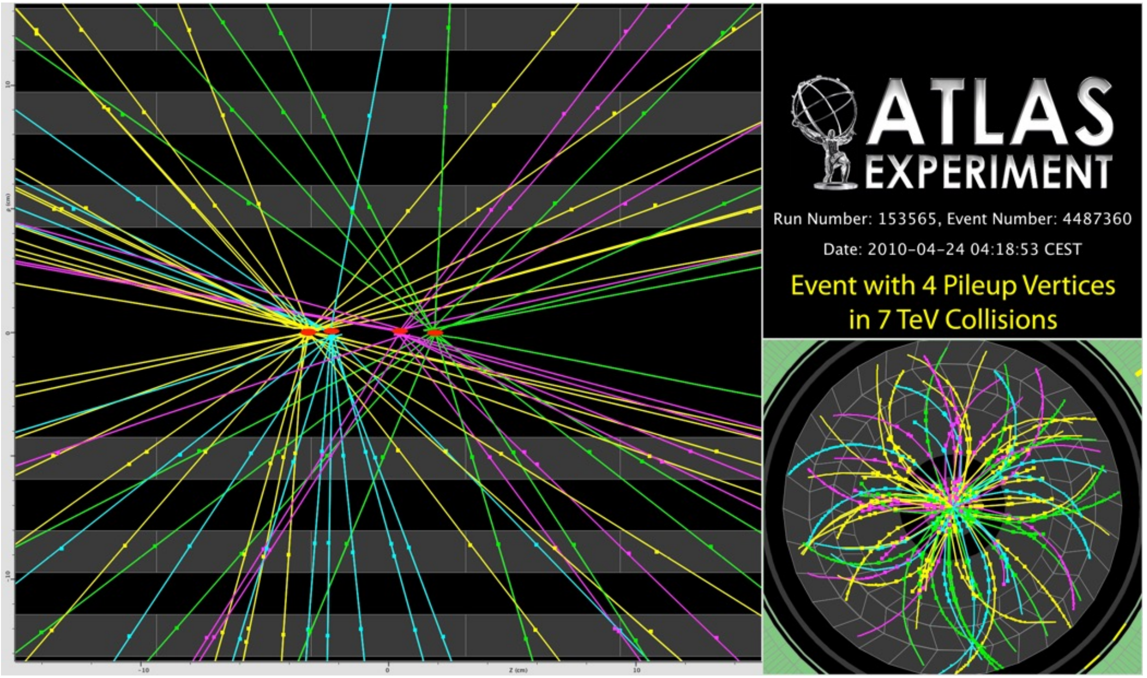
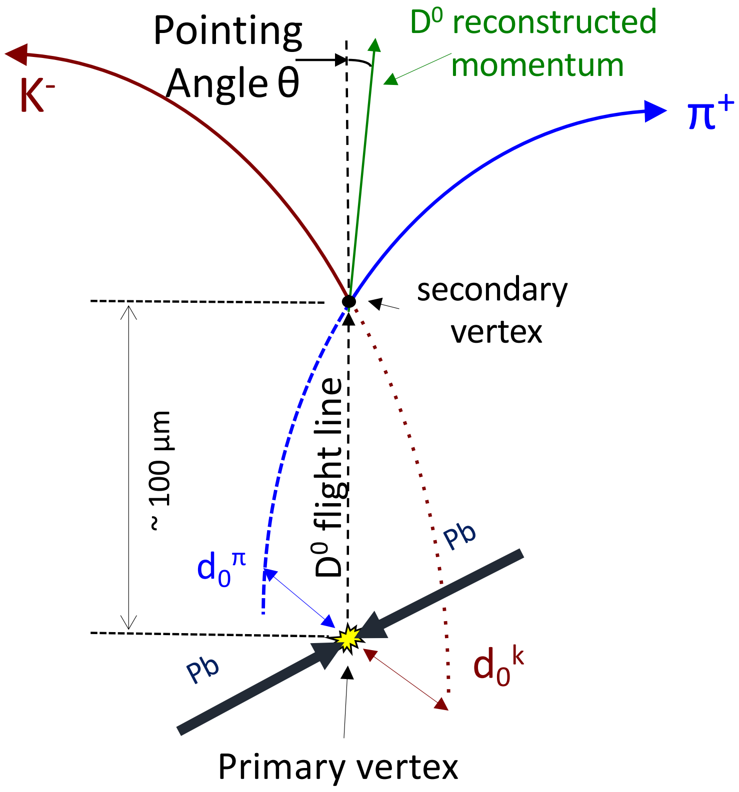
Vertexing in high luminosity environment

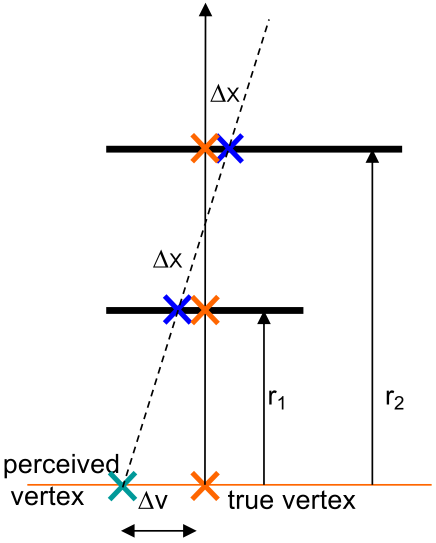
Pileup of 10



HI-LUMI LHC: Pileup of 200

Secondary vertex determination





$$\Delta v = \Delta x \bullet \sqrt{\frac{r_2^2 + r_1^2}{(r_2 - r_1)^2}}$$

- Go closer to the impact point
- Reduce the material budget

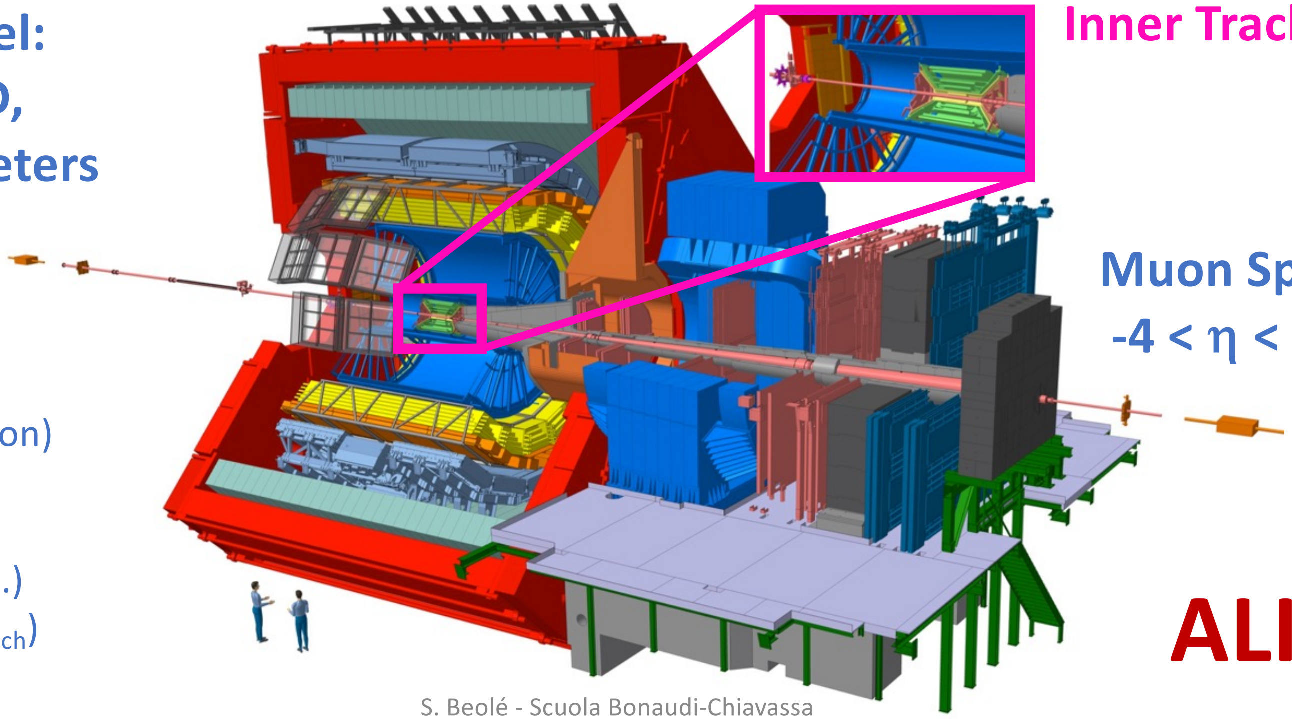
to have a better resolution

The ALICE experiment

The ALICE experiment

- ALICE is the experiment at the LHC specifically designed for studying heavy ion collisions
- The main goal is exploring the deconfined phase of QCD matter → quark-gluon plasma

LHC Pb-Pb → **large energy density** (> 15 GeV/fm^3) & **large volume** (~ 5000 fm^3)



Central Barrel:
Tracking, PID,
EM-Calorimeters
$|\eta| < 0.9$

Inner Tracking System

Muon Spectrometer
$-4 < \eta < -2.5$

ACORDE (cosmics)
Forward detectors:
- AD (diffraction selection)
- V0 (trigger, centrality)
- T0 (timing, lumi)
- ZDC (centrality, ev. sel.)
- FMD (N_{ch}) PMD (N_γ, N_{ch})

ALICE 1

ALICE Upgrades in LS2

Motivation:

High-precision measurements of **rare probes** at **low transverse momentum**

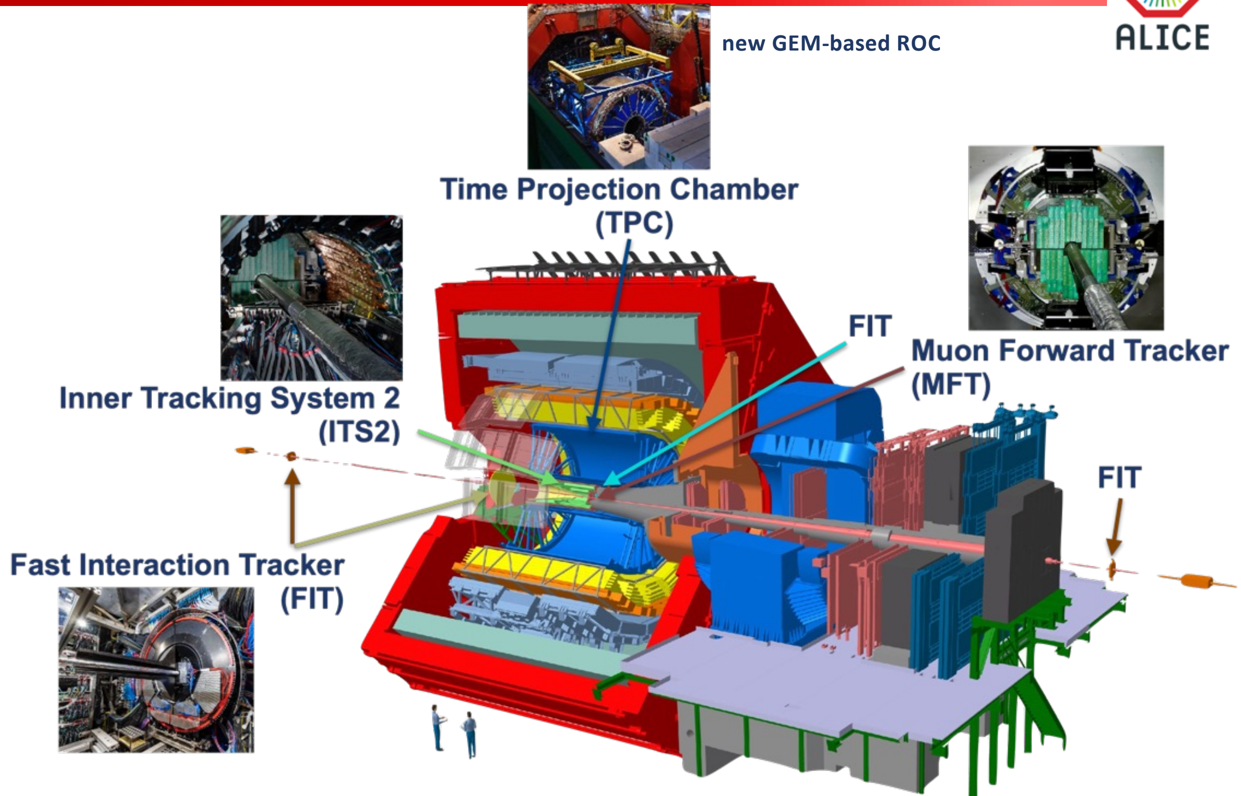
- **Cannot be selected by hardware trigger**
- Need to record large minimum-bias data sample**: read out all Pb-Pb interactions** up to the **maximum collision rate of 50 kHz**

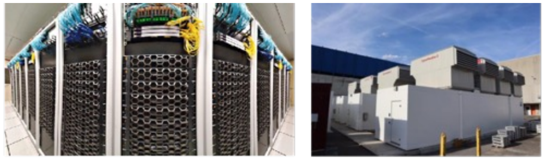
Goal:

- **Gain factor 100 in statistics for min bias sample w.r.t. runs 1+2**
- **Improve vertex reconstruction and tracking capabilities**

Strategy:

- **new ITS**, **MFT**, **FIT, TPC ROC**
- **update FEE of most detectors**
- **new integrated Online-Offline system (O^2)**





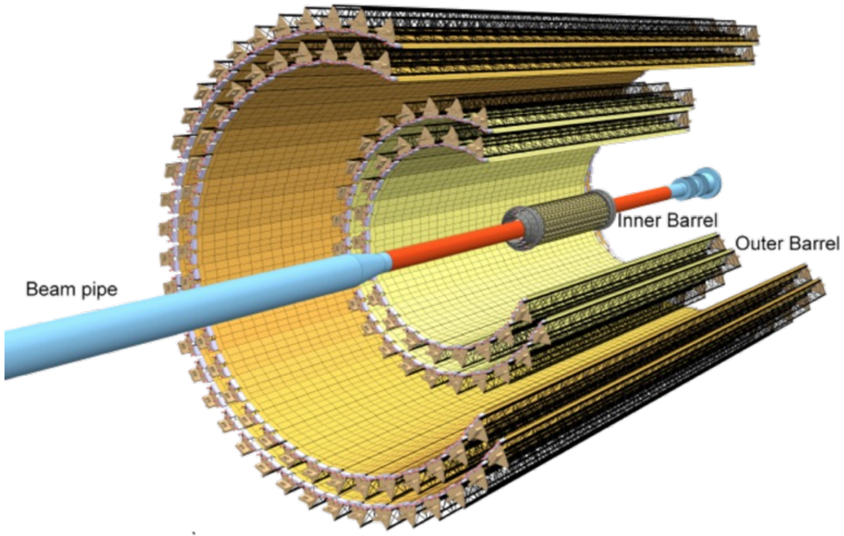
Integrated Online-Offline system (O²)

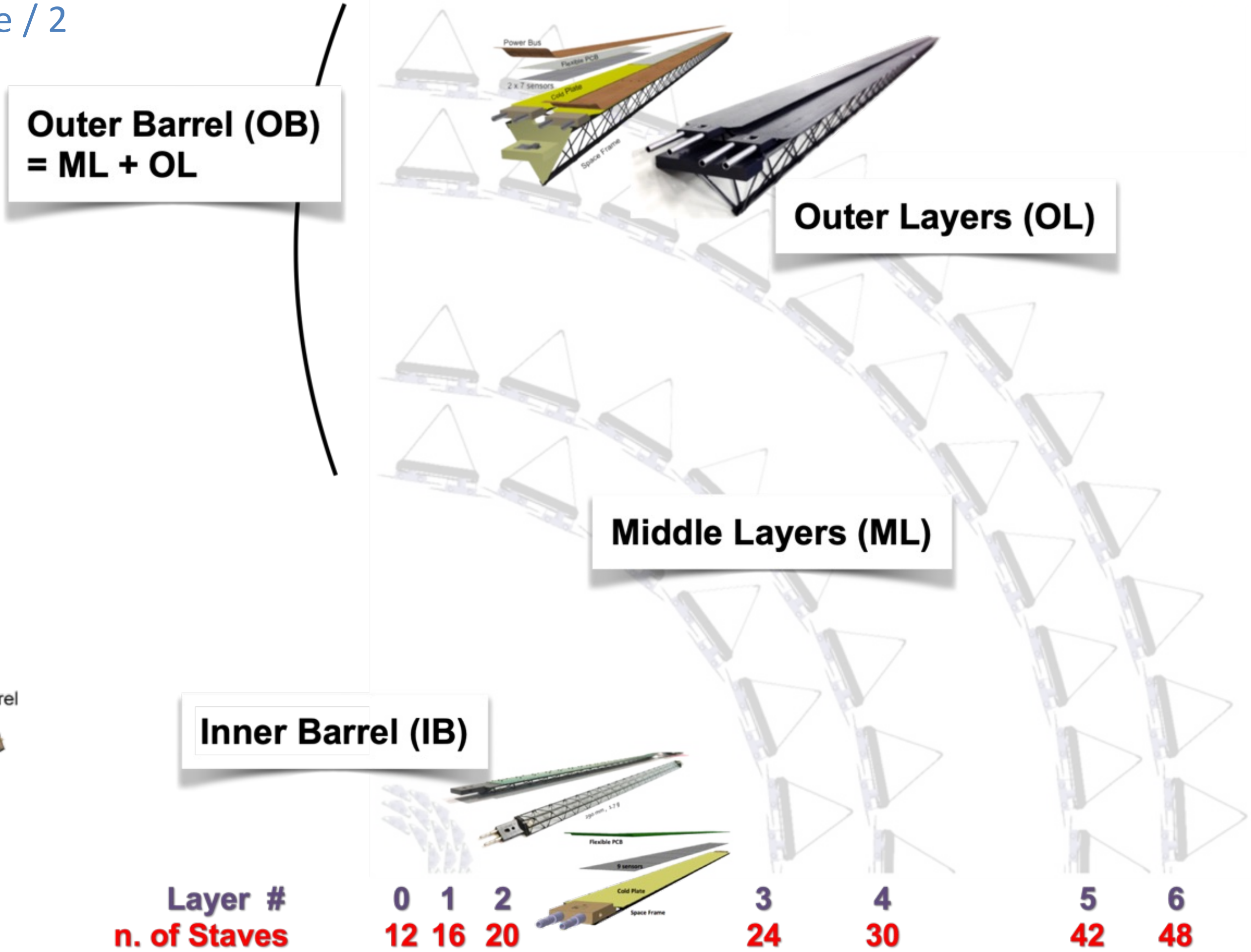
Readout upgrade
TOF, TRD, MUON, ZDC, Calorimeters

ALICE 2

The new ITS

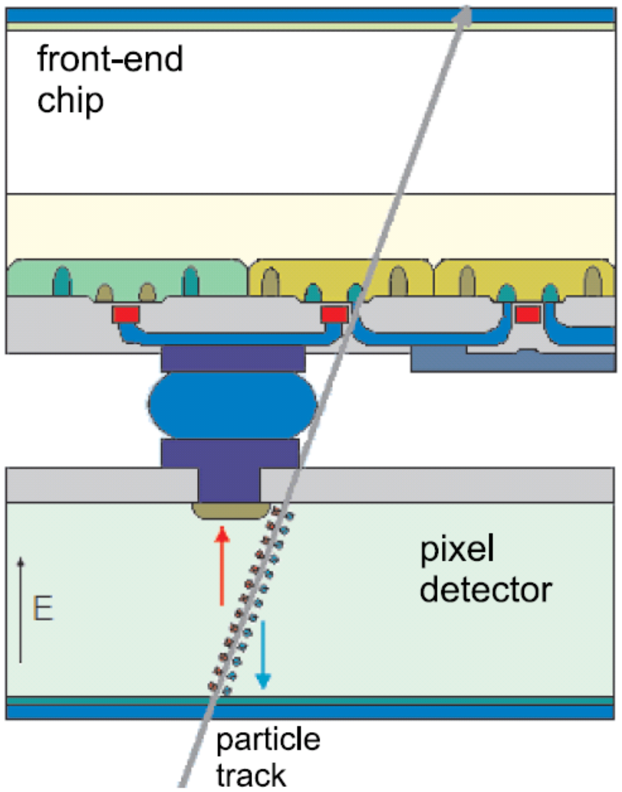
- 7 Layers, all pixel detectors (3 inner / 2 middle / 2 outer)
  from R = 22 mm to R = 400 mm
- 192 Staves (48 IL / 54 ML / 90 OL)
- Ultra-lightweight support structure and cooling
- 10 m^2 active silicon area, 12.5 x 10^9 pixels
- **was 0.2 m^2, 9.8 x 10^6 pixels in ITS1 SPD**





Layer #	0	1	2	3	4	5	6
n. of Staves	12	16	20	24	30	42	48

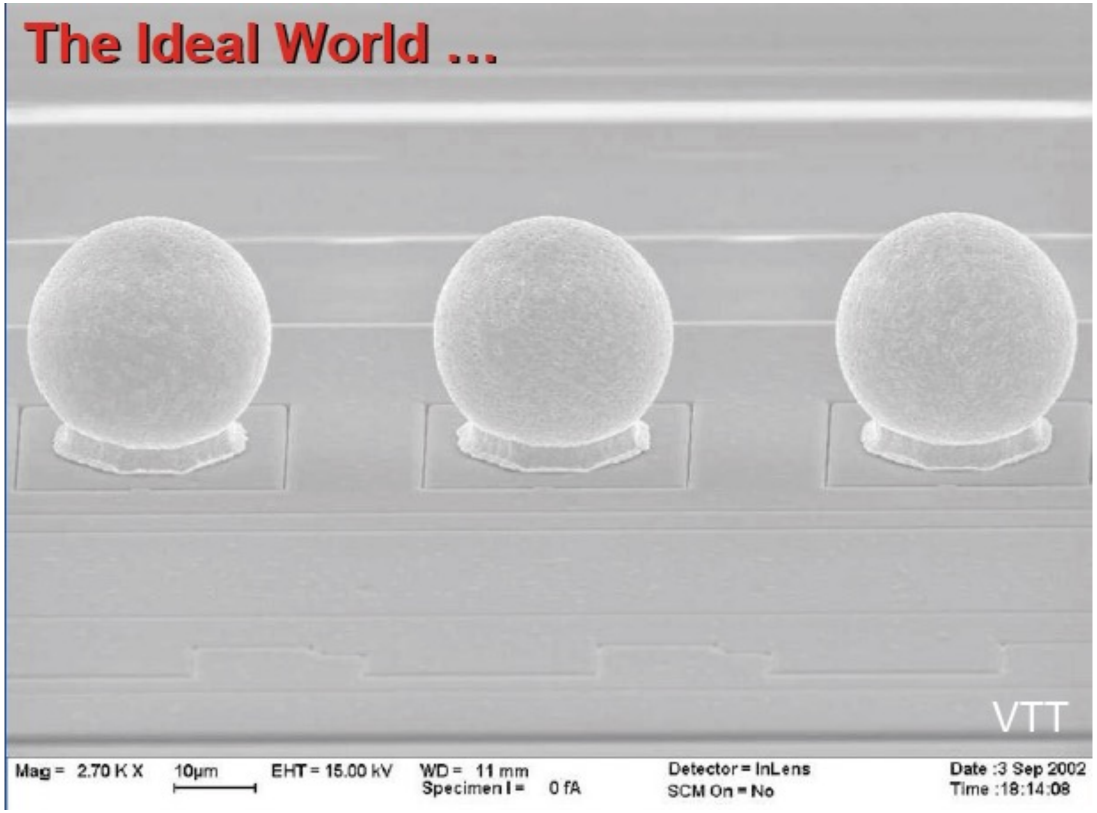
Hybrid pixel detectors



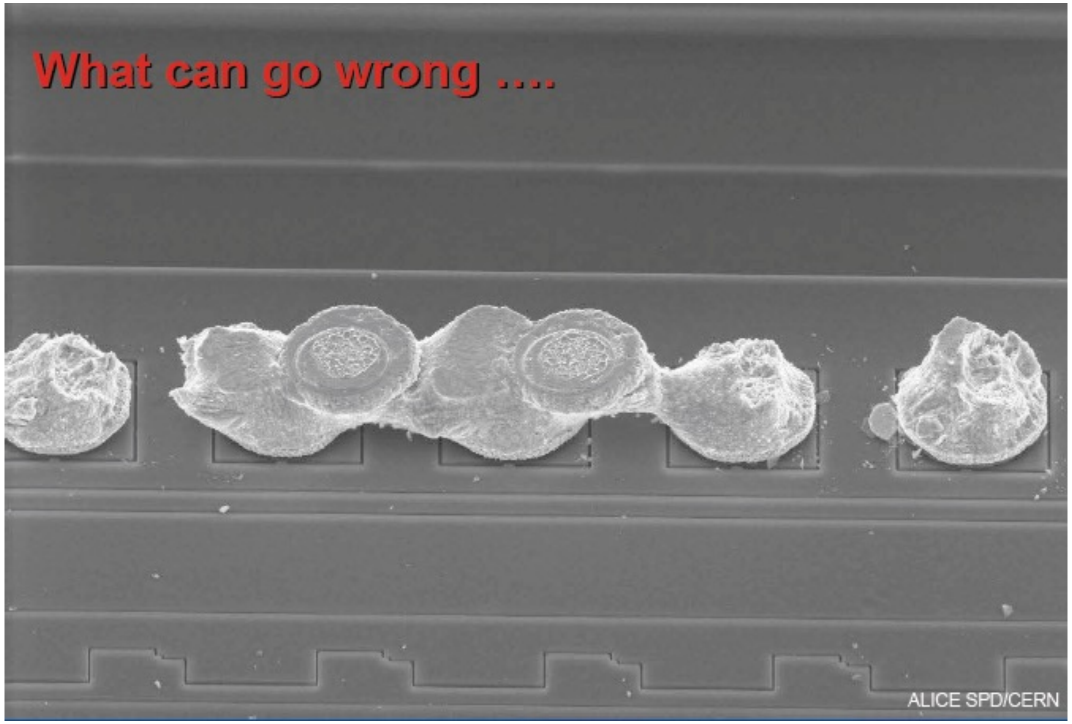
- 1 silicon layer for the sensor
- 1 silicon layer for the electronics
- each pixel is connected to the corresponding electronics channel with a bump bond

- total thickness ≅ 150 + 150 = 300 μm

Bump bonding



Bump bonding



New generation trackers: CMOS sensors

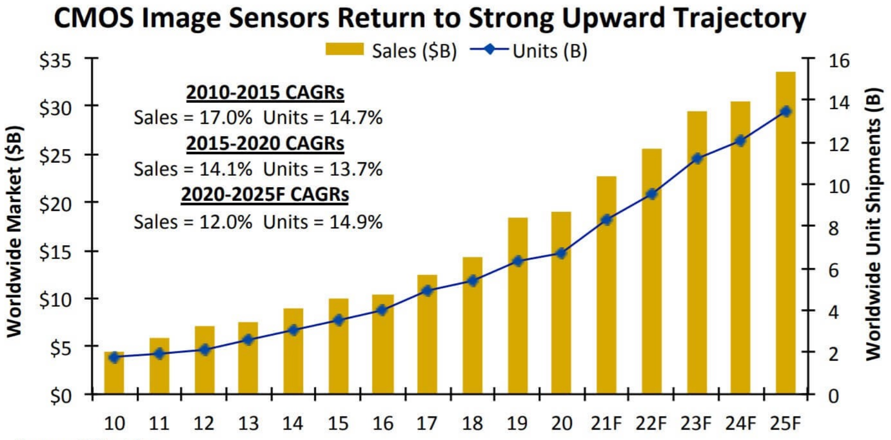
Digital Imaging Revolution

- Start of the “digital imaging revolution” began with the invention of the Charge-Coupled Device (CCD) in 1969
- Boyle and Smith’s invention improved commercial and consumer products for decades and is one of the most important technological innovations of the past half-century
    - Nobel Prize in Physics 2009 Willard S. Boyle and George E. Smith *"for the invention of an imaging semiconductor circuit - the CCD sensor.”*
- Since its inception, digital imaging has progressed through improvements in CCDs and with the emergence of Complementary Metal-Oxide Silicon (CMOS) Image Sensor technology

CMOS Imaging Sensor (CIS)

(Re-) Invented in the early ‘90

- **All-in-one: Electronic Camera On Chip**
- **CMOS technology ⇨much lower production cost, integration of complex functionalities**
- Very small pixels (today ≲1µm, 40M pixel)
- lower power consumption and Increased speed (column- or pixel- parallel processing)



Source: IC Insights

Figure 1

Drivers of CIS development and sales

- camera phones, vehicles, machine vision, human recognition and security, scientific/medical
- **cellular camera phones account for 60% of the sales**
- > 90% of the total image sensor sales in 2021 (it was 74% in 2012, 54% in 2007)

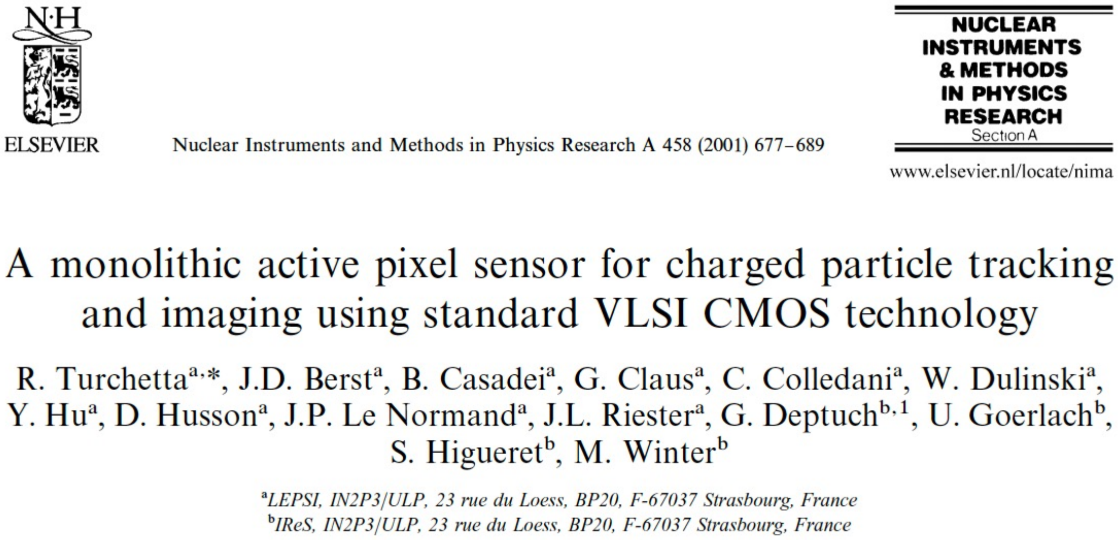
In 2022: 380 sensors/sec, @2.1$/sensor, 6.8M 300mm wafers (480000 m^2 ≈ **8000 ALICE 3 silicon tracker**)

The inception of CMOS APS for charged particles

In 2001, Turchetta et al. started the R&D process to develop a charged particle sensors based on CIS technology.

- Implanted in lightly doped (P-) epitaxial silicon layer
- grown on top of the highly doped (P++) substrate

The charge collection diode is made of the junction between the NWELL and the P-type epitaxial layer



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Nuclear Instruments and Methods in Physics Research A 458 (2001) 677–689

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

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A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta[a,*], J.D. Berst[a], B. Casadei[a], G. Claus[a], C. Colledani[a], W. Dulinski[a], Y. Hu[a], D. Husson[a], J.P. Le Normand[a], J.L. Riester[a], G. Deptuch[b,1], U. Goerlach[b], S. Higueret[b], M. Winter[b]

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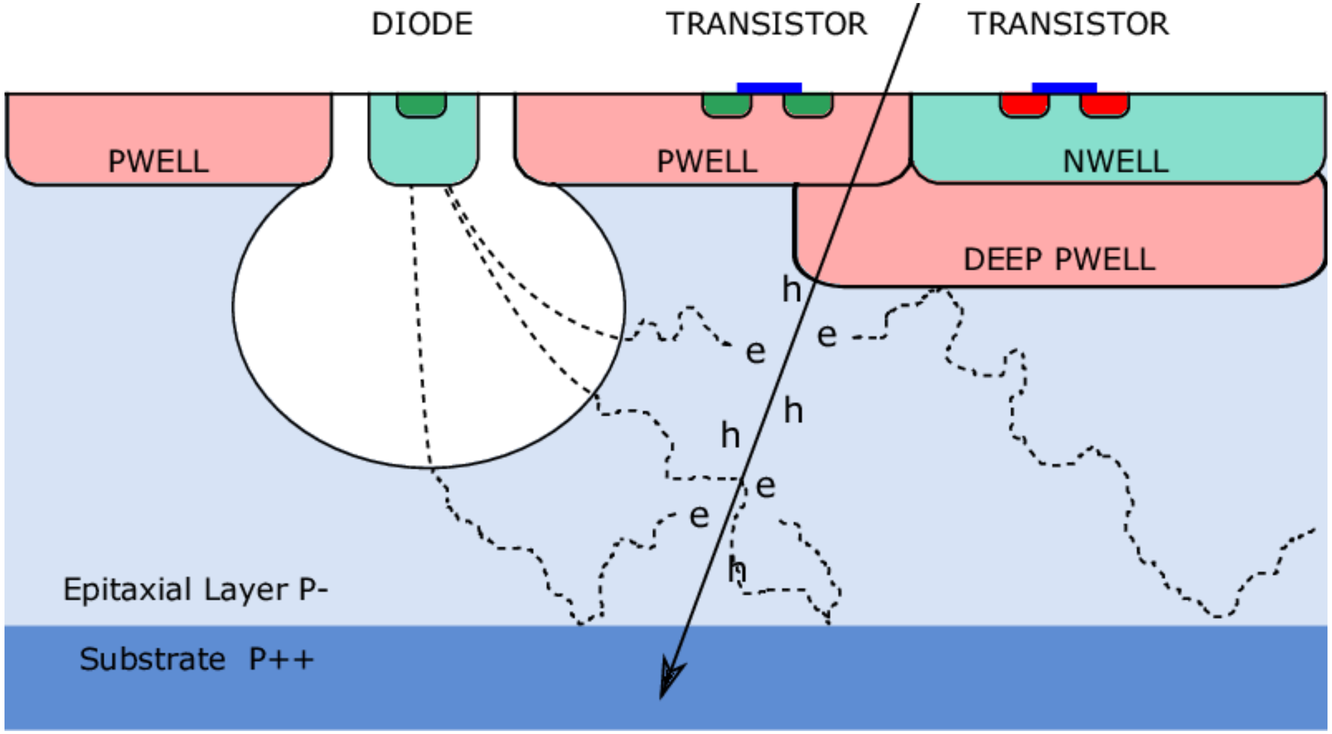
Monolithic pixel detector



electronics

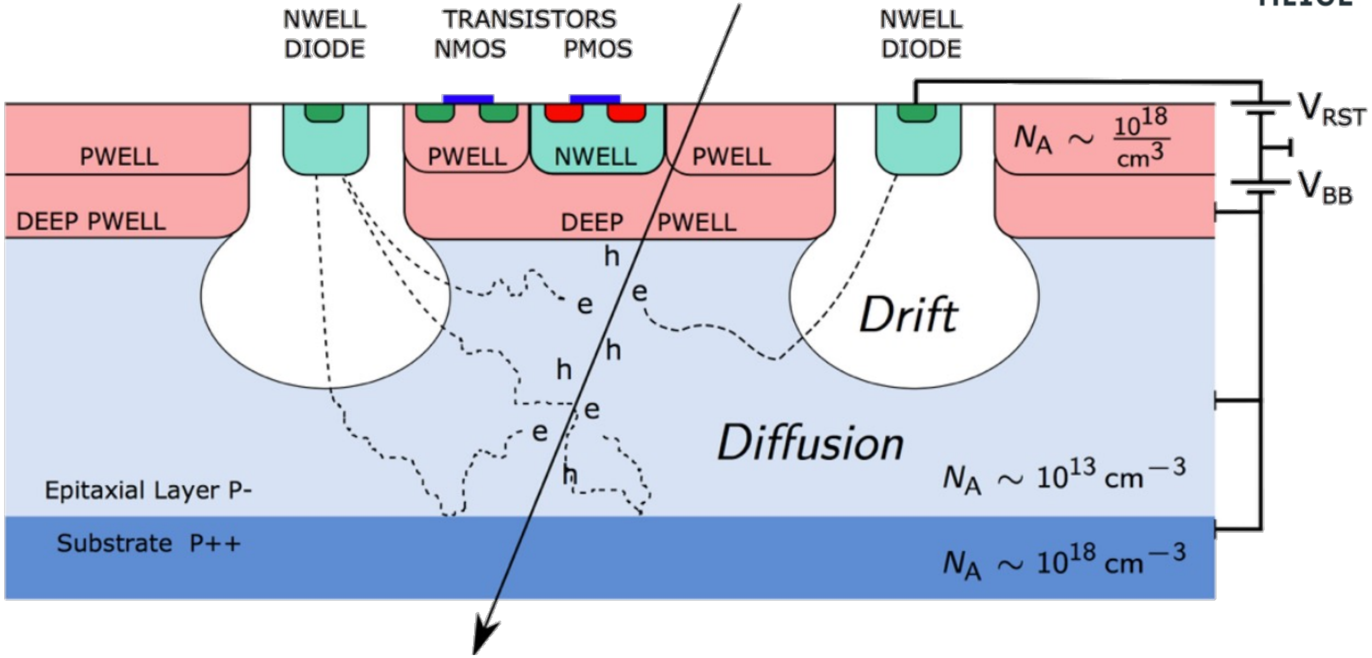
sensitive area

MAPS: CMOS monolithic active pixel sensor

MAPS: sensor and electronics on the same substrate

Exploits commercial CMOS imaging sensor process to detect charge particles

A few modifications needed: DEEP P-WELL to shield CMOS circuitry and avoid loss of efficiency



main advantages:

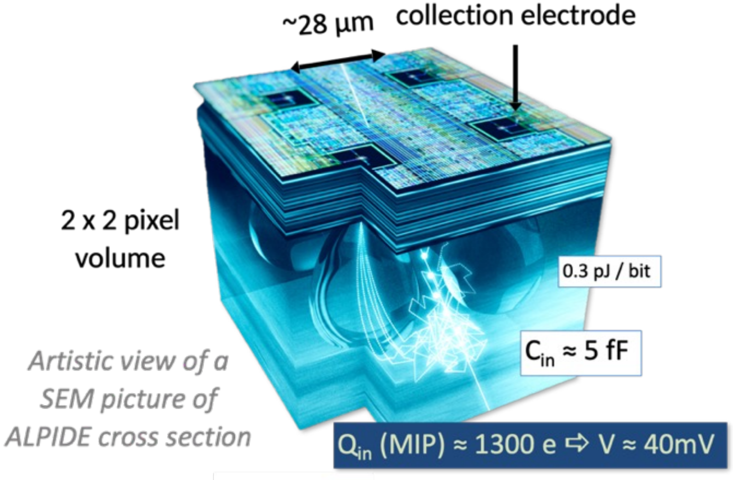
- thin sensor (all in 1 layer, thinned down to <50μm)
- easy integration
- low noise
- low power consumption

disadvantages:

- Signal charge is collected from the non-depleted layer, diffusion dominated and prone to trapping after irradiation
- Deep well and substrate limit extension of the depletion: to fix this -> pixel design/process modification.

ALPIDE Monolithic Pixel Sensor

CMOS Pixel Sensor – Tower Semiconductor 180nm CMOS Imaging Sensor (CIS) Process



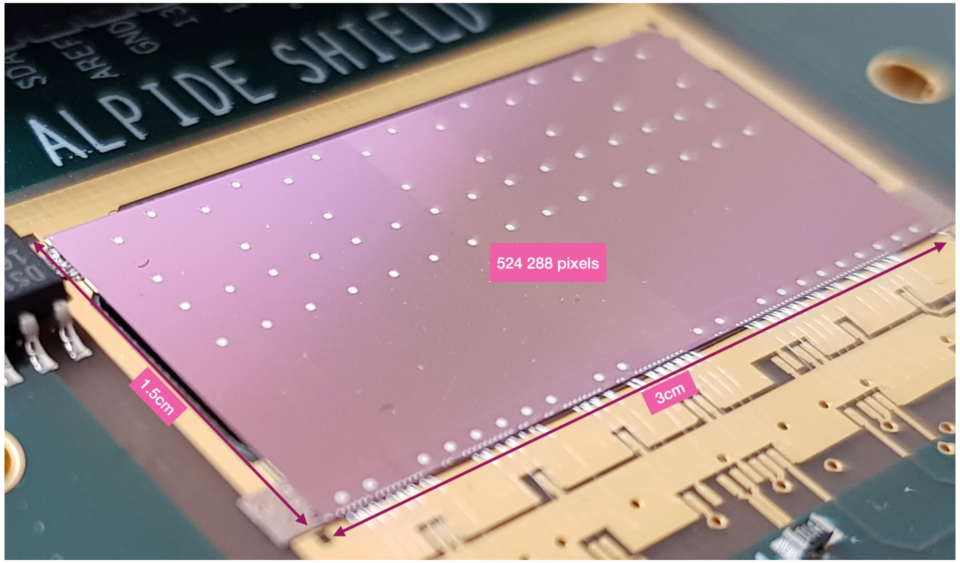
Artistic view of a SEM picture of ALPIDE cross section

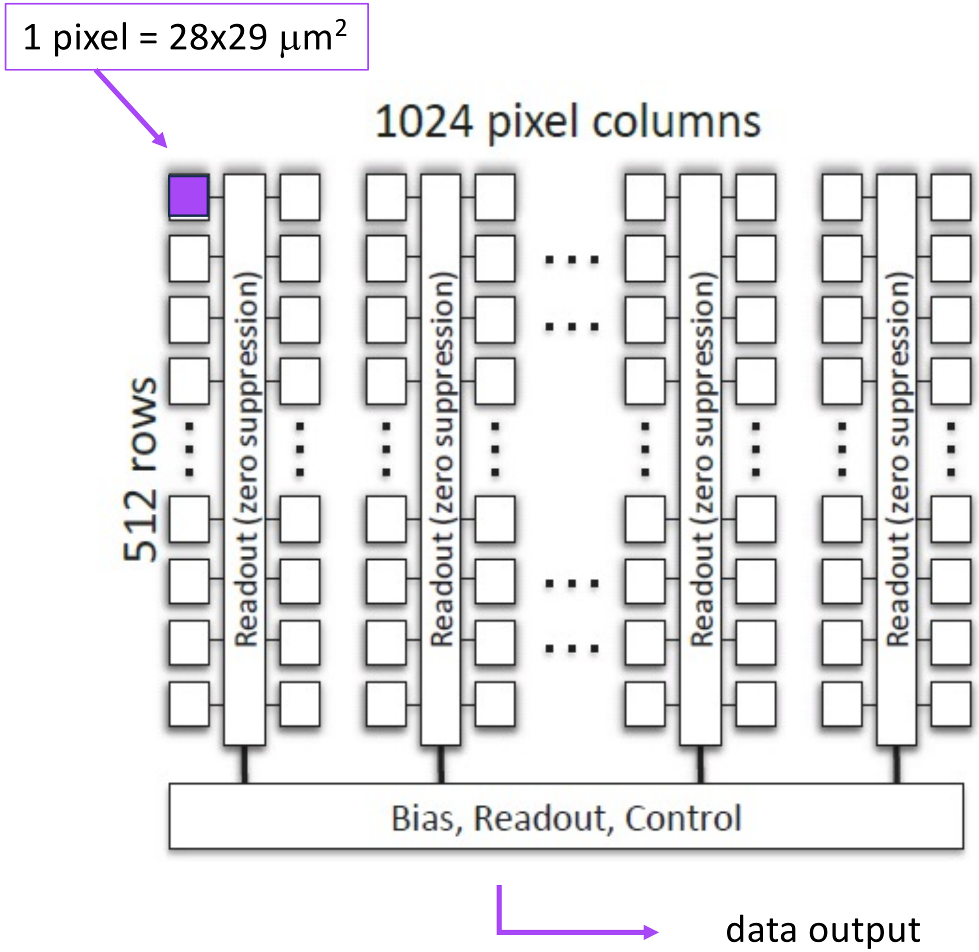
ALPIDE Key Features

- In-pixel: Amplification, Discrimination, multi event buffer
- **In-matrix zero suppression**: priority encoding
- **Ultra-low power < 47mW/cm² (< 140mW full chip)**
- **Detection efficiency > 99%**

- **Spatial resolution ~5μm**
- Low fake-hit rate: << 10^{-6}/pixel/event (10^{-8}/pixel/event measured in data taking)
- Radiation tolerance: >270 krad (TID), > 1.7 10^{13} 1MeV/n_{eq} (NIEL)

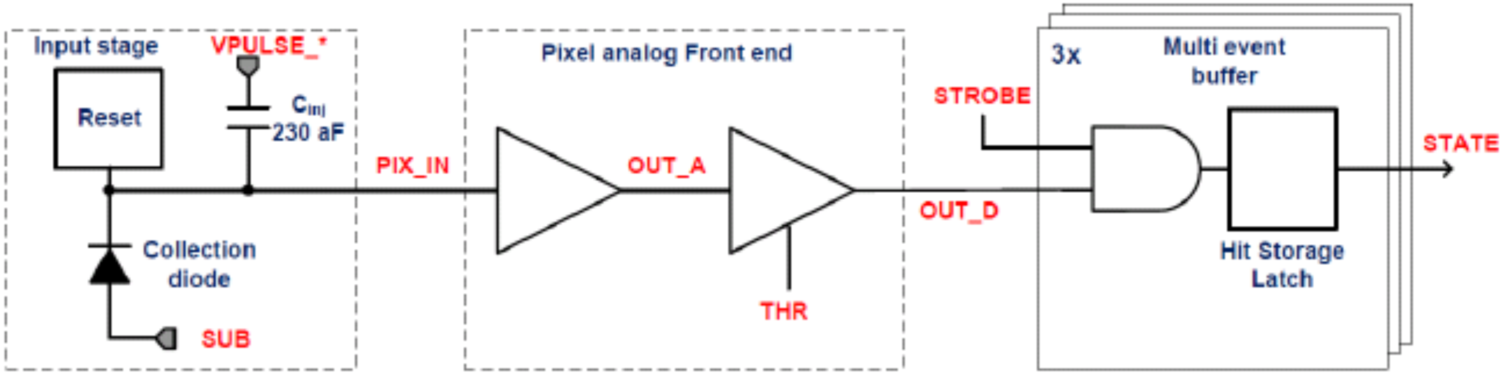
Pixel matrix

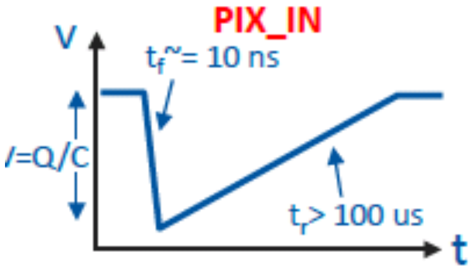


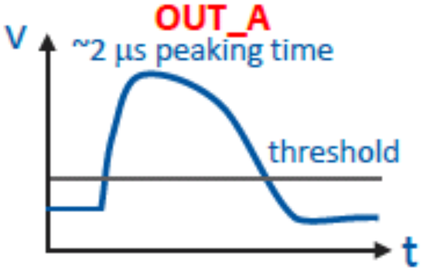


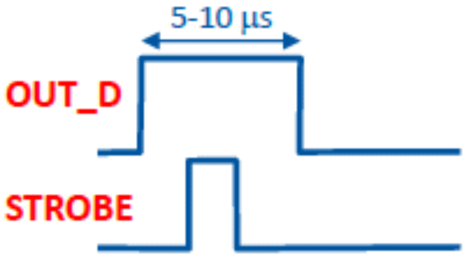
data output

Pixel cell


Input stage
VPULSE_*
Reset
C_{inj}
230 aF
Collection diode
SUB
PIX_IN
Pixel analog Front end
OUT_A
THR
STROBE
OUT_D
3x
Multi event buffer
Hit Storage Latch
STATE


PIX_IN
V
t_f~= 10 ns
/=Q/C
t_r> 100 us
t


OUT_A
V
~2 μs peaking time
threshold
t


5-10 μs
OUT_D
STROBE

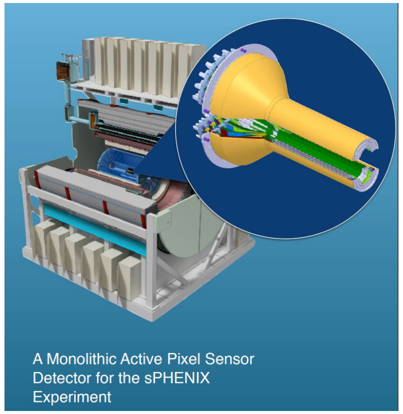
ALPIDE and other developments

With permission. Article online

- R&D effort within the ALICE collaboration
  - excellent collaboration with foundry
  - more than 70k chips produced and tested
  - ALICE ITS pioneers large area trackers built of MAPS (EIC, ALICE 3, FCC?)

- in parallel studies to optimise process to reach full depletion and improve time response and radiation hardness up to 10^{15} 1MeV/n_{eq}

Adopted or considered for other experiments: **HADES, CBM, PANDA, NUSTAR, NA61, CSES2-Limadou, iMPACT, COMPASS++/AMBER, pCT, ePIC…**

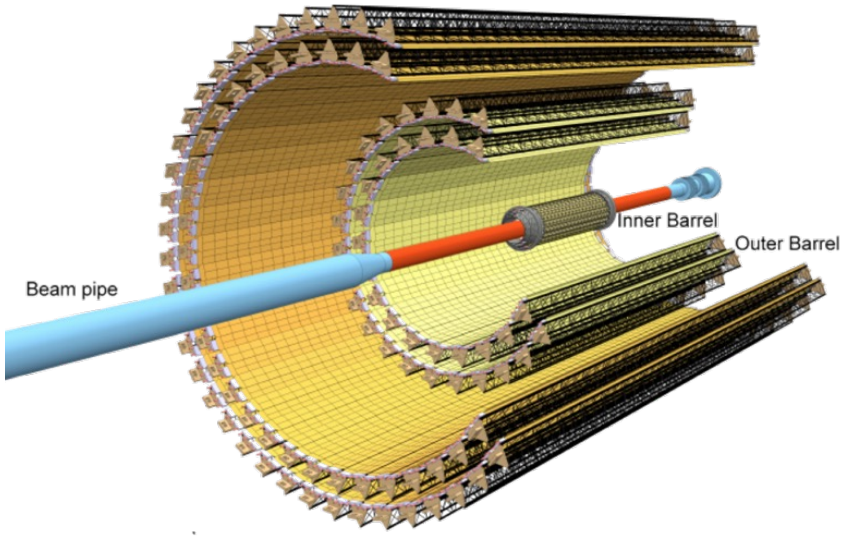


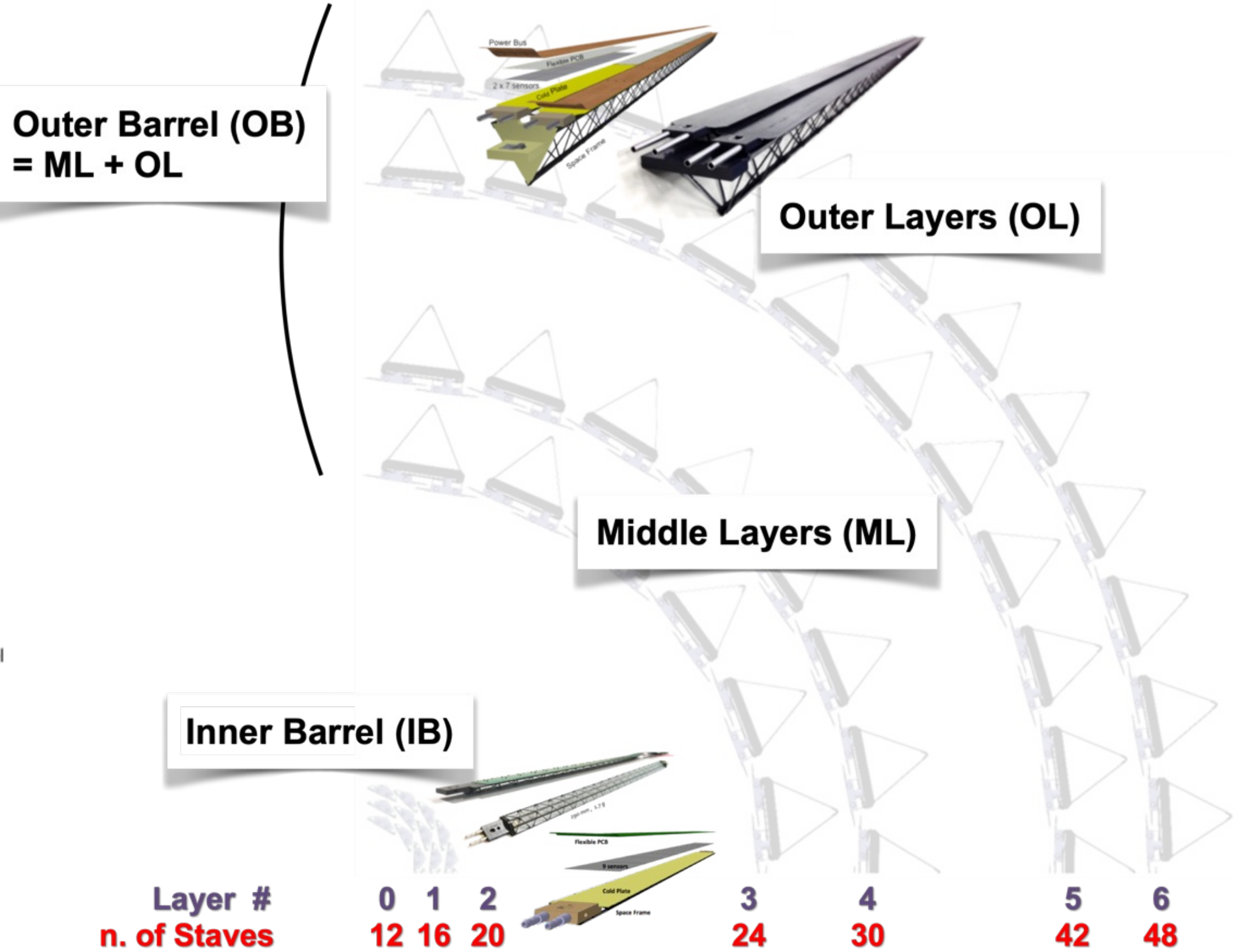
A Monolithic Active Pixel Sensor Detector for the sPHENIX Experiment

Detector replicas for new experiments
sPHENIX MVTX @RHIC

The largest MAPS pixel detector (so far)

- 7 Layers (3 inner / 2 middle / 2 outer) from R = 22 mm to R = 400 mm
- 192 Staves (48 IL / 54 ML / 90 OL)
- Ultra-lightweight support structure and cooling
- 10 m^2 active silicon area, 12.5 x 10^9 pixels





Outer Barrel (OB) = ML + OL

Outer Layers (OL)

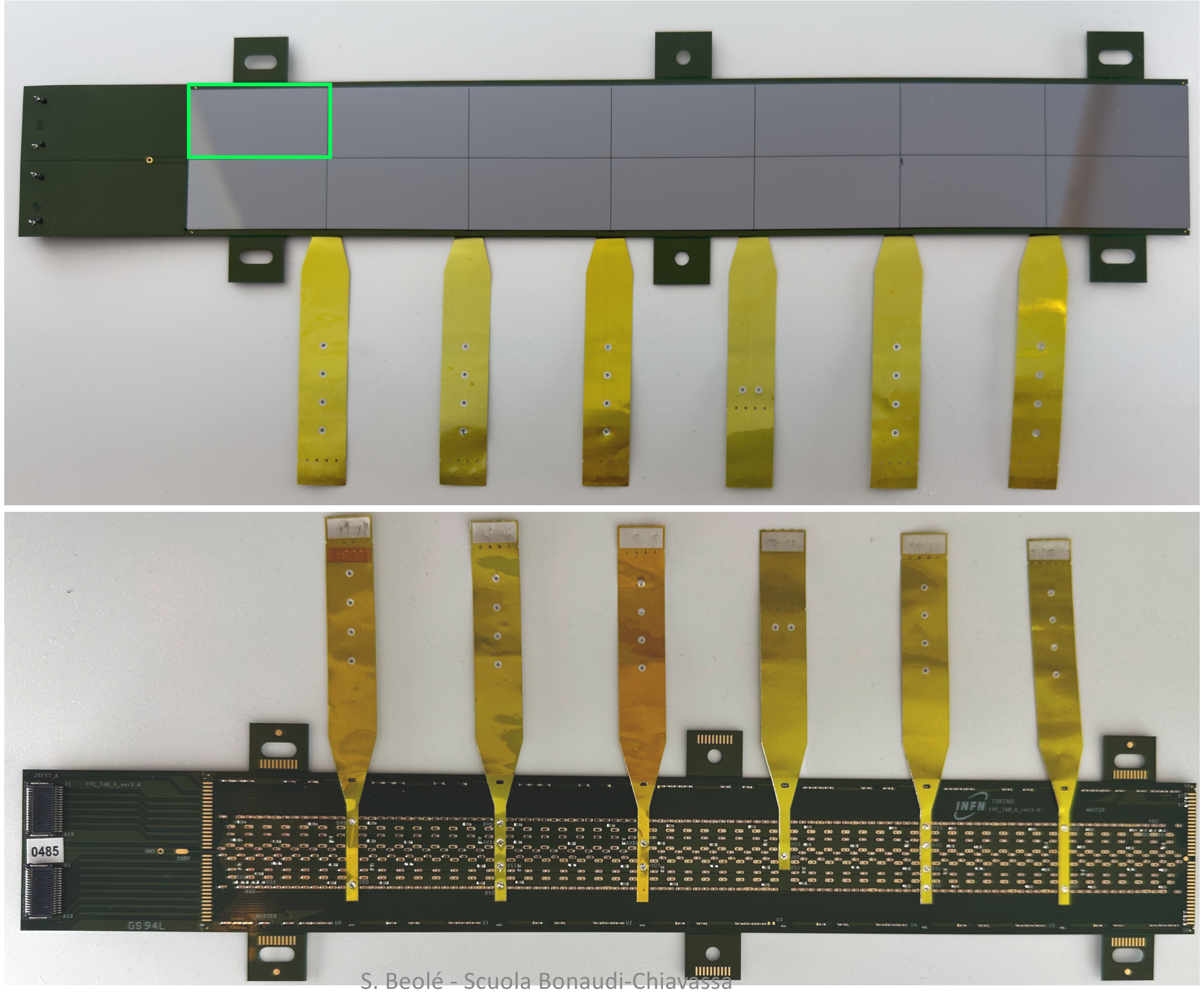
Middle Layers (ML)

Inner Barrel (IB)

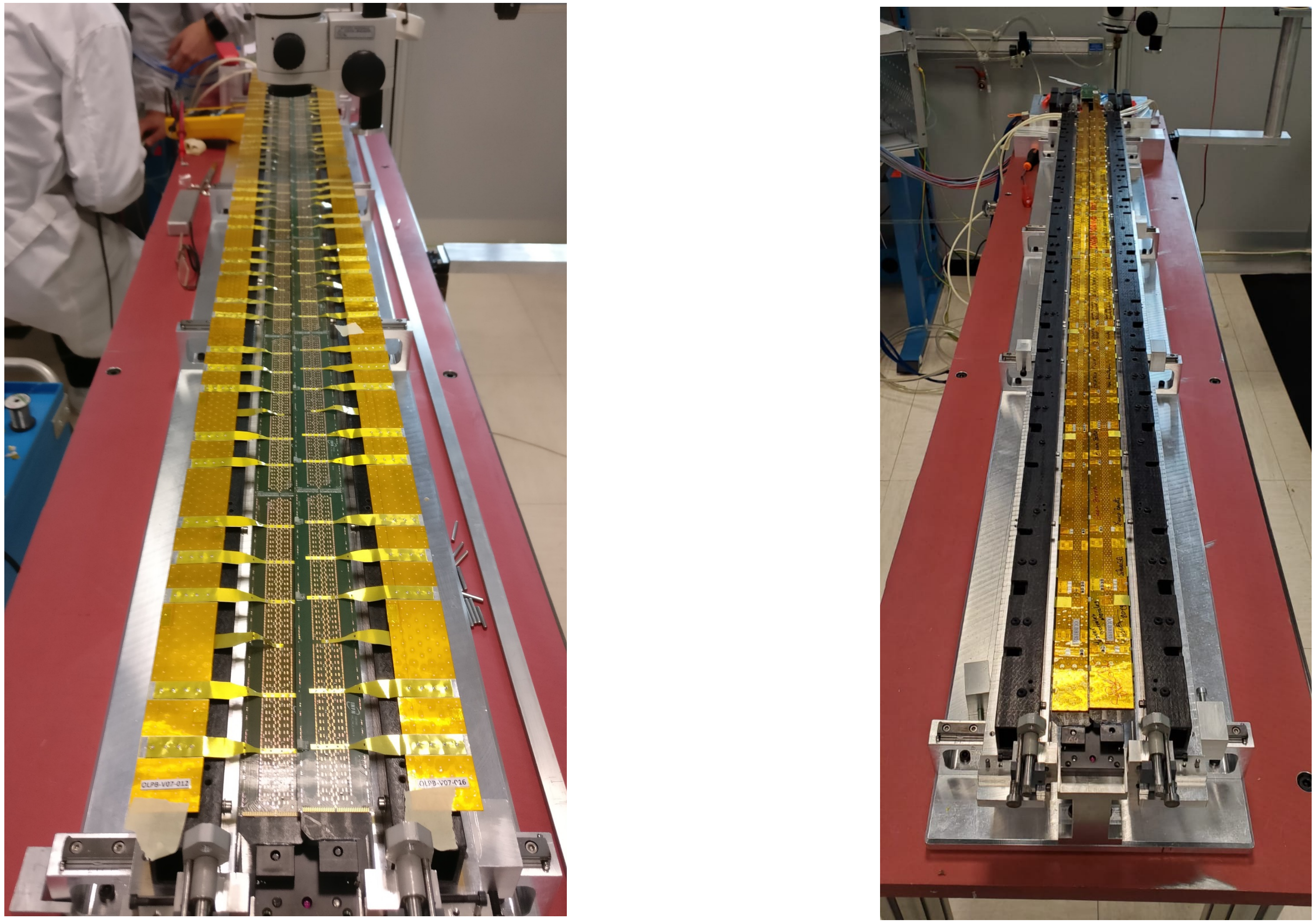
Layer #	0	1	2	3	4	5	6
n. of Staves	12	16	20	24	30	42	48

Tiling up: chips to modules

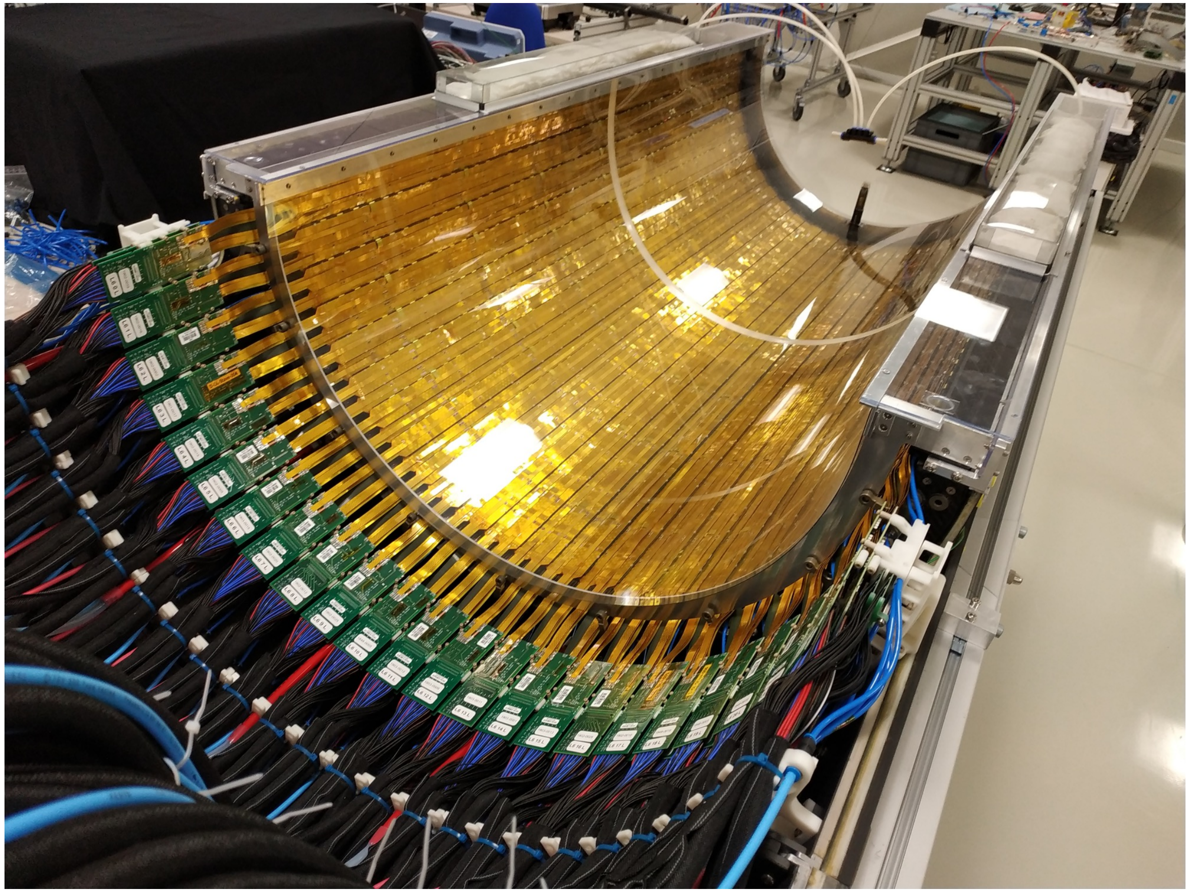
1 ALPIDE = 1.5 x 3 cm^2



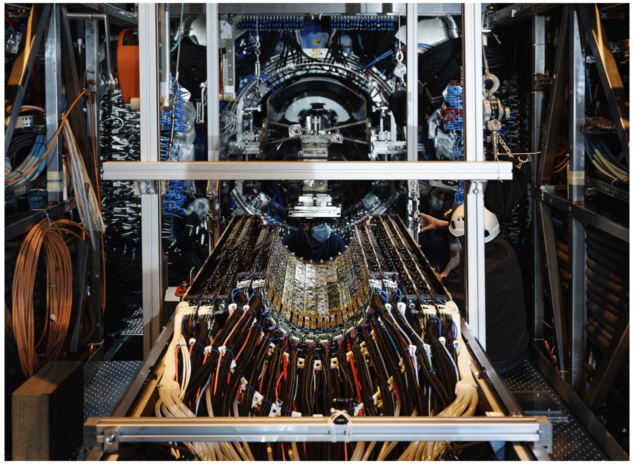
Tiling up: modules to staves



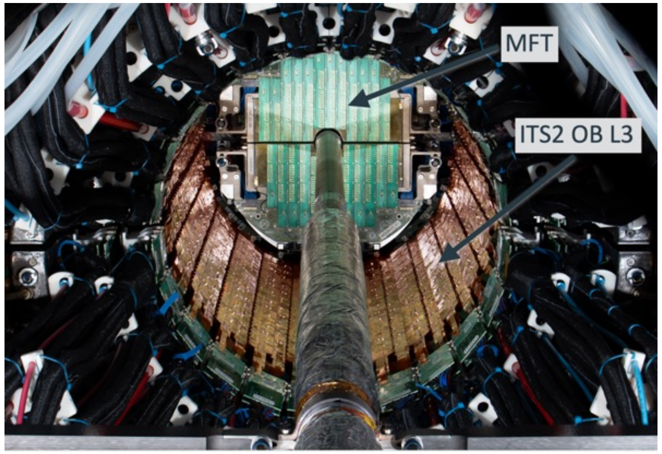
Stave to layers



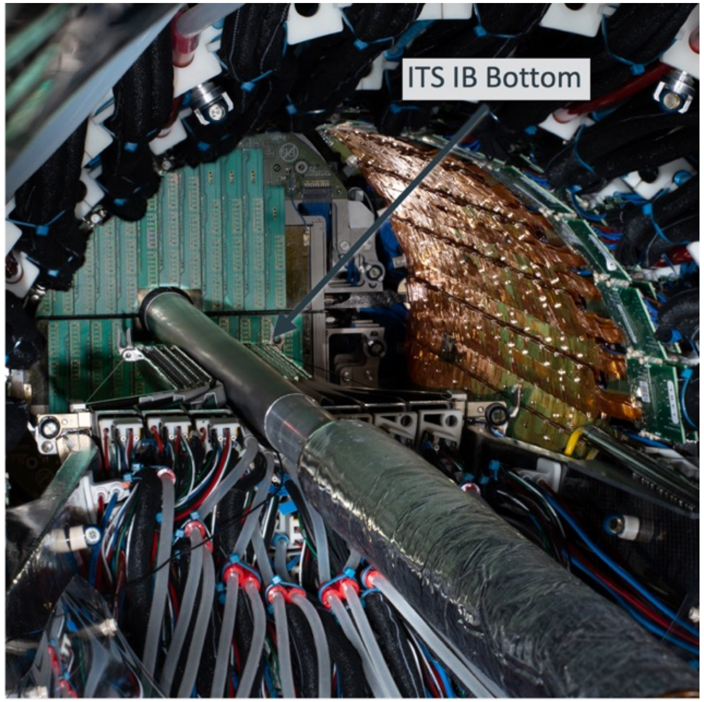
ITS installation



ITS Bottom half barrel insertion



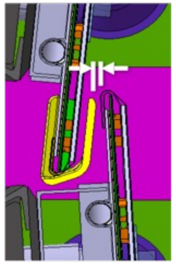
ITS Outer Barrel surrounding the beam pipe, MFT in the back



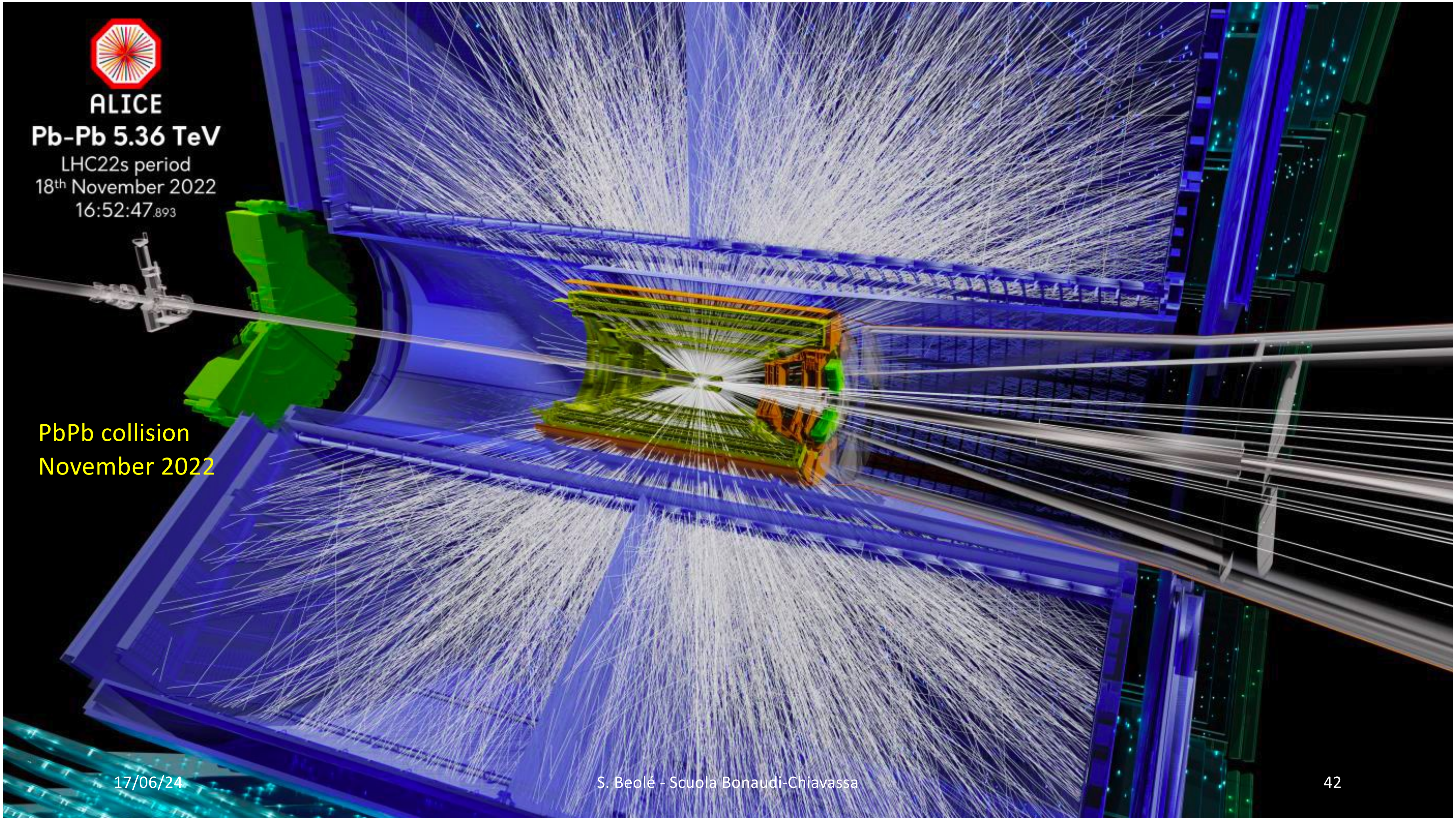
ITS Inner Barrel Bottom and Outer Barrel

- Installation challenges
  - Precise positioning around the beam pipe (nominal clearance ~ 2 mm)
  - Manipulating from 4 m distance
  - Difficult to see actual position by eye
  - precise mating of top and bottom barrel halves (clearance between adjacent staves ~ 1.2 mm)
- Dry-installation tests on the surface to test and exercise procedures
- Use of 3D scans, surveys and cameras

1.2 mm nominal clearance



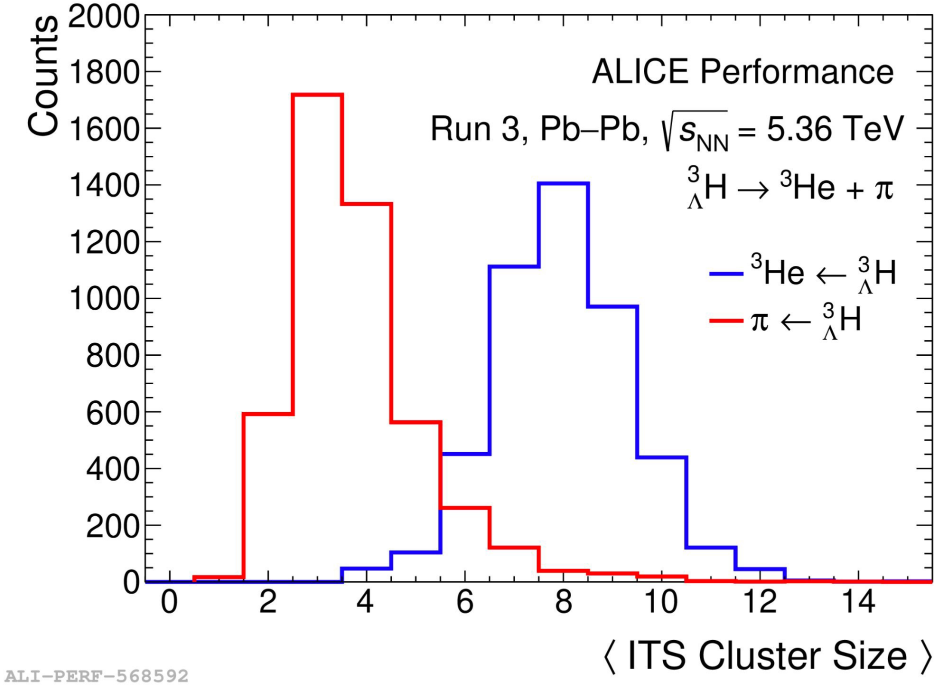
OB stave edge clearance when fully mated

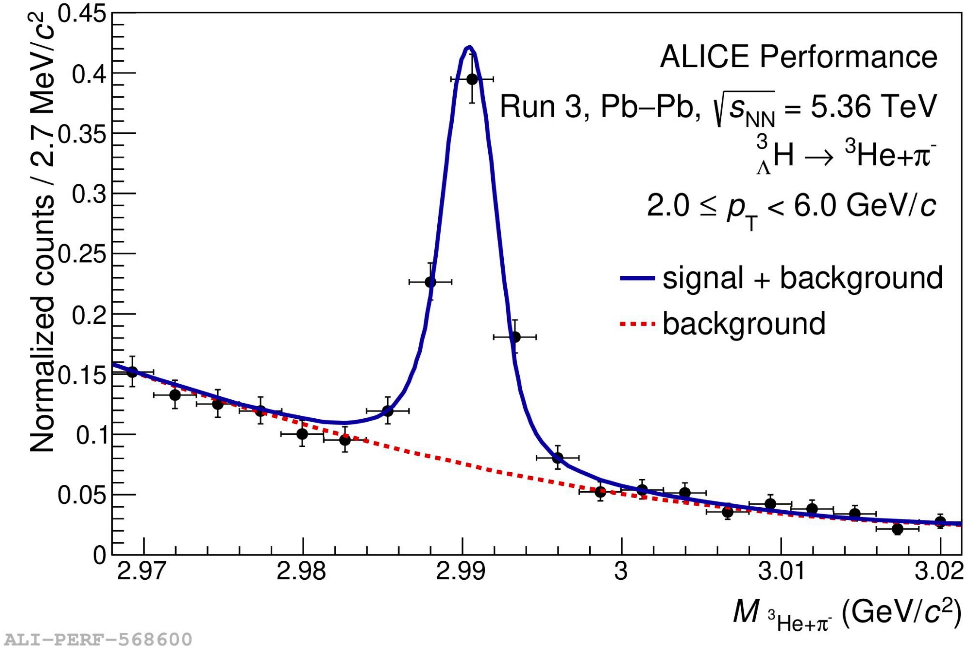


PbPb collision
November 2022

ITS PID from cluster size

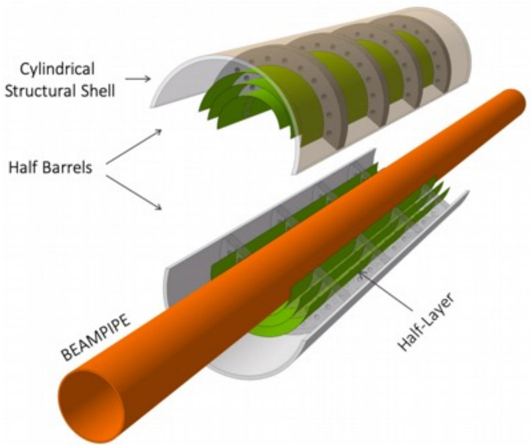
- Hypertriton two-body decay channel reconstruction
  - Use of ITS cluster size to tag ^{3}He daughter track and reduce ITS-TPC fake matchings (π vs ^{3}He)
  - PID capabilities of a silicon digital detector !

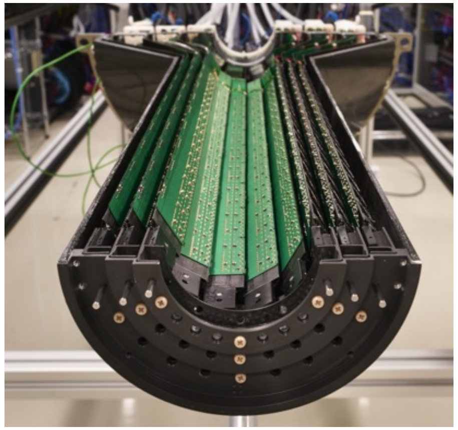




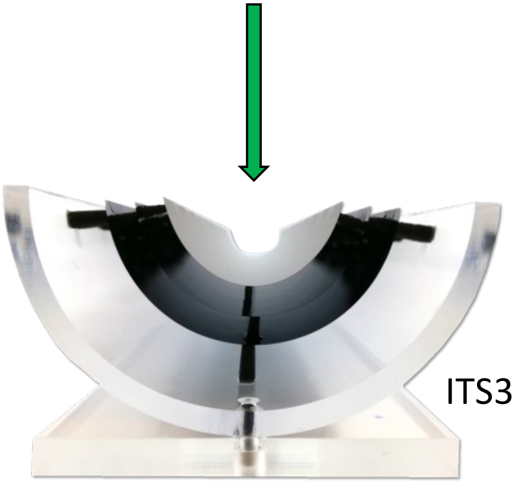
Can we improve further?

ALICE 2.1: ITS3 the "all silicon" detector





ITS2 Inner Barrel

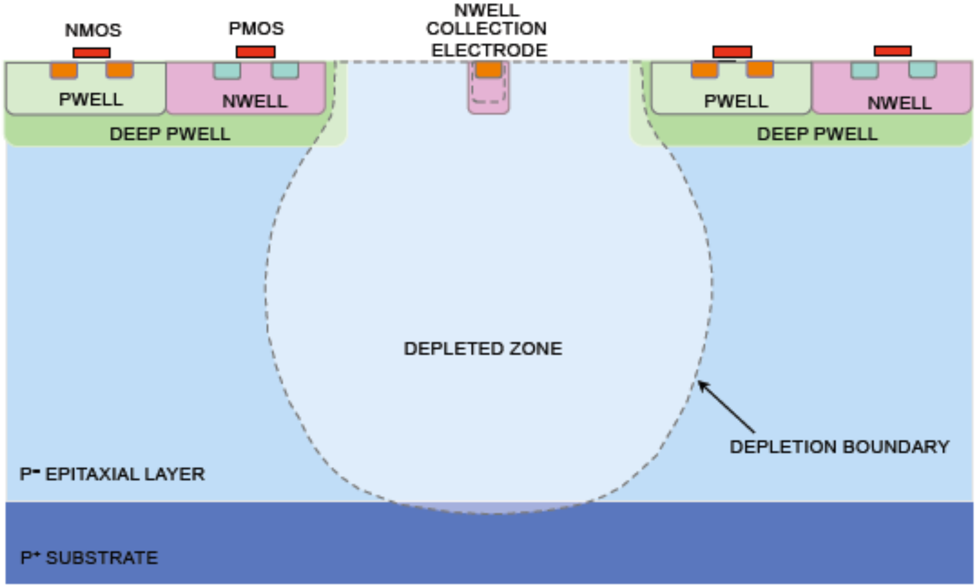


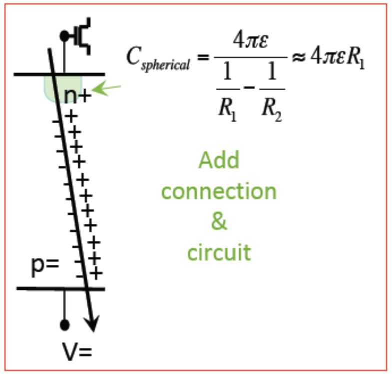
ITS3 mechanical mockup

- GOAL for ALICE ITS3:
  - improve determination of primary and secondary vertices at high rate
    - go closer to interaction point
    - **reduce material budget by a factor of 7 (X/X_0 0.35%→0.086%)**
- "SILICON ONLY" TRACKER?
  - exploit stitching → large area sensors
  - thin and bend → sigle sensor half layers

Improvement of sensor detection efficiency: full depletion

ALPIDE: sensitive epitaxial layer not depleted





$$C_{spherical} = \frac{4\pi\varepsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\varepsilon R_1$$

Add connection & circuit

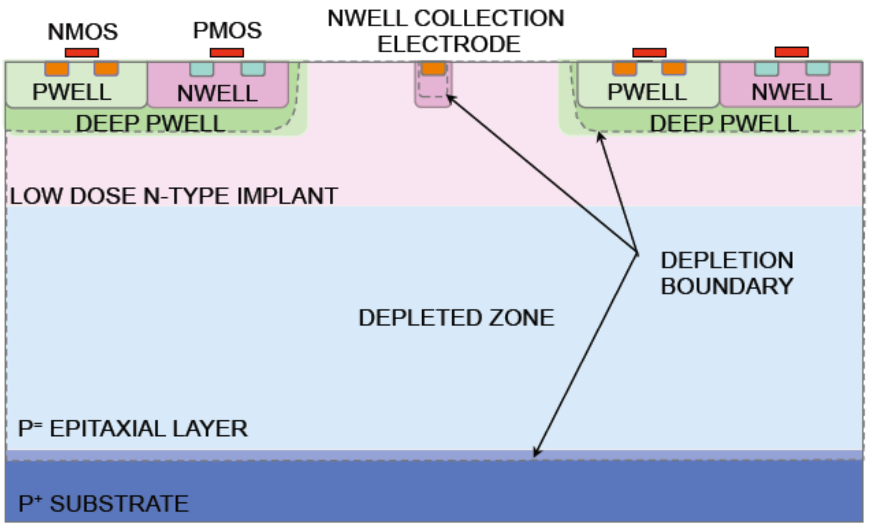
Planar junction
Depletion width $= \sqrt{\dfrac{2\mathcal{E}|V|}{qN_A}}$

Spherical junction
Outer depletion radius $= \sqrt[3]{\dfrac{2\mathcal{E}|V|}{qN_A}\dfrac{3R_1}{2}}$

- Tower Semiconductor 180nm CMOS imaging sensor process
- **Signal charge is collected from the non-depleted layer,** diffusion dominated and prone to trapping after irradiation
- Planar vs spherical junction
  - Planar junction: depletion thickness proportional to **square root of reverse bias**.
  - Spherical junction : depletion thickness proportional only to **cubic root of reverse bias**, inner radius R1 to be kept small for low capacitance
- Deep well and substrate limit extension of the depletion: to fix this -> pixel design/process modification.

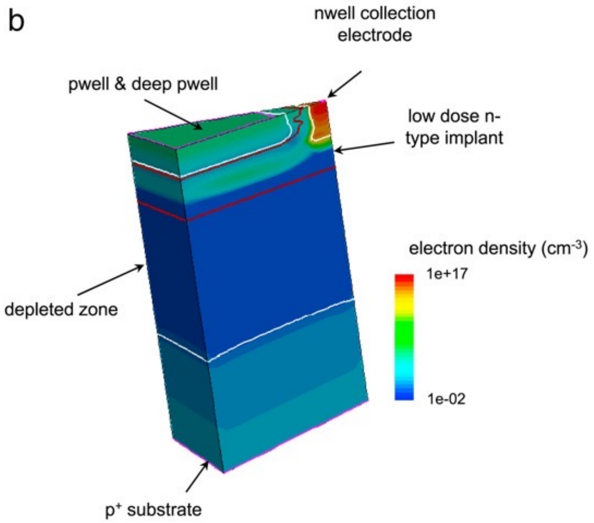
W. Snoeys

Sensor optimization (1): DEPLETED MAPS



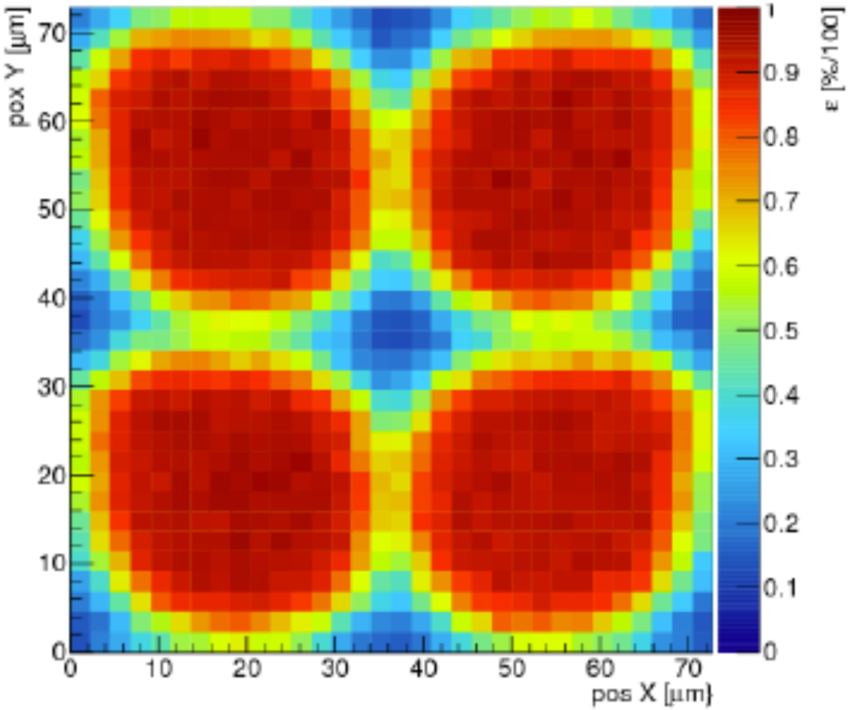
https://doi.org/10.1016/j.nima.2017.07.046 (180nm)

- GOAL: create planar junction using deep **low dose n-type implant** and deplete the epitaxial layer
- first studies within ALICE R&D: Investigator chip
- interest from ATLAS followed by many others: MALTA/TJ MONOPIX development (Bonn, CPPM, IRFU and CERN)



Tower Semiconductor 180nm

Sensor optimization (1): results



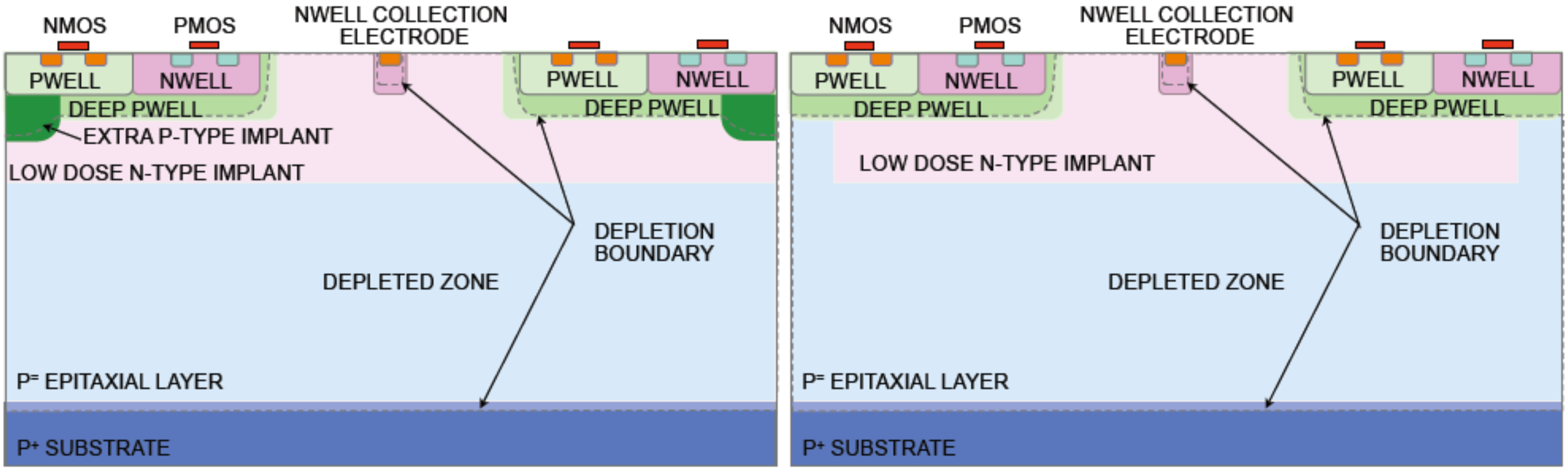
https://doi.org/10.1016/j.nima.2019.162404

However:

- efficiency loss at ~ 10^{15} 1 MeV n_{eq}/cm^2 on the pixel edges and corners due to a too weak lateral field
- Lateral electric field not sufficient to push the deposited charge towards the small central electrode.
- Efficiency decreases in pixel corners
- Effect amplified by radiation damage

Tower Semiconductor 180nm

Sensor optimization (2): improvement of the lateral field

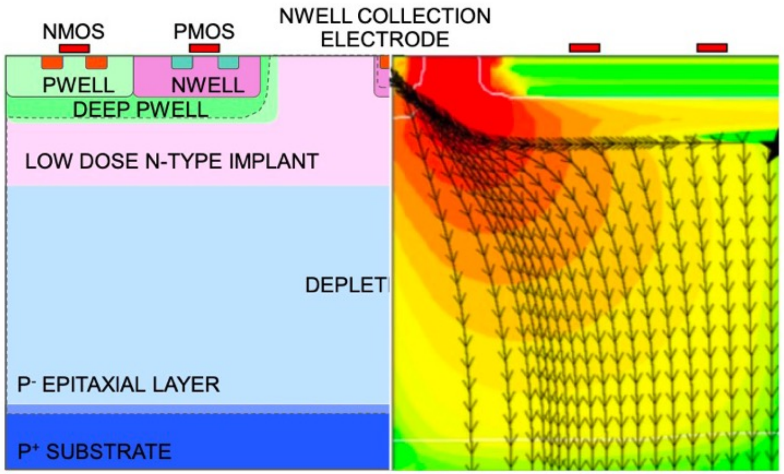


3D TCAD simulation M. Munker et al. PIXEL2018 https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

- Additional deep p-type implant or gap in the low dose n-type implant improves lateral field near the pixel boundary and accelerates the signal charge to the collection electrode.

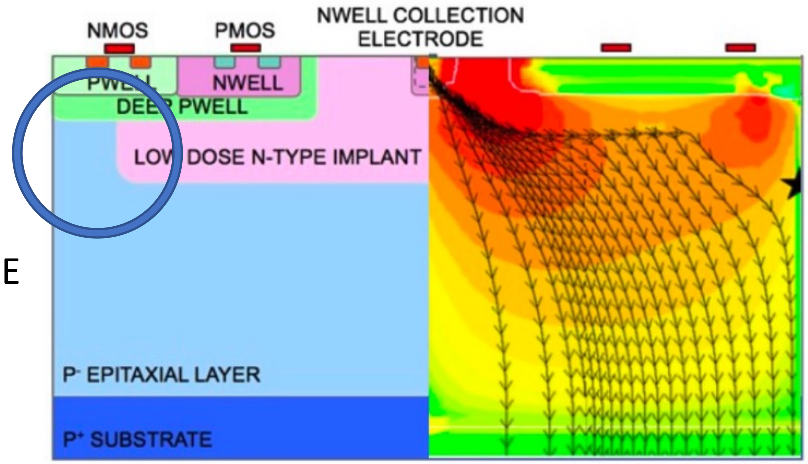
Tower Semiconductor 180nm

Sensor optimization (2): improvement of the lateral field



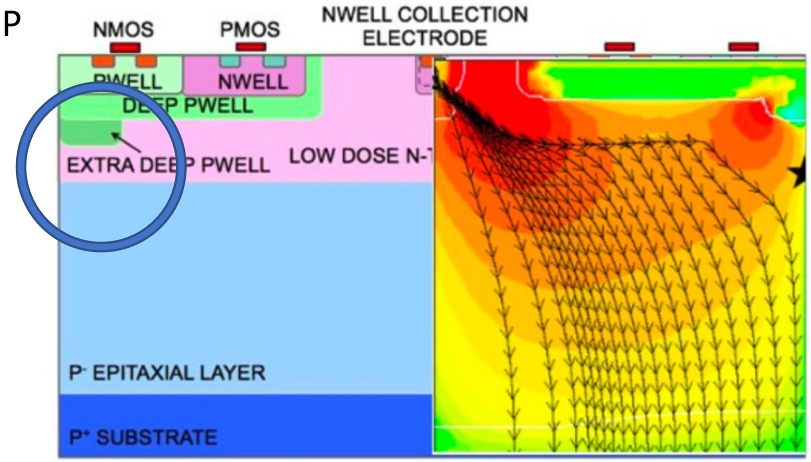
Standard modified process

GAP IN THE
N LAYER



Gap in the n- layer (NGAP)

EXTRA DEEP
P-WELL



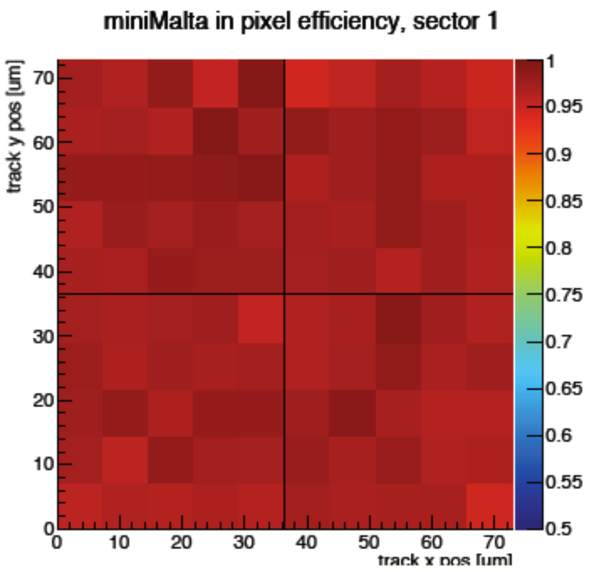
Extra deep p-well (EDPW)

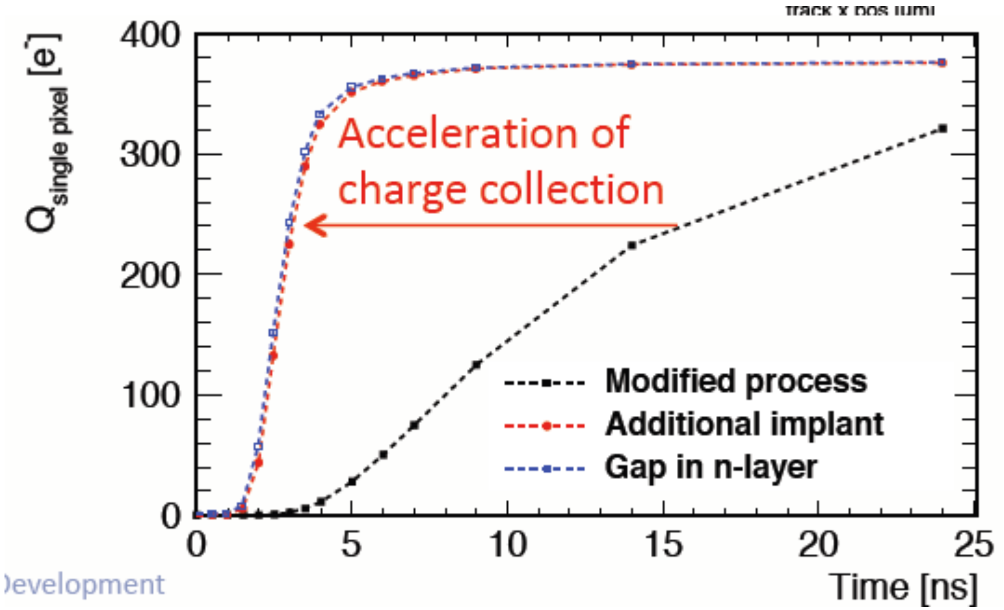
Process modifications to improve charge collection in the pixel edges

3D TCAD simulation M. Munker et al. PIXEL2018 https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

Tower Semiconductor 180nm

Sensor optimization (2): results





- Full detection efficiency at 10^{15} n_{eq}/cm^2
- better sensor timing

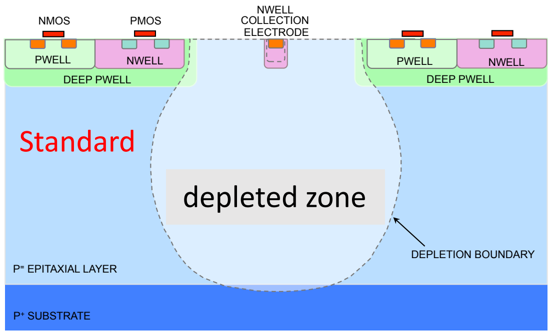
H. Pernegger et al., Hiroshima 2019,
M. Dyndal et al 2020 JINST 15 P0200

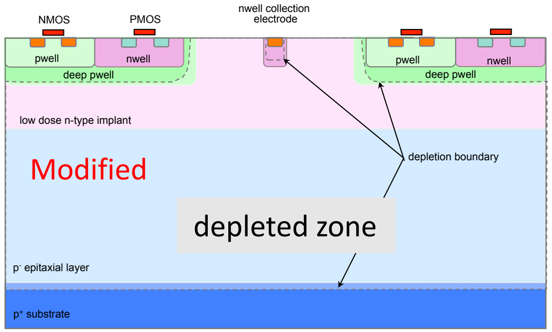
3D TCAD simulation M. Munker et al. PIXEL2018
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

Tower Semiconductor 180nm

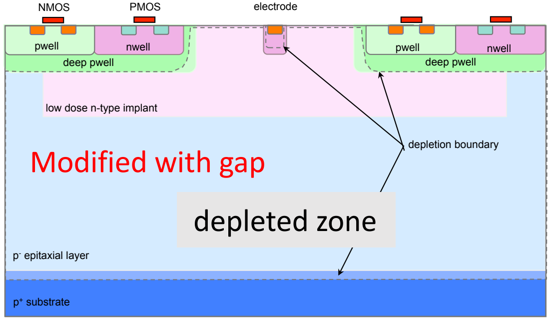
Optimization of the 65nm sensor

- GOAL: create planar junction using deep **low dose n-type implant** and **deplete the epitaxial layer**: same approach as 180nm
- Additional deep p-type implant or **gap in the low dose n-type implant improves lateral field near the pixel** boundary and accelerates the signal charge to the collection electrode.
- Process modification as side activity of ALICE R&D
- Further optimised within ATLAS R&D
- Following the experience with 180 nm, the 65 nm CIS process could be modified
- Full depletion: faster charge collection, higher radiation hardness



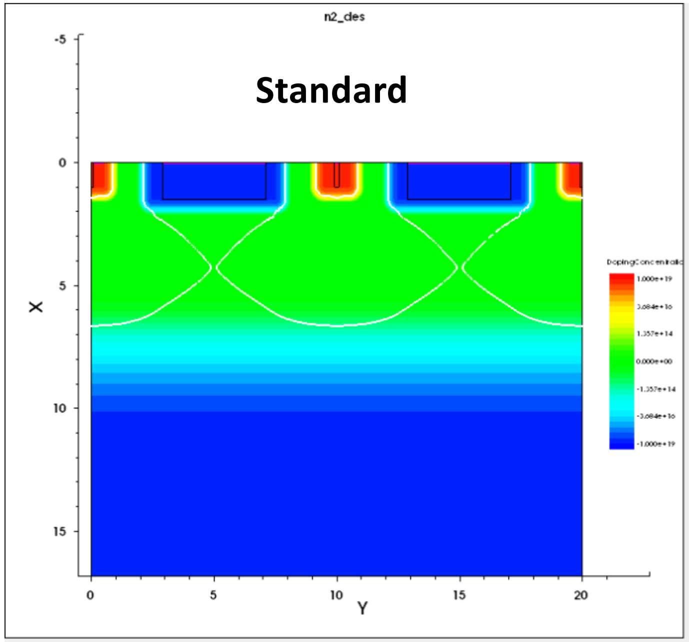


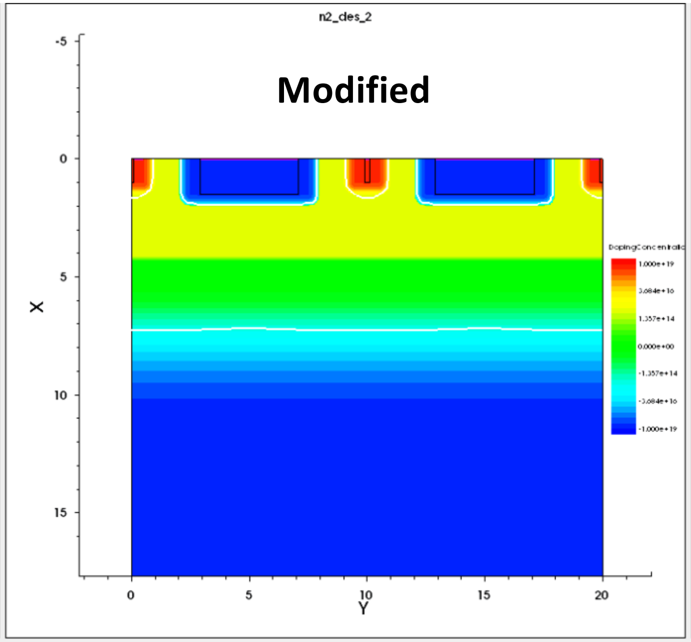
https://doi.org/10.1016/j.nima.2017.07.046

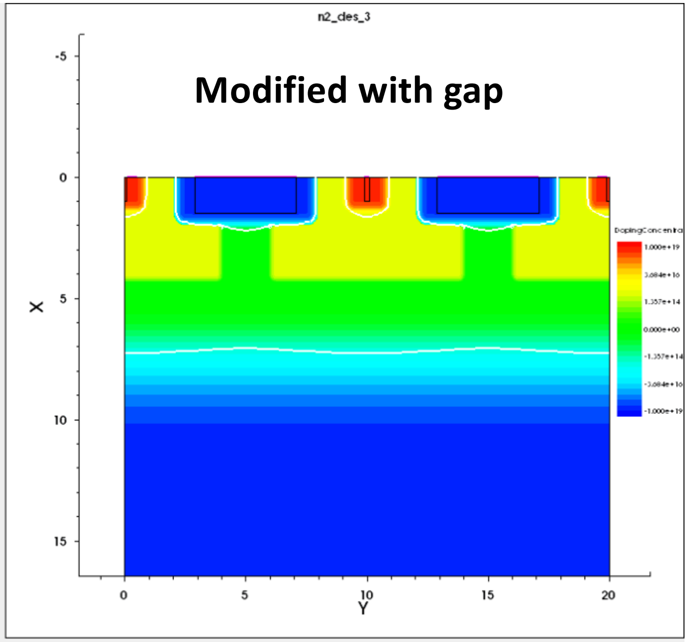


https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

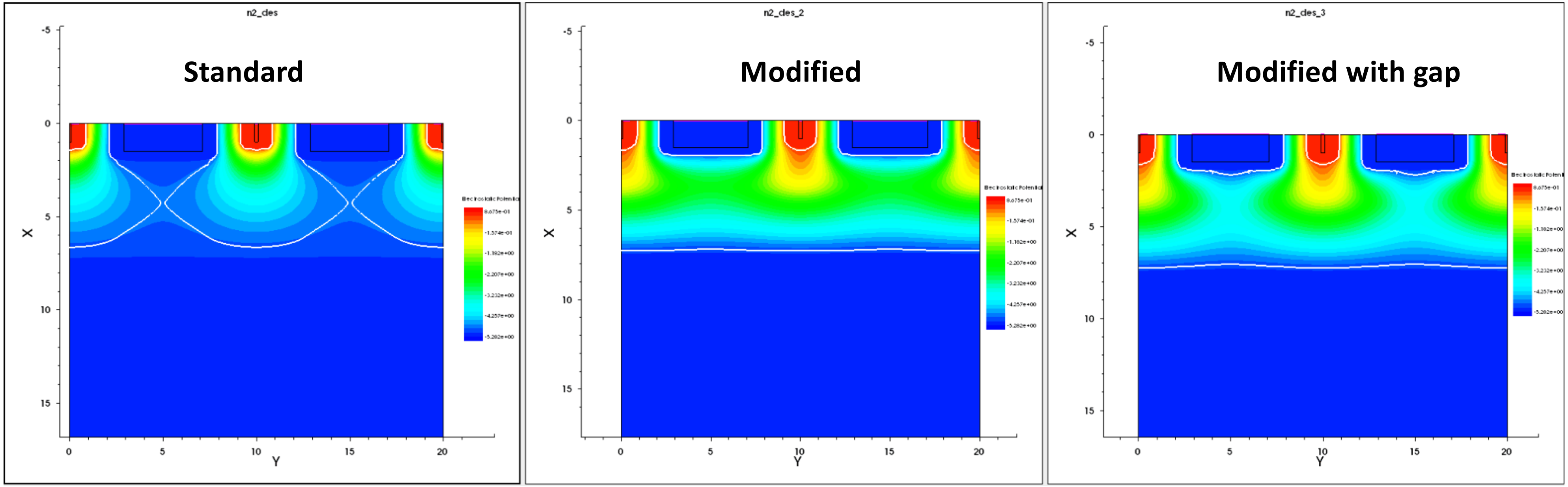
Doping profiles


Standard


Modified


Modified with gap

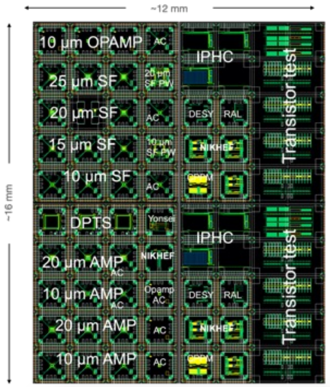
Electrostatic Potential

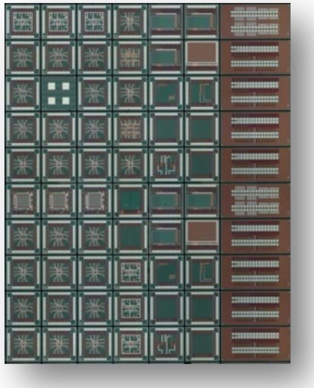


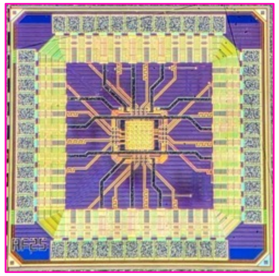
Completed R&D: 65nm technology validation

- ALICE ITS3 together with CERN EP R&D
  - leverages on experience with 180 nm (ALPIDE)
  - excellent links to foundry
- **Main goals:**
  - Learn technology features
  - Characterize charge collection
  - Validate radiation tolerance
- **Pixel prototype chips: APTS, CE65, DPTS**

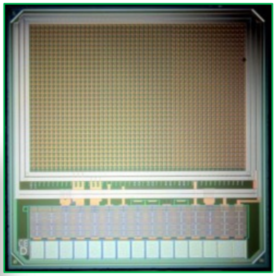
- Testing since September 2021:
  - **huge effort shared among many institutes**
  - laboratory tests with ^{55}Fe source
  - beam tests @ PS, SPS, Desy, MAMI



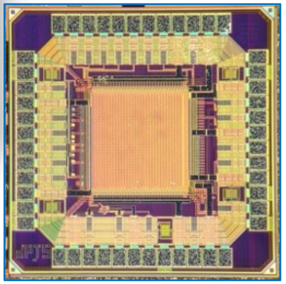




APTS:
- 6×6 pixel matrix
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
  1. Traditional source follower (APTS-SF)
  2. Very fast OpAmp (APTS-OA)
- 4 pitches: 10, 15, 20, 25 µm



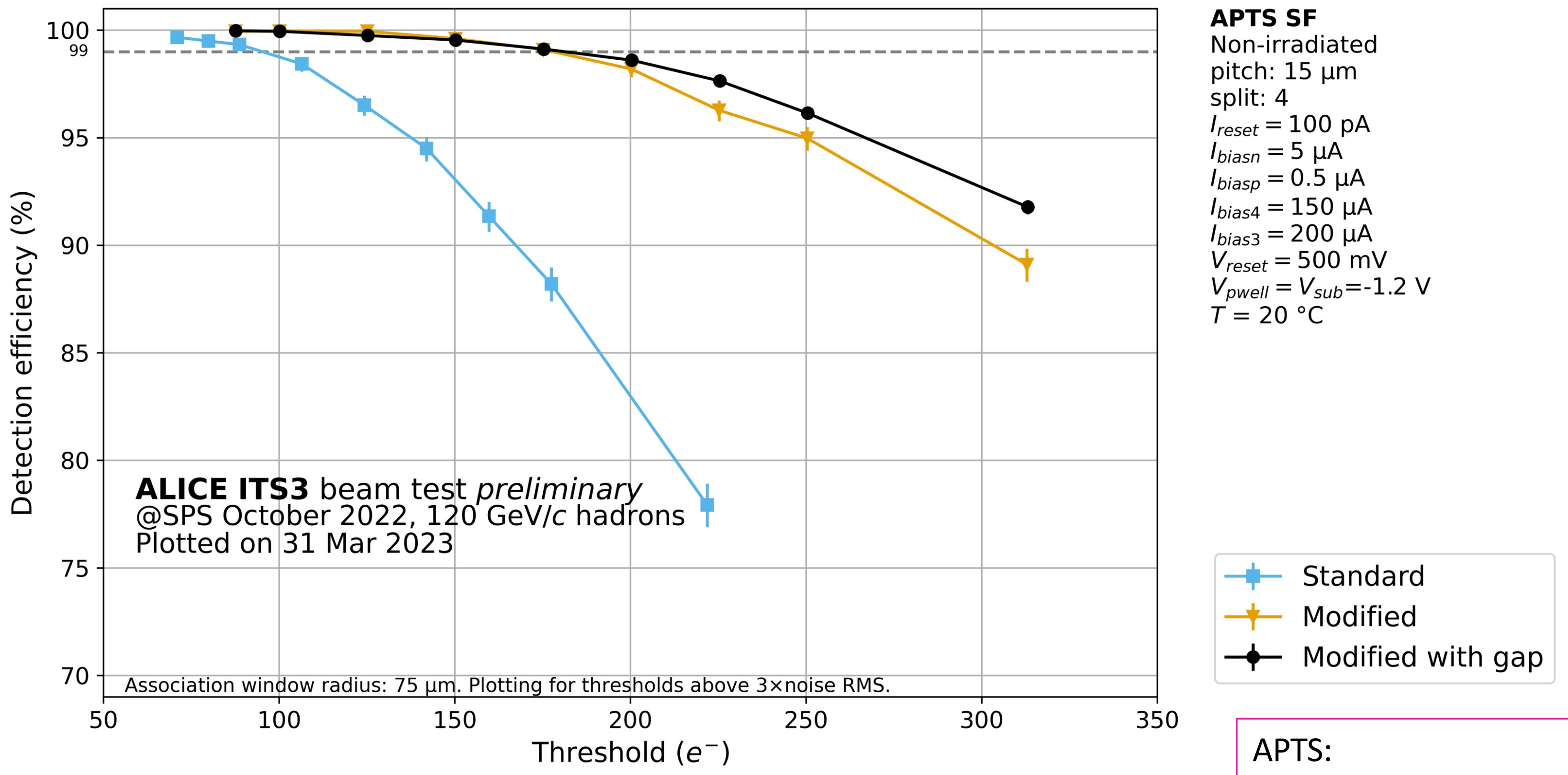
CE65:
- 2 matrix sizes, 15 or 25 µm pitch
- Rolling shutter readout (50 µs integration time)
- 3 in-pixel architectures:
  1. AC-coupled amplifier
  2. DC-coupled amplifier
  3. Source follower



DPTS:
- 32×32 pixel matrix
- Asynchronous digital readout
- Time-over-Threshold information
- Pitch: 15×15 µm^2

AREA: 1.5×1.5 mm^2

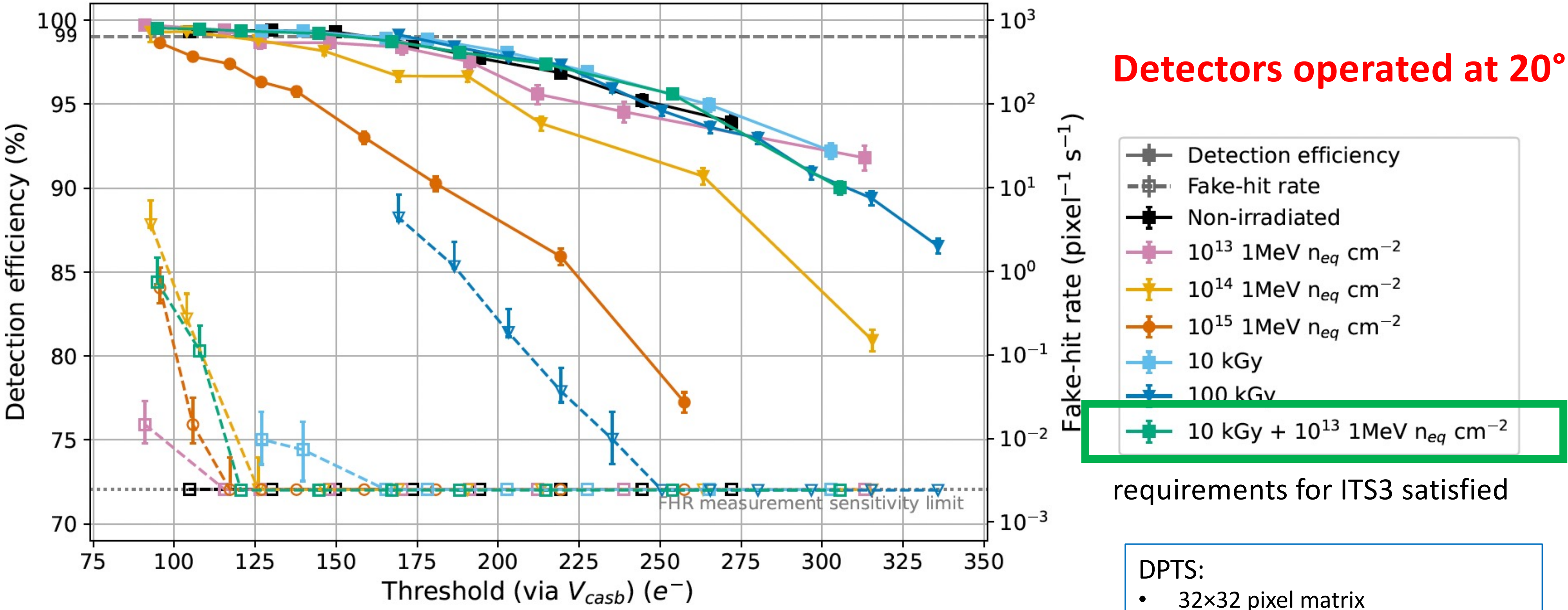
Results for APTS: detection efficiency



APTS SF
Non-irradiated
pitch: 15 µm
split: 4
I_{reset} = 100 pA
I_{biasn} = 5 µA
I_{biasp} = 0.5 µA
I_{bias4} = 150 µA
I_{bias3} = 200 µA
V_{reset} = 500 mV
V_{pwell} = V_{sub}=-1.2 V
T = 20 °C

APTS:
- 6×6 pixel matrix
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
  1. Traditional source follower (APTS-SF)

DPTS: radiation hardness



Detectors operated at 20°C

requirements for ITS3 satisfied

>99% detection efficiency even after 10^{15} NIEL for 15 µm pixels at room temperature

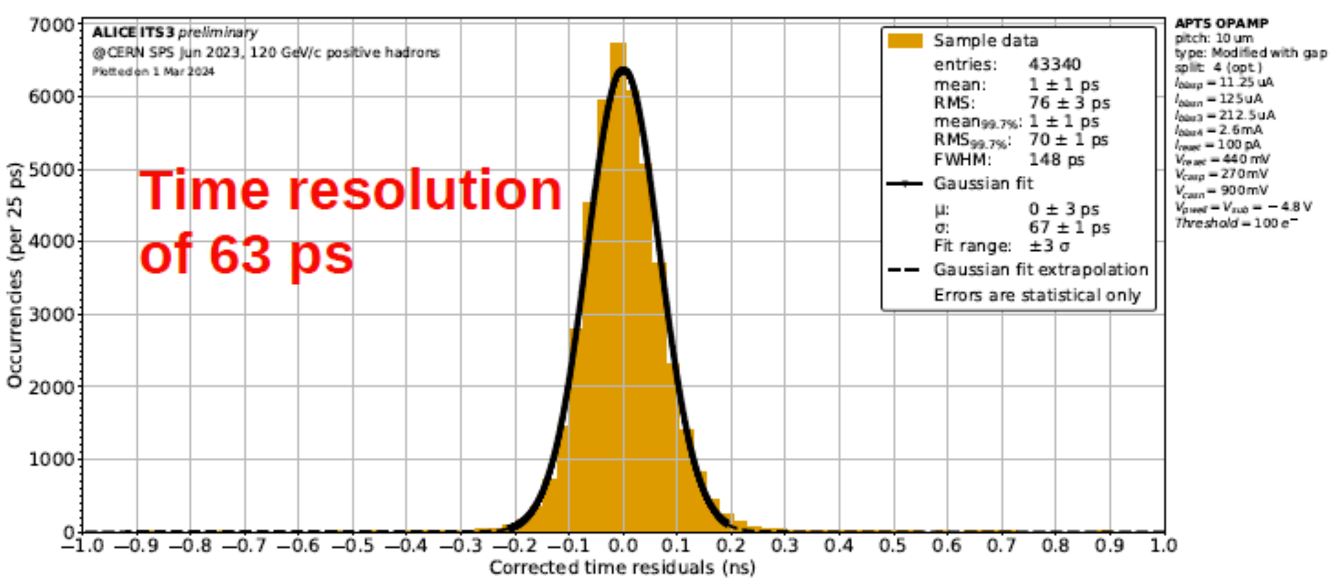
DPTS:
- 32×32 pixel matrix
- Asynchronous digital readout
- Time-over-Threshold information
- Pitch: 15×15 µm^2

https://doi.org/10.1016/j.nima.2023.168589

Results for APTS OpAmp: timing resolution

- Analog output test structure to test the timing performance of the technology

- First results from June 2022 beam test available:
  - timing performance
  - efficiency



Time resolution of 63 ps

Results for APTS OpAmp: timing resolution

- Analog output test structure to test the timing performance of the technology
- First results from June 2022 beam test available:
    - timing performance
    - efficiency

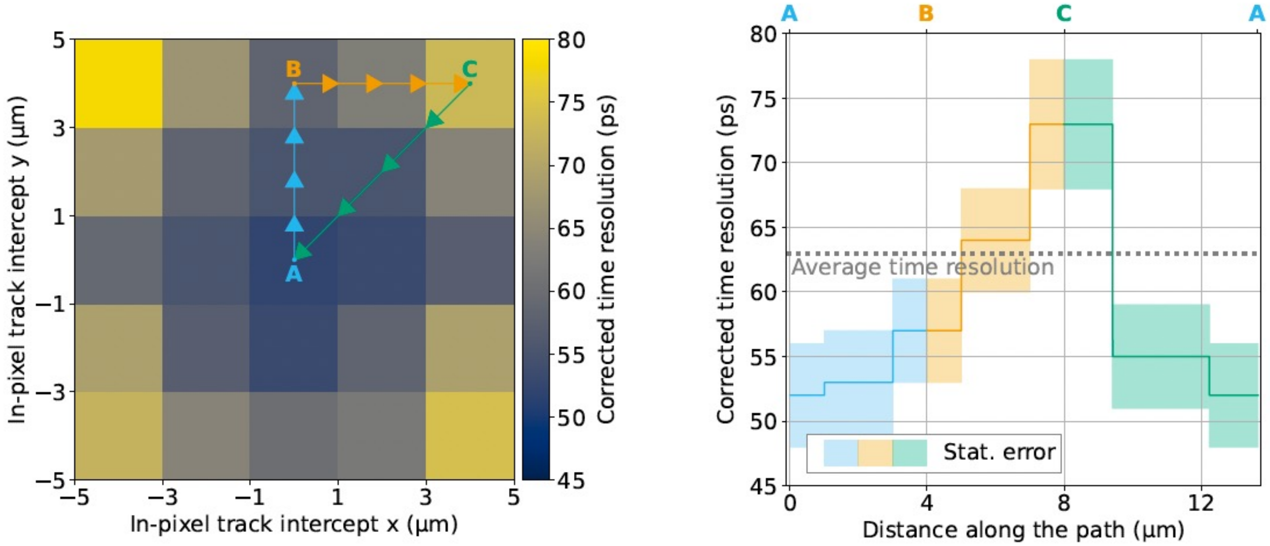


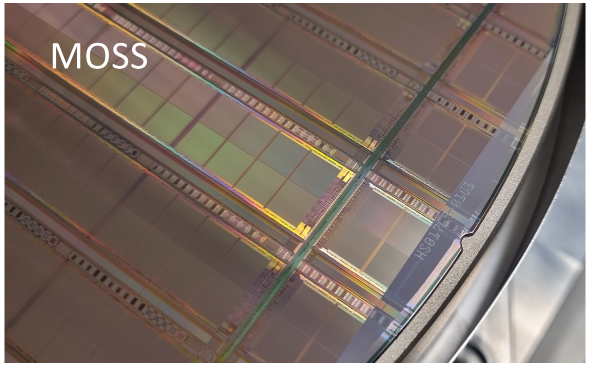
Figure 14: Left: corrected in-pixel time resolution of the modified with gap structure operated at $V_{sub}=-4.8\,V$. Right: time resolution variation along the path from the pixel center to the edge, and to the corner.

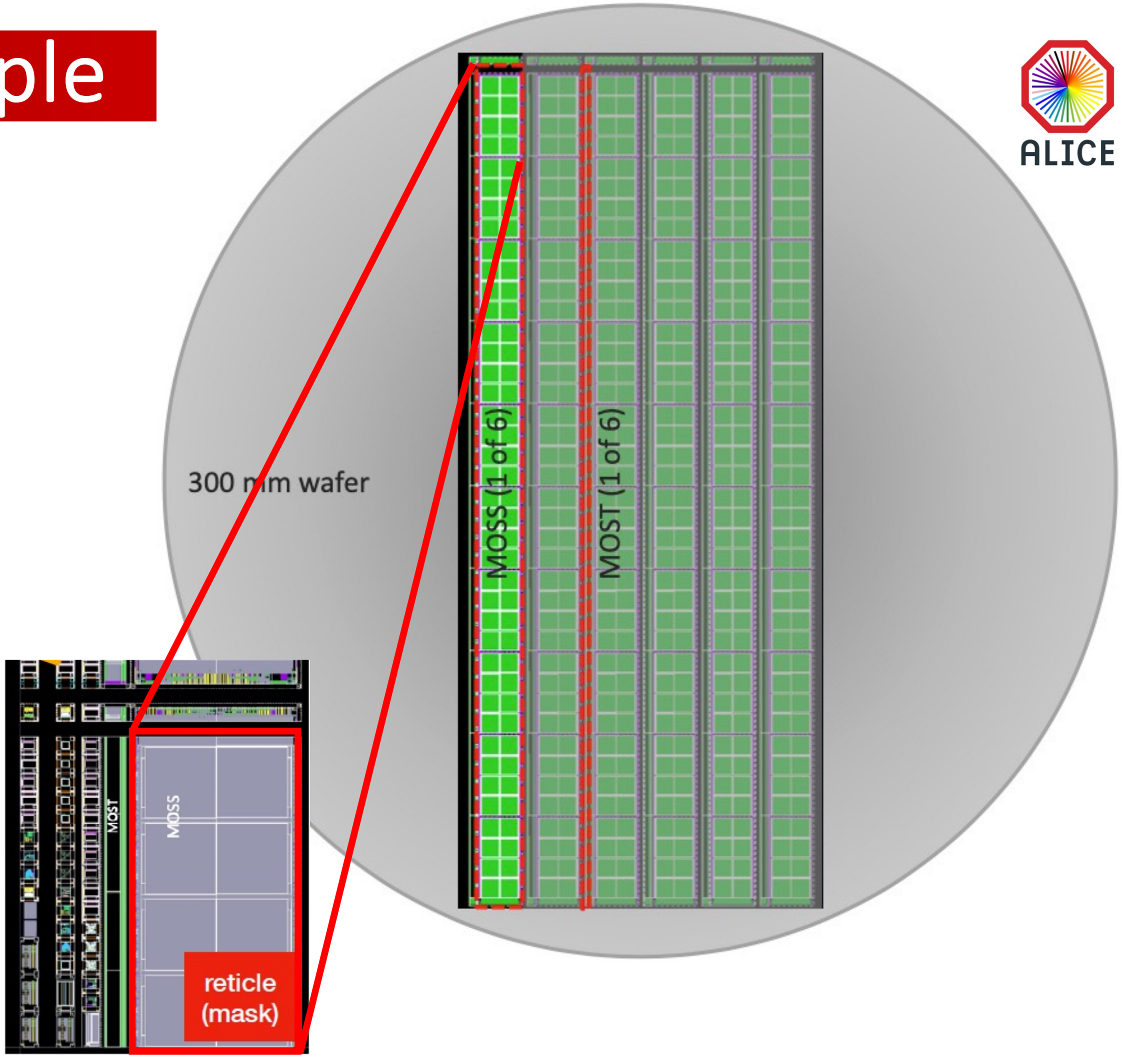
Large area sensors: exploiting stitching

Stitching simplified principle

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - typical sizes of few cm^2
  - modules are tiled with chips connected to a flexible printed circuit board
- New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - actively used in industry
  - a 300 mm wafer can house a chip to equip a full half-layer
  - *requires dedicated chip design*

ER1 wafer





MOSS carrier card, bonding tests

Chip development roadmap

PAST

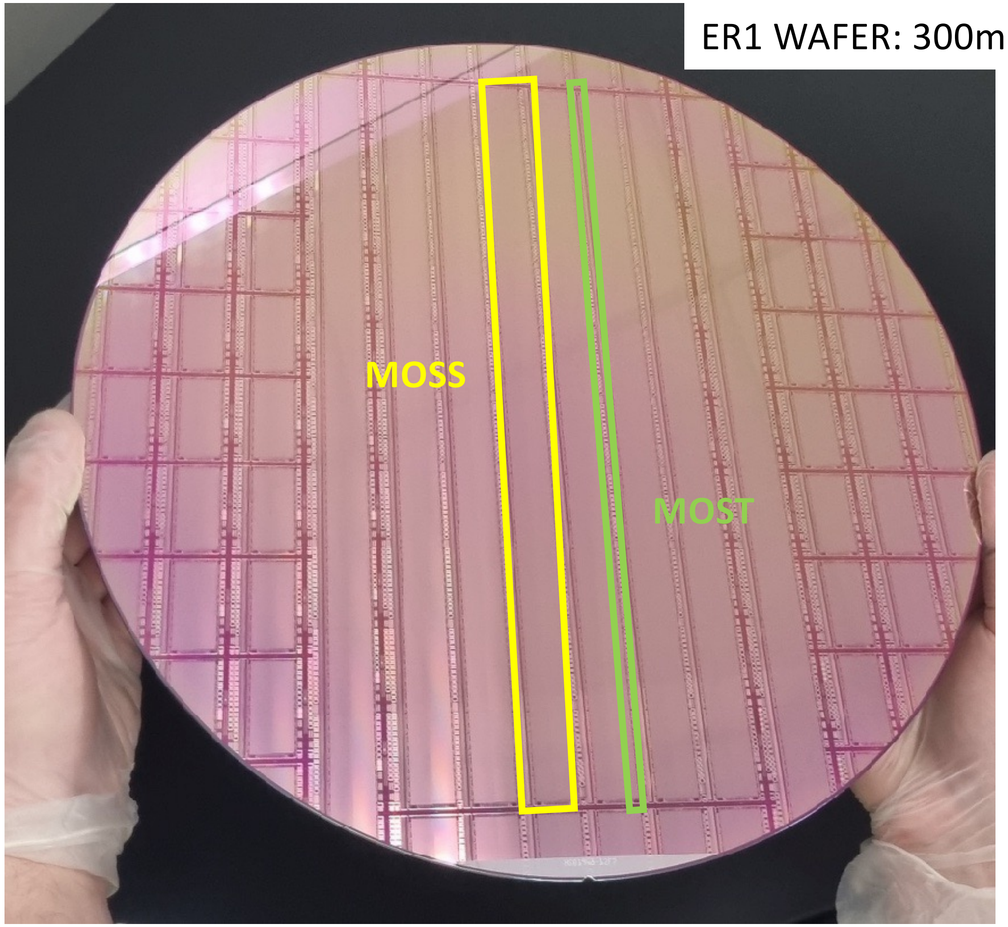
- **MLR1: first MAPS in TPSCo 65nm** (2021) - successfully qualified the 65nm process for particle detectors

PRESENT

- **ER1: first stitched MAPS** (2023)
  - large design "exercise"
  - "**MOSS**": 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 µm2): conservative design, different pitches
  - "**MOST**": 2.5 x 259 mm, 0.9 MPixel (18 x 18 µm2): more dense design

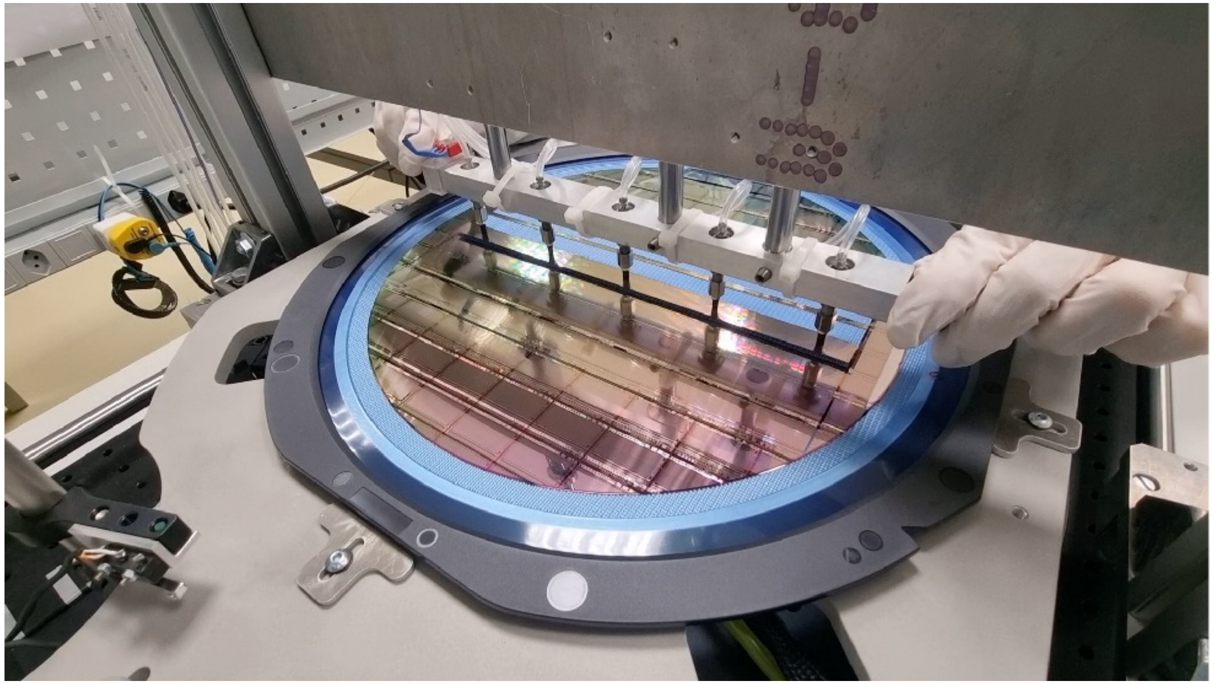
FUTURE

- **ER2: first ITS3 sensor prototype** (fall 2024)
- **ER3: ITS3 sensor production** (end of 2025)

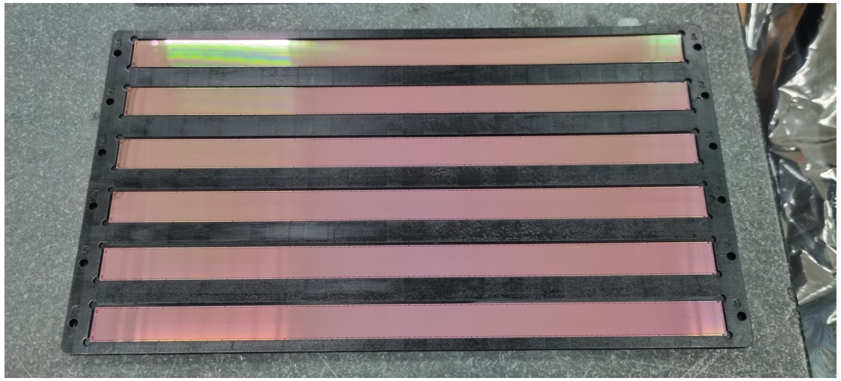

ER1 WAFER: 300mm

Prototypes: handling

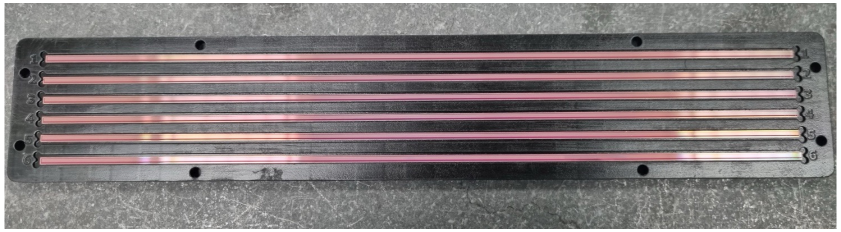
- ER1 wafers are thinned down to 50 µm
- Tools to pick, handle and ship chips have been developed



MOSS

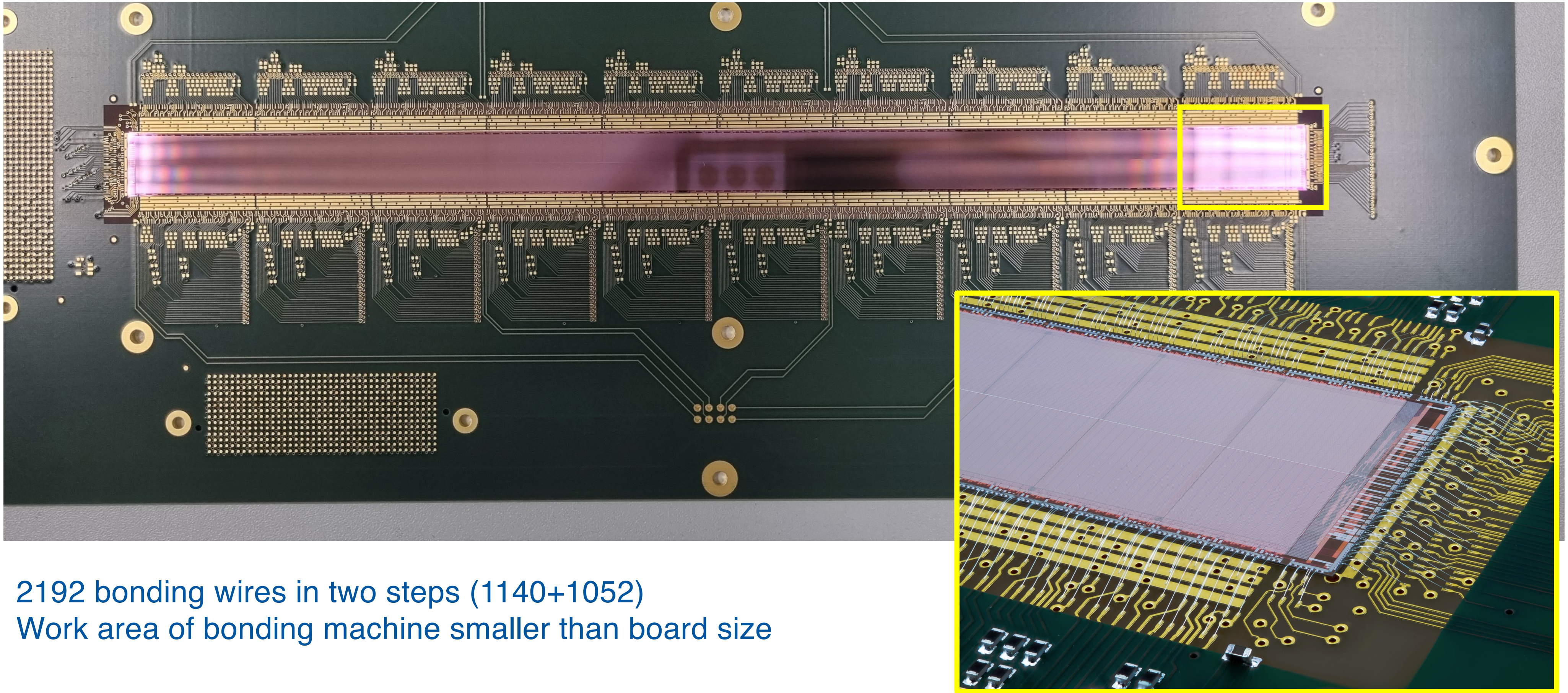


MOST



A set of dedicated tools have been developed — handling is under control

Assembly on carrier boards

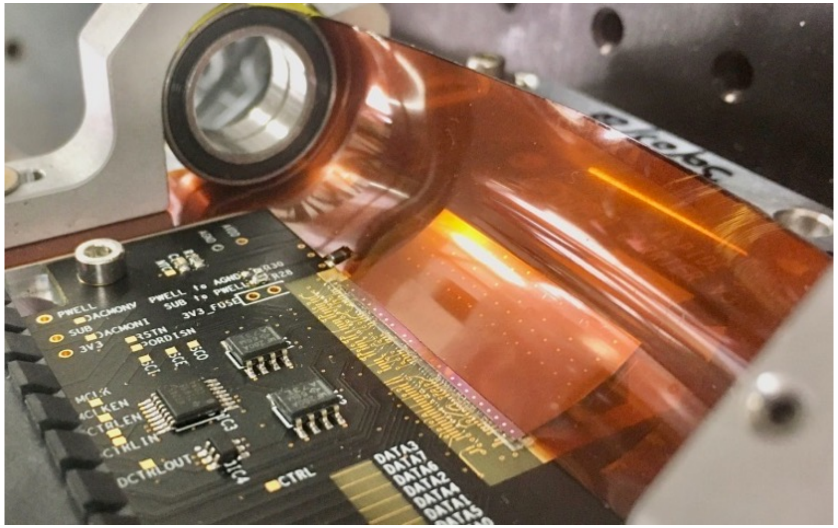


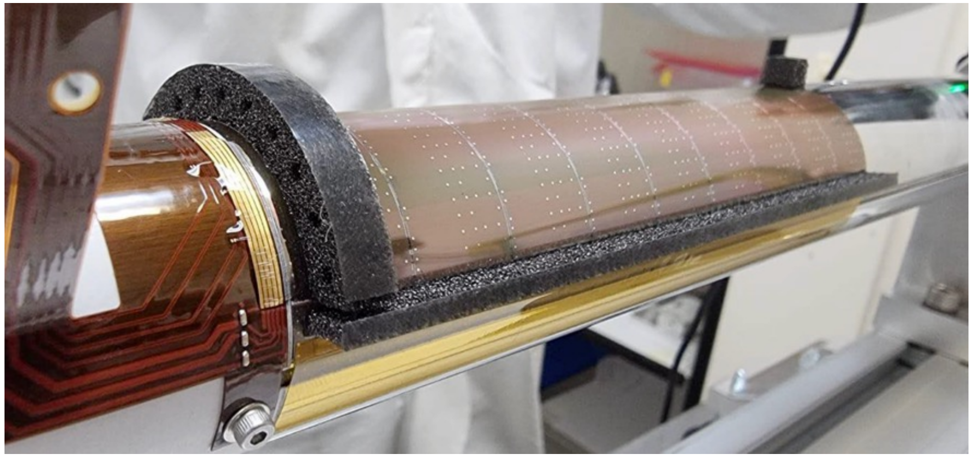
2192 bonding wires in two steps (1140+1052)
Work area of bonding machine smaller than board size

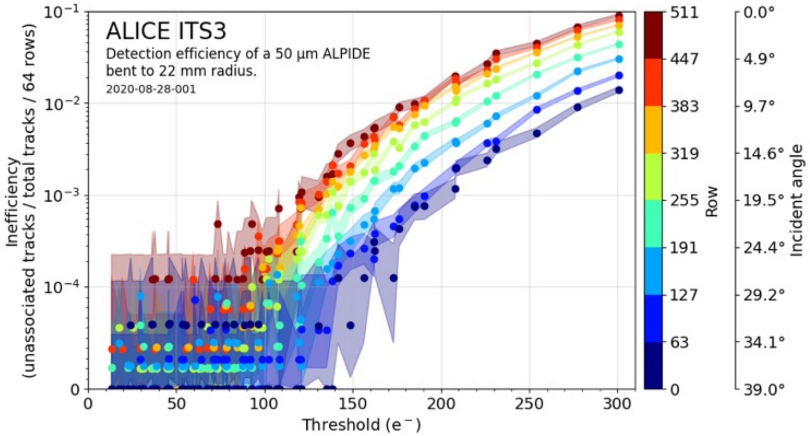
ONGOING R&D

Thinning and Bending of CMOS sensors: 180nm

- Bending of 180nm small size MAPS
  - 50 µm thick ITS2 chip (ALPIDE) bent to 22 mm showed excellent efficiency in the beam test in 2020
  - no significant variation in the performance
- Development of tools to bend large area silicon sensors: SuperALPIDE (9x2 ALPIDE die)

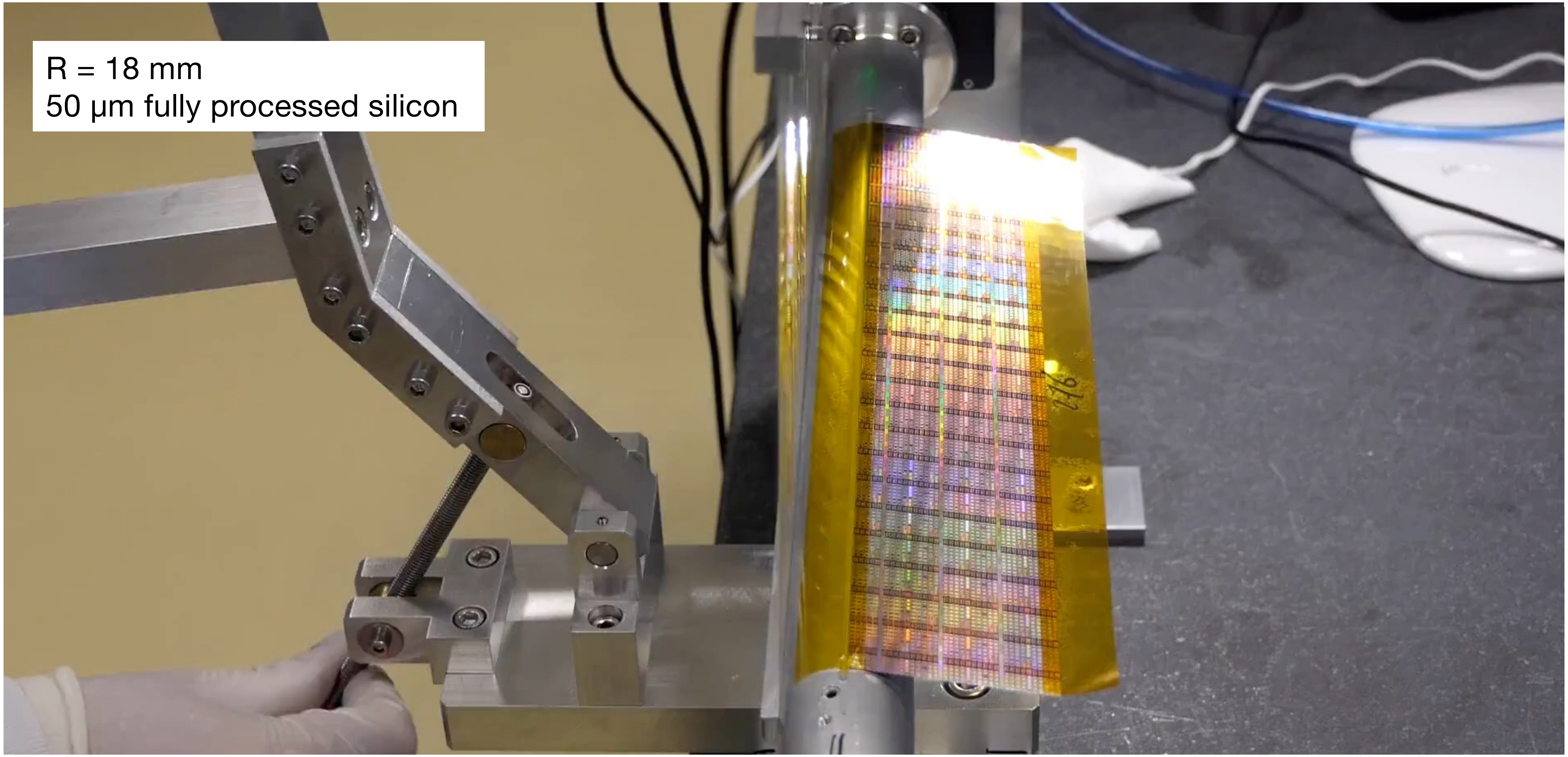




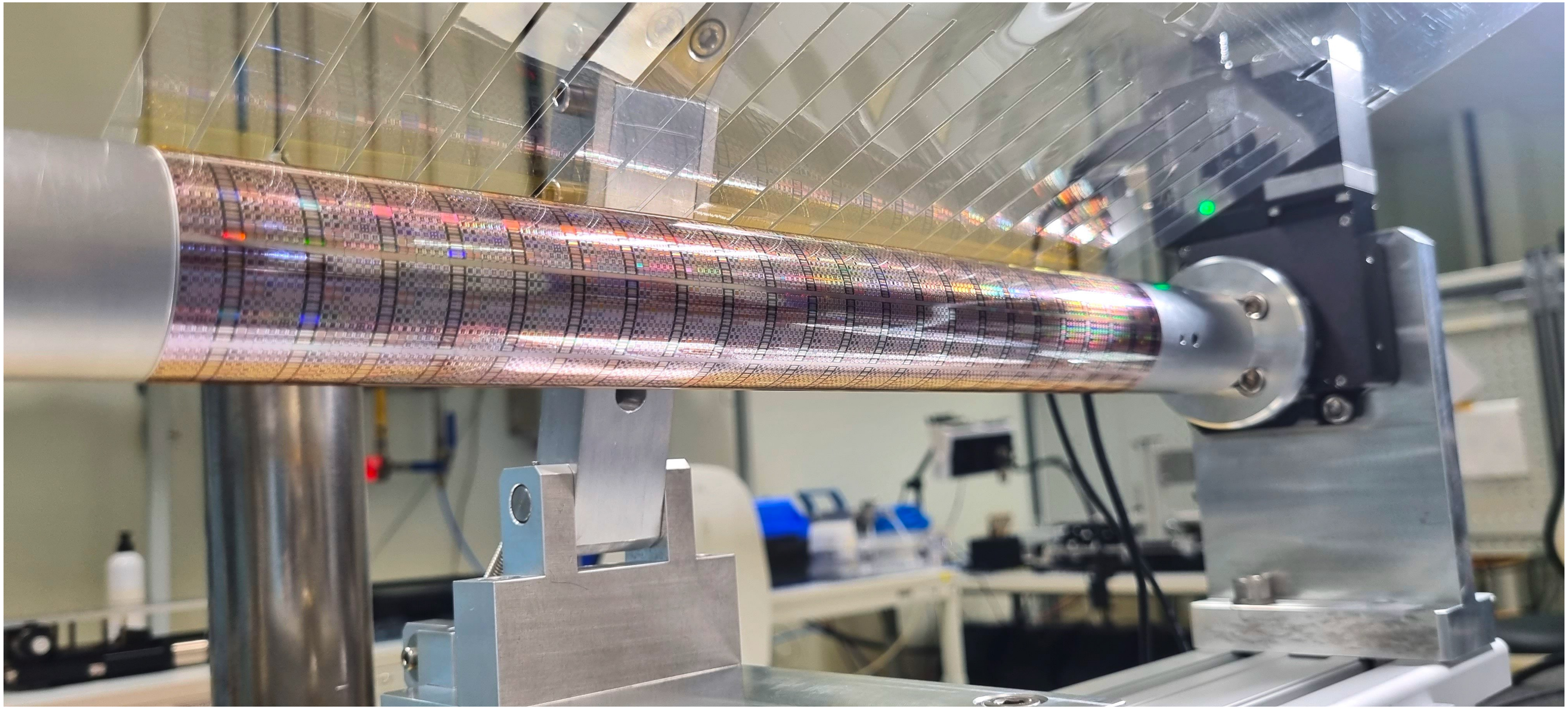


https://doi.org/10.1016/j.nima.2021.166280

Bending of fully processed wafers


R = 18 mm
50 µm fully processed silicon

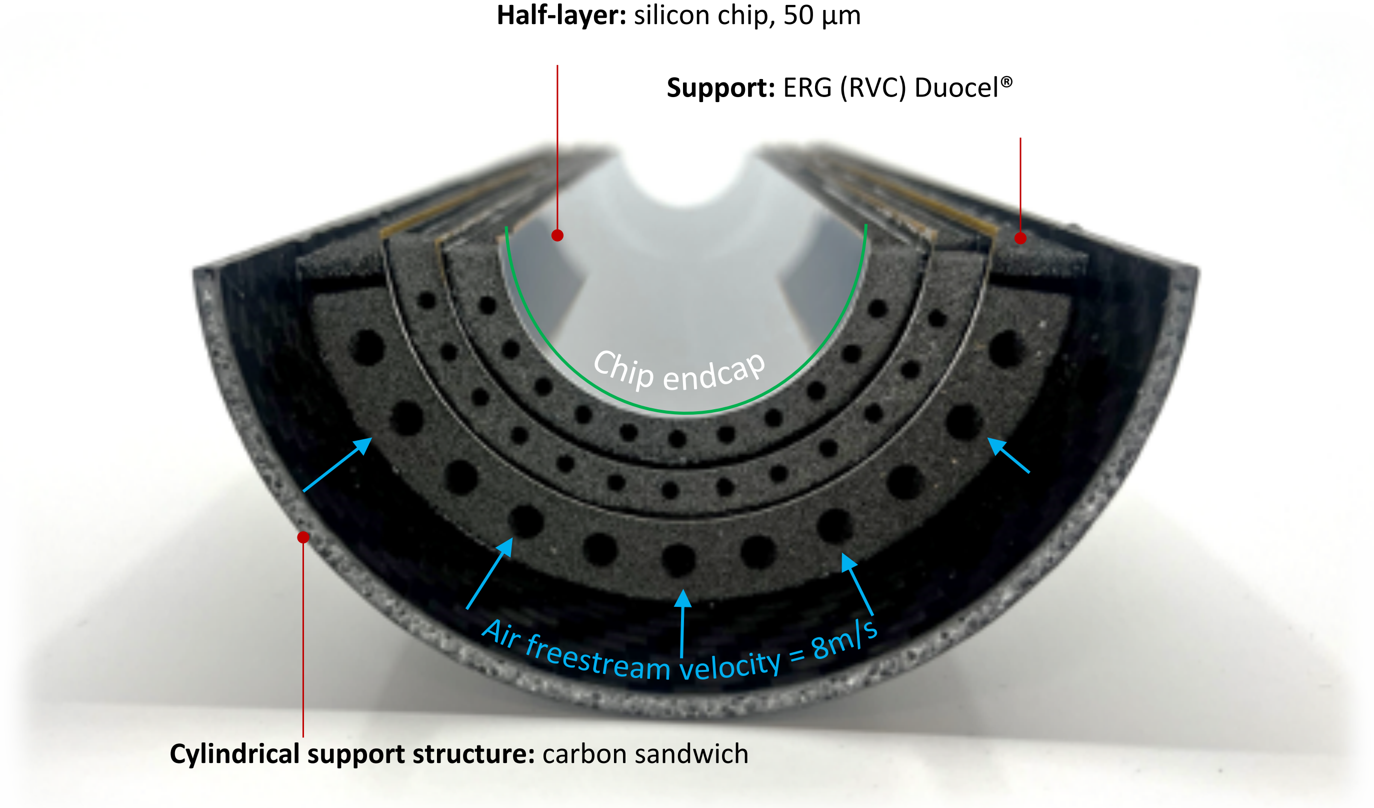
Bending of fully processed wafers

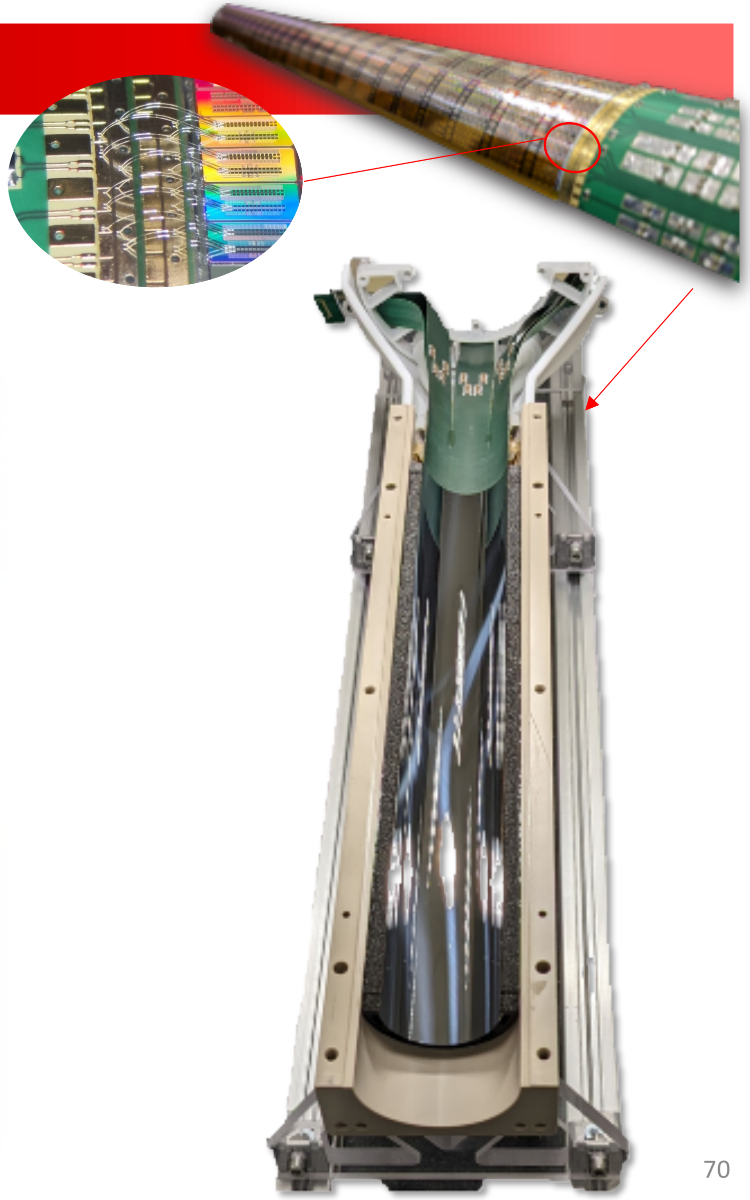


R = 18 mm
50 µm fully processed silicon

Mechanical highlights

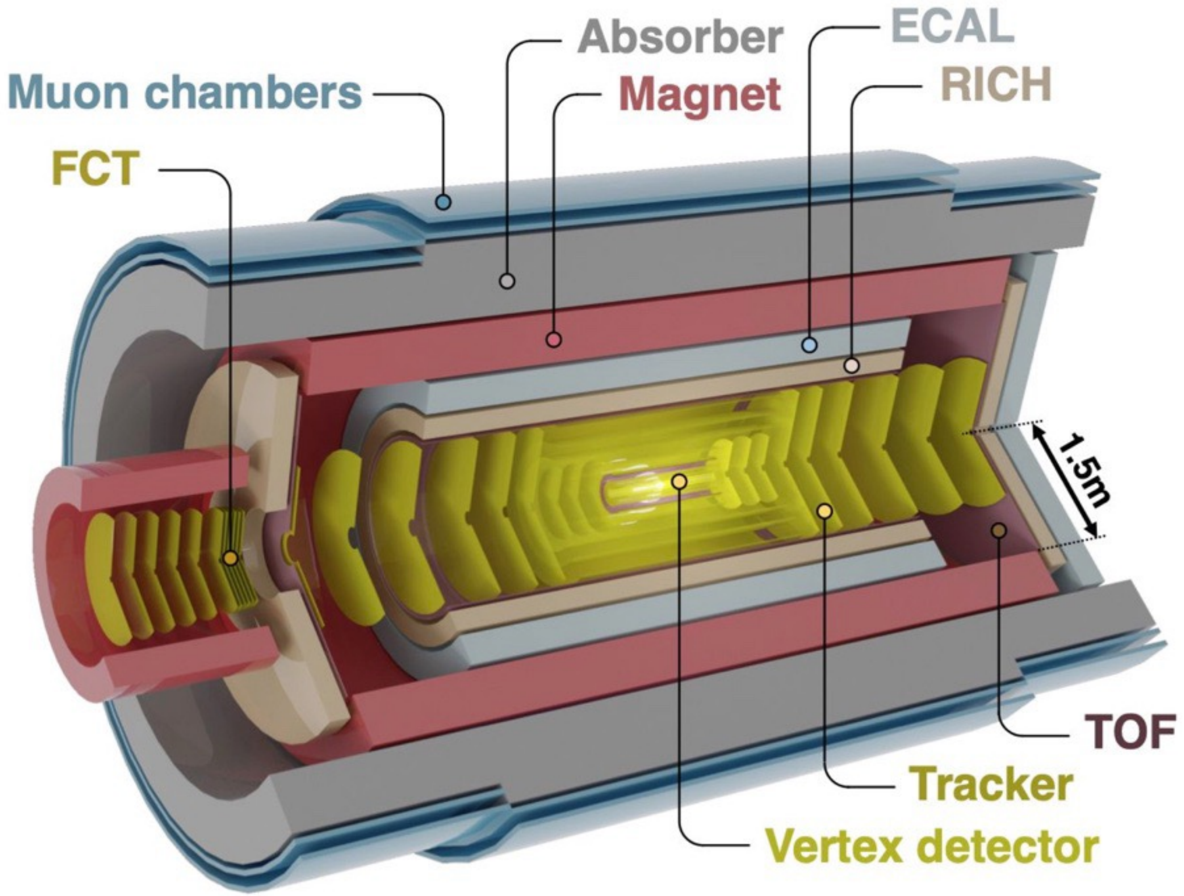
- Prototype with integrated wafer-size sensor (L0-like) wire bonded to a FPC
- Prototype with final-grade materials for thermo-elasticity tests





A silicon only experiment?

ALICE 3 (LHC LS4, 2033-34) the next concrete large-scale HEP application



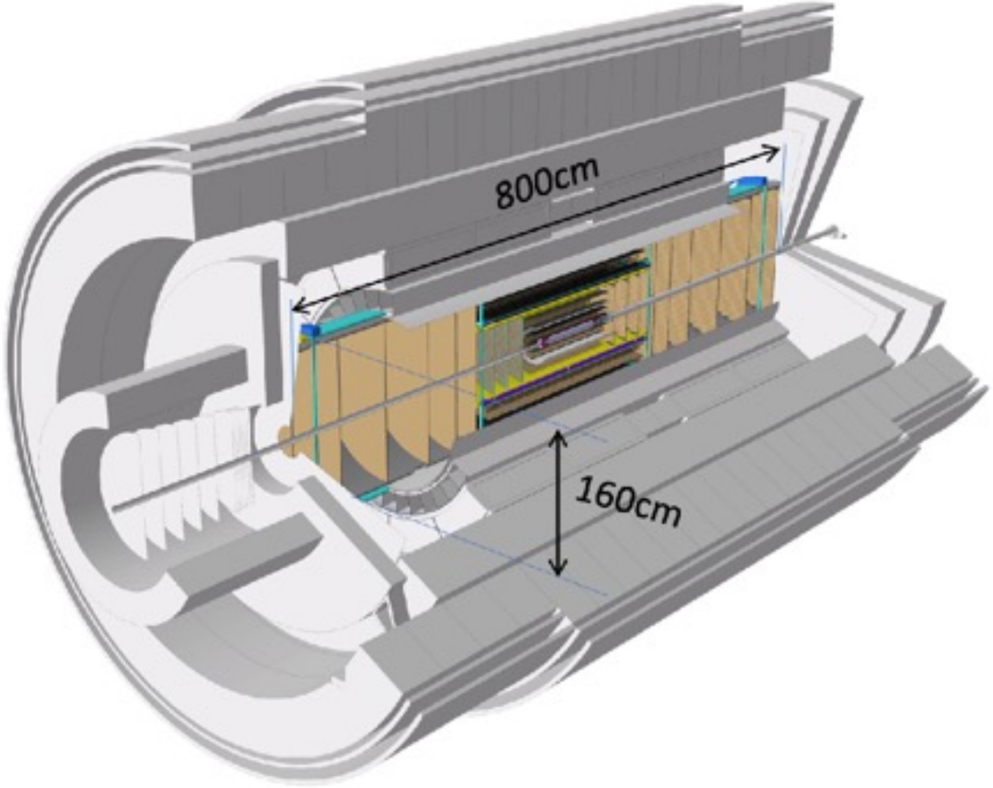
Largely based on CMOS technology

- ultra-precise (2.5 μm resolution) in-vacuum vertex detector
- large-area (O(60 m2)) vertex detector
- time of flight (20 ps)

- Will be a main driver for the technology development for the next decade

- De-facto prototype of an FCC-ee detector

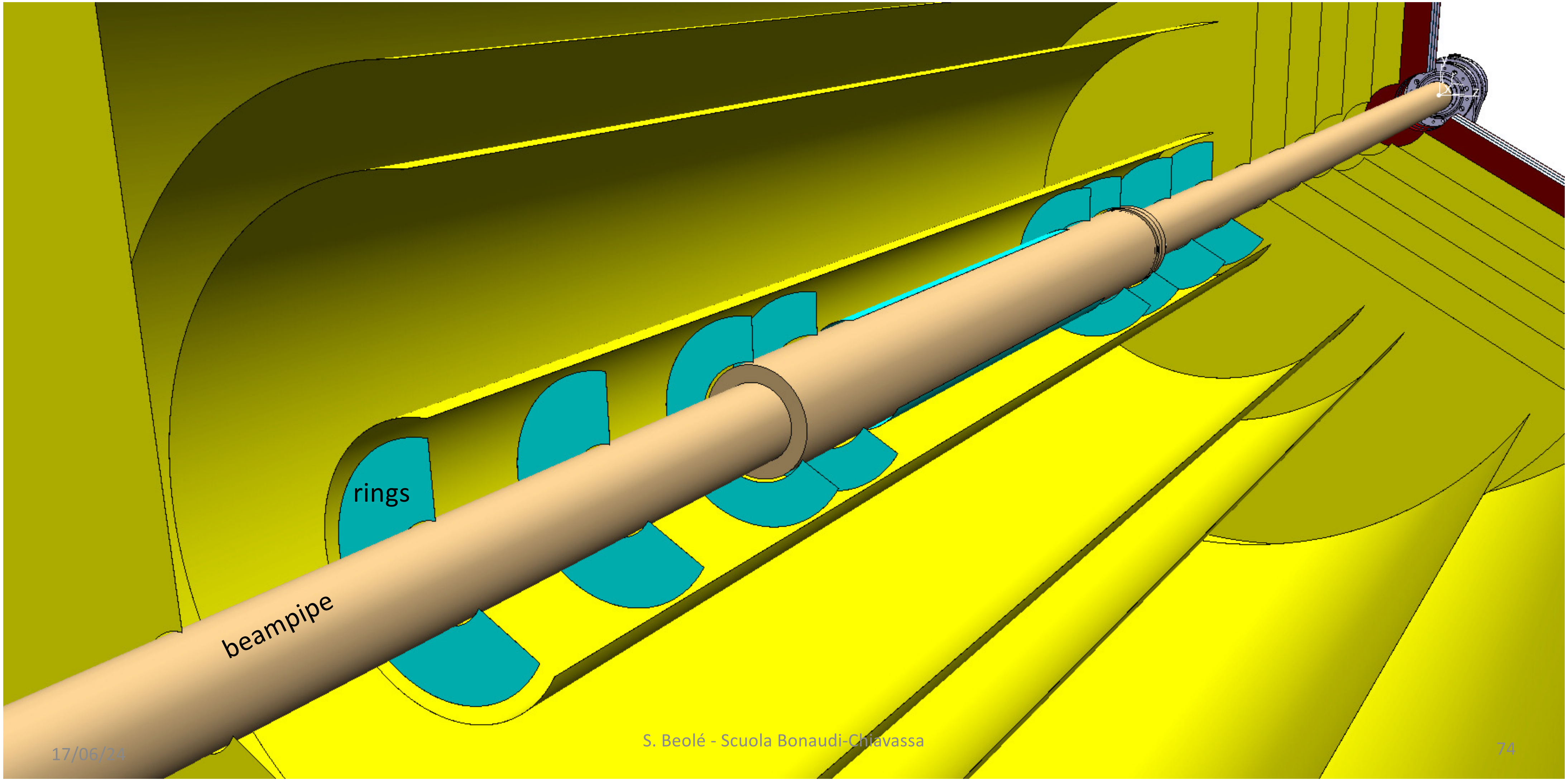
ALICE3 Outer Tracker



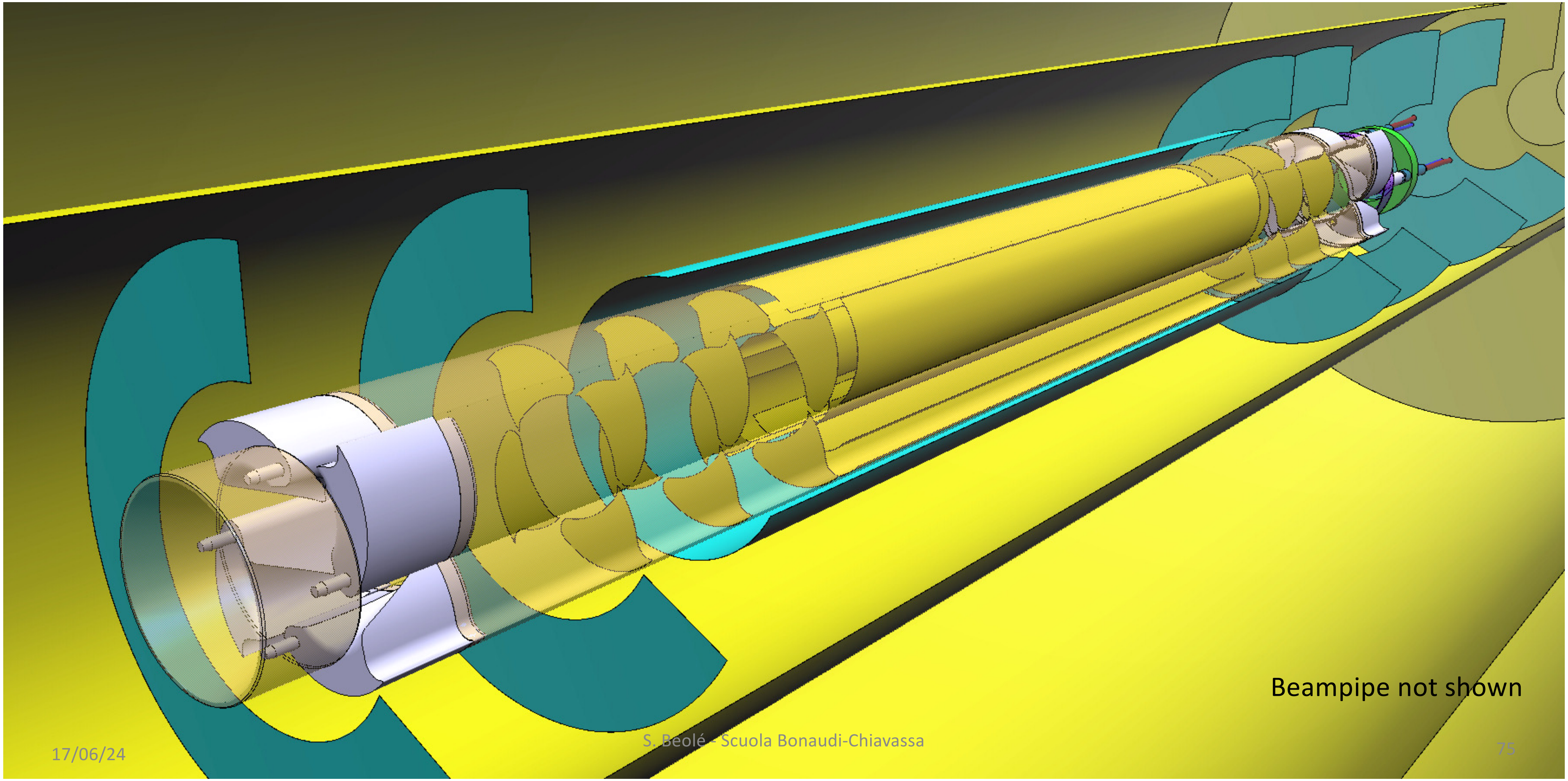
60 m² silicon pixel detector

- large coverage: ±4η
- high-spatial resolution: ≈ 10 µm
- very low material budget: X/X0 (total) ≲ 10%
- low power: ≈ 20 mW/cm²
- **module (O(10 x 10 cm²)) concept based on industry-standard processes** for assembly and testing

IRIS: inside the beampipe

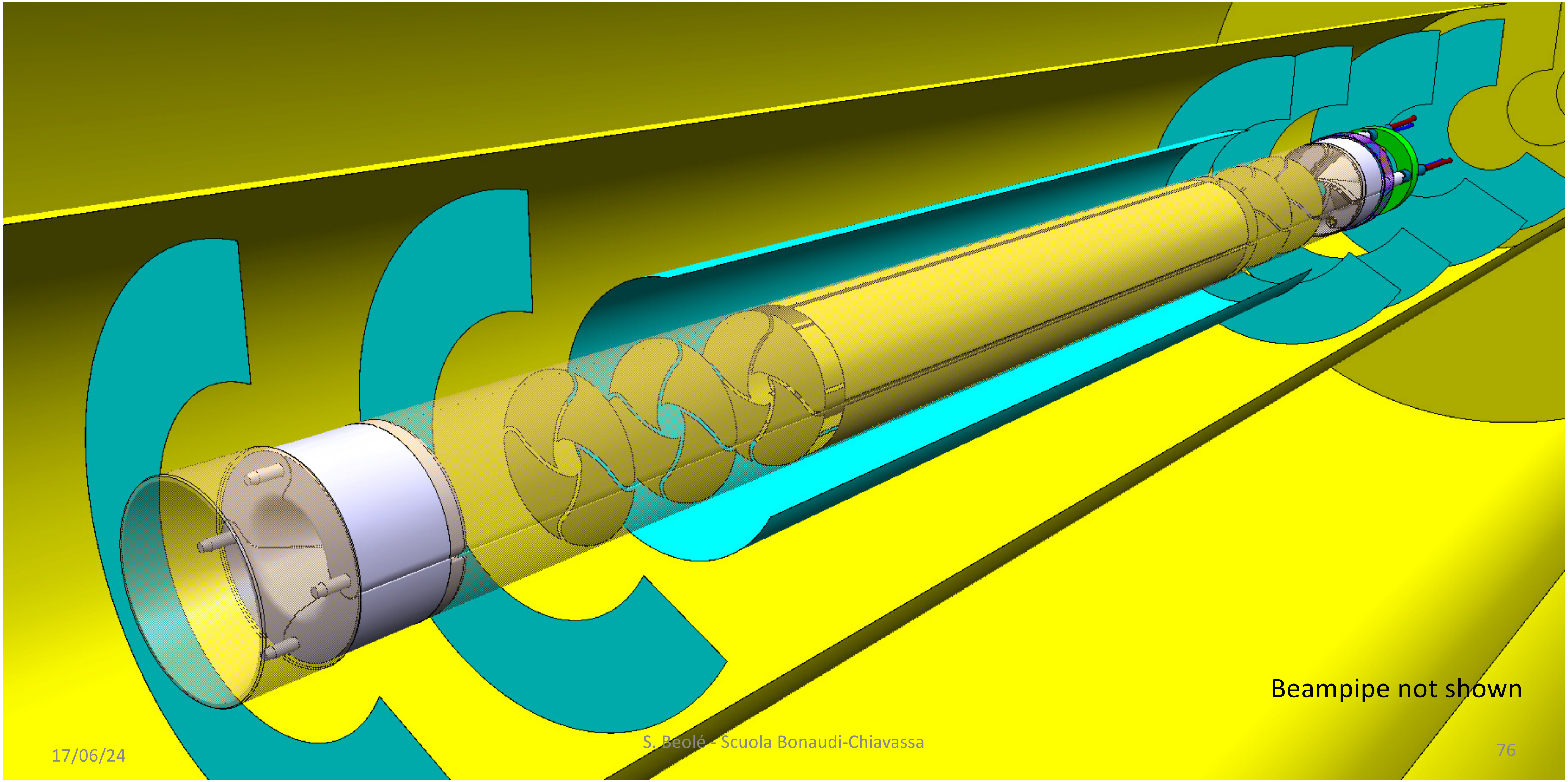


IRIS: inside the beampipe



Beampipe not shown

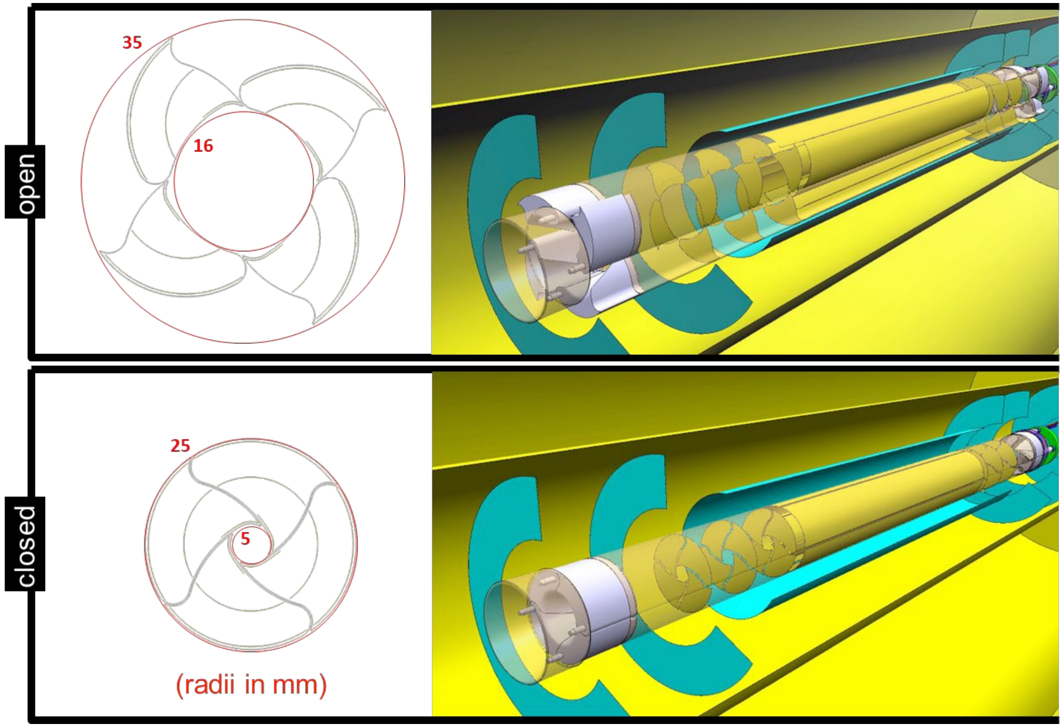
IRIS: inside the beampipe



Beampipe not shown

Vertex Detector: Iris inside the beam pipe

- Based on wafer-scale, ultra-thin, curved MAPS
  - radial distance from interaction point: **5 mm (inside beampipe, retractable configuration)**
  - unprecedented spatial resolution: ≈ 2.5 µm
  - … and material budget: ≈ 0.1% X0/layer
  - at radiation levels of: ≈ 10^{16} 1MeV n_{eq}/cm^2 + 300 Mrad
  - and hit rates up to: 94 MHz/cm^2

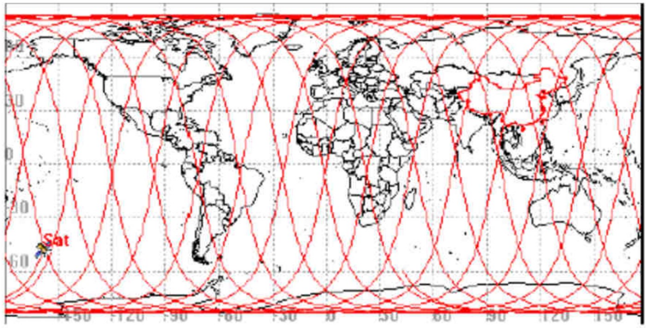


MAPS in SPACE

CSES-02 scientific mission objectives

- Monitoring of the electromagnetic near-Earth space environment
- Analysis of the ionospheric and plasmaspheric fluctuations
- Measurements of iono-magnetospheric perturbations possibly due to seismo-electromagnetic phenomena
- Study of fluxes of high & low energy charged particles precipitating from the Inner Van Allen radiation belt
- Measurements of magnetospheric and solar activity
- Monitoring of the e.m. anthropic effects at low Earth orbit altitude
- Observations of e.m. transient phenomena caused by tropospheric activity

CSES-02 planned orbit
-82.6° to +82.6° latitude
500 km altitude
Sun-synchronous
180° phase difference wrt CSES-01
Operating temperature: -30 to +50°C
Operating pressure:6.65·10-3 Pa



CSES-02 main characteristics
Orbit maneuver capability
Full-time operational
Mass: 900 kg
Power: 900 W
Storage: 512 Gbyte
Life cycle: > 6 years

CSES-02 payload

The High Energy Particle Detector on board of CSES-02

First detector hosting monolithic active pixel sensors (MAPS) for the tracking of charge particles in space

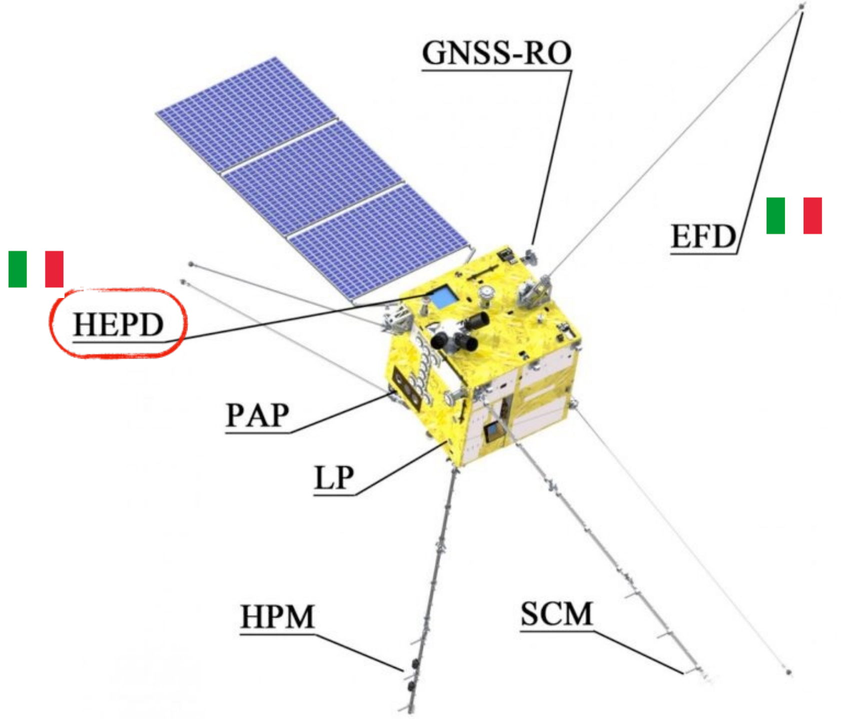
HEPD-02 main requirements	
Data budget	100 Gb/day
Mass budget	50 kg
Power budget	45 W
Electron kinetic energy range	3 MeV ÷ 100 MeV
Proton kinetic energy range	30 MeV ÷ 200 MeV
Angular resolution	≤10° for e^- with E > 3 MeV
Energy resolution	≤10% for e^- with E > 5 MeV
Pointing	Zenith

Scientific goals and main features

> measure the increase of the electron and proton fluxed due to short-time perturbations of the radiation belts

> detect different particle populations (solar, trapped, galactic, etc.) according to the satellite position and energy

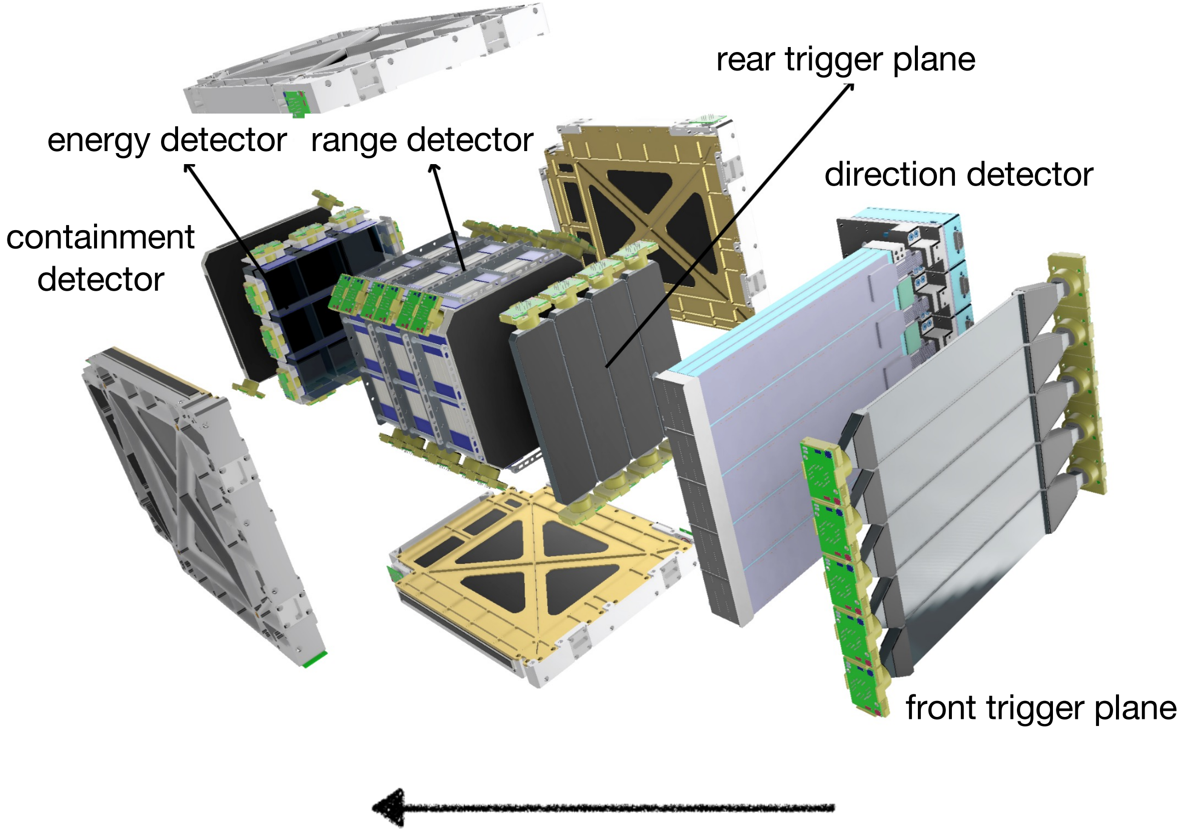
> implements trigger configuration dedicated to gamma rays on a time basis of 5 milliseconds



https://cses.web.roma2.infn.it/?page_id=198

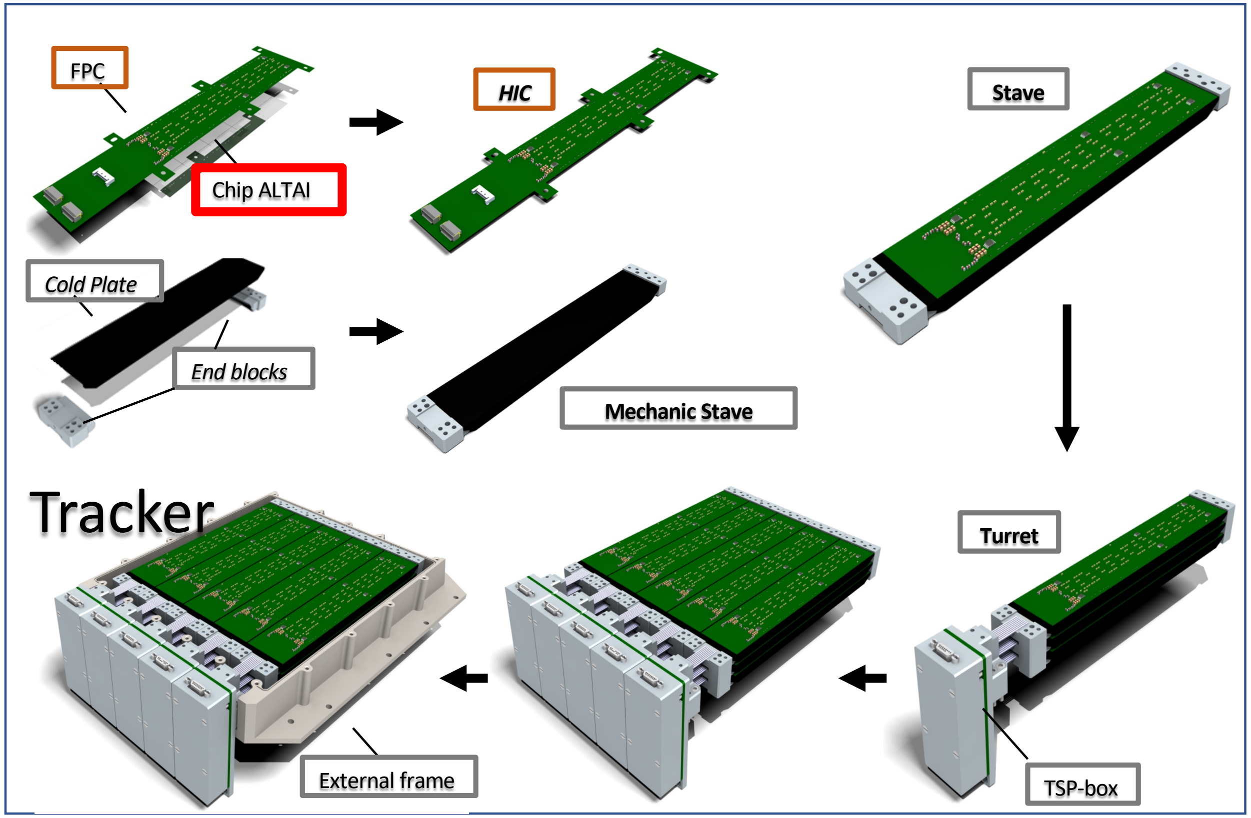
High Energy Particle Detector (HEPD-02)

- front trigger plane (200×180 mm$_2$)
  5 plastic scintillator bars (2 mm thick)
- direction detector (tracker)
  five standalone tracking modules
- rear trigger plane (150 x 150 mm$_2$)
  4 plastic scintillator bars (8 mm thick)
- range detector (150 x 150 x 10 mm$_3$)
  12 plastic scintillator planes
- energy detector (150 x 150 mm$_2$)
  2 crystal (LYSO) scintillator planes
  3 x 2 bars (25 mm thick each)
- containment detector
  plastic scintillator planes (8 mm thick)
  4 lateral and 1 bottom plane



Monolithic Active Pixel Sensors: first use in space

Limadou HEPD02 on the CSES2 mission



An 80 megapixel CMOS camera for charged radiation

Advantages:

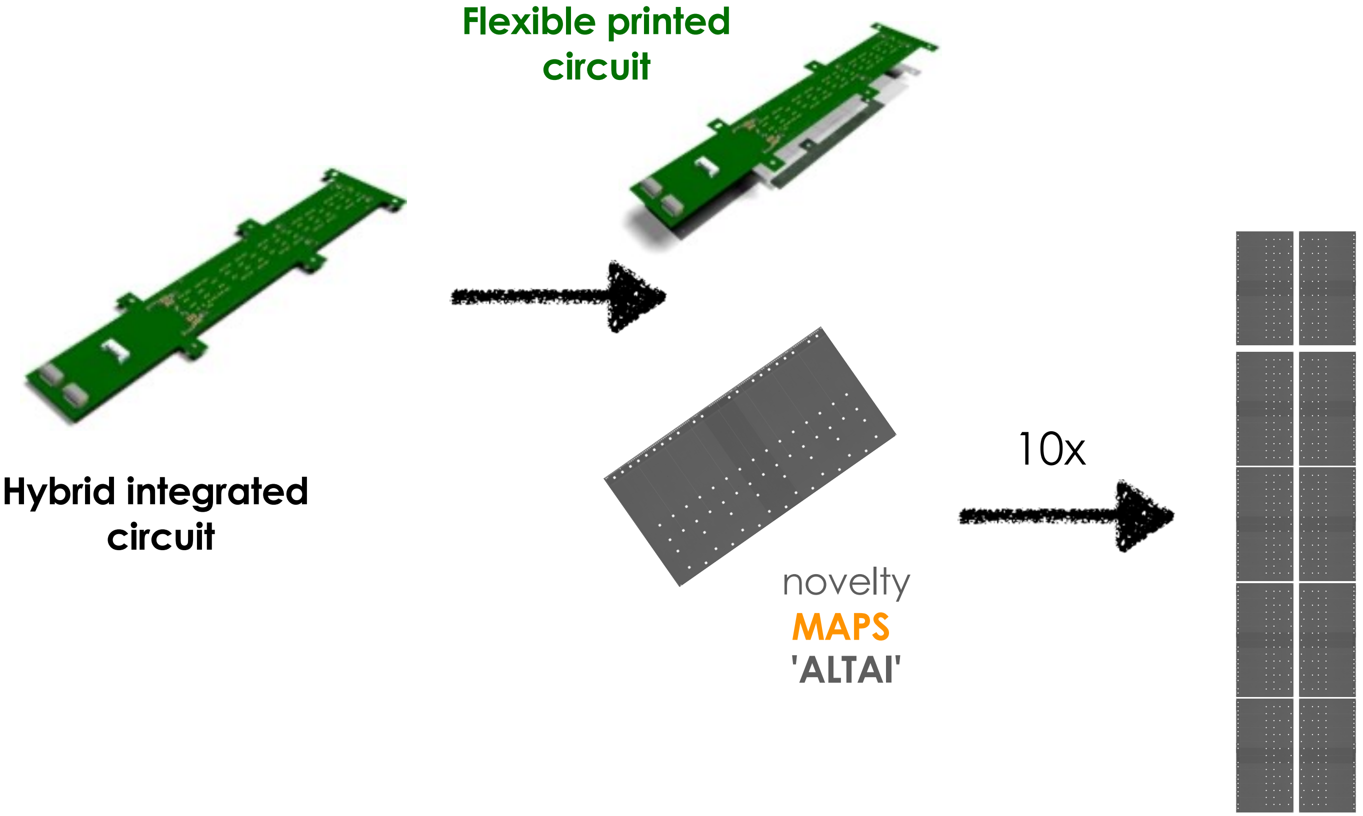
- reduces systematic uncertainties on tracking: down to 4um single-hit resolution
- no multi-hit degeneracy
- Extremely low material budget: 50um thin, control and read-out based on ultra-thin (180 um) flexible printed circuits
- Cheaper than standard microstrips
- Monolithic: in-pixel FE electronics: unmatchable S/N ratio (10^{-8} fake hits per trigger)

Challenges for use in space

- Tradeoff for mechanical supports: avoid multiple scattering but withstand launch acceleration and vibrations
- Limited power budget
- Heat dissipation
- Digital readout: limited information about charge

DD construction

Modules composing the tracker



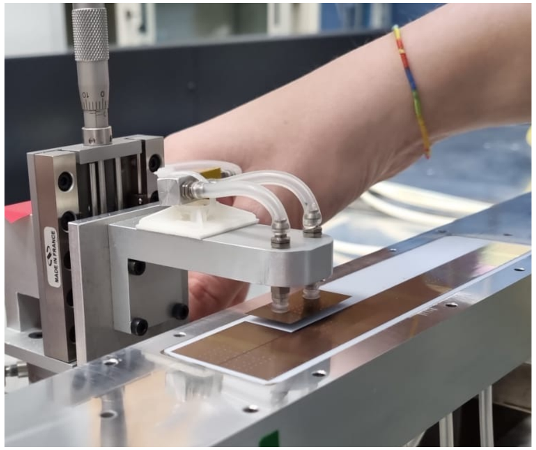
Flexible printed circuit

Hybrid integrated circuit

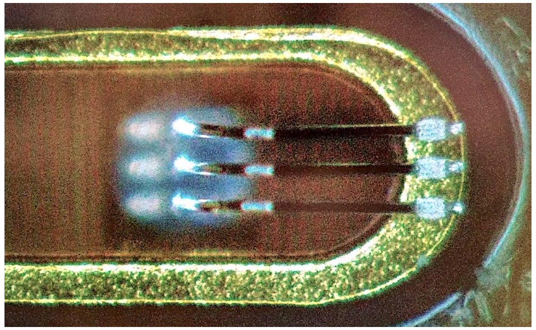
novelty **MAPS** **'ALTAI'**

10x

ALTAI alignment with CMM

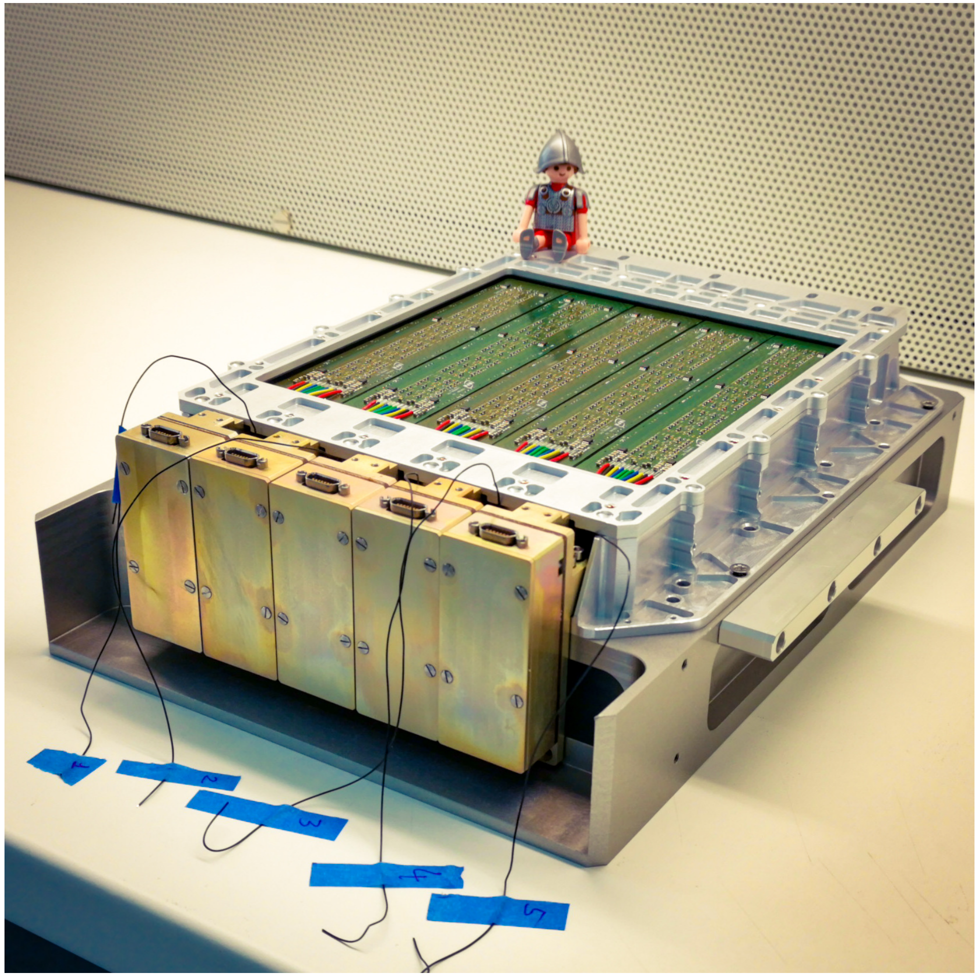


wire bond through the FPC



Monolithic Active Pixel Sensors: first use in space

LIMADOU 利瑪竇



Summary

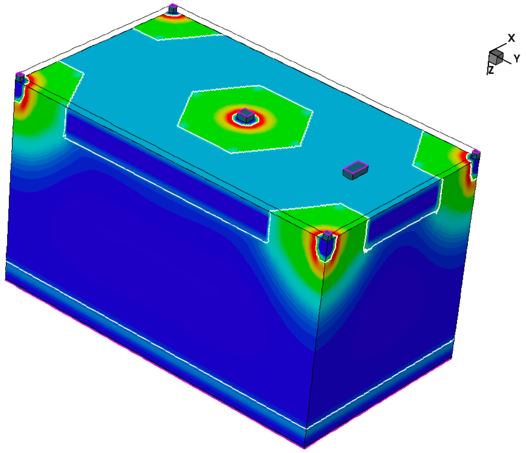
- CMOS sensors in 180nm technology successfully used for large area pixels only trackers
  - **used in ALICE (ITS2, MFT), sPhenix, CSES2/Limadou (Space)** and considered for other experiments (modified process)
  - limited by slow charge collection
  - process modification needed -> many developments ongoing
- Future developments rely on wafer scale sensors (ITS3, ALICE3)
  - **65nm TPSCo technology validated!!**
  - extremely successful characterization campaign completed (with contribution by many groups interesed in the technology)
  - large area stitched sensors: characterization started
- Extensive R&D ongoing:
  - bending of wafer scale sensors
  - mechanical support and cooling studies

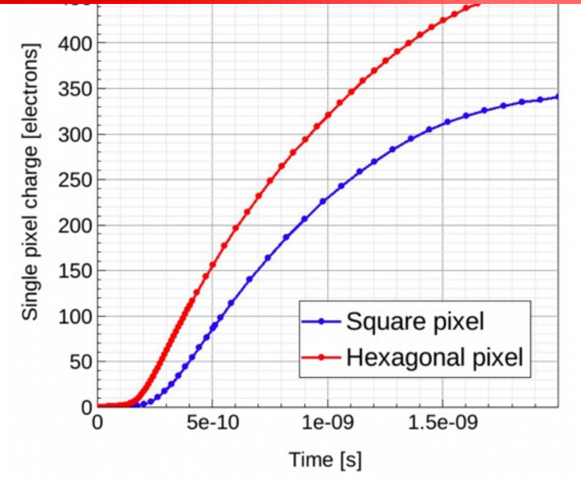
ADDITIONAL SLIDES

FASTPIX

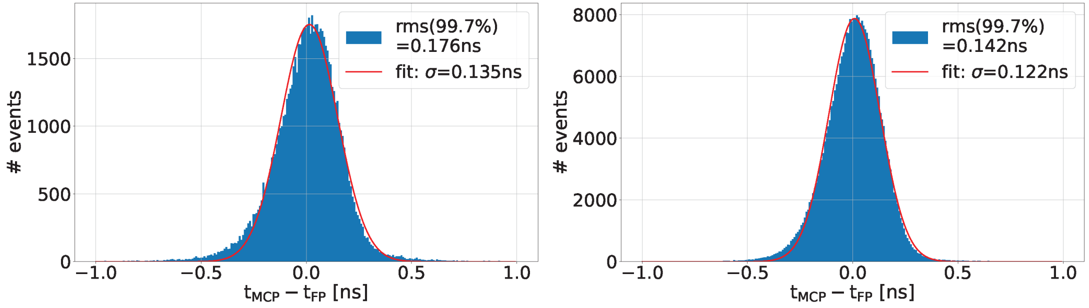
- Hexagonal design reduces the number of neighbors and charge sharing → **higher efficiency**
- Hexagonal design minimizes the edge regions while maintaining area for circuitry → **faster charge collection**
- Optimisations important not only for timing, but also for efficiency and radiation tolerance

Simulated hexagonal unit cell – electrostatic potential:





Preliminary test-beam results showed MIP time resolution of approximately 120-130 ps



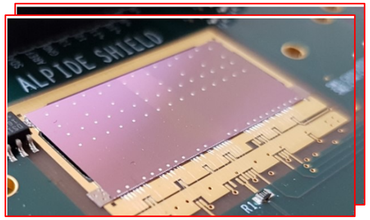
(a) (b)

Seed-pixel time residuals after timewalk correction for the inner region of the 10 µm (**a**) and 20 µm (**b**) pitch matrix.

J. Braach et al. Instruments 6 (2022) 13

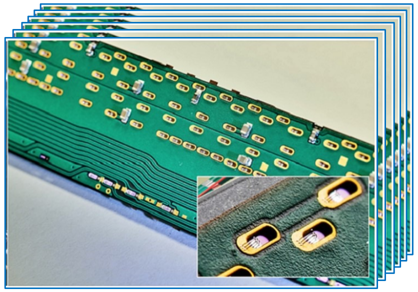
Tower Semiconductor 180nm

A long and complex journey....



chip test

FPC test

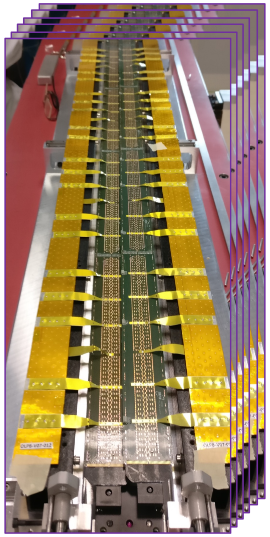


HIC assembly

HIC characterization

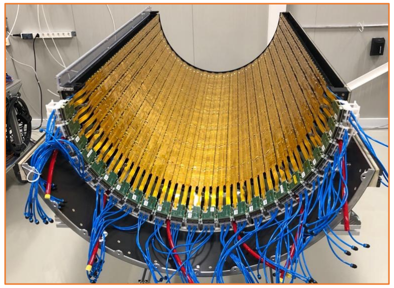
CP and SF characterization

for OB: PB characterization



Stave assembly

Stave characterization



Half layer assembly

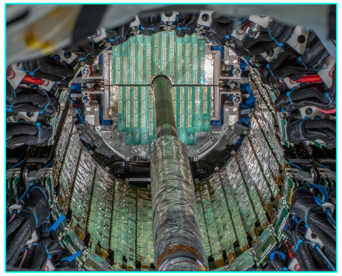
Half layer characterization

Half barrel assembly

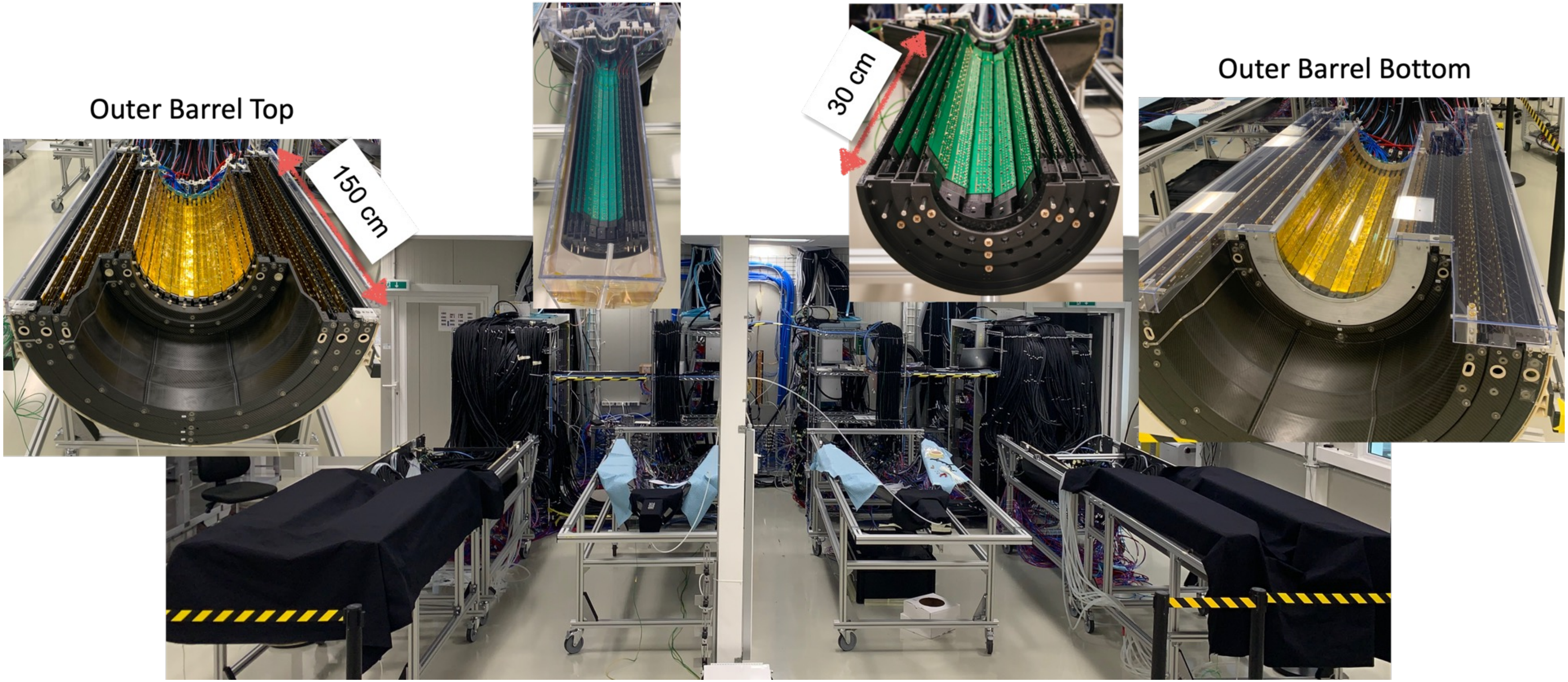
Half barrel characterization

Installation

commissioning



On-Surface Commissioning



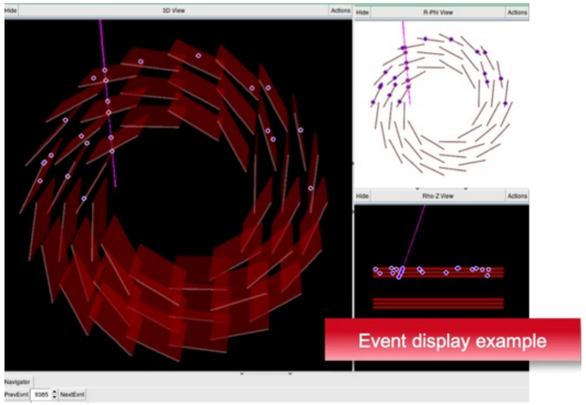
Outer Barrel Top

Inner Barrel Top

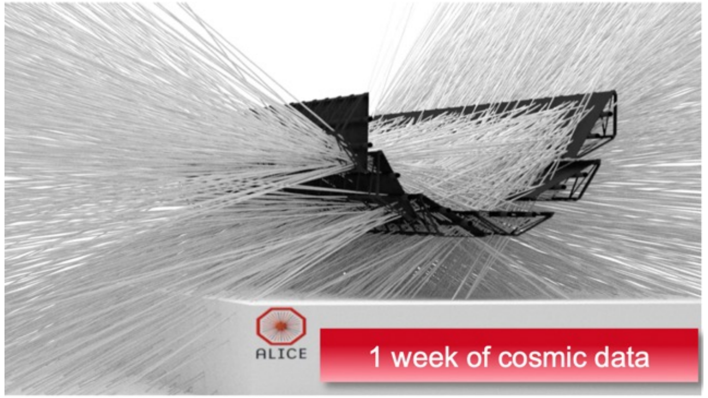
Inner Barrel Bottom

Outer Barrel Bottom

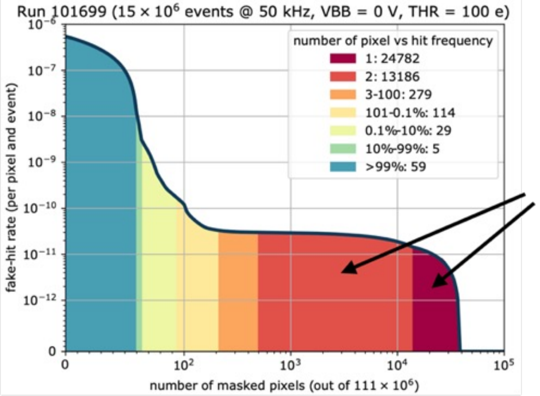
On-Surface Commissioning results



Event display example



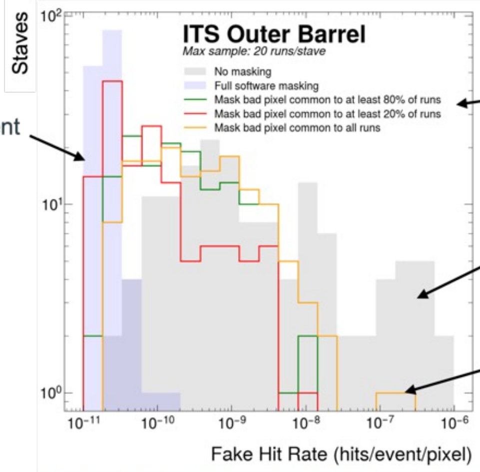
1 week of cosmic data



Hits from cosmic muons

- Cosmics tracks reconstructed
- IB: fake-hit rate of 10^{-10} / pixel / event
  - Achieved by masking fraction of 10^{-8} pixels
- OB: fake-hit rate of 10^{-8} / pixel / event
  - Achieved by masking noisy pixels common to all runs

Offline masking: FHR 10^{-10} / pixel / event



Requirement: 10^{-6} / pixel /event

Exclusion of broken double-columns

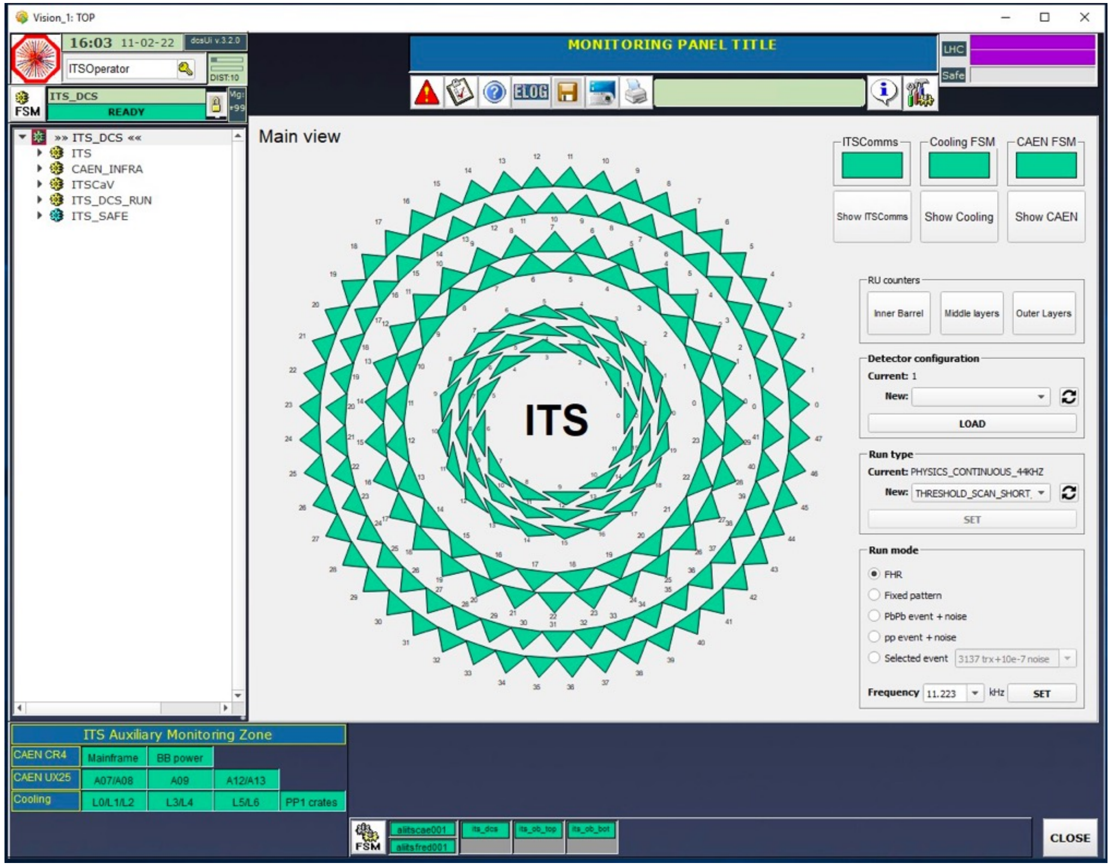
Masking noisy pixels common to all runs
→ realistic estimate for hardware masking

Excellent Fake-Hit Rate (FHR) in the entire OB

Detector Control System

- DCS ready to control detector in all phases of operation:
  - Controls and configures pixel chips and entire infrastructure
  - Error recovery during a run to continue running with minimal data loss
  - Detector functionality implemented in C++ library (pixel chips, readout cards, regulator boards)
  - GUI, FSM and alarms in Siemens WinCC OA
  - fully integrated into ALICE DCS

- Routinely used during commissioning and Pilot Beams



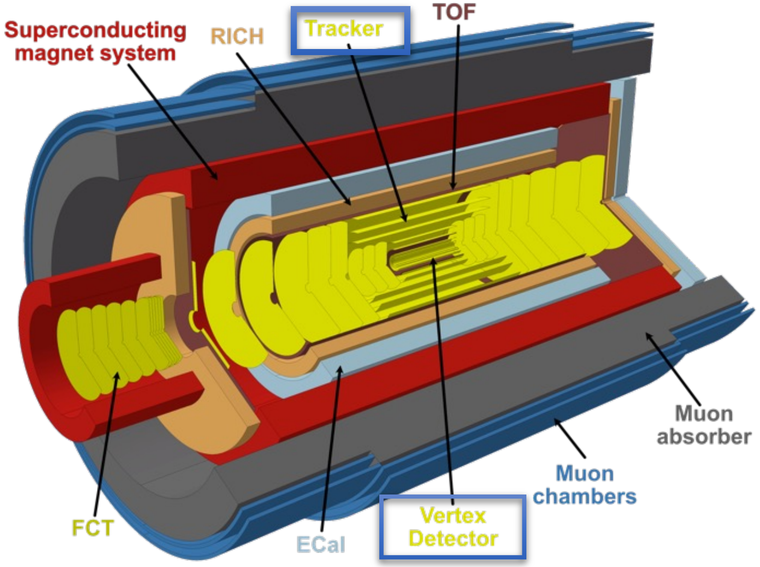
Detector configuration
Current: 1
New:

Run type
Current: PHYSICS_CONTINUOUS_44KHZ
New: THRESHOLD_SCAN_SHORT_

Run mode
● FHR
○ Fixed pattern
○ PbPb event + noise
○ pp event + noise
○ Selected event 3137 trx+10e-7 noise

Frequency 11.223 kHz

ALICE 3: tracker + vertex detector



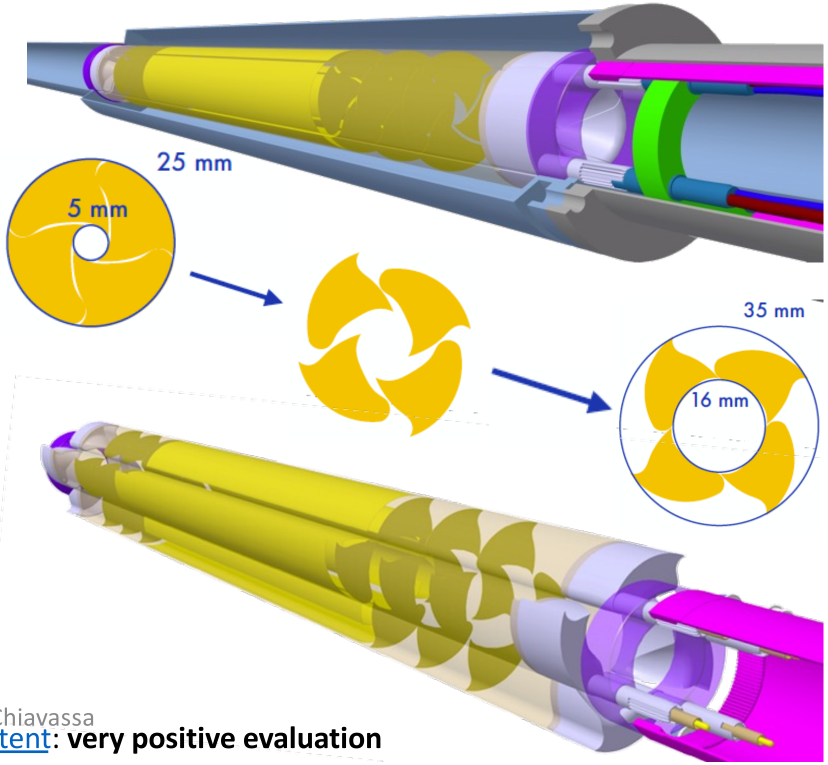
GOALS:

- **Tracking and PID over large acceptance**
- **Excellent vertexing**
- **Continuous readout**

REQUIREMENTS

- **Tracker:** low power, large surface **60 m^2** (challenges: yield, fill factor)
  - Monolithic CMOS sensors with timing (4D tracking)
- **Vertex detector:** very close to IP (challenges: high rate, high radiation load)
  - Retractable detector (iris tracker) $R_{in} \approx 5$ mm
  - Wafer-scale monolithic CMOS sensors

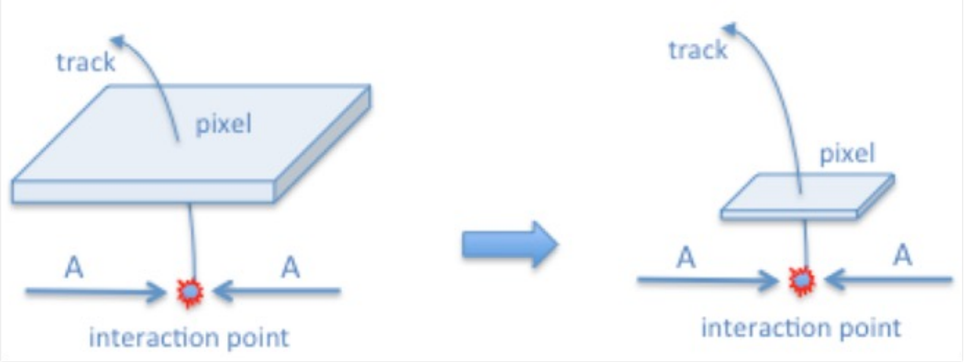
- **Conceptual study of iris tracker**
  - wafer-sized, bent MAPS (leveraging on ITS3 activities)
  - rotary petals (thin Be walls) for secondary vacuum
  - match beampipe parameters (impedance, aperture, …)
  - feed-throughs for power, cooling, data
- **R&D programme** on mechanics, cooling, radiation tolerance

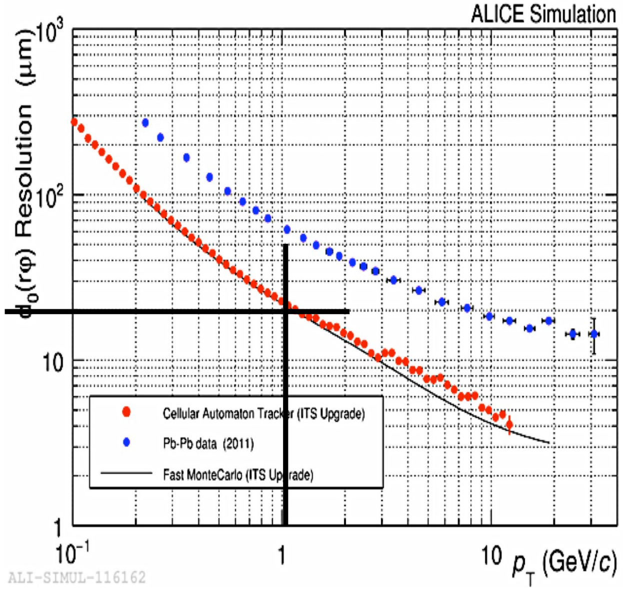


[CERN-LHCC-2022-009] LHCC review of Letter of Intent: **very positive evaluation**

New ITS (ITS2) Design Objectives

- **Improve impact parameter resolution** by factor ~3 in rϕ and factor ~5 in z at p_T = 500 MeV/c
    - Get closer to Interaction Point: 39 mm -> 23 mm
    - **Reduce material budget:** **1.14% X_0 -> 0.35% X_0 (inner layers)**
    - **Reduce pixel size:** **50 x 425 μm^2 -> ~30 x 30 μm^2**
- **Improve tracking efficiency and p_T resolution at low p_T**
    - Increase number of track points: 6 -> 7 layers
- **Fast readout**
    - Readout of Pb-Pb collisions at 50 kHz (ITS1: 1 kHz) and p-p at 400 kHz





ITS TDR: J. Phys. G: Nucl. Part. Phys. 41 (2014) 087002

Calibration

The Challenge:

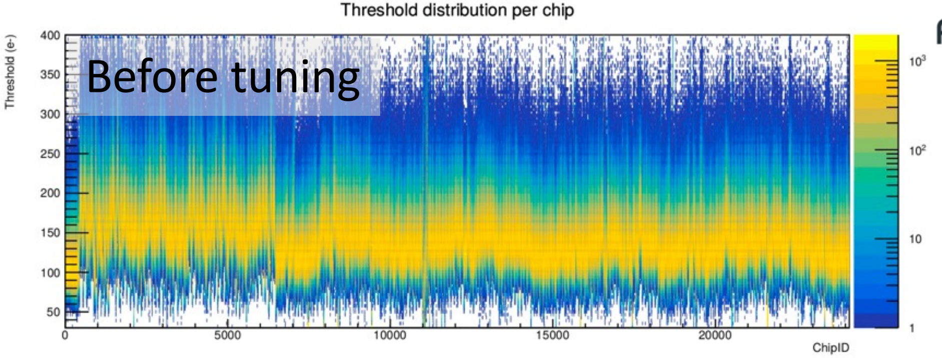
- Online calibration of 12.5 billion channels
- Threshold scan of full detector: > 50 TB of event data
- Several scans to be run sequentially
  - Threshold tuning (adjust thresholds to target)
  - Threshold scan (measure actual thresholds)

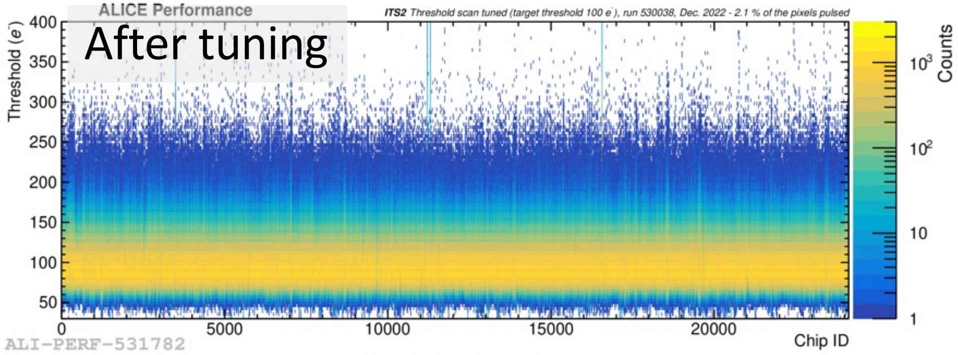
Procedure:

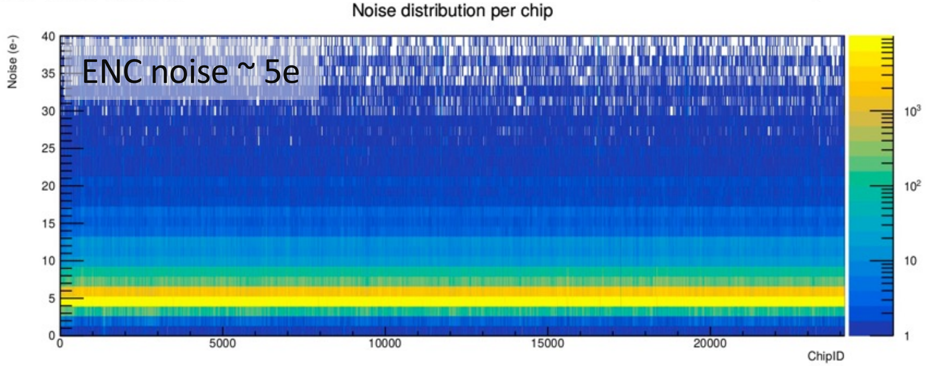
- DCS performs actual scans: configure and trigger test injections
- Scan runs in parallel but independently on all staves
- Distributed analysis on event processing nodes
- full procedure takes **less than 30 minutes**

Results:

- Scan with online analysis successfully run on full detector
- before tuning: settings used in surface commissioning, detector already fully efficient
- After tuning: Thresholds very stable on all the chips: RMS of threshold distribution compatible with what we had during production
- ENC noise ~ 5e$^-$

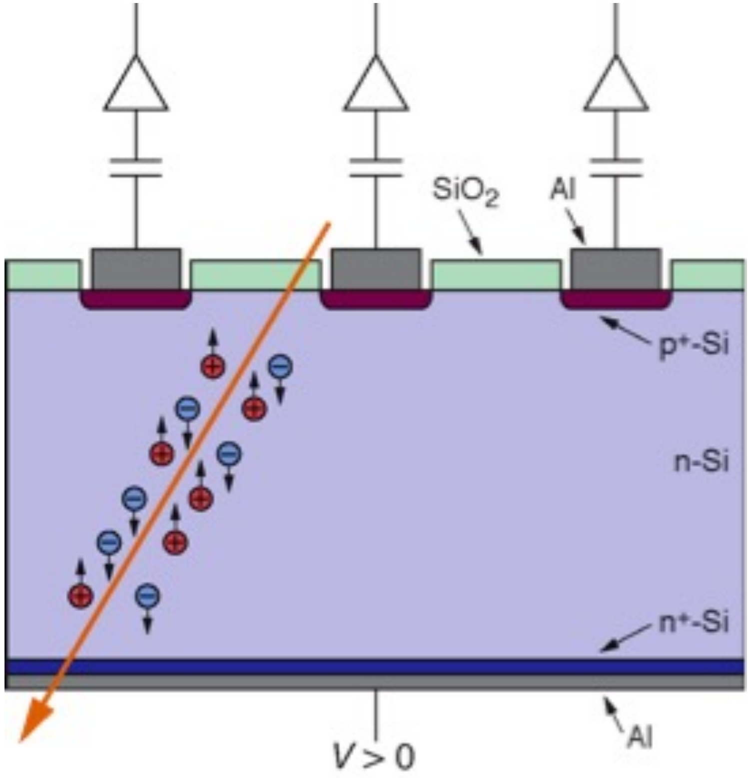




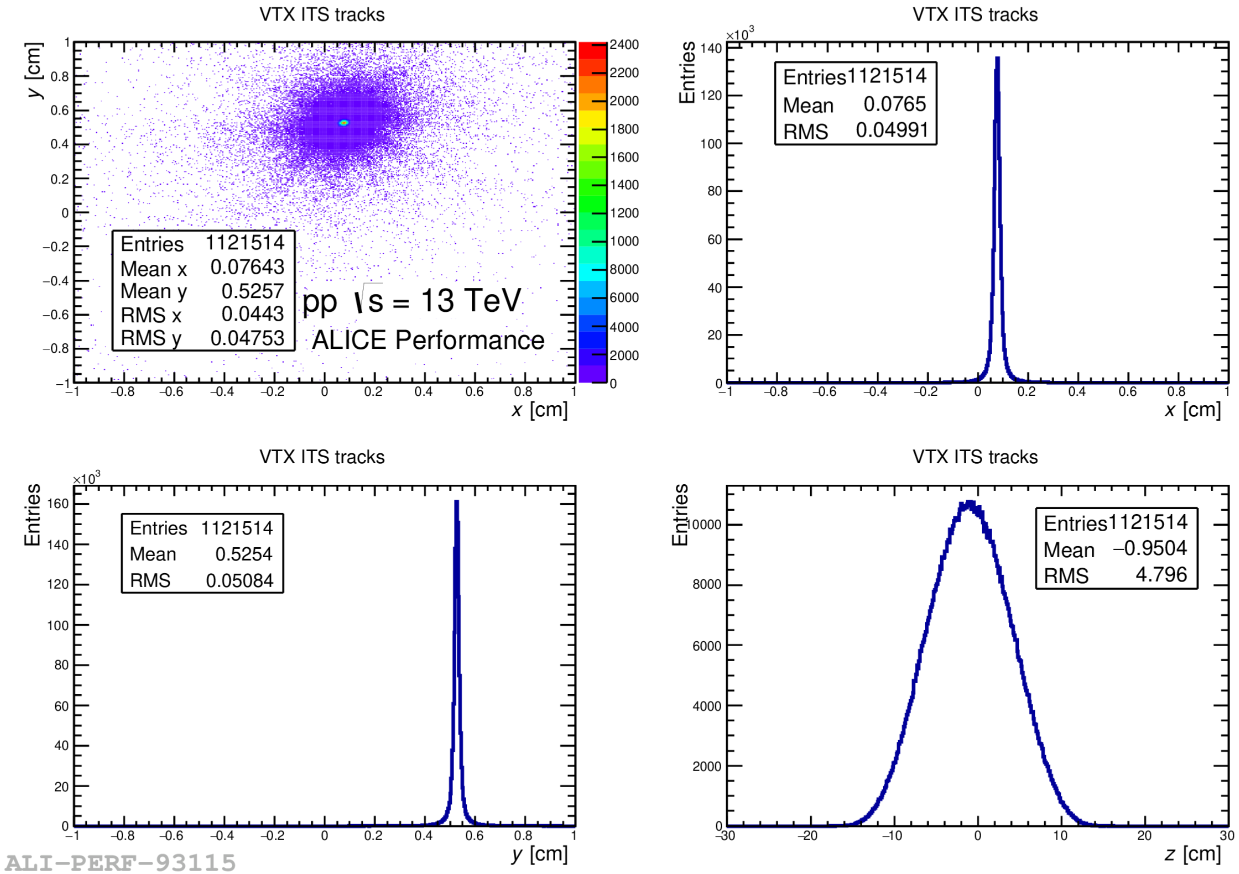


Position sensitive silicon detector: working principle

segmented electrodes: position measurement



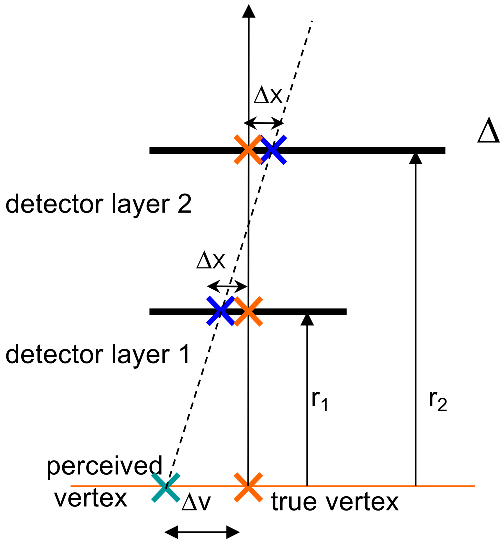
Vertexing



ALI−PERF−93115

What determines the impact parameter resolution?

Vertex projection from two points: a simplified approach (telescope equation)



$$\Delta v = \Delta x \bullet \sqrt{\frac{r_2^2 + r_1^2}{(r_2 - r_1)^2}}$$

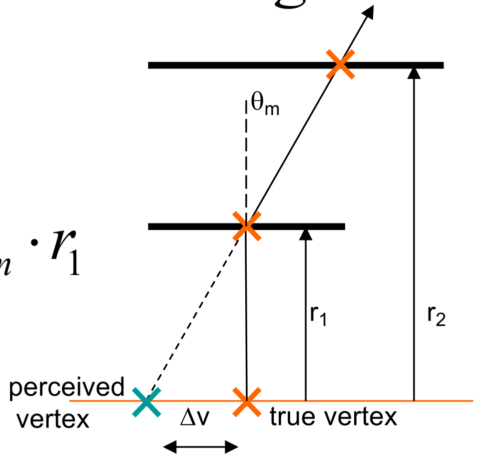
Go closer to the impact point to have a better impact parameter resolution!!

Multiple Scattering

$$\theta_m = \frac{13.6 Mev}{\beta \cdot c \cdot p} \cdot z \cdot \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \ln\left(\frac{x}{X_0}\right)\right]$$

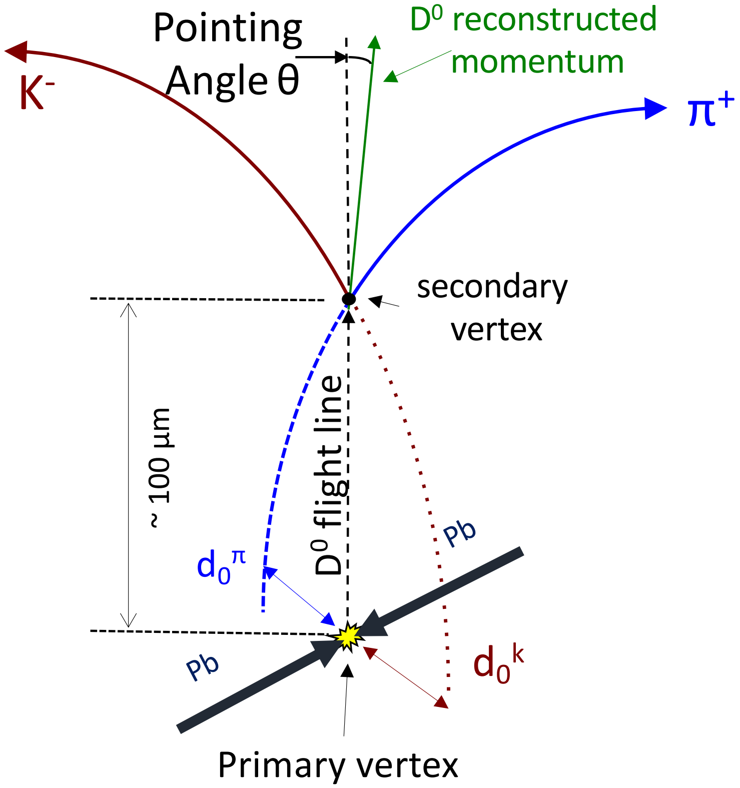
$$X_0 = \text{radiation length}$$

$$\Delta v = \theta_m \cdot r_1$$



Reduce the material budget to improve the impact parameter resolution!!

Secondary vertex reconstruction



- Example: ALICE ITS1

Particle	Decay Channel	cτ (µm)
D^0	$K^-\pi^+$ (3.8%)	123
D^+	$K^-\pi^+\pi^+$ (9.5%)	312
	$K^+K^-\pi^+$ (5.2%)	150
	$p K^-\pi^+$ (5.0%)	60