

Testing and Integration in SR1



Istituto Nazionale di Fisica Nucleare



UNIVERSITÀ DEGLI STUDI
DI GENOVA

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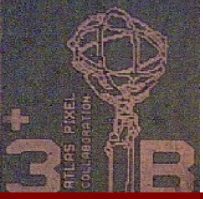
Andreas Korn

(University College London)

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UCL



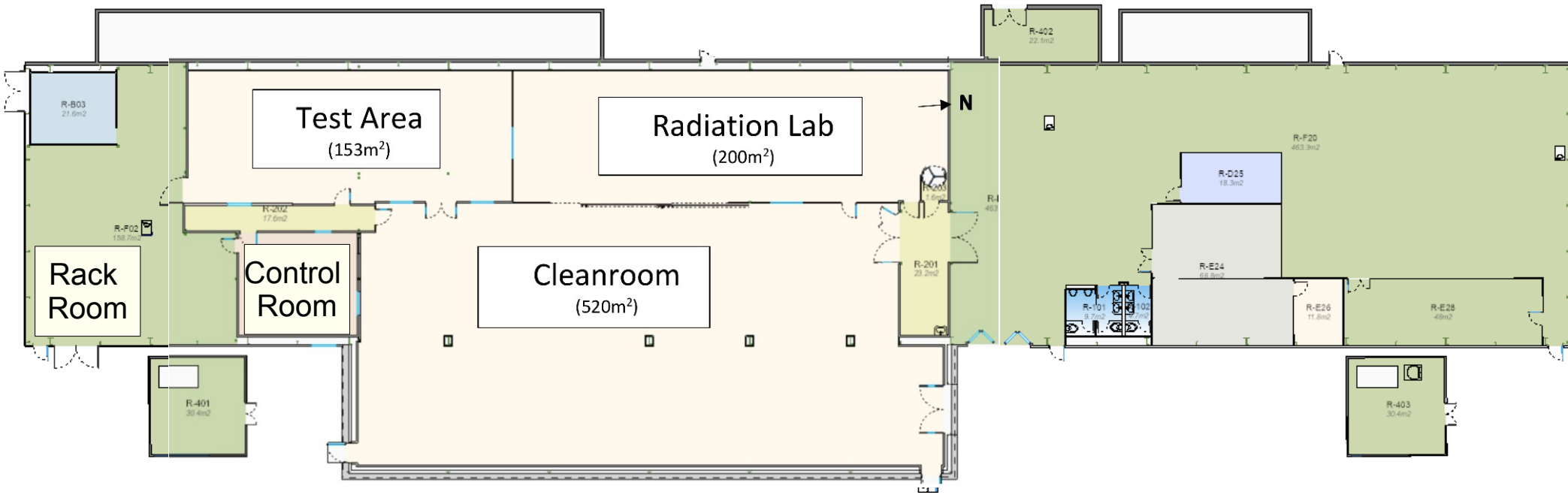
Disclaimer

- I am by no means an expert on integration
- My view is rather DAQ centric
- Many thanks to Benedikt, Marianne and Susanne for material and suggestions
- Work is due to their efforts, errors are all mine

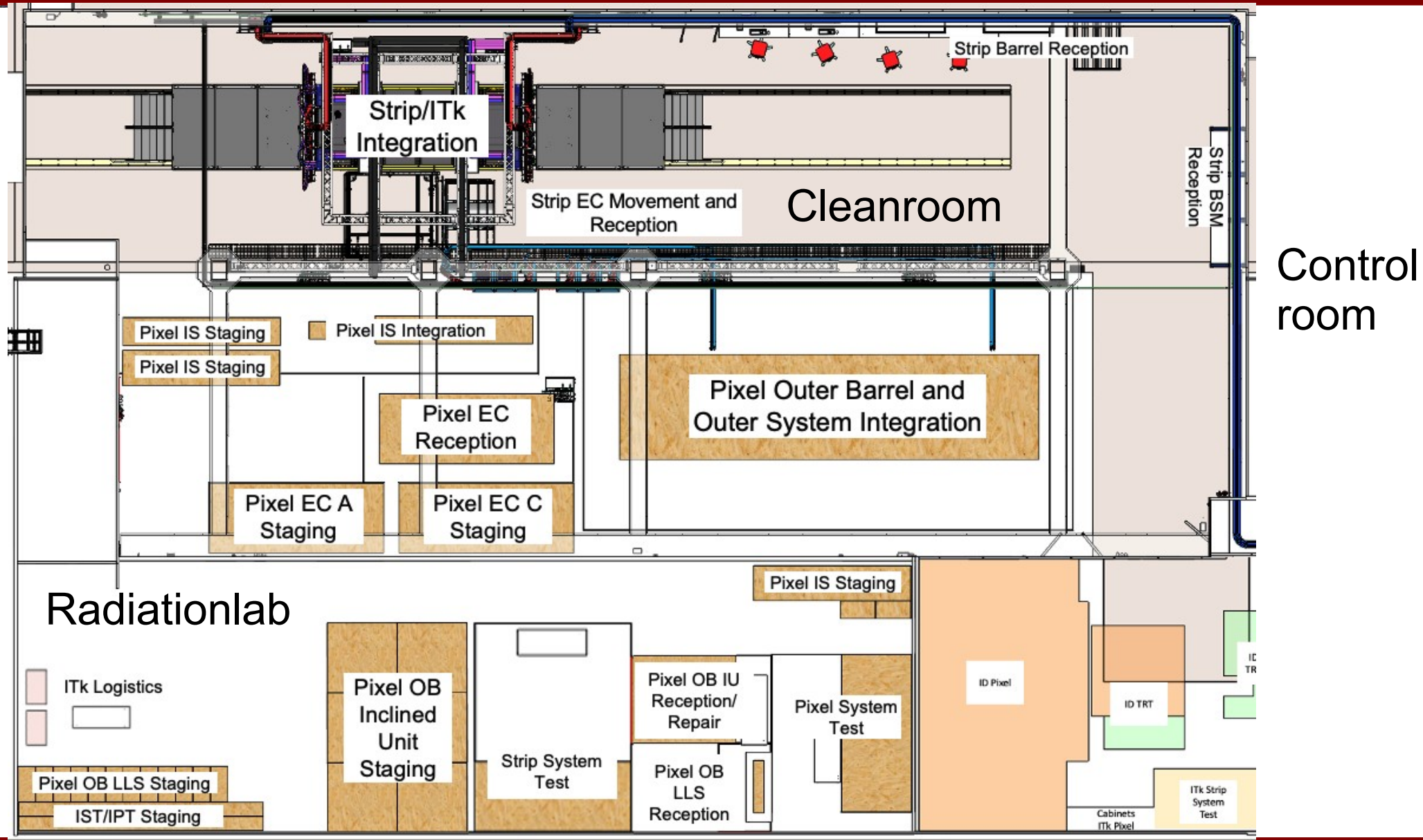
Overview

- SR1 at CERN
 - Major staging and test area
 - Slice test
 - Prep ongoing, first parts expect this summer
 - First test of large scale system
- Integration
 - EC to arrive 04/2027
 - Bringing the detector together
 - Essential health and reception test
 - First test of “real” system

SR1 Layout



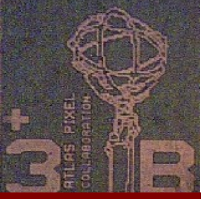
SR1 Layout



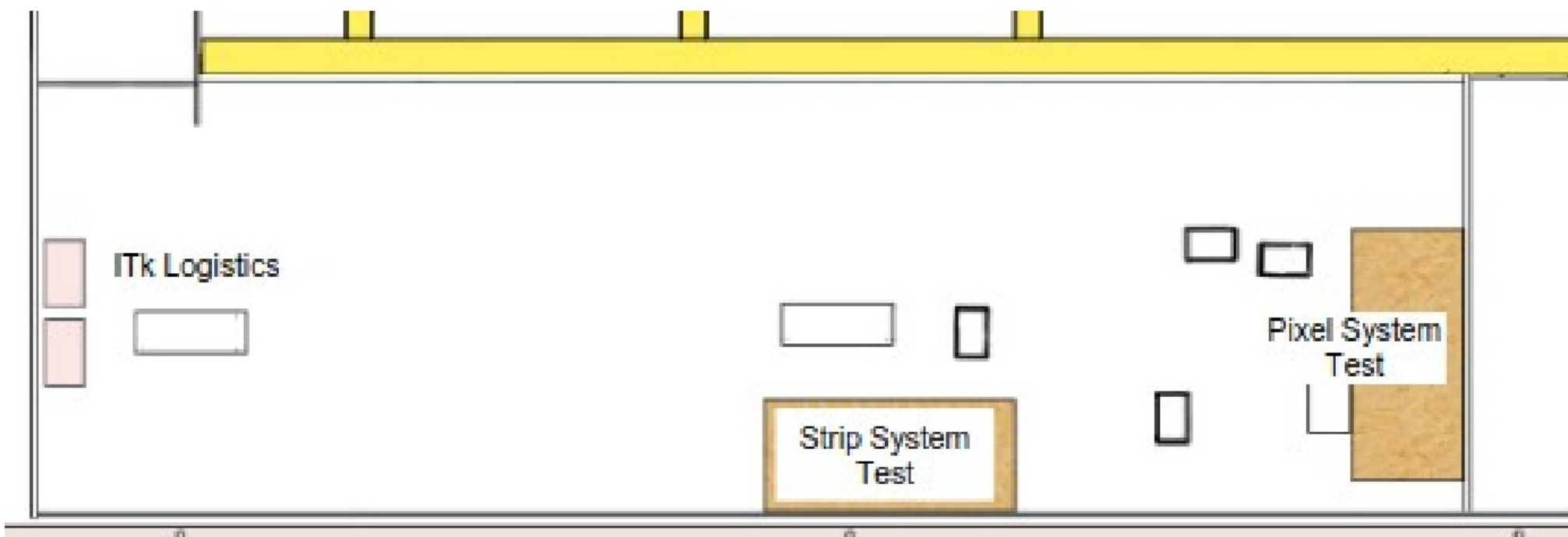
Control room

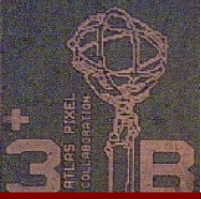
Slice Test

- In the SR1 Radiationlab at CERN
- Timescale: ongoing, first items expected summer24
- First time to test larger scale system
- First time to test different systems together
- Important testing ground for all systems
 - especially DAQ
 - "realistic PP1 and on/off-detector cables"
- Very tight timescale → need to use existing systems
 - Pre-production power supplies
 - pre phase-2 DAQ



SR1 Radiation lab layout





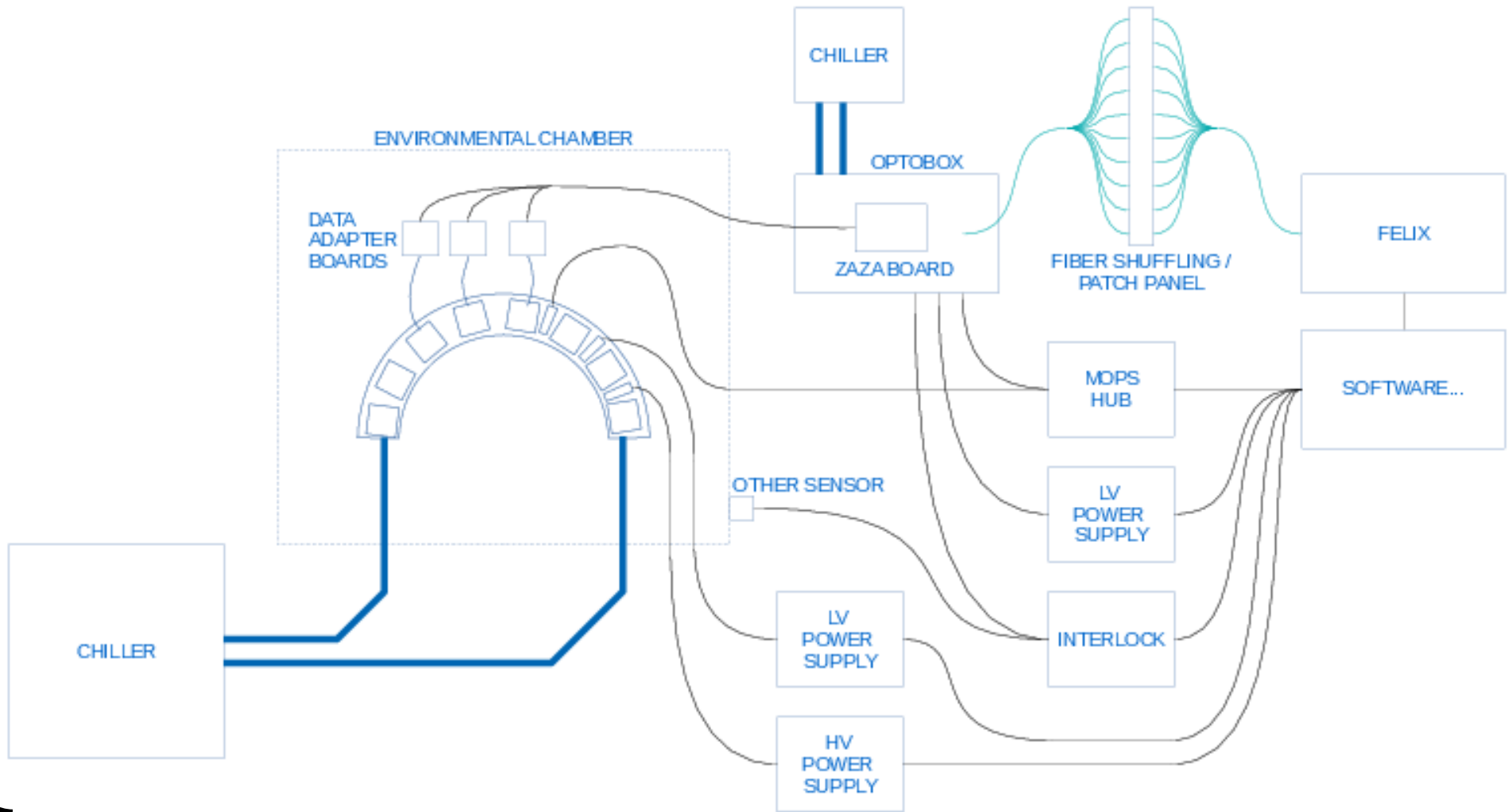
Expected Loaded Local Supports

LLS type	modules	SP chains	HV channels	MOPS chips	Tiloc NTCs	power [W]
EC L2	16	2	4	2	2	163
OB L2 flat	36	4	8	4	4	414
SR1 slice Σ	52	6	12	6	6	577

- 52 pixel modules (EC: “Ring2”)
- Potentially + strip systems
- Possibly explore data emulators

Overview

Hardware Chain – Initial Testing



Ben Smart

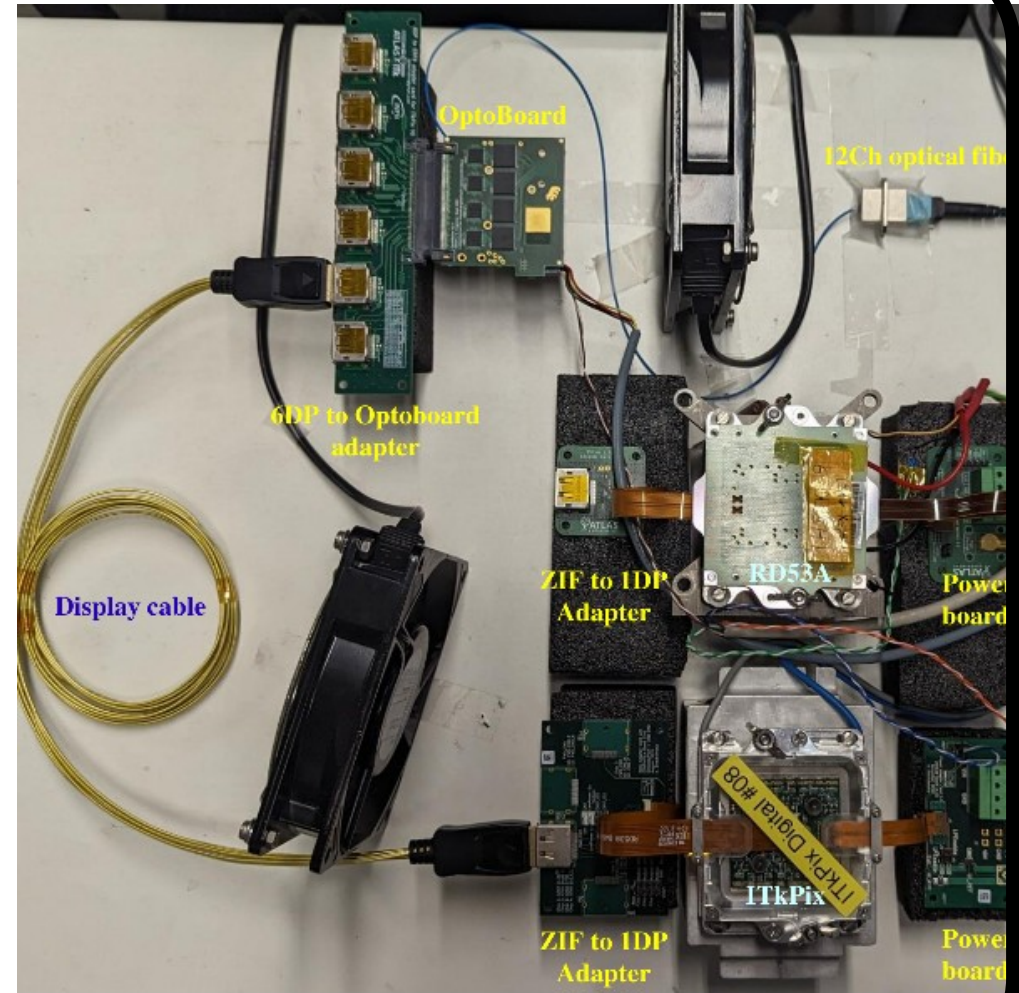
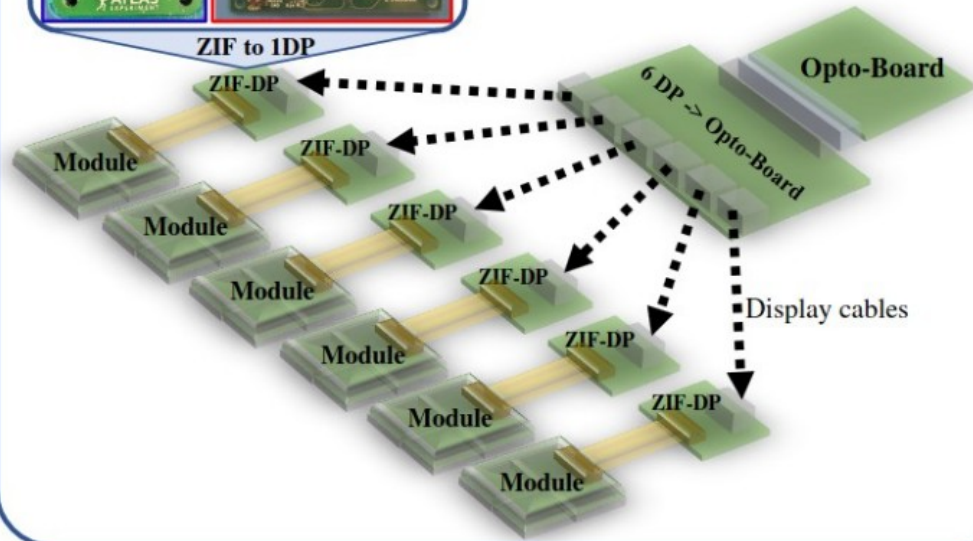
5

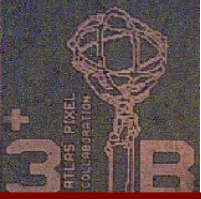
Zazaboard to Optoboard

6 DP to Opto-Board adapter card



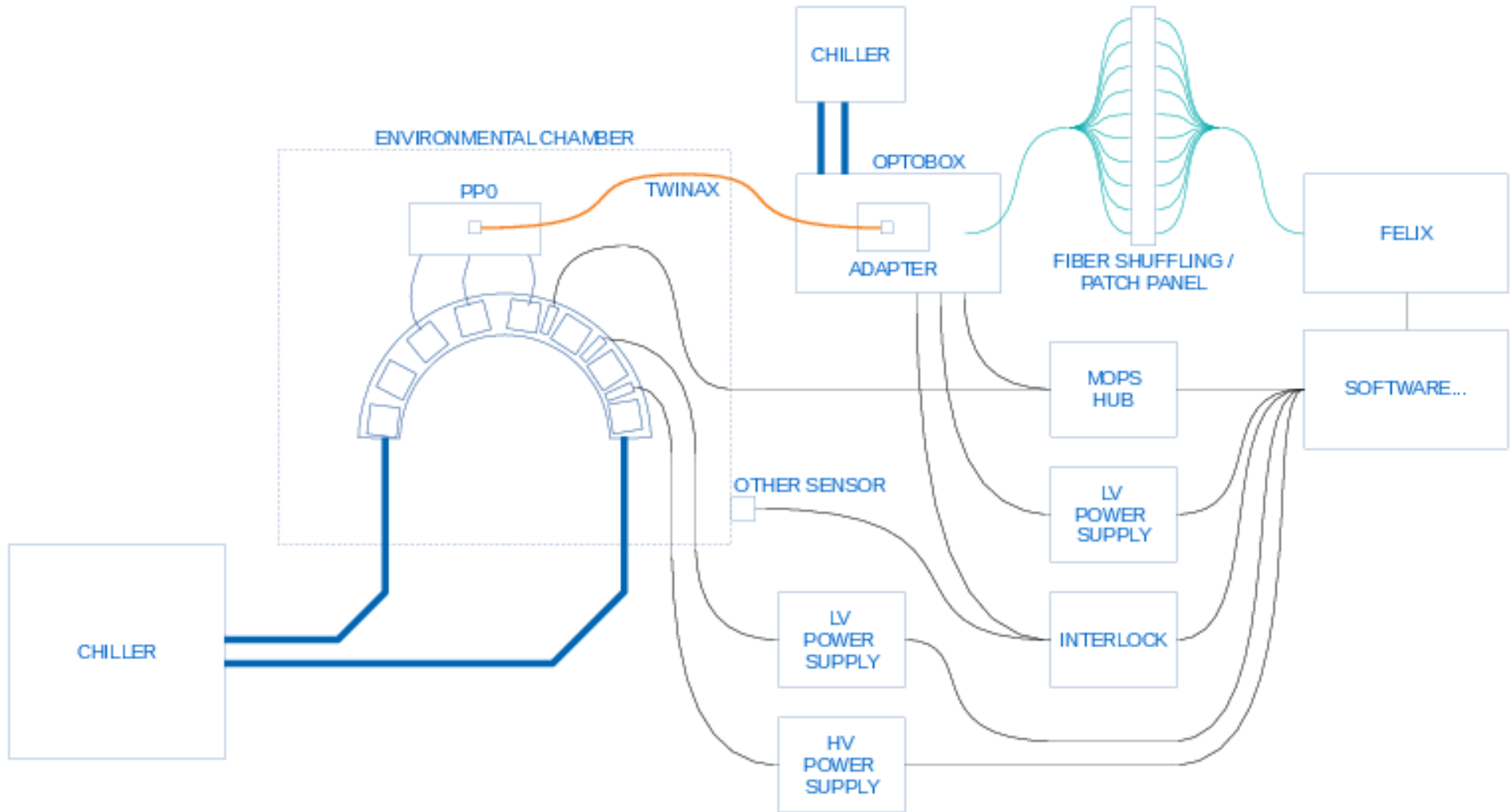
Modules must have internal AC decoupling for serial powering mode!



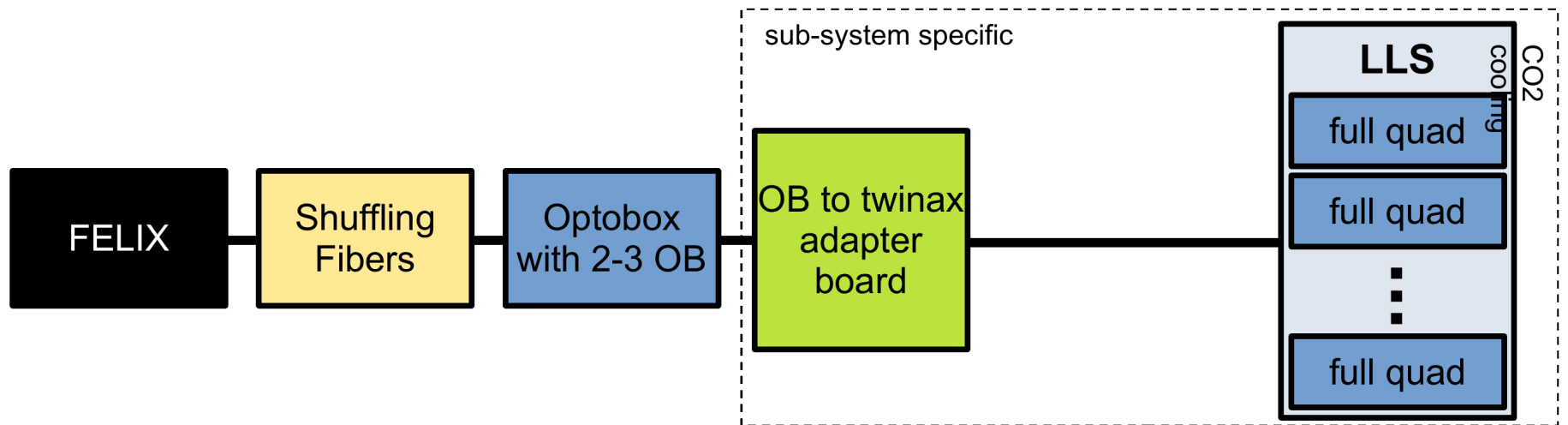
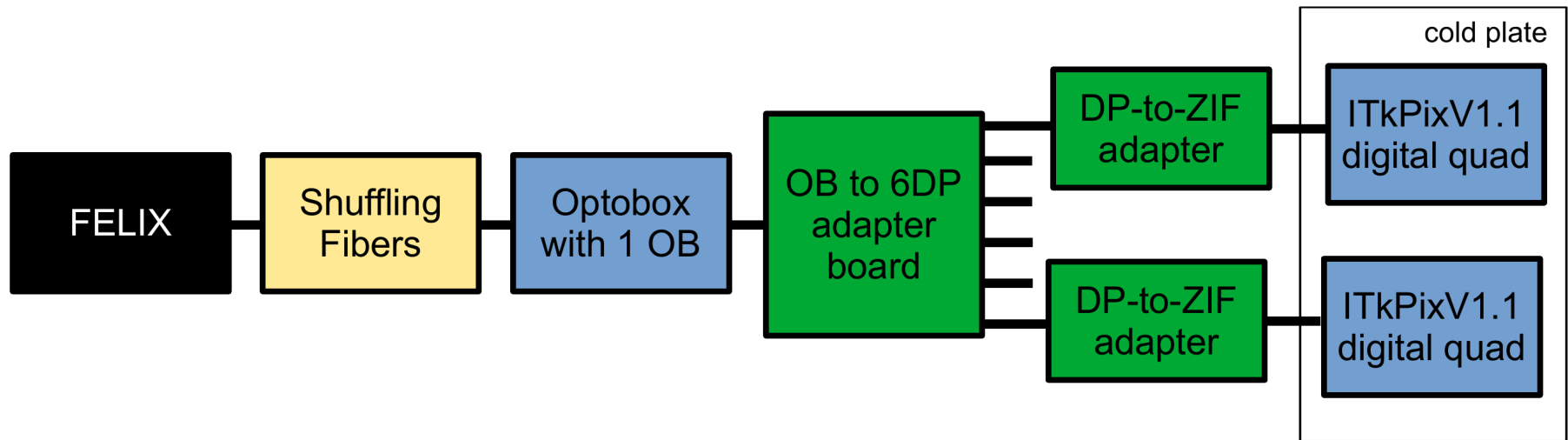


Overview: Slice Test Setup

Hardware Chain – Production



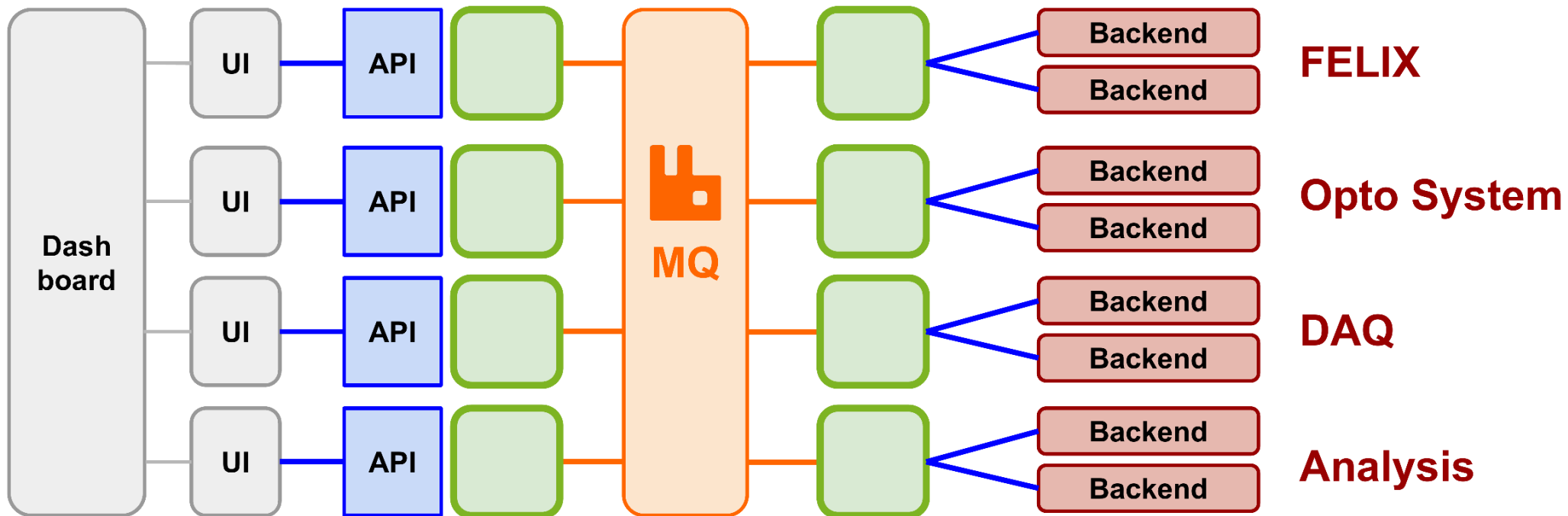
Readout Overview



DAQ Sketch

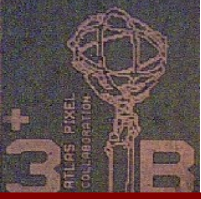
- Current phase 1 DAQ plan very module QC centric
 - Need to scale to multi modules
 - Microservices being deployed
- testing and feedback crucial

Gerhard Brandt



<https://indico.cern.ch/event/1395925/contributions/5905085/attachments/2837431/4958710/Scan%20Calibration%202024-04.pdf>

DAQ/Calibration GUI Sketch



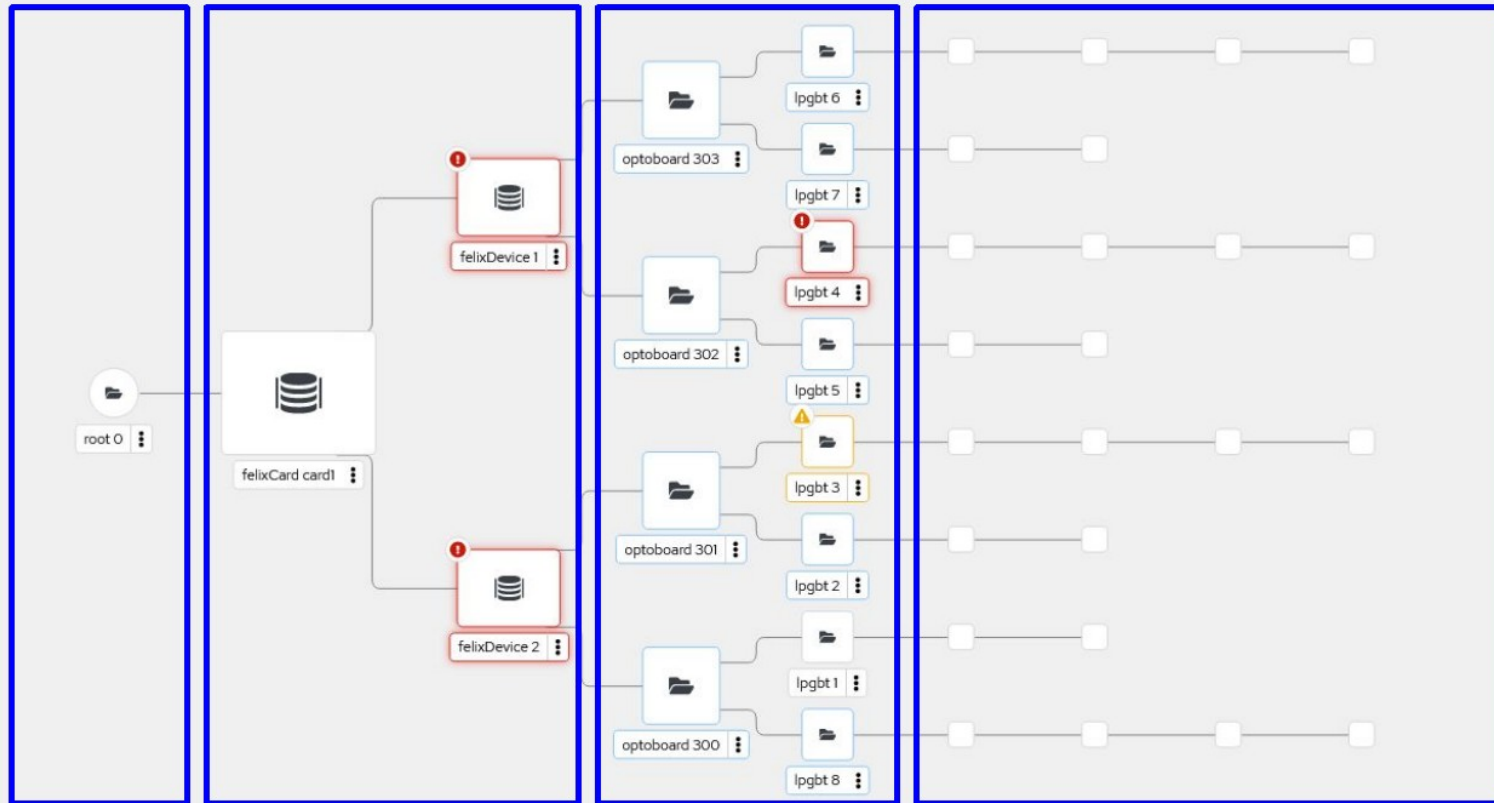
Topology Services

Runkey

FELIX

OptoSystem

Supports/Modules



microservices

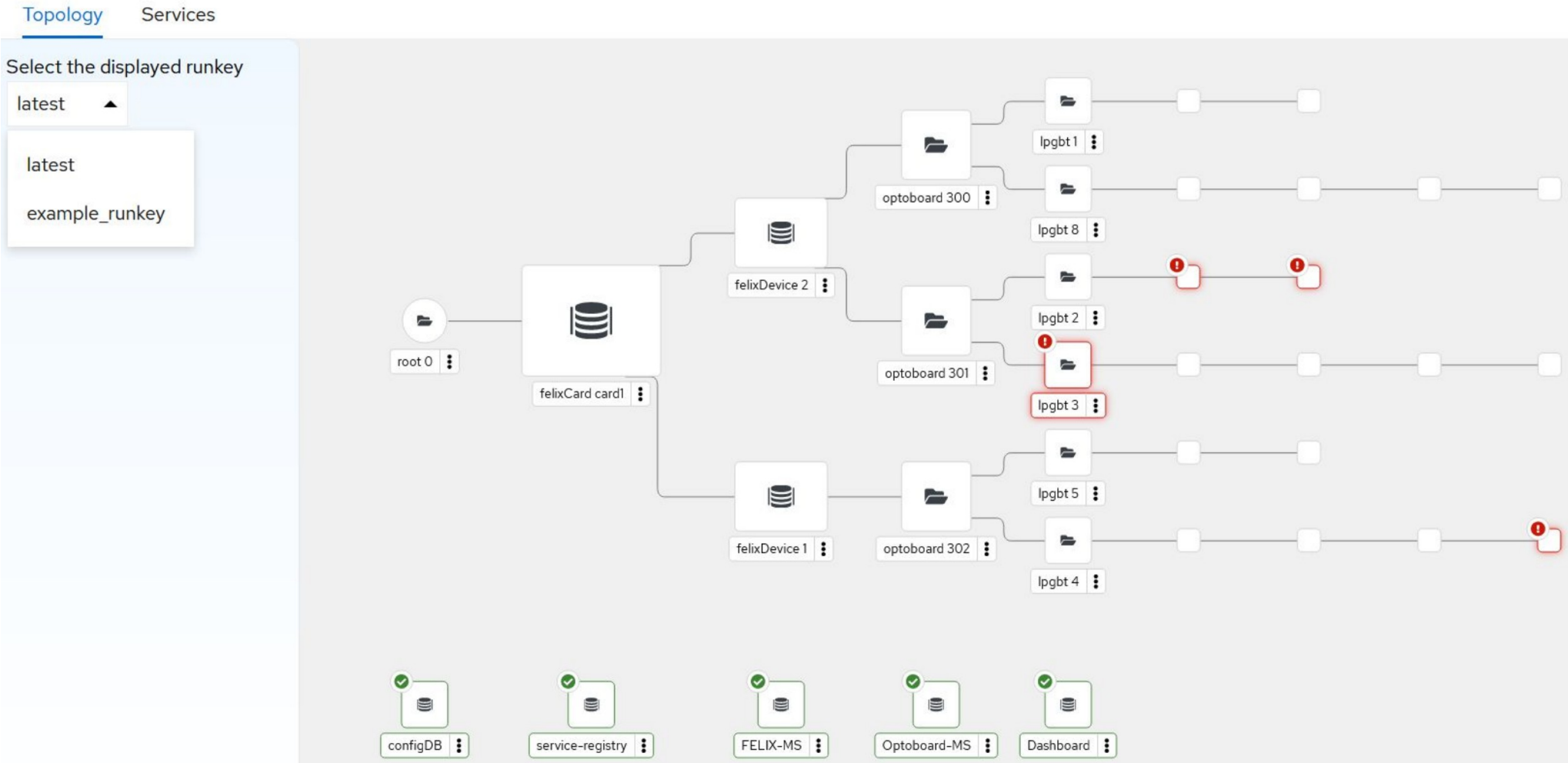
Show Logs

Gerhard Brandt

Perspectives

- Topology
- Service cards
- Nodes
- ...

Summary



Expert Panel Example

Optoboard GUI

Configure all Optoboards Edit GUI Configuration LLSQC-OB7 Health Celery health

OB7

Select device: lpgbt1

Read register Read back: Set Equalization

Select a register

Write register Read back: Med Frequency Channel 0

Select a register High Frequency 0

Value to be written

Perform BERT BER limit: Swap polarity Link (Rx/Tx) Tx

Uplink 0 Meas Time 12 Link number 0

Set Phase Mode Select mode

Group 0 Phase 0

Configure Manual selection

lpgbt to configure

gbcrc to configure

Read Status

lpGBT status

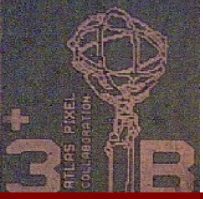
```
2024-04-24 01:57:58,662 - WARNING - CommWrapper.py - ICNetioNextHandler library not found, check if installed
2024-04-24 01:58:00,780 - INFO - celeryTasks.py - Executing run_startup_task at worker_ready signal...
2024-04-24 01:58:00,784 - INFO - celeryTasks.py - run_startup_task executed!
2024-04-24 01:58:00,786 - INFO - celeryTasks.py - Loading...
2024-04-24 01:58:00,788 - WARNING - InitOpto.py - Using lpgbt-com for IC communication with optoboard OB7
2024-04-24 01:58:00,789 - INFO - InitOpto.py - Current working directory: /root
2024-04-24 01:58:00,790 - INFO - InitOpto.py - No config path provided, using default configuration file
2024-04-24 01:58:00,790 - INFO - InitOpto.py - Initialising config from /usr/local/lib/python3.9/site-package
```

```
{
  "defaultConf": {
    "LLSQC-OB7": {
      "OB7": {
        "optoboa": {
          "vtrx_v": {
            "Configu": {
              "config_": {
                "debug": {
                  "flx_G": {
                    "flx_d": {
                      "configI": {
                        "test_mo": {
                          "commTod":
```


Expert Panel Example

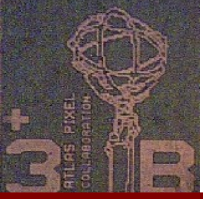
		Home	Monitoring	FelixOff								
Links :		0	1	2	3	4	5	6	7	8	9	10
Optical Power Read Advanced	TX:	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
	RX:	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Optical link alignment Read		<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Electrical link alignment Read	0 :	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
	4 :	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
	8 :	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
	12 :	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
	16 :	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
	20 :	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
	28 :	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
29 :	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	

primary IpGBTs appears when optoboard is powered on



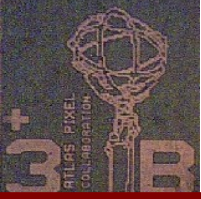
DAQ Status

- A lot of development ongoing, still a lot more needed
- Very limited experience with multi-modules
- Need DB infrastructure
- Need calibration and analysis system
 - that can handle larger structures
- Need reliable and fully functional DAQ backend
- Eventually will need optimisation (scan time)
- Slice test is crucial testing ground
- Without thorough testing: DAQ & system will not be ready

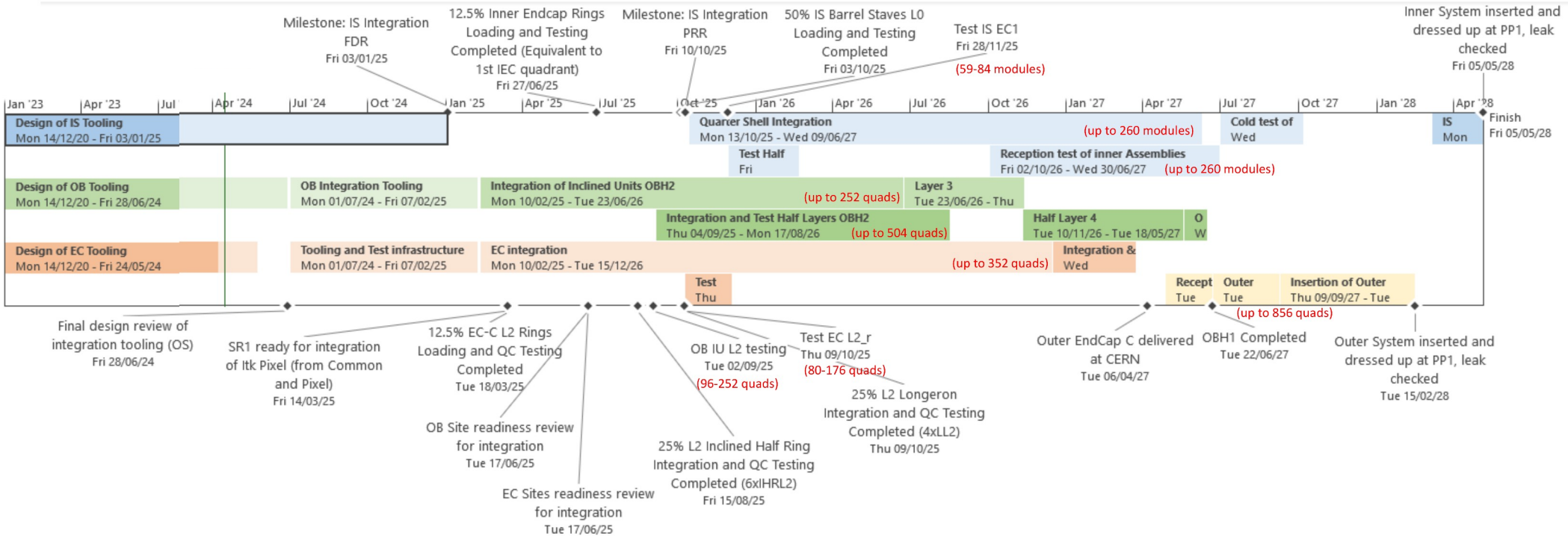


Integration Setup

- Integration in SR1 at CERN
- Installation summer 2024-2025
- Start with Outer Barrel Integration
 - Split between bldg. 161 (OB IU) and SR1 (layer)
 - Up to 504 quads!
- EC testing in Frascati and Liverpool from 2025
- EC expected to arrive in SR1 ~04/2027
 - EC: up to 352 quads
 - First EC will be EC C, second EC A



Testing timeline in ITk Pixel Integration

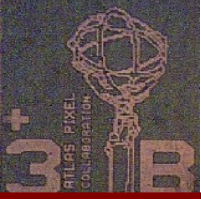


Validated DAQ and scan and analysis framework for testing needed to run electrical tests.
 Scans are IV, VI, MinHealth¹, ReducedPixelFailure¹, Thermaltest based on register read information, some in low power mode.

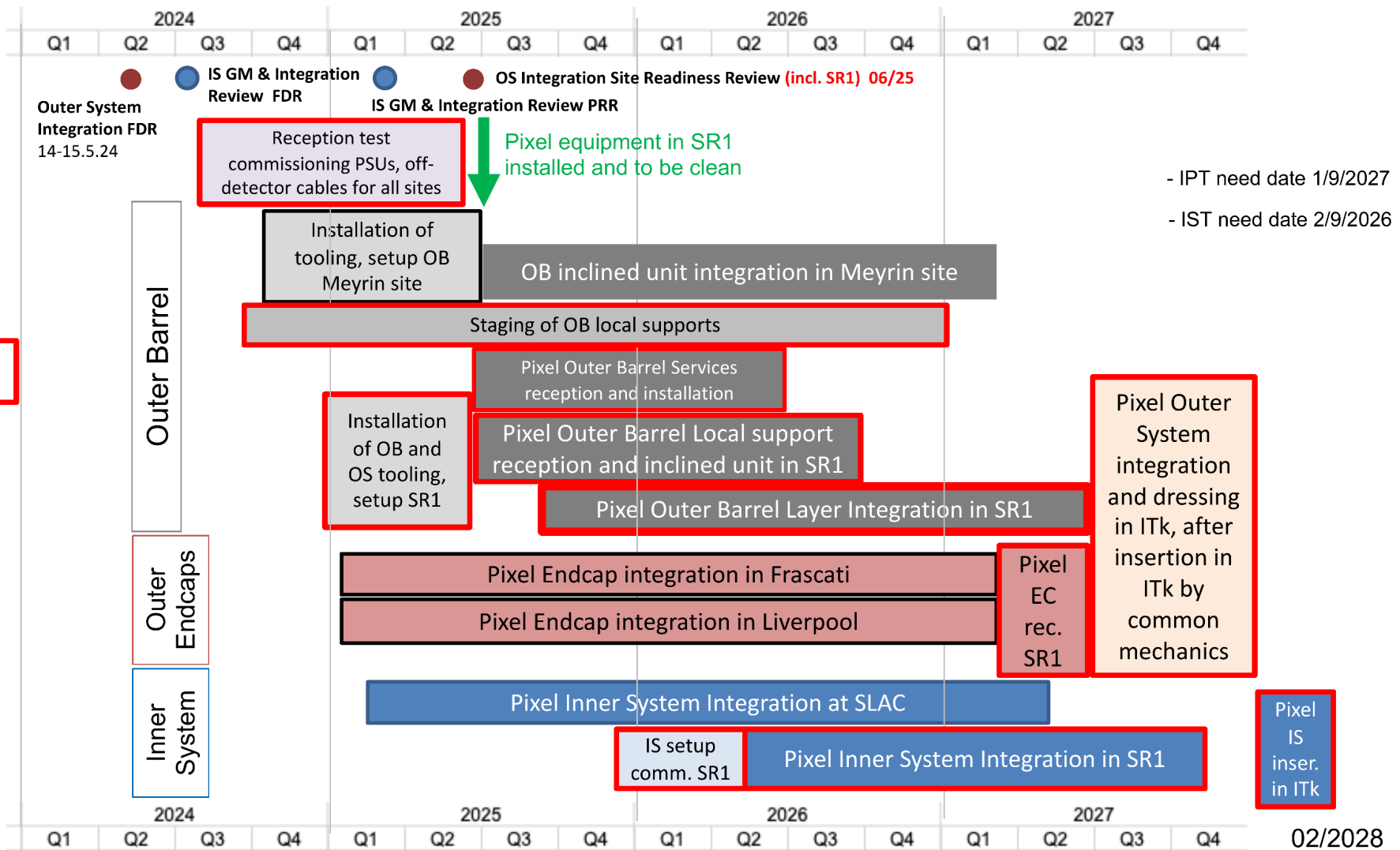
¹Module QC doc and [EDMS 2685862](#) <https://indico.cern.ch/event/1395925/contributions/5905784/attachments/2839231/4962387/PixelIntegrationOverview-AUWApr24-SK.pdf>



Detailed Timeline



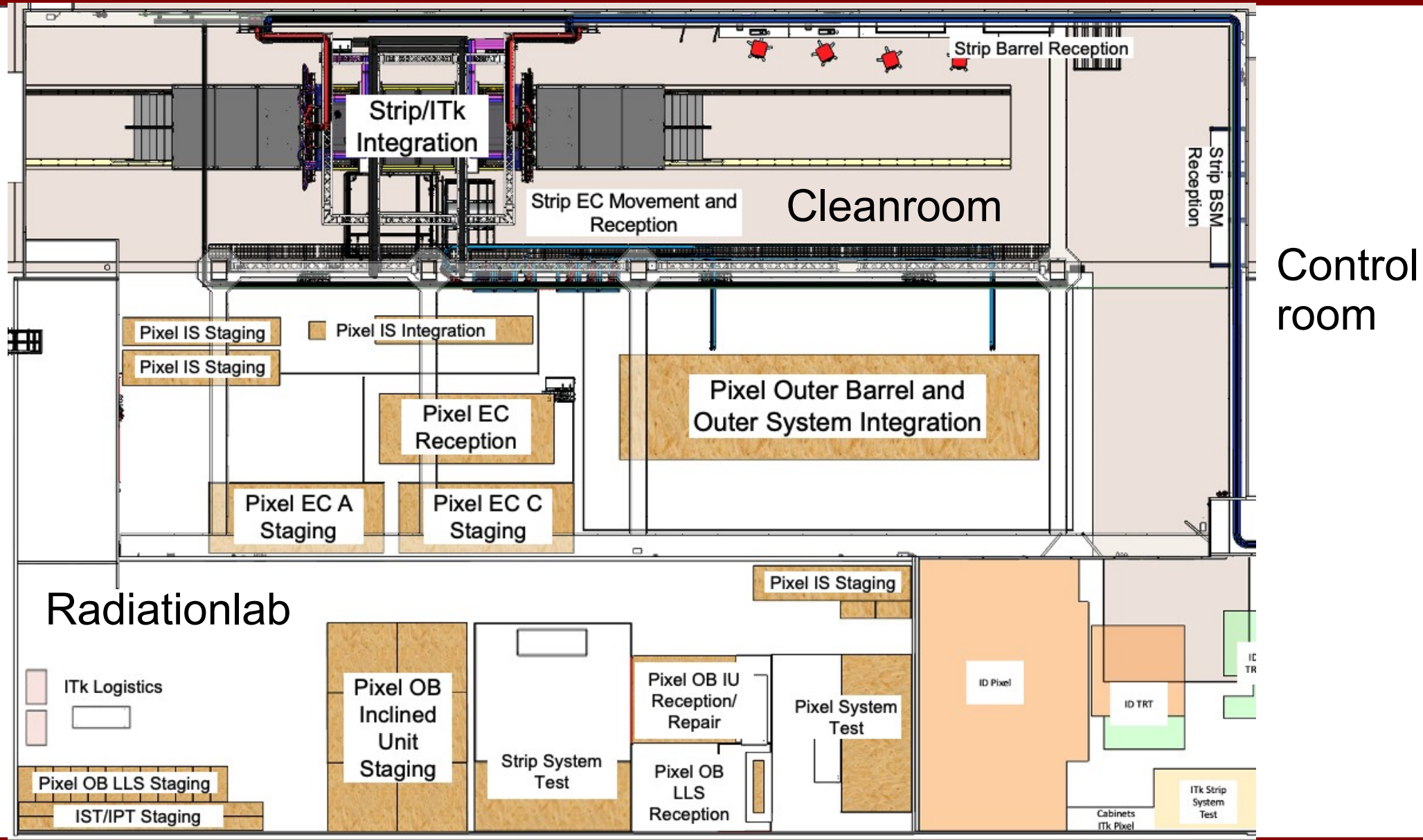
Reviews



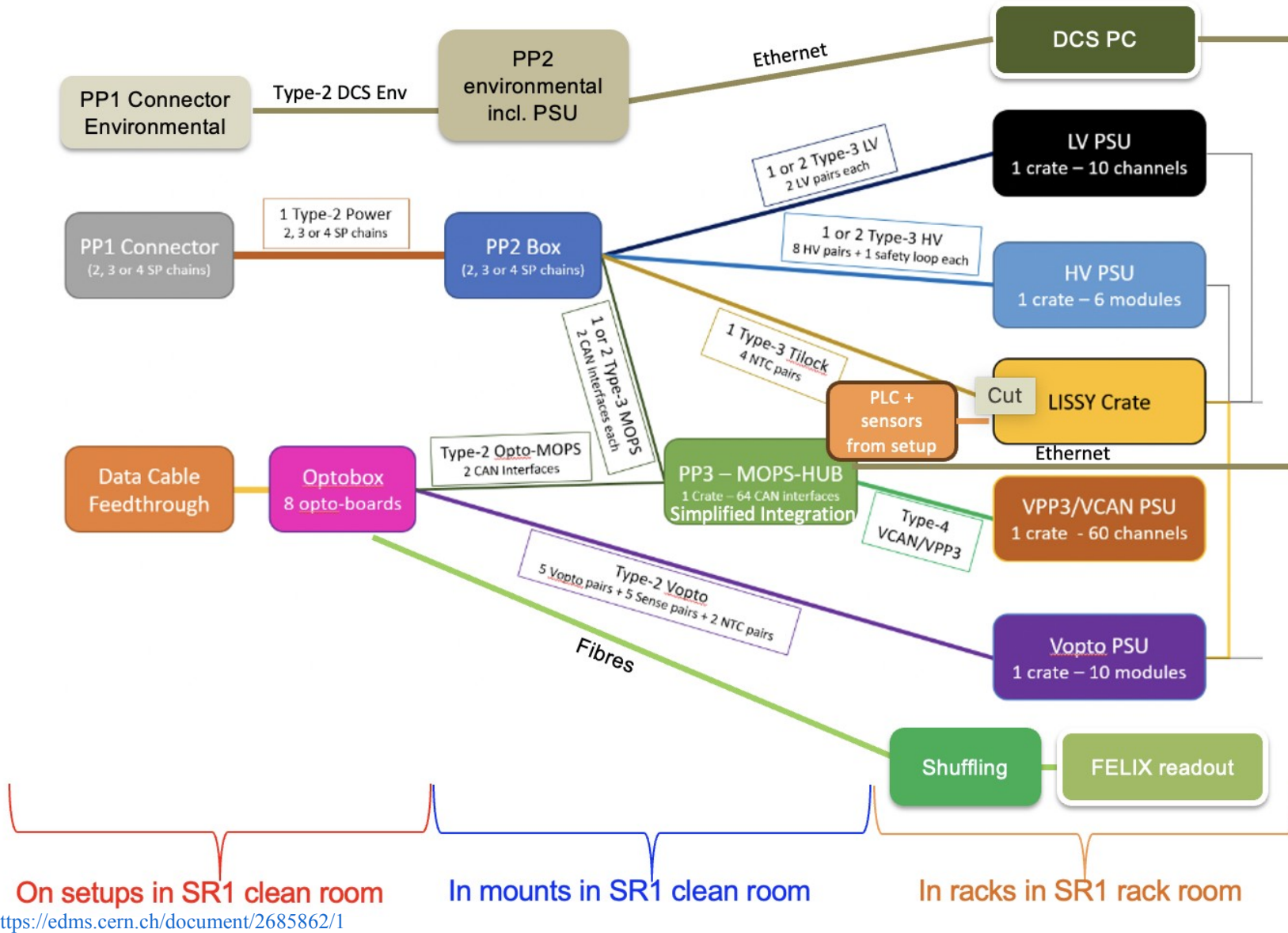
13.3.24

Overview of ITk Pixel Integration in SR1 - Susanne Kuehn

SR1 Layout

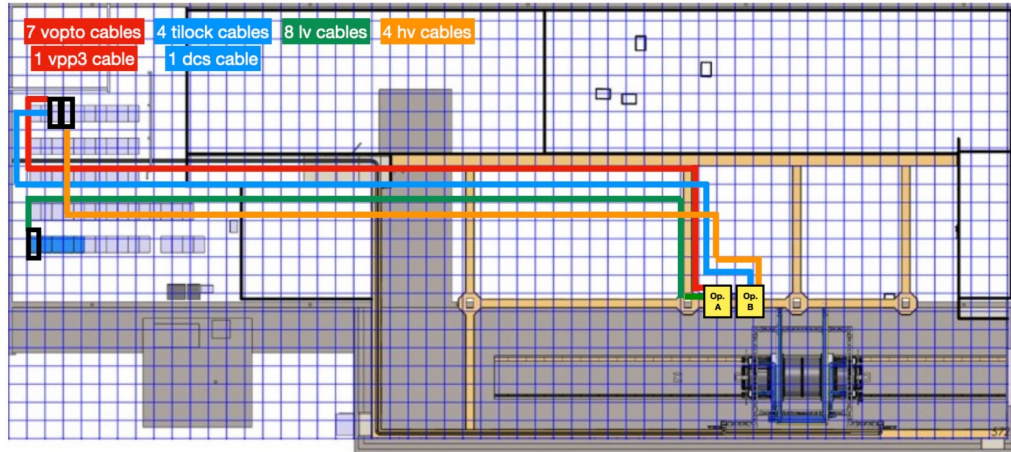


Services Summary

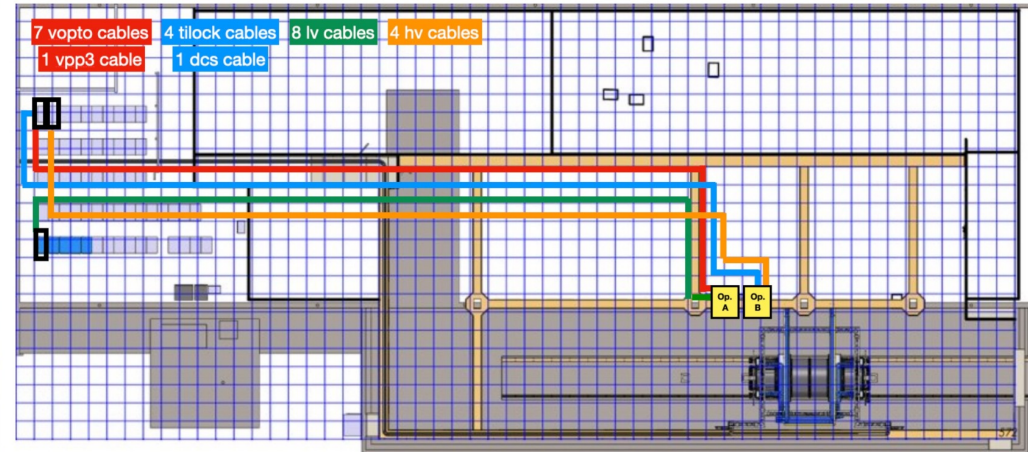


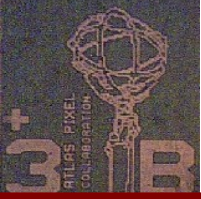
Services Routing

EC-1

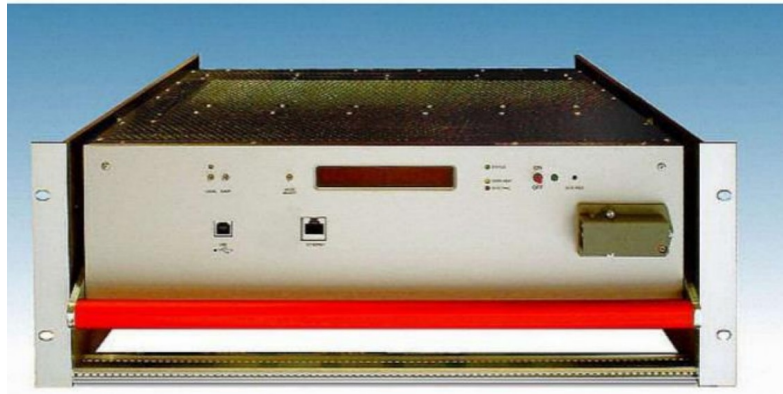


EC-2





Power Supplies



Lot 2 PL5xx System

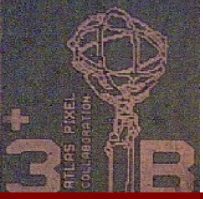


Lot 3 (HV PSU)



Lot 1 MPOD System

<https://edms.cern.ch/document/2931241/1>

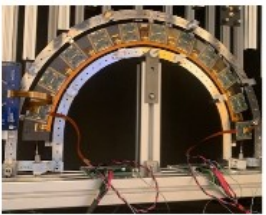


Integration Tests

- Performance Test
- Check against existing scan data from LLS tests
(<https://gitlab.cern.ch/atlas-itk/pixel/module/itkpix-electrical-qc>)
 - Needs CO2 cooling
- Electrical Low Power Tests with limited cooling
 - LP scans, noise
 - Read V, T from chip registers
→ DAQ register reads essential!
 - BER/eye tests
- Ping Test
 - LV/NTC resistance, Leakage current
 - data links resistance/capacitance

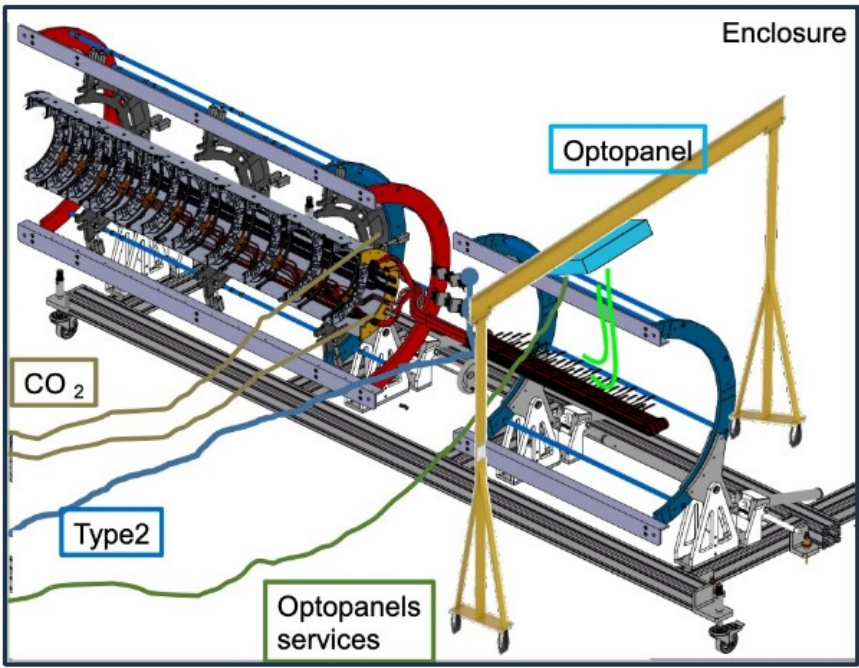
Electrical Testing Stages in Outer Endcap Integration

1. Loaded local support (half-ring) reception test (up to 26 quads)
2. Half-rings in half-layer shell all layers in 5 testing steps (in one testing step up to 16 SP-chains, 352 up and 176 down links)

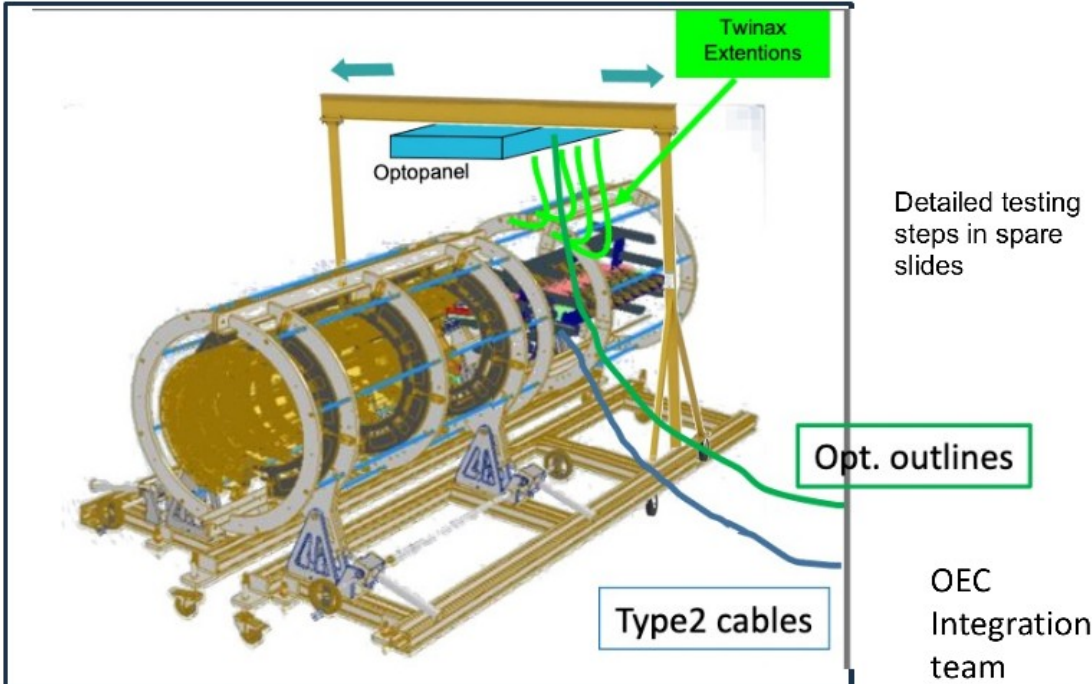


- Testing in normal power and in low power mode foreseen

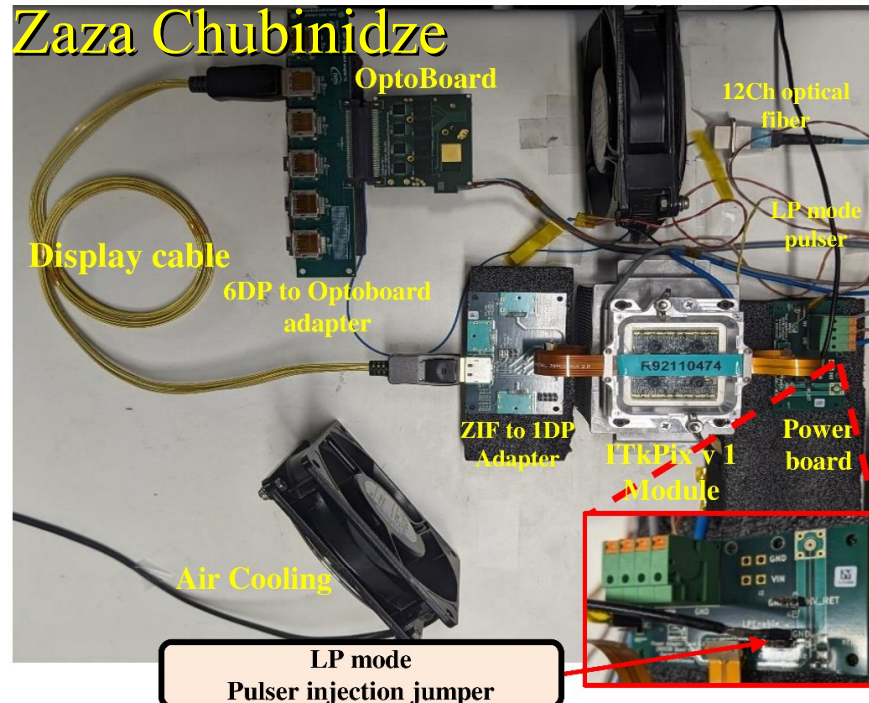
3. Full endcap all layers in 10 testing steps (in one testing step up to 16 SP-chains, 352 up and 176 down links)



Not to scale, environmental enclosures and services not shown



Low Power Mode Testing



- Half-rings need testing without CO2 cooling → Low Power mode
- Scan with one enabled CoreColumn at a time
- Analog scans needed?
- 3 Watts can be dissipated by Fans
- Limited experience with LP scans → further testing and investigation needed

- Module power in LPM is 1.55V, 2.012A --- **3.1W**
- Pulser with “square wave” 1.2Vpp, 100Khz

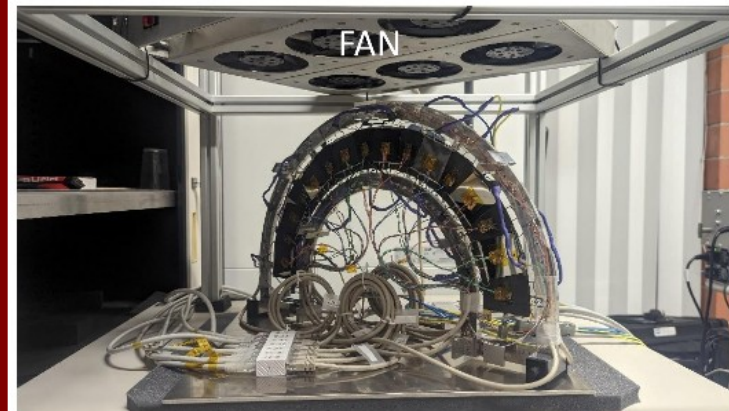
```
{
  "config": {
    "max": 50,
    "min": 0,
    "step": 1,
    "nSteps": 5
  },
  "loopAction": "Rd53bCoreColLoop"
},
{
  "config": {
    "max": 50,
    "min": 0,
    "step": 1,
    "nSteps": 50,
    "disableUnused": true
  },
  "loopAction": "Rd53bCoreColLoop"
}
```

Modify Scan console config (std_analogscan.json)

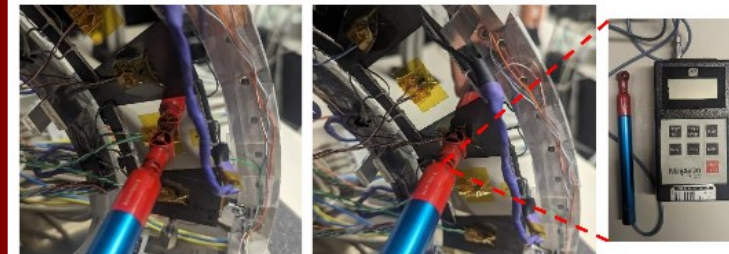
Chip config: EnCoreCol0/1/2/3 = 0/0/0/0

Low Power Mode Testing

Dummy thermal Half Ring on LPM with convection



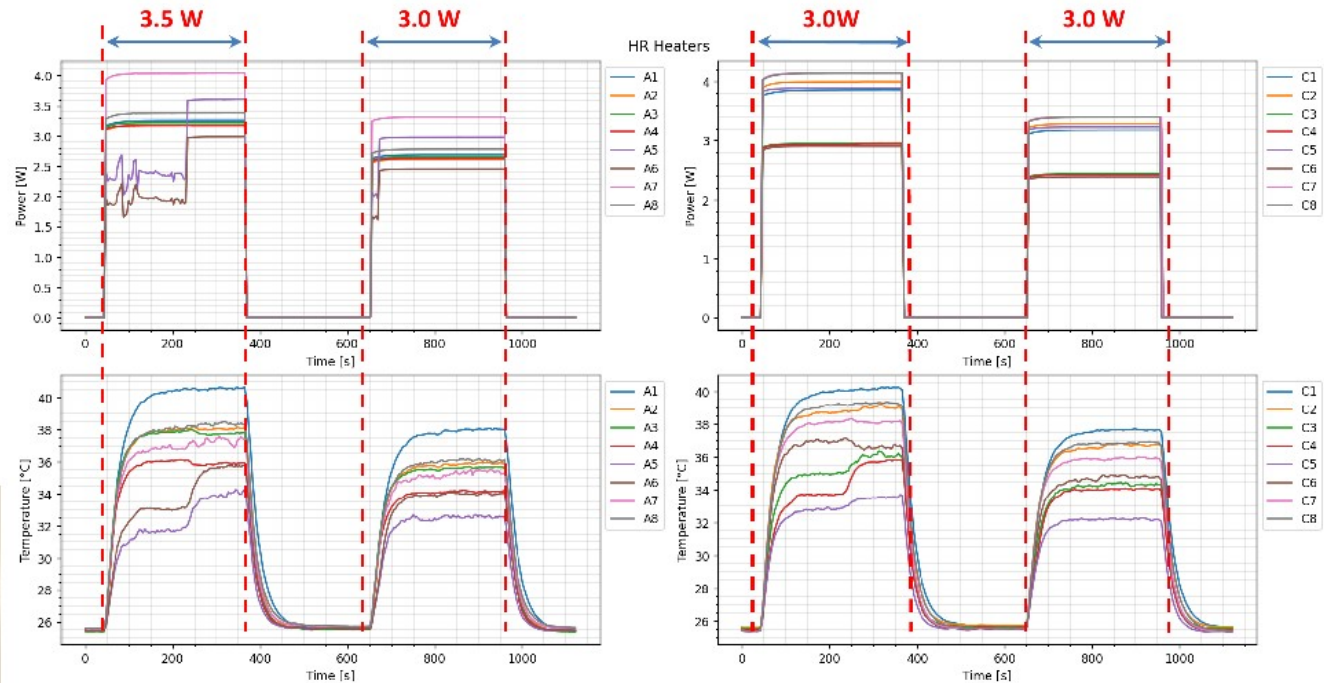
HR setup with active Fans



Measure air flow rate near to HR surface

Heaters with P>=3W	A7	A5	C1	C2	C5	C7	C8
Air velocity m/s	3.6	5.7	2.8	5.3	4.2	3.3	3.2

Air velocity ≥ 4 m/s is enough to maintain T



- Thermal Half Rings was tested with heaters under **avg 3W and 3.5W** with **active convection**.
- Air flow was vertical directed to HR, where was measured flow rate for **different points of HR by flow meter**.
- The avg heaters temperature are under **40°C**.

Zaza Chubinidze

<https://indico.cern.ch/event/1353986/contributions/5866686/attachments/2823320/4931112/LP%20mode%20testing%20for%20integration%20and%20LLS.pdf>

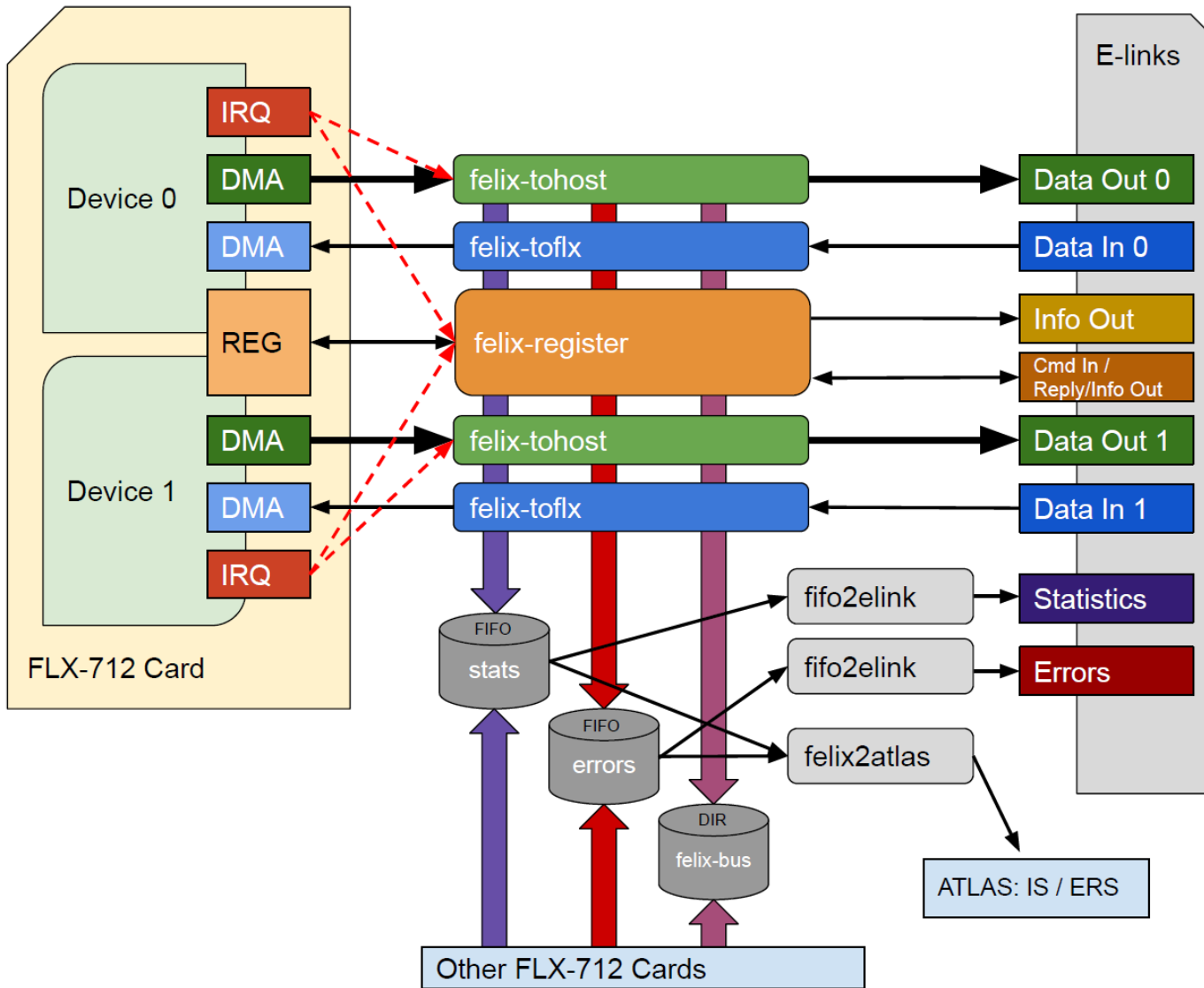
Summary

- Slice Test in SR1
 - crucial testing ground
 - Need to use the time to develop large scale system
 - Without it we will not be ready for integration
- Integration at SR1
 - installation/preparation progressing
 - Site readiness review in summer 2025
 - Will rely on DAQ and systems being ready
 - Need to ensure all functionality (low power, large scale views) available

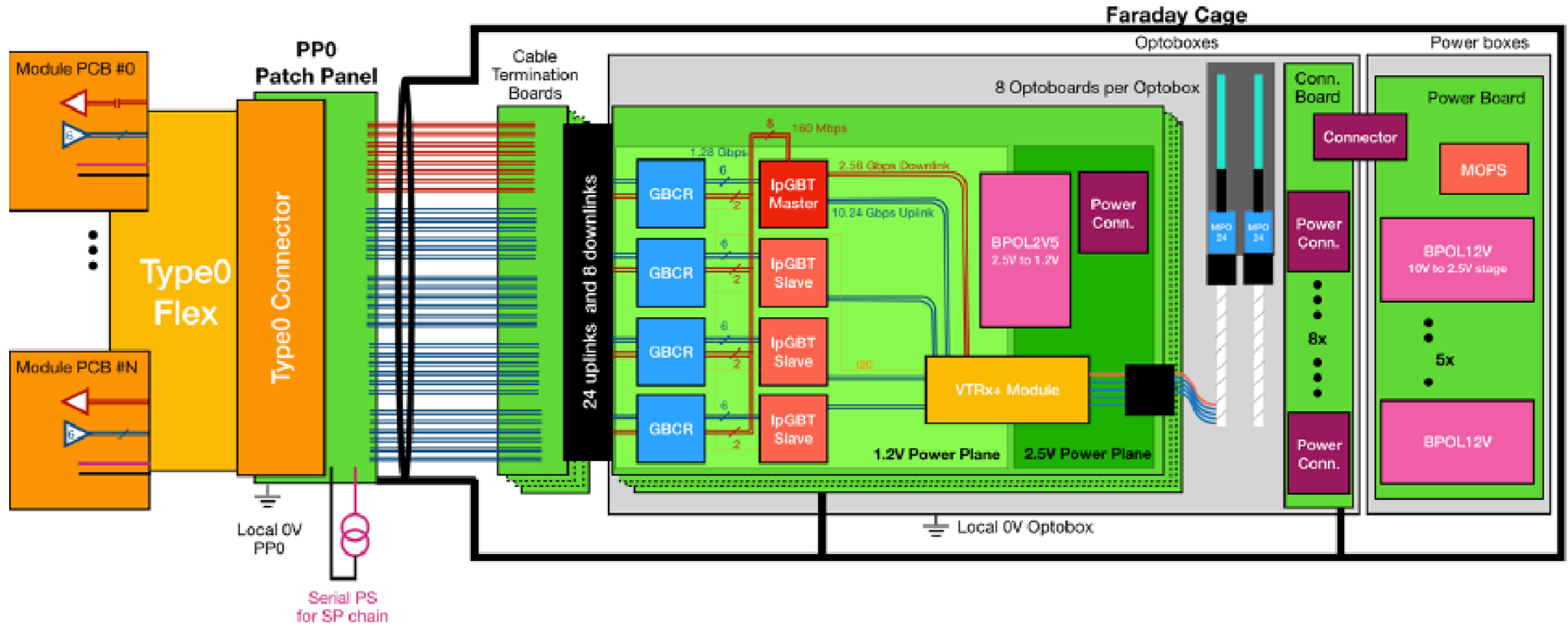
Bonus

Bonus Slides

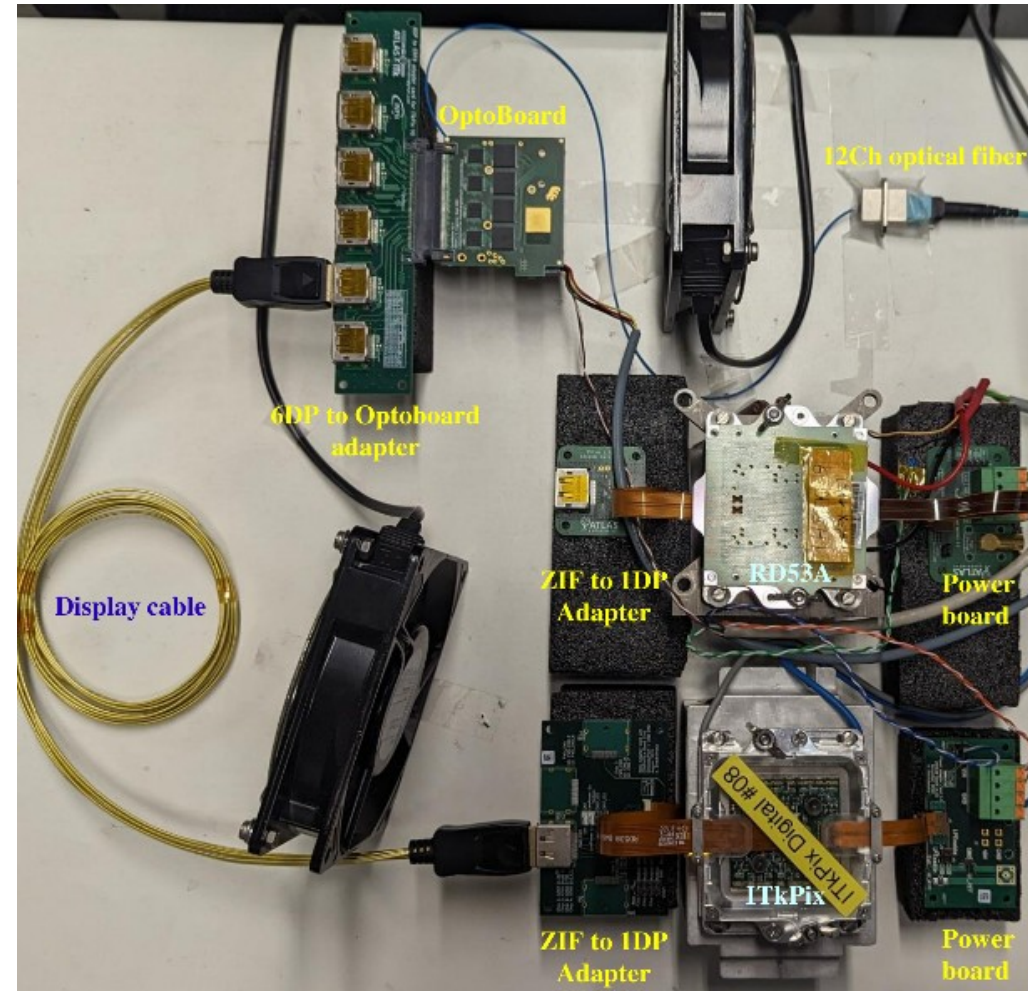
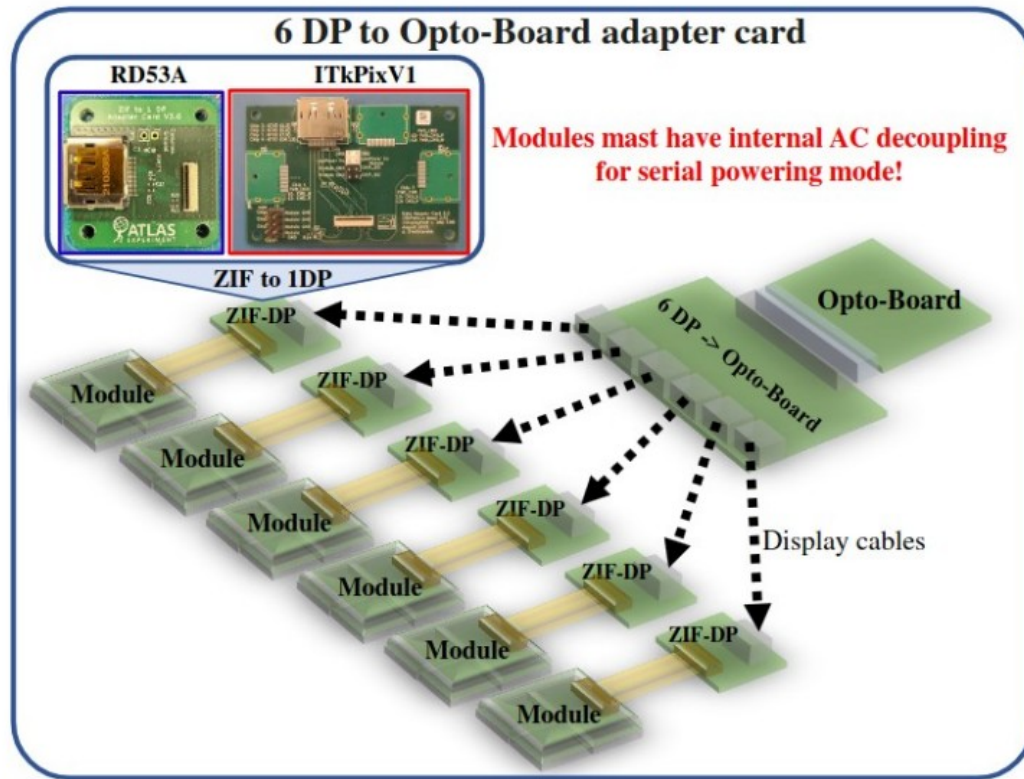
Summary



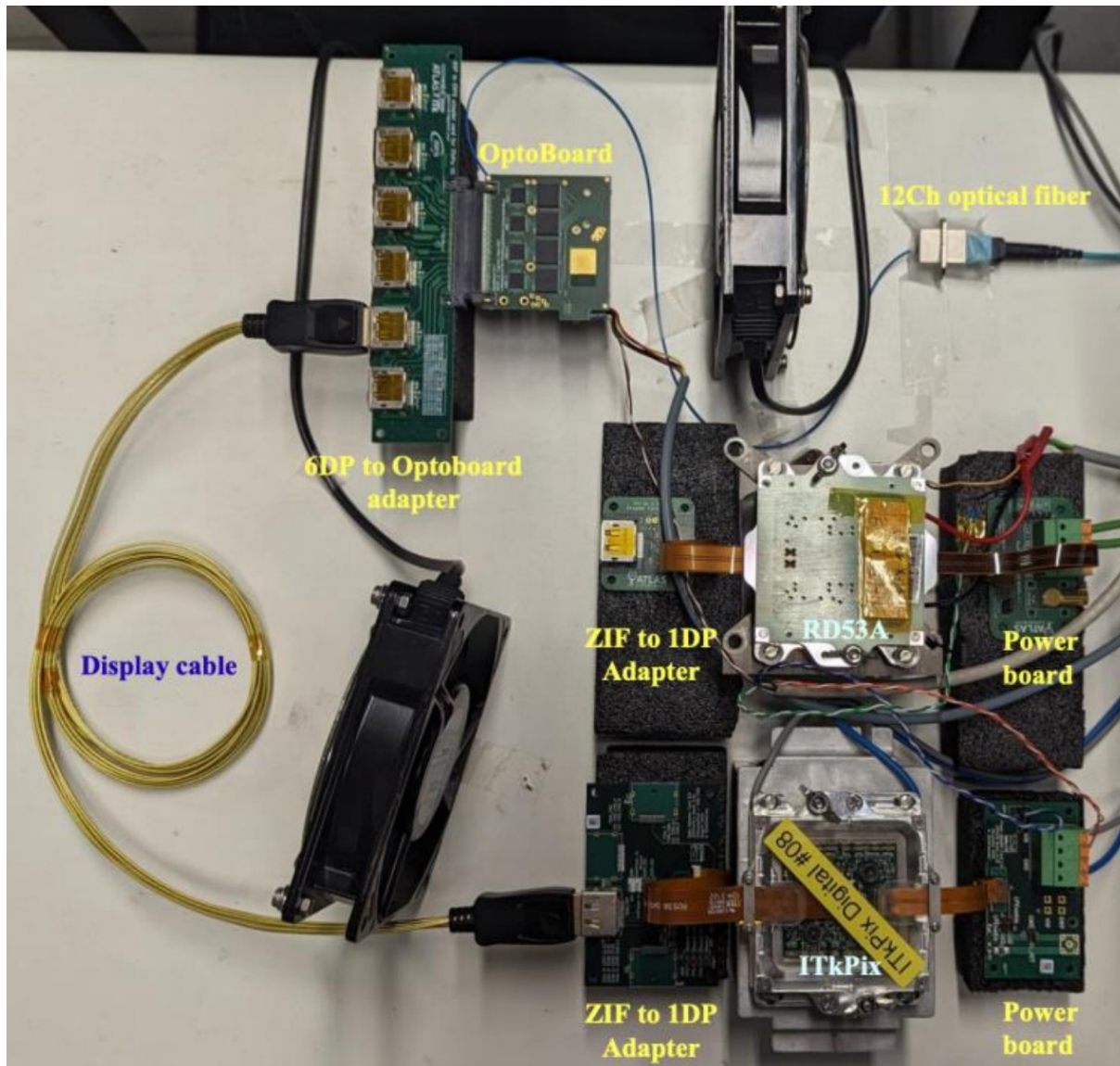
Provisions OptoBoards



Zazaboard to Optoboard



Summary



Summary

Felix-star (FW-trigger)

SCC v1.1

Quad v1.1

Scan time: 5.4 s
 Analysis: 701 ms
 Configuration: 2181 ms
 Processing: 0 ms

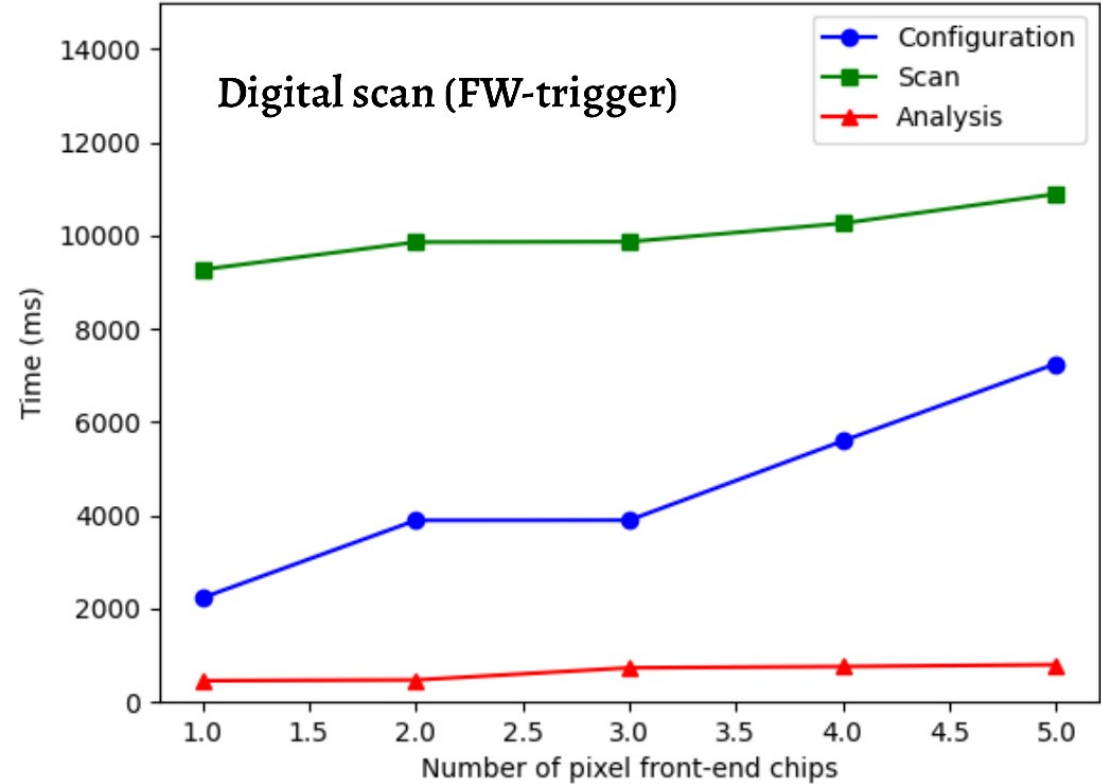
Scan time: 6.041 s
 Analysis: 718 ms
 Configuration: 7163 ms
 Processing: 0 ms

Scan time: 5.394 s
 Analysis: 565 ms
 Configuration: 2184 ms
 Processing: 0 ms

Scan time: 6.163 s
 Analysis: 754 ms
 Configuration: 7147 ms
 Processing: 0 ms

Scan time: 201.598 s
 Analysis: 820 ms
 Configuration: 2195 ms
 Processing: 0 ms

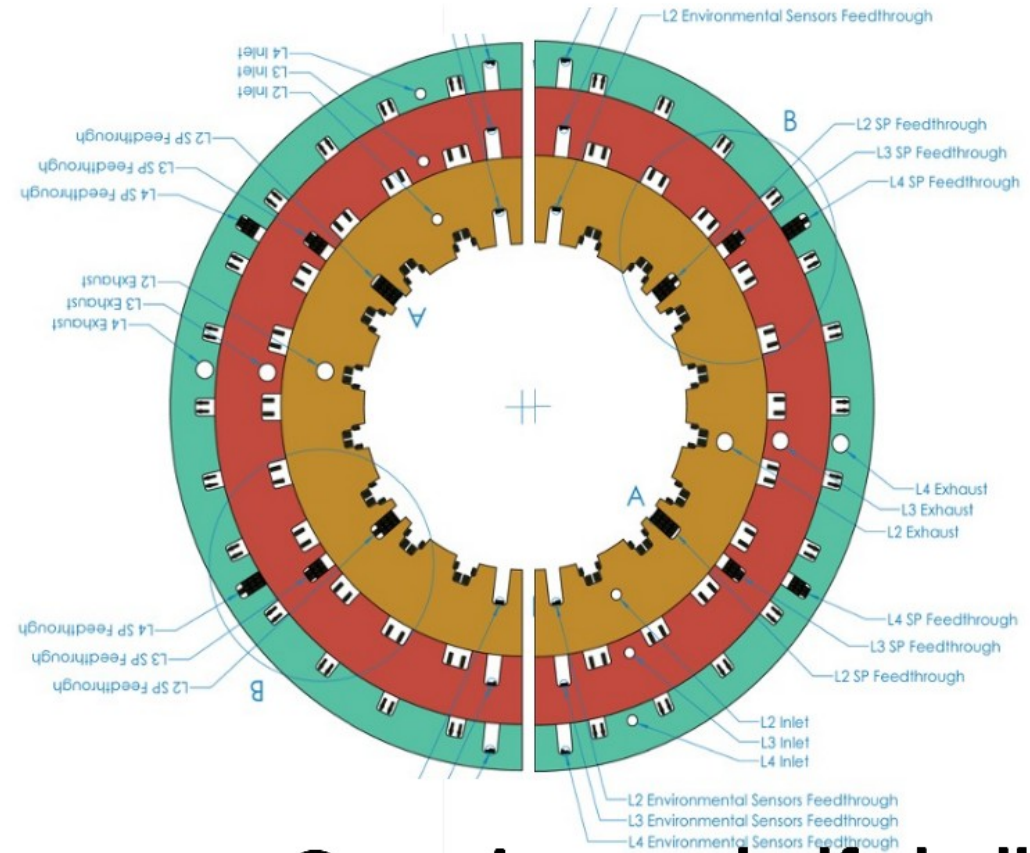
Scan time: 256.783 s
 Analysis: 823 ms
 Configuration: 7200 ms
 Processing: 0 ms



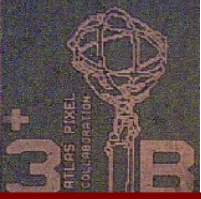
Summary

- **Grouping per half-shell and per layer**
- L2: 11, L3: 8, L4: 9 half-rings
- **Manifolding inside PP1:** exhausts and supplies of two half-shells combined in one cooling feed-through
- **Type-1 services exit per layer**

Testing steps	Detector section
Step 1,6	6 HR L2
Step 2,7	5 HR L2
Step 3,8	8 HR L3
Step 4,9	9 HR L4 / 2
Step 5,10	9 HR L4 / 2

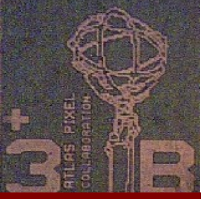


Susanne Kühn

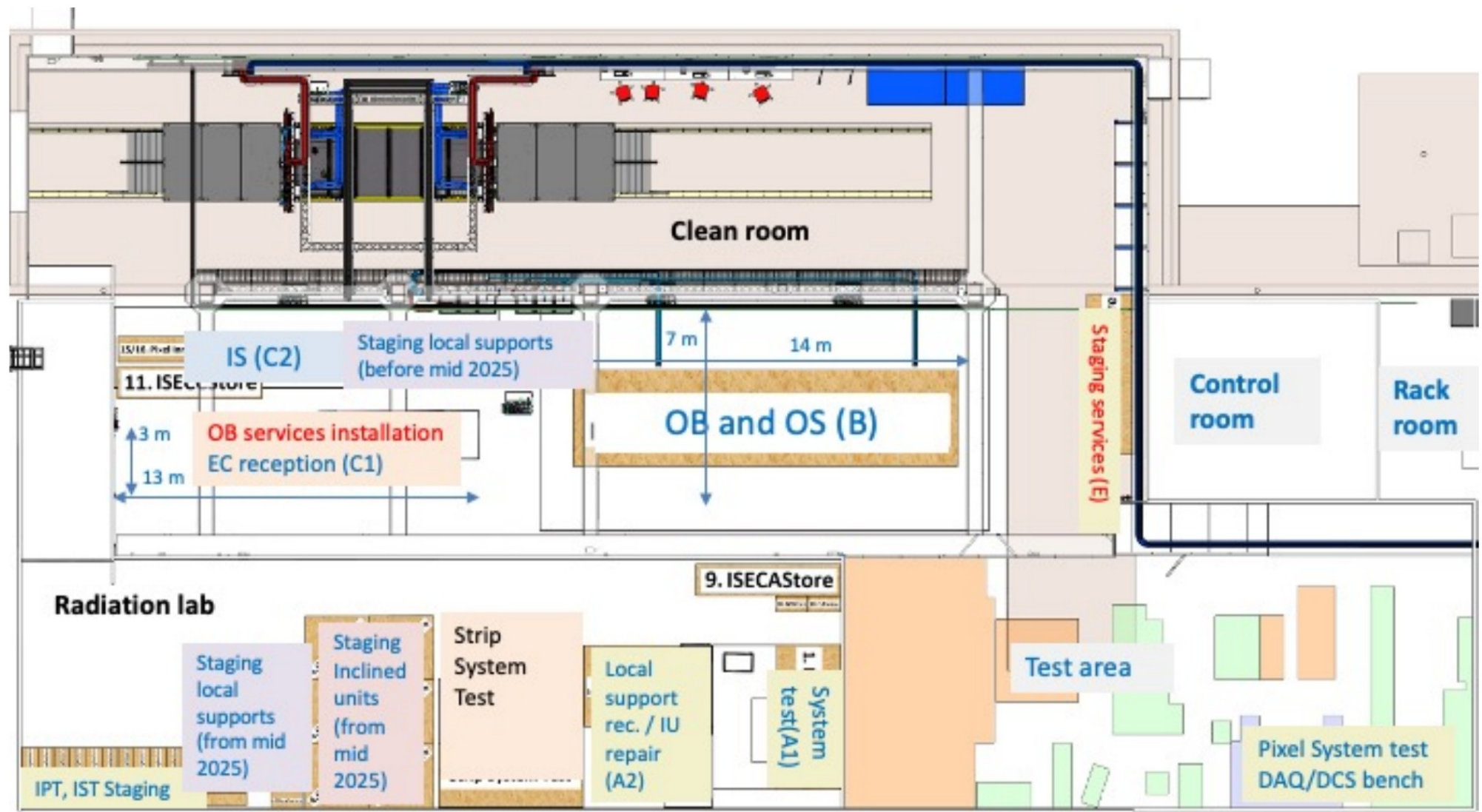


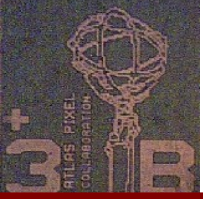
Summary

Test step	Detector Tested Section	Number of Serial Power Chains	Number Data (Up/Down) Links	Number of Modules
1/6	5 HR L2 (0.5 link/FE) left/right	10	160/80	80
2/7	6 HR L2 (1 link/FE) left/right	12	384/96	96
3/8	8 HR L3 (0.5 link/FE) left/right	16	352/176	176
4/9	4 HR L4 (0.25 link/FE) left/right	8	104/104	104
5/10	5 HR L4 (0.5 link/FE) left/right	10	182/130	130



SR1 Layout





A Side Step

A tool to easily manipulate module and chip configs in python:

```
python pixel-config-viewer/scripts/manipulate_config.py -h
```

```
usage: manipulate_config [-h] [-o OUTPUT_FILE] [-f {Y,YARR,I,ITK}] [-c {0,1,2,3} [{0,1,2,3} ...]] [-e CHIPSENBLED]
```

```
[-s {0,1,2,3,7}] [-l {0,1,2,3}] [--enableColumn CORECOLUMN] [--enableAllPix ALL_PIX]
```

```
[--enableColPix startCol endCol value] [--enableRowPix Col startRow endRow value]
```

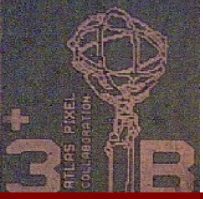
```
connectivity_file
```

Easy access, manipulation and conversion of pixel configs

Example:

```
python pixel-config-viewer/scripts/manipulate_config.py CONFIGS/L2_warm_YARR.json -o itktttest.json --enchips "1001"
```

<https://gitlab.cern.ch/akorn/pixel-config-viewer>



Summary