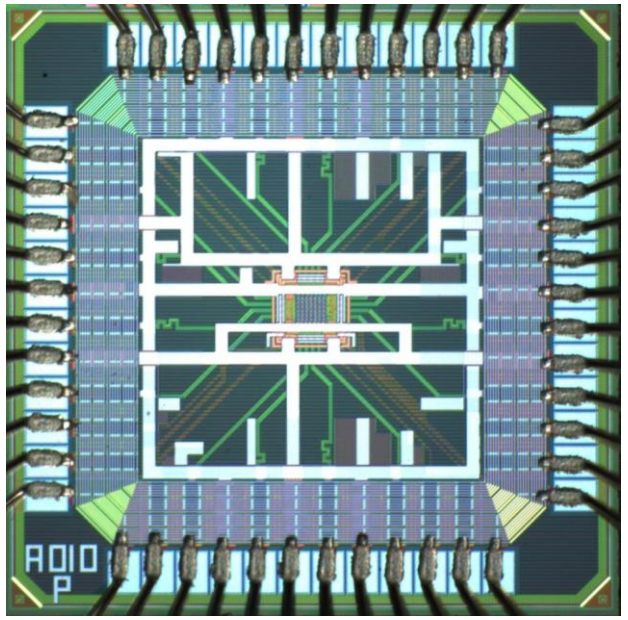
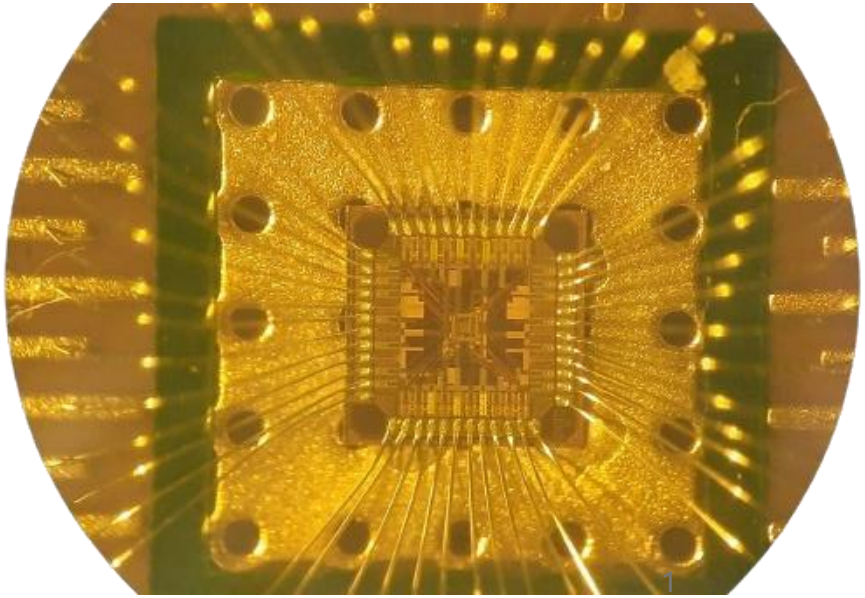


Status of the Analogue Pixel Test Structure characterization of Monolithic Sensors with Operational Amplifier



Angelo Colelli, Francesco Barile, Rajendra Patra,
Shyam Kumar, Triloki Triloki
University of Bari and INFN sez. Bari - Italy

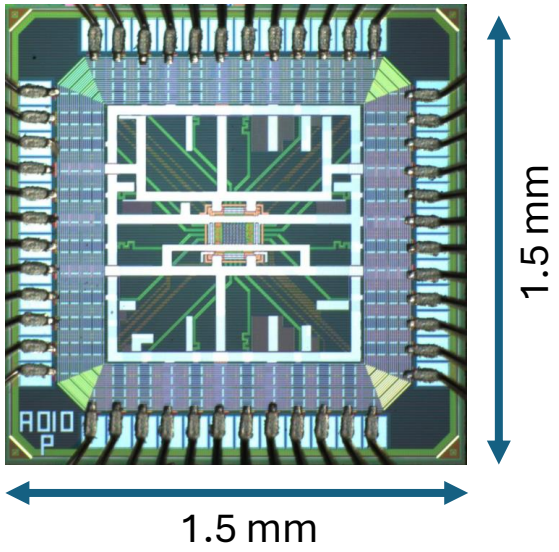
The Analogue Pixel Test Structure with Operational Amplifier

The APTS OpAmp is a prototype test structure based on TPSCo CMOS 65 nm ISC technology

Chip Characteristics:

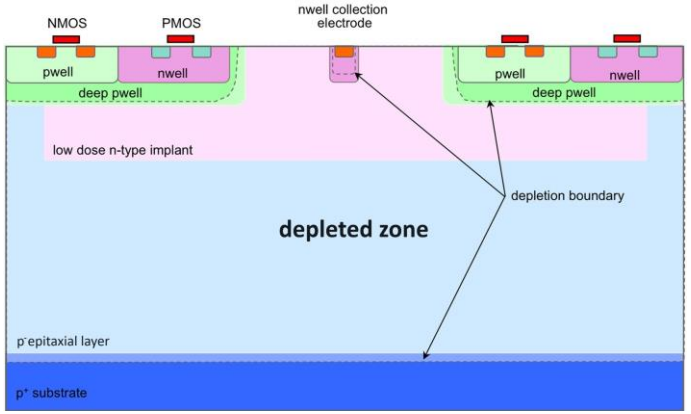
- **matrix sizes:** 6×6 pixels
- **pixel pitch:** 10, 15, 20, 25 µm
- **Output drivers**: **Op**erational **Amp**lifier
- **Readout**: direct analogue of the 4x4 central submatrix[1]
- **Coupling**: DC/AC
- **Biasing**: 0 ÷ -5V (DC) - 0 ÷ 50V (AC)

[1]The others 20 are dummy pixels allowing to minimize the distorsion of the electric field.



Modified with gap pixel designs:

- A gap of 2.5 µm has been created at the pixel boundaries.
- Reduction of the charge sharing among neighbouring pixels is expected due to an enhanced lateral electric field



Biasing scheme: AC and DC chips

Reverse sensor bias:

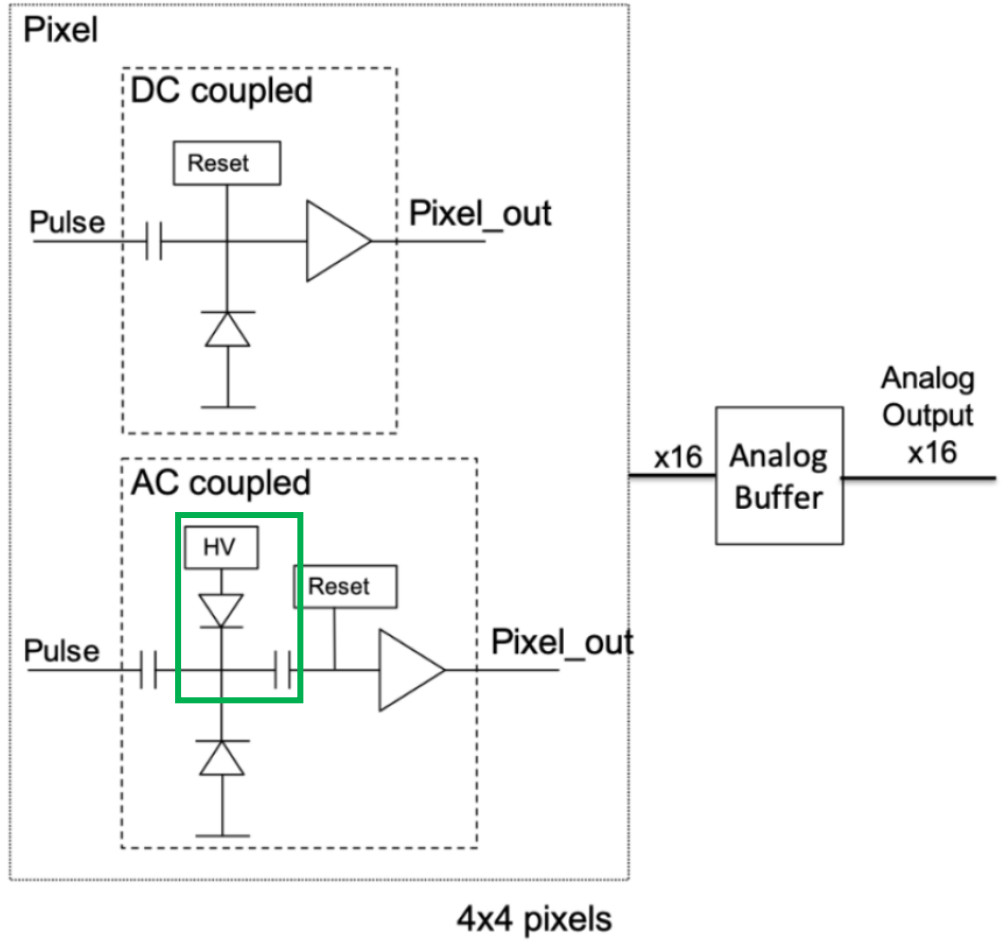
- a negative bias voltage on the p-type substrate in DC
- a positive bias voltage on the n-well collection electrode in AC

In the DC coupling:

- the sensing node or collection electrode remains directly connected to the gate of the input transistor

In the AC coupling:

- the sensing node voltage cannot be withstood by transistors, therefore a capacitor is introduced between the sensing node and the gate of the input transistor



https://espace.cern.ch/ep-project-rnd-tpsco65/Shared%20Documents/MLR1/Datasheets/APTS_Datasheet_v1.8.pdf

https://iopscience.iop.org/article/10.1088/1748-0221/18/01/C01065

Experimental Setup

Power supply

Rohde&Schwarz HAMEG HMP4040

DAQ

MLR1 DAQ board (FPGA-based):

- Powering and biasing the chip.
- Hosting the ADCs that sample the 16 pixels at 4 MSa/s.

0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

Proximity and carried card:

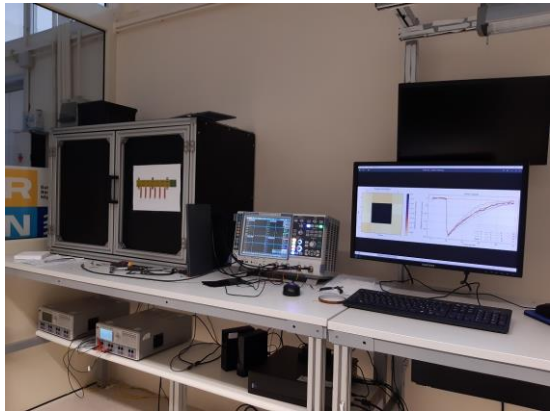
- Designed specifically for each chip flavour

Oscilloscope

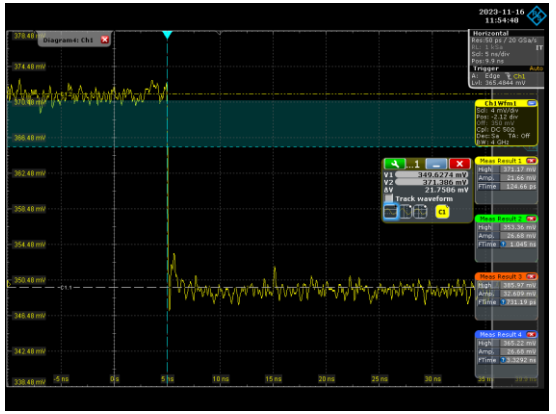
0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

Rohde & Schwarz RTO 1044

- Bandwidth: 4 GHz
- Sampling Rate: 20 GSa/s



Lab @ University of Bari and INFN



Waveform at 20 GSa/s. Time window 50 ns

Laboratory Activities

- The chips testing is performed as follow:

- Data Analysis:

AC – DC coupling chip comparison
searching for the best chip configuration

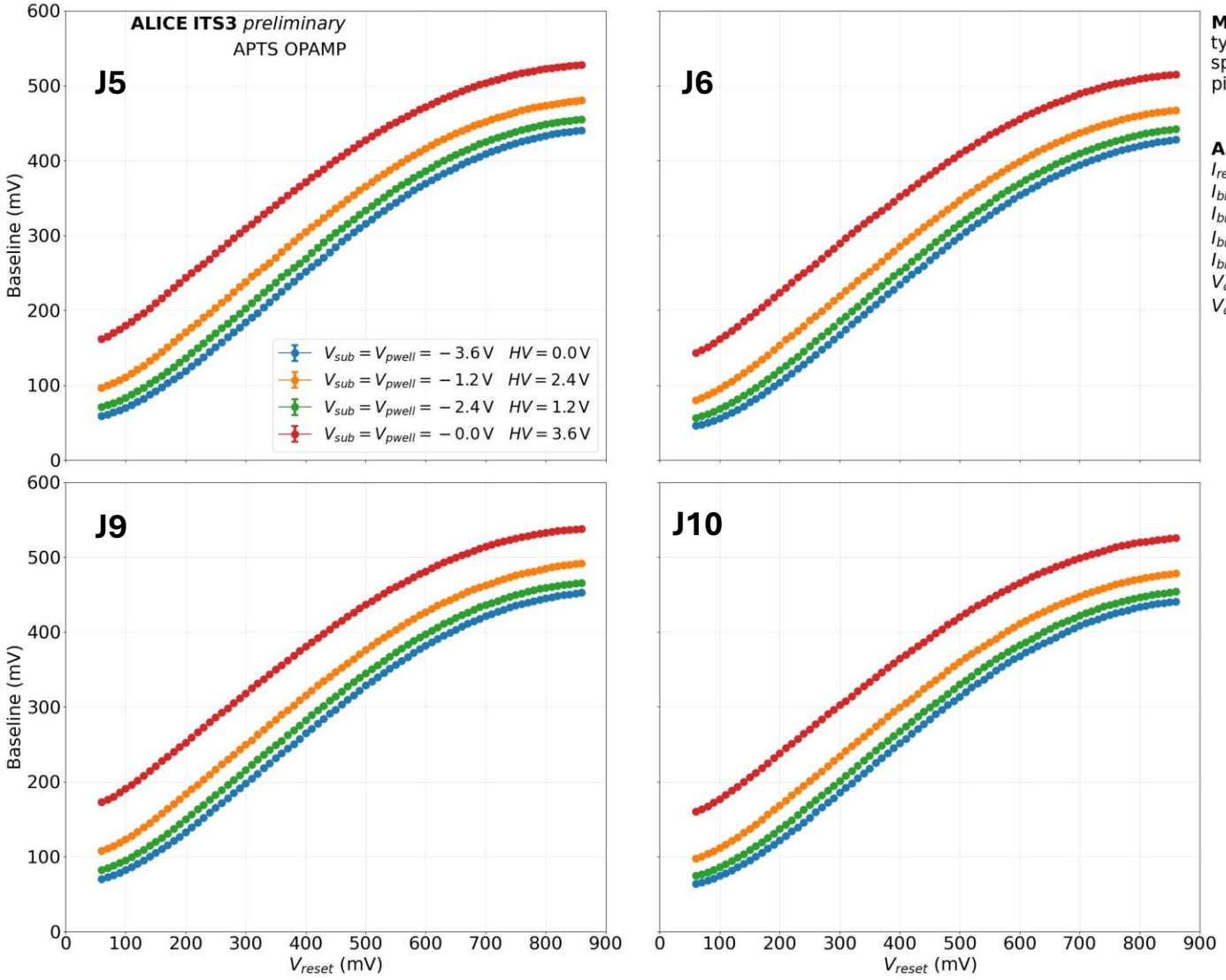
AC – DC chips Configuration

- Different bias configurations have been investigated:

	HV (V)	V_{sub} (-V)	V_{pwell} (-V)
AC	0	3.6	3.6
	1.2	2.4	2.4
	2.4	1.2	1.2
	0	0	3.6
DC		3.6	3.6

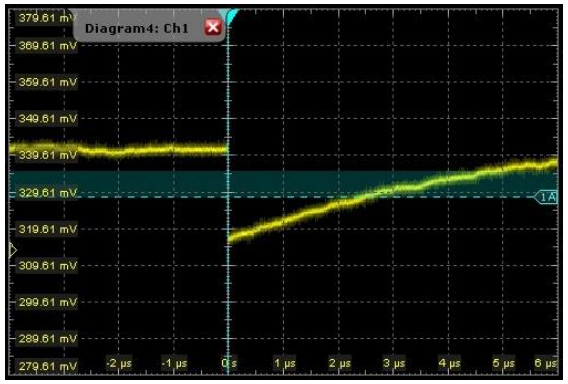
- For each of them baseline, derivative, amplitude, falltime and slope have been calculated
  - Number of trigger = 100

Baseline for AC chip



MLR1
type: modified with gap
split: 4
pitch: 10 µm

APTS OA
I_{reset} = 100 pA
I_{biasn} = 125 µA
I_{biasp} = 10.0 µA
I_{bias4} = 2600 µA
I_{bias3} = 200 µA
V_{casp} = 270 mV
V_{casn} = 900 mV



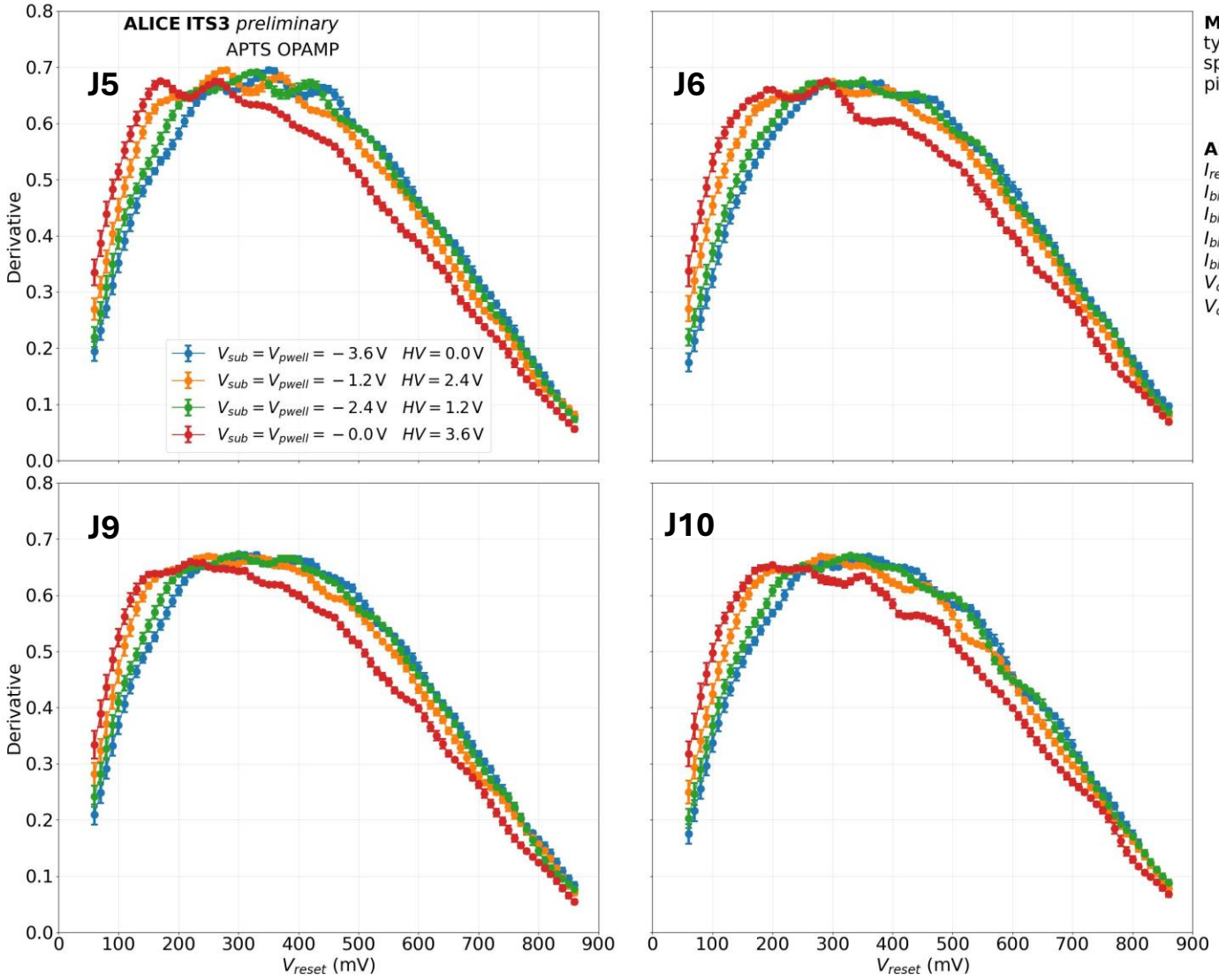
0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

- Signal variation w.r.t. Reset Voltage, $\boldsymbol{V_{reset}}$

V_{reset} restores the collection electrode to the baseline voltage

The higher the bias (HV)
the higher the baseline

Derivative for AC chip



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$V_{casp} = 270$ mV
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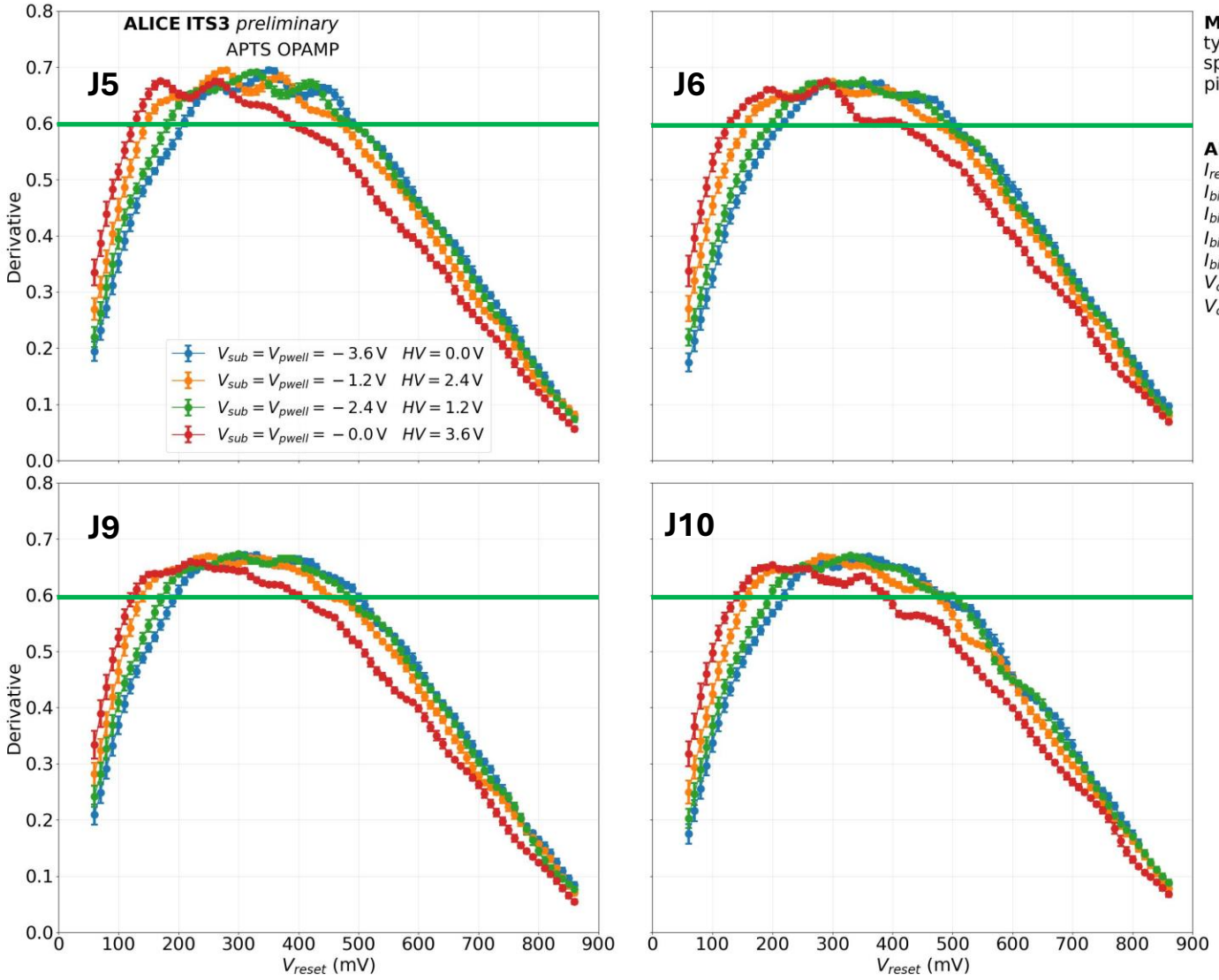
0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

- The Derivarive is defined as: $\Delta Baseline/\Delta V_{reset}$

Derivative for AC chip



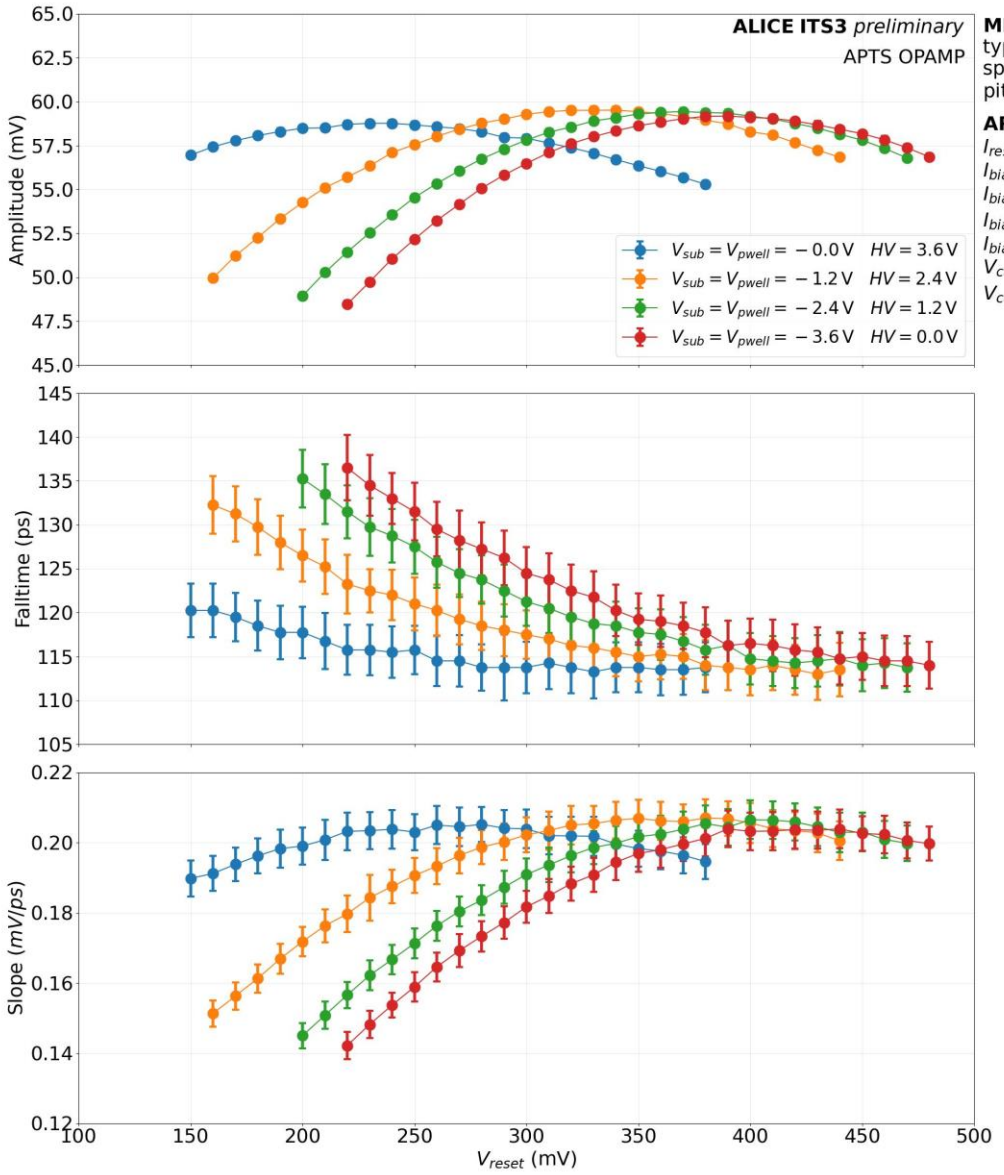
MLR1
type: modified with gap
split: 4
pitch: 10 µm

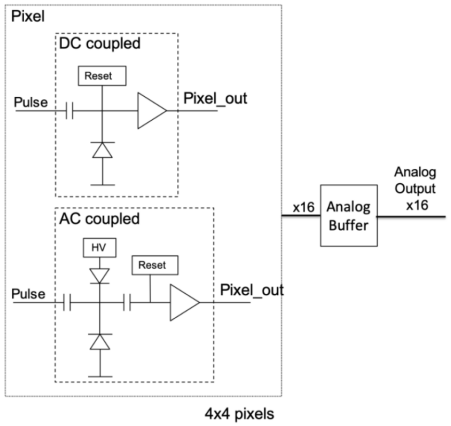
APTS OA
$I_{reset} = 100$ pA
$I_{biasn} = 125$ µA
$I_{biasp} = 10.0$ µA
$I_{bias4} = 2600$ µA
$I_{bias3} = 200$ µA
$V_{casp} = 270$ mV
$V_{casn} = 900$ mV

0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

- The Derivarive is defined as: $\Delta Baseline/\Delta V_{reset}$
- Stable values for Derivative greater than 0.6 represent the best circuitry response.

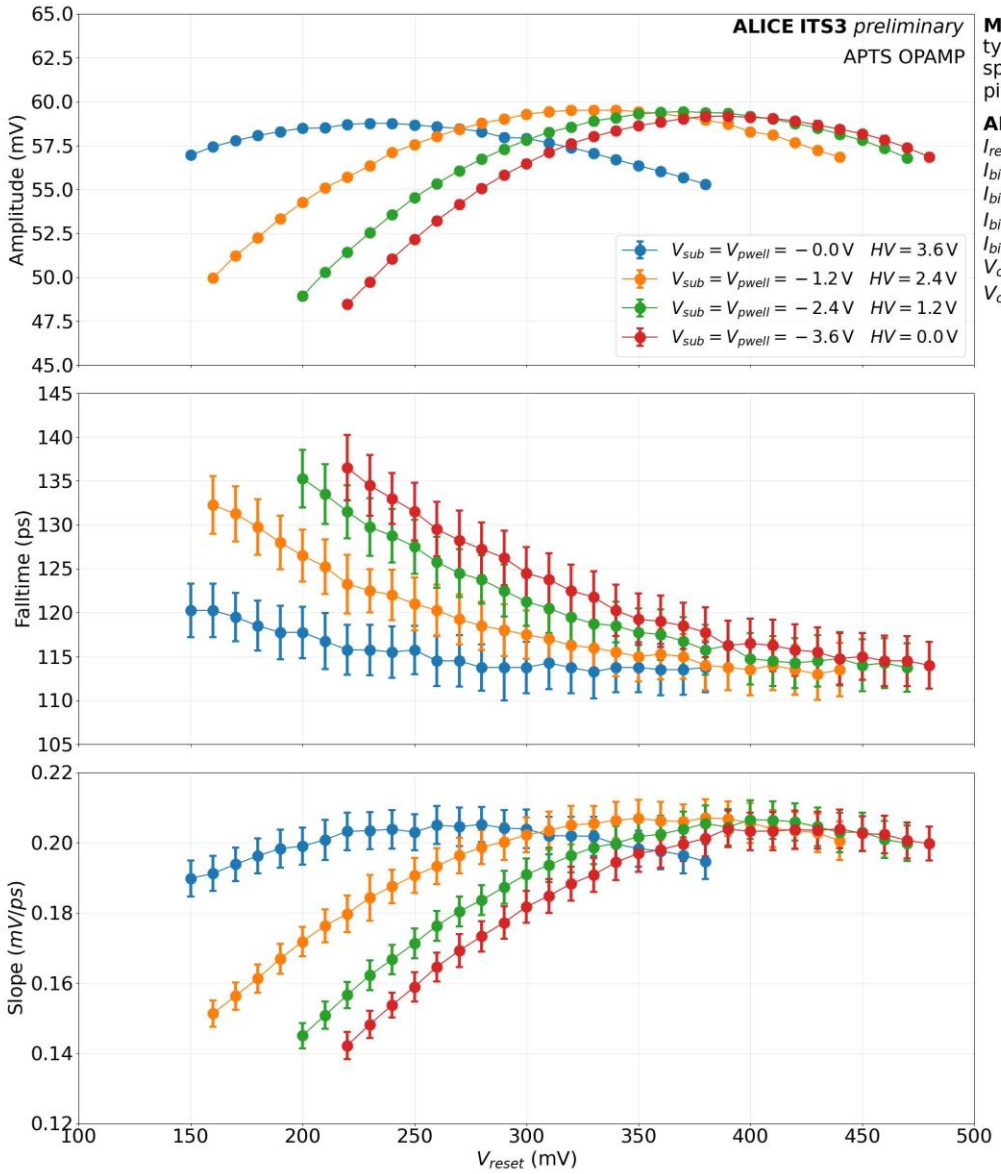
Amplitude, Falltime and Slope for AC

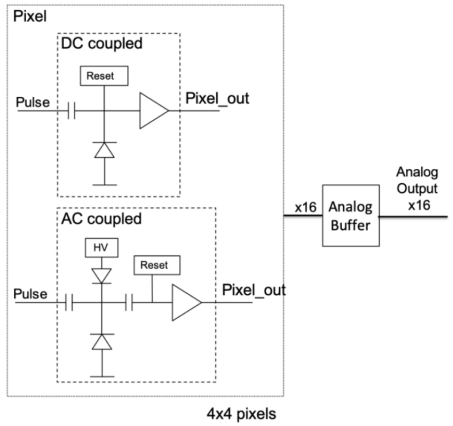




- Pulsing by electronic charge injection into the circuitry to simulate diode data collection.
- The Slope is defined as: $0.4 * Amplitude/Ftime$

Amplitude, Falltime and Slope for AC





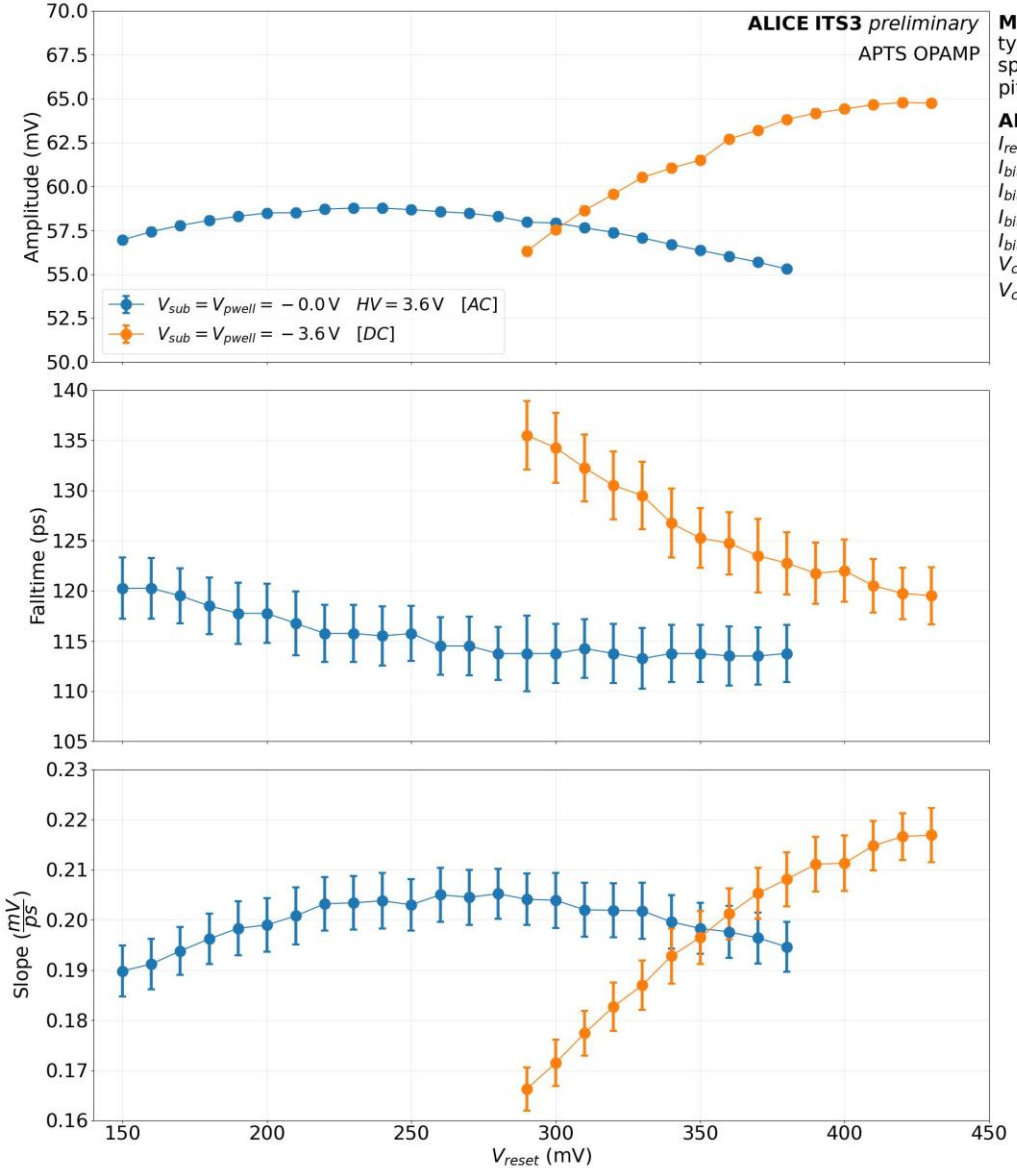
- Pulsing by electronic charge injection into the circuitry to simulate diode data collection.
- The Slope is defined as: $0.4 * Amplitude/Ftime$

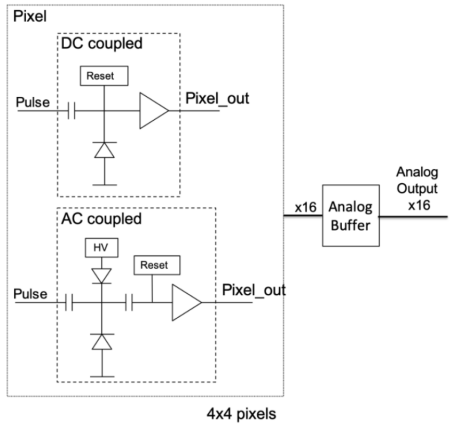
The configuration:

HV = 3.6V and $V_{sub} = V_{pwell} = 0.0$ V

- more stable form the point of view of the Slope
- it has the lowest falltime values.

Amplitude, Falltime and Slope AC - DC comp.





- Pulsing by electronic charge injection into the circuitry to simulate diode data collection.
- The Slope is defined as: $0.4 * Amplitude/Ftime$

The configuration:

HV = 3.6V and $V_{sub} = V_{pwell} = 0.0$ V

- more stable form the point of view of the Slope
- it has the lowest falltime values.

w.r.t. the DC coupled chip at the same bias

Summary

- Best configuration in terms of low falltime and stable slope for the AC coupled chip for :

$$HV = 3.6V \text{ and } V_{sub} = V_{pwell} = 0.0\ V$$

- Start data taking with ^{55}Fe using the previous bias configuration

Backup

AC – DC chips Configuration

- Different bias configurations have been investigated:

	HV (V)	V_{sub} (-V)	V_{pwell} (-V)
AC	0	1.2	1.2
	1.2	0	0
DC		1.2	1.2

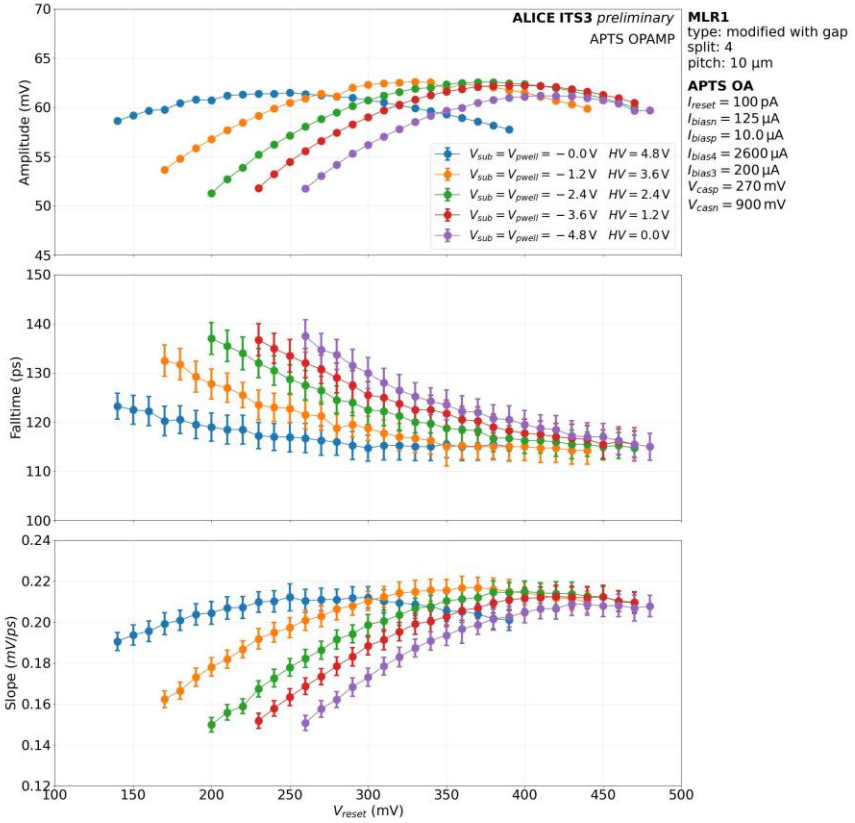
	HV (V)	V_{sub} (-V)	V_{pwell} (-V)
AC	0	2.4	2.4
	1.2	1.2	1.2
	0	2.4	2.4
DC		2.4	2.4

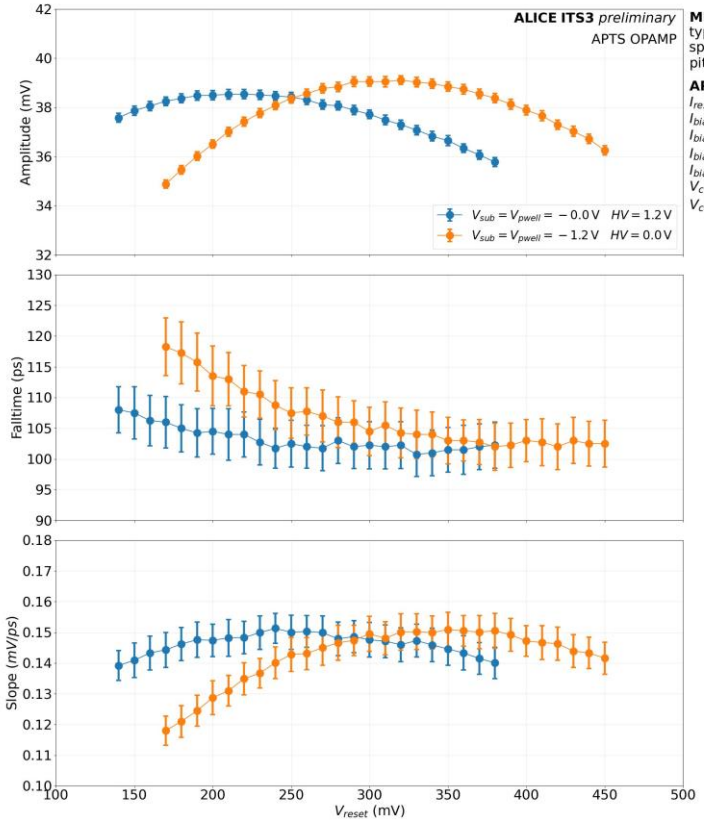
	HV (V)	V_{sub} (-V)	V_{pwell} (-V)
AC	0	3.6	3.6
	1.2	2.4	2.4
	2.4	1.2	1.2
	0	0	3.6
DC		3.6	3.6

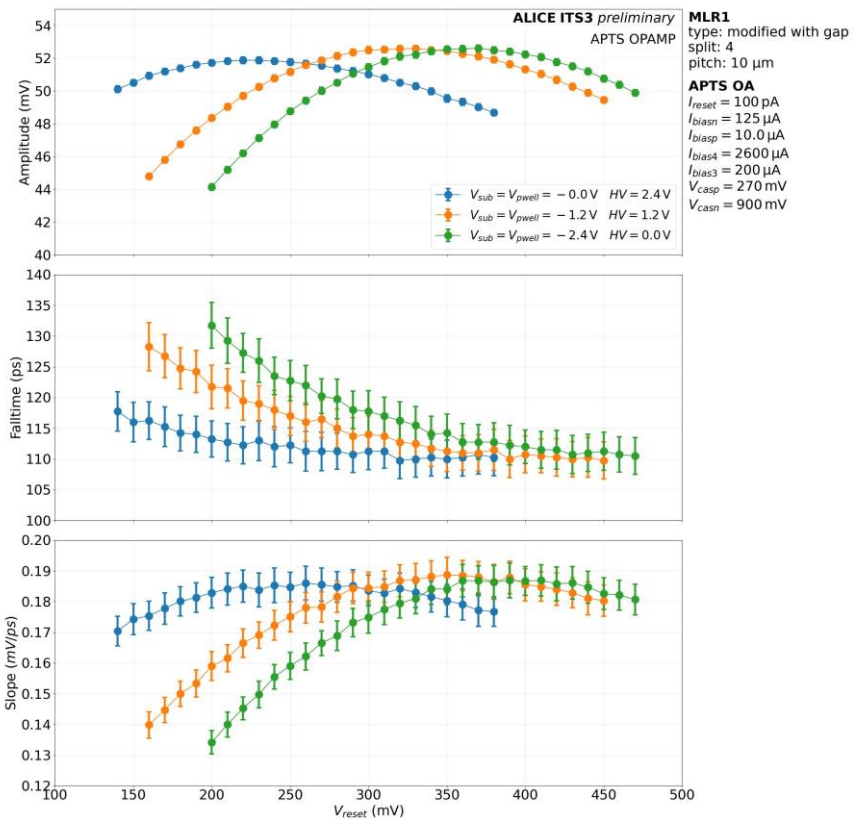
	HV (V)	V_{sub} (-V)	V_{pwell} (-V)
AC	0	4.8	4.8
	1.2	3.6	3.6
	2.4	2.4	2.4
	1.2	3.6	3.6
	4.8	0	0
DC		4.8	4.8

Number of trigger = 100

Amplitude, Falltime and Slope for AC

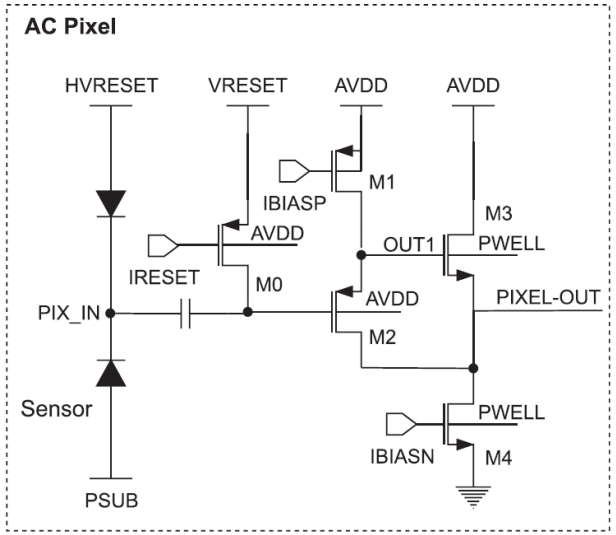


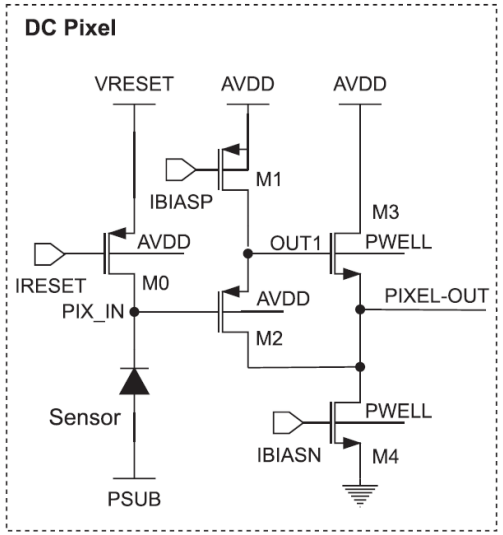


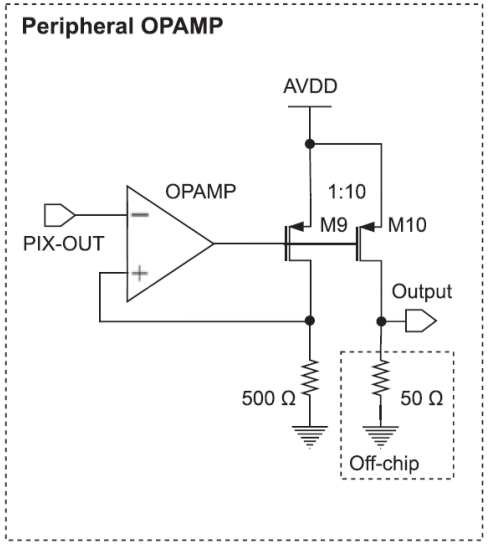


The Analogue Pixel Test Structure with Operational Amplifier

Readout chain:







- **AC coupling:**
  - A capacitor is introduced between the sensing node and input transistor gate.
  - The sensing node is reset via a diode.
  - Substrate tied to the ground.
- **DC coupling:**
  - The sensing node is directly connected to the input transistor gate.
  - The sensing node is reset by a PMOS transistor.
  - A negative bias is applied to the substrate and to the bulk of NMOS transistors.

Operational Amplifier (OpAmp):
maximize speed capability to characterize charge collection time in the sub-nanosecond range.