dRICH SiPM bias distribution

Roberto Preghenella
INFN Bologna

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preghenella@bo.infn.it

Bias distribution

Topics of interest

- Topology of the Bias distribution
  - a diagram/schematic illustrating the approach
- Granularity of the Bias supplies
  - how many SiPMs (or groupings of) are to be fed from a single Bias supply channel?
- Bias Channel counts and need for distribution chassis
- Temperature dependencies
  - Bias compensation, measurement and compensation, etc.
- Bias supply/gain stability and noise requirements
- Configuration controls with reference to SiPM serial numbers

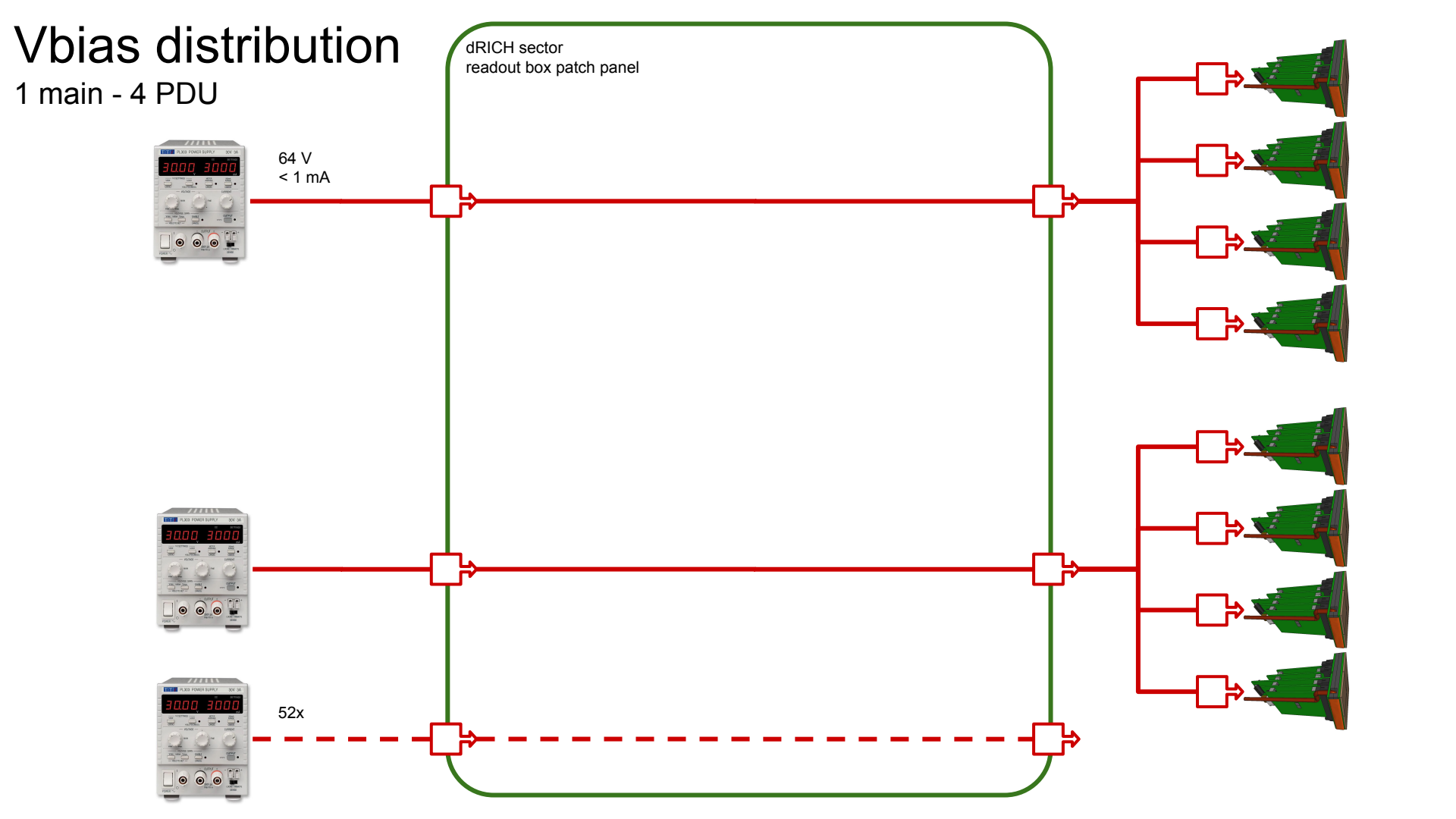
dRICH bias voltage distribution

bias voltage to SiPM sensors
we have two bias voltages to distribute to SiPM

- **HIGH VOLTAGE (Vbias)**
  - this is the normal operation mode for Physics
  - reverse bias to SiPM
  - < 55 V
  - < 1 μA / sensor
- **ANNEALING VOLTAGE (Vann)**
  - when doing annealing recovery of radiation damage
  - forward bias to SiPM
  - < 12 V
  - < 150 mA / sensor

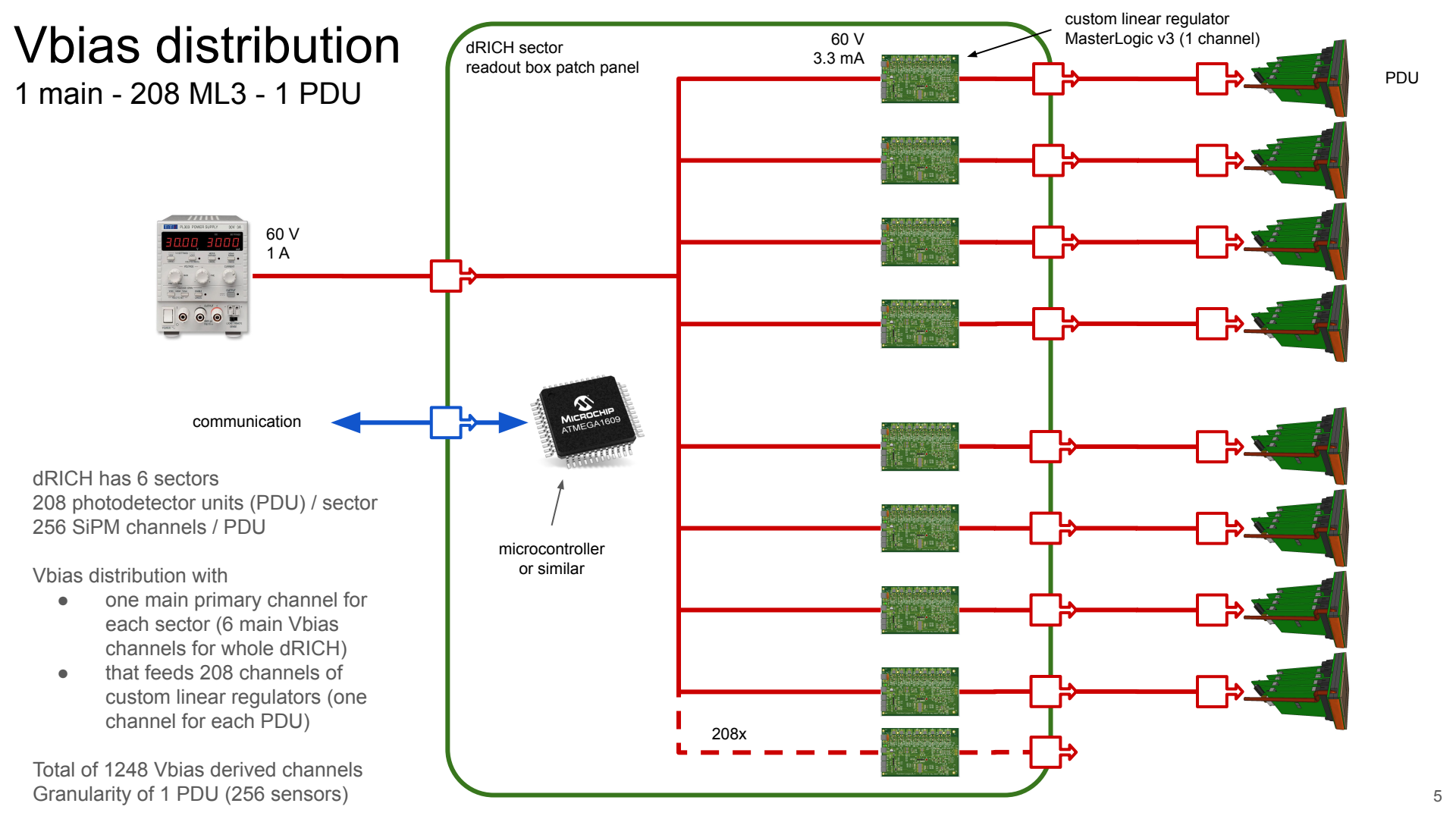
Vbias distribution

1 main - 4 PDU



Vbias distribution

1 main - 208 ML3 - 1 PDU



dRICH has 6 sectors
208 photodetector units (PDU) / sector
256 SiPM channels / PDU

Vbias distribution with

- one main primary channel for each sector (6 main Vbias channels for whole dRICH)
- that feeds 208 channels of custom linear regulators (one channel for each PDU)

Total of 1248 Vbias derived channels
Granularity of 1 PDU (256 sensors)

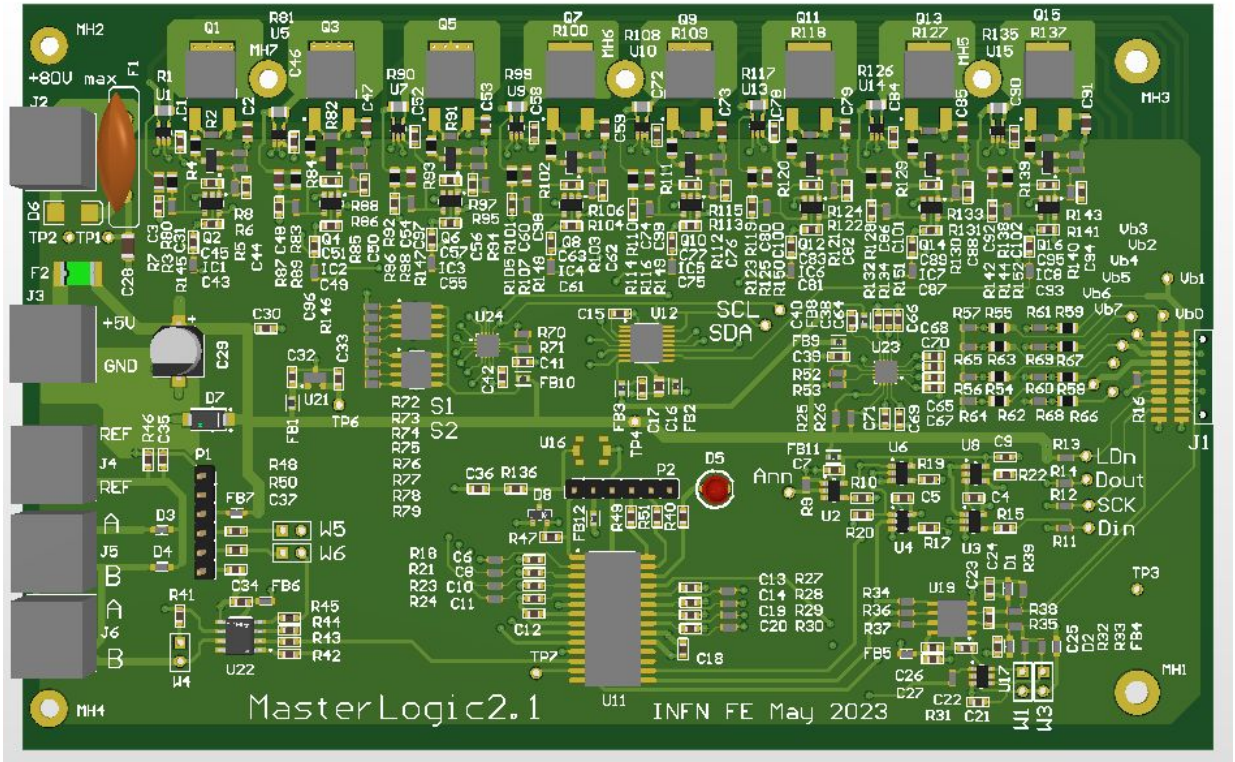
The Masterlogic v2

we developed and operated in the dRICH beam test in October 2023 the MasterLogic v2 card (evolution of the MasterLogic v1 card).

the card hosts

- 8 channels made of identical circuits for linear regulation of Vbias from 0 to Vin (80 V max)
- a microcontroller (PIC) for external communication (RS485)
- voltage & current monitor

the MasterLogic v2 card hosts more features that are needed for beam test operations. Some of them will be delegated to the RDO, other might be included or dropped.



The Masterlogic v3 and the patch panel

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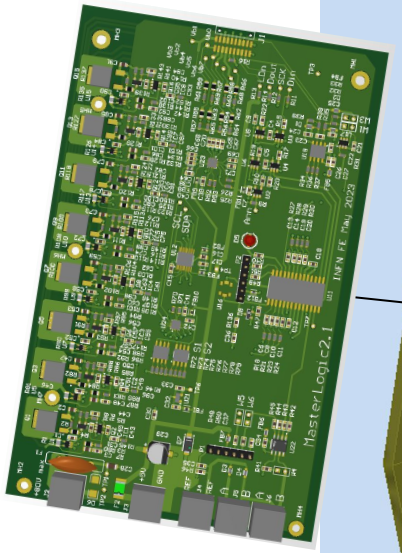
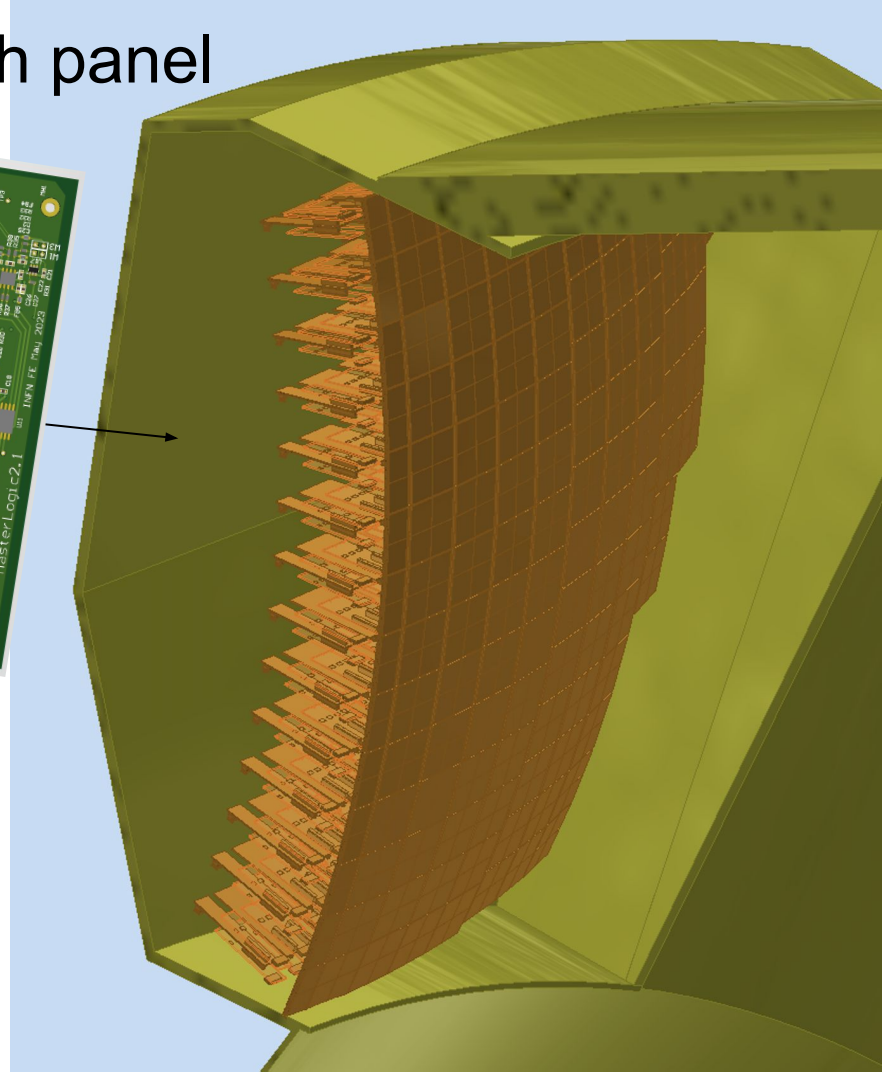
- 8 channels made of identical circuits for linear regulation of Vbias from 0 to Vin (80 V max)
- a microcontroller (PIC) for external communication (RS485)
- current monitor?
- something else?

the MasterLogic v2 card hosts more features that are needed for beam test operations. Some of them will be delegated to the RDO, other might be included or dropped.

a future evolution might be a MasterLogic v3 card to plug onto the dRICH readout box patch panel for Vbias and Vann control and distribution (and perhaps more features).



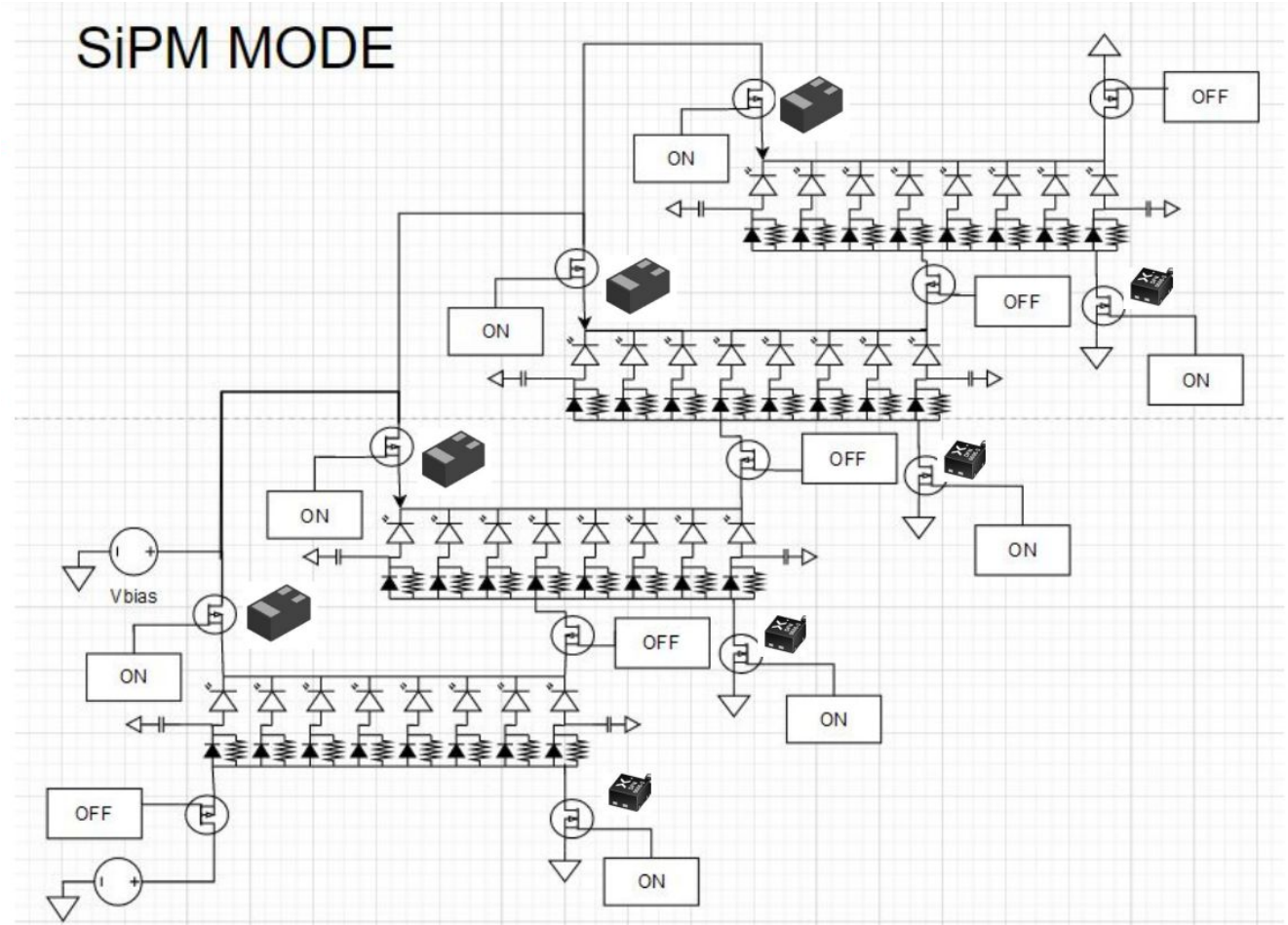


Vbias distribution

summary table

	**1 main 1 PDU**	 **1 main 4 PDU**	**1 main 52 ML3 4 PDU**	**1 main 208 ML3 4 PDU**
$N_{primary}$	1248	312	6	6
$N_{primary}$ / sector	208	52	1	1
$V_{primary}$ (V)	60	60	60	60
$I_{primary}$ (A)	< 1 mA	< 1 mA	250 mA	1
Granularity	256	1024	1024	256
uController	no	no	yes	yes

Vbias distribution



the circuit foreseen to allow both normal operation of SiPM (reverse bias) and self-annealing (forward bias) allows to inhibit the Vbias to a granularity of 8 SiPM.

might come at handy in case of troubles with Vbias distribution in a specific SiPM → inhibit Vbias in a string of 8 SiPM sensors while the rest of the PDU can still be operated

digital switches (MOSFET) controlled by RDO

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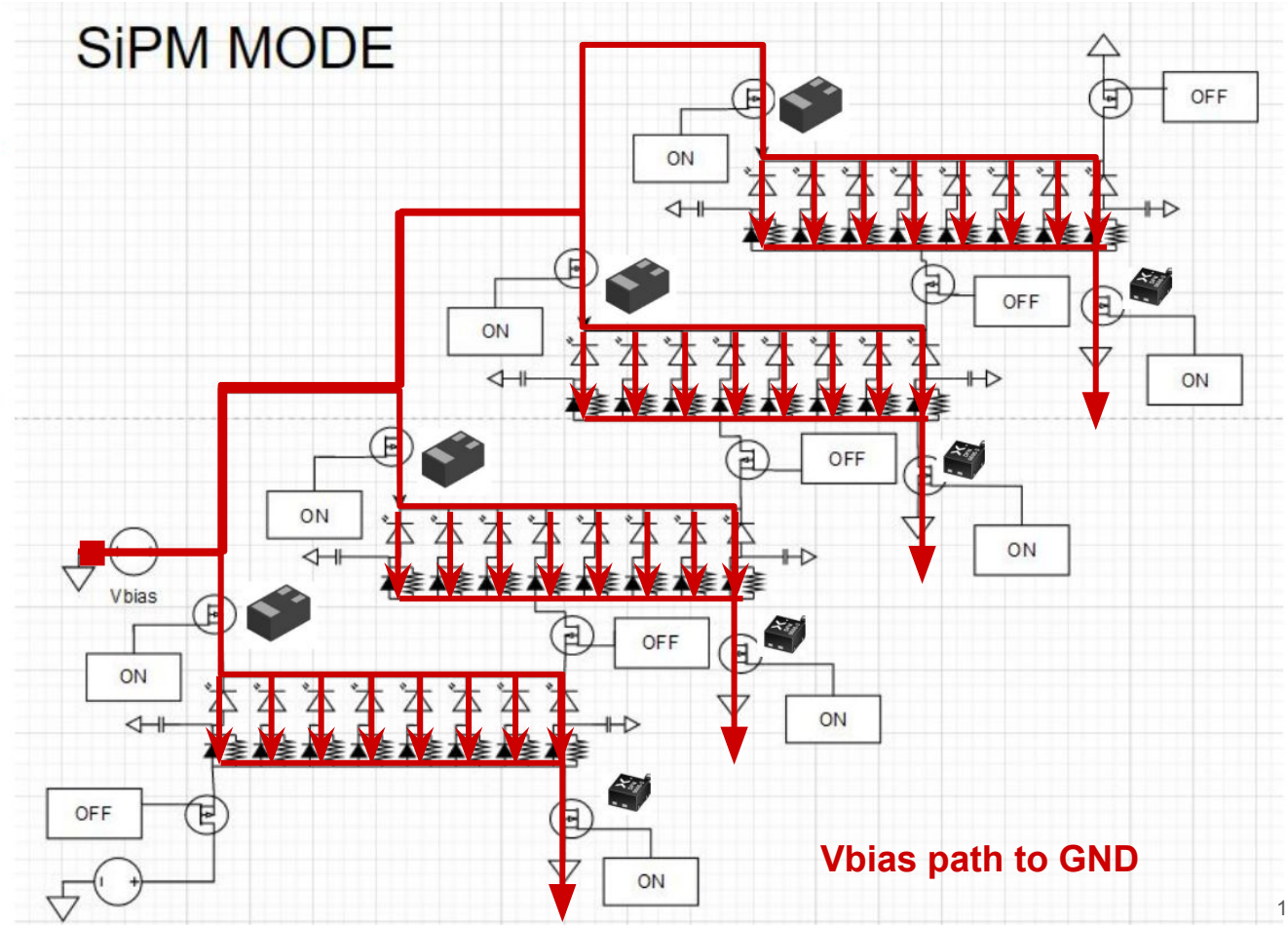

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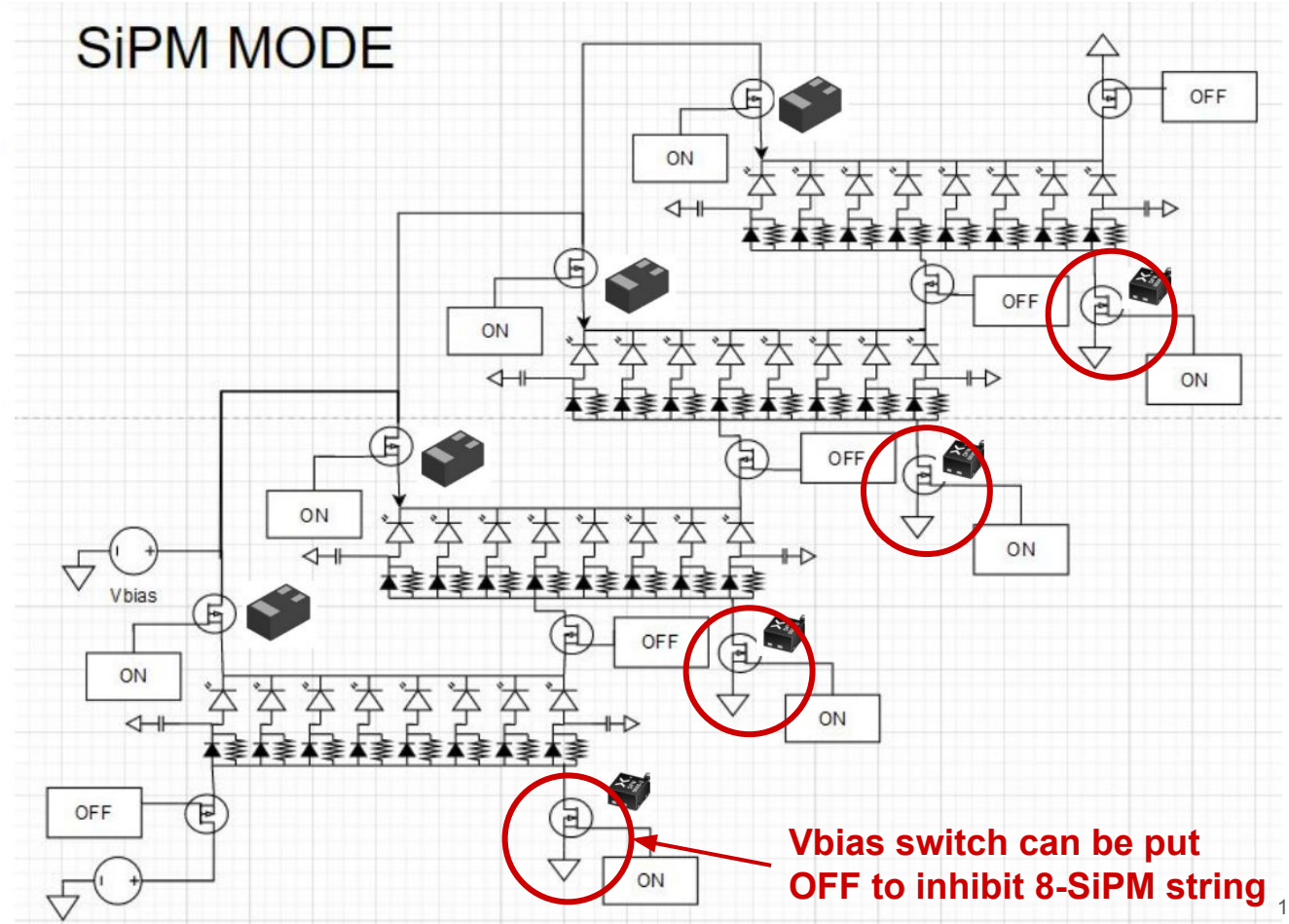


Vann distribution

1 main - 4 drivers - 1 PDU

48 V
8 A

Vann distribution with

- 52 main primary channels for each sector (total 6 sectors)
- each channel feeds 4 octal channel drivers to select which portions of the 4 PDUs will undergo annealing
- typically one full PDU at a time

52x

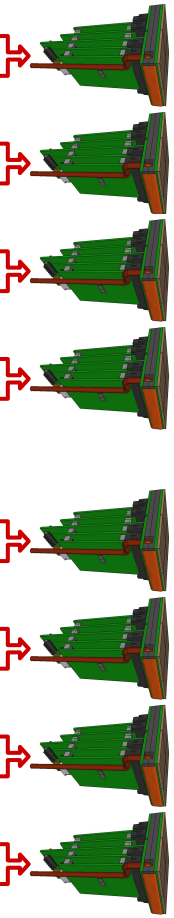
dRICH sector
readout box patch panel

microcontroller
or similar

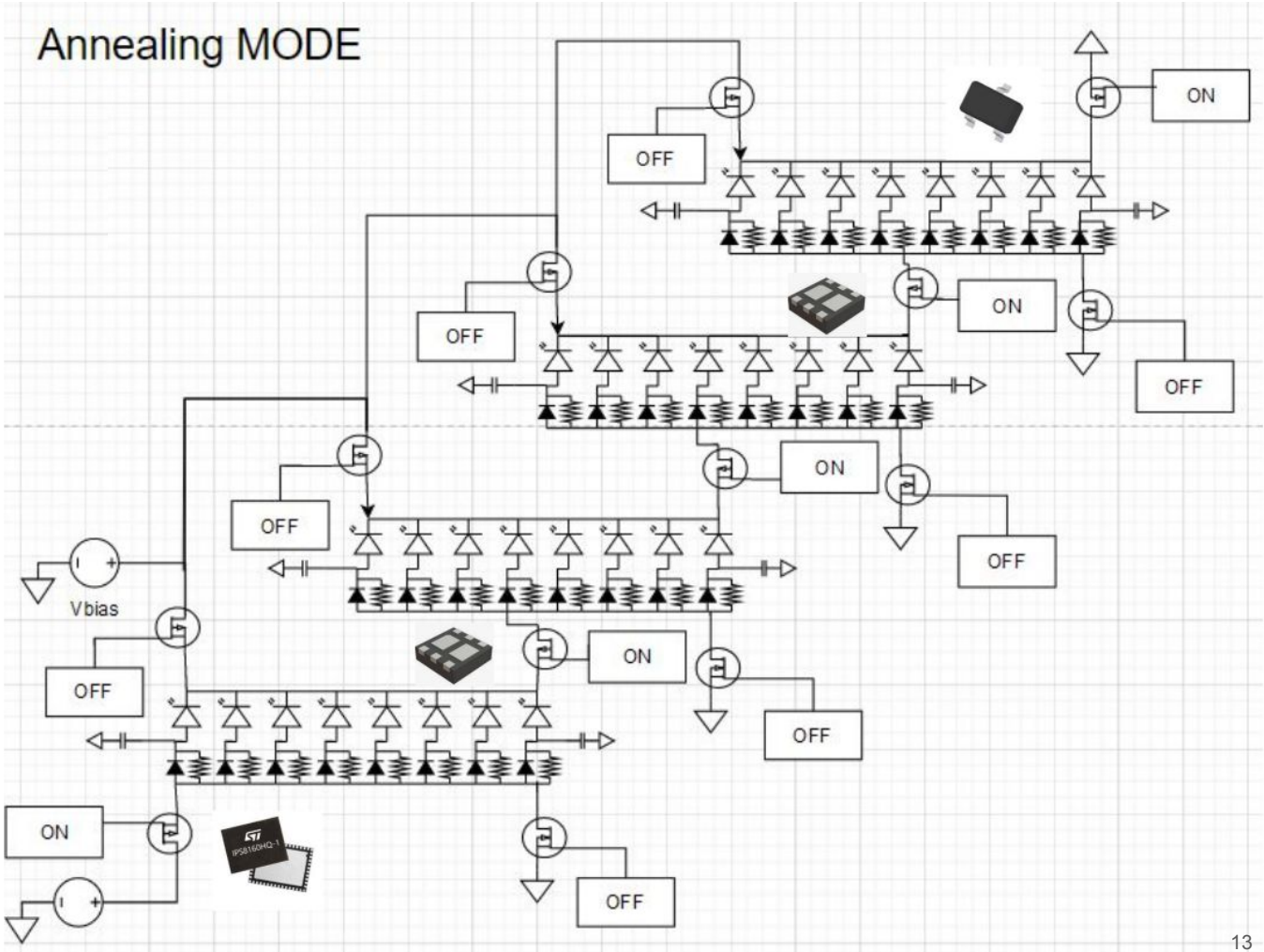
8x channel annealing driver

208x

PDU



Vann distribution



forward-bias annealing current for each sensor can reach up to 100 mA
to keep annealing current low we foresee to forward-bias the SiPM in series of 4 SiPM strings

note: this approach should work but has to be tested to prove its performance

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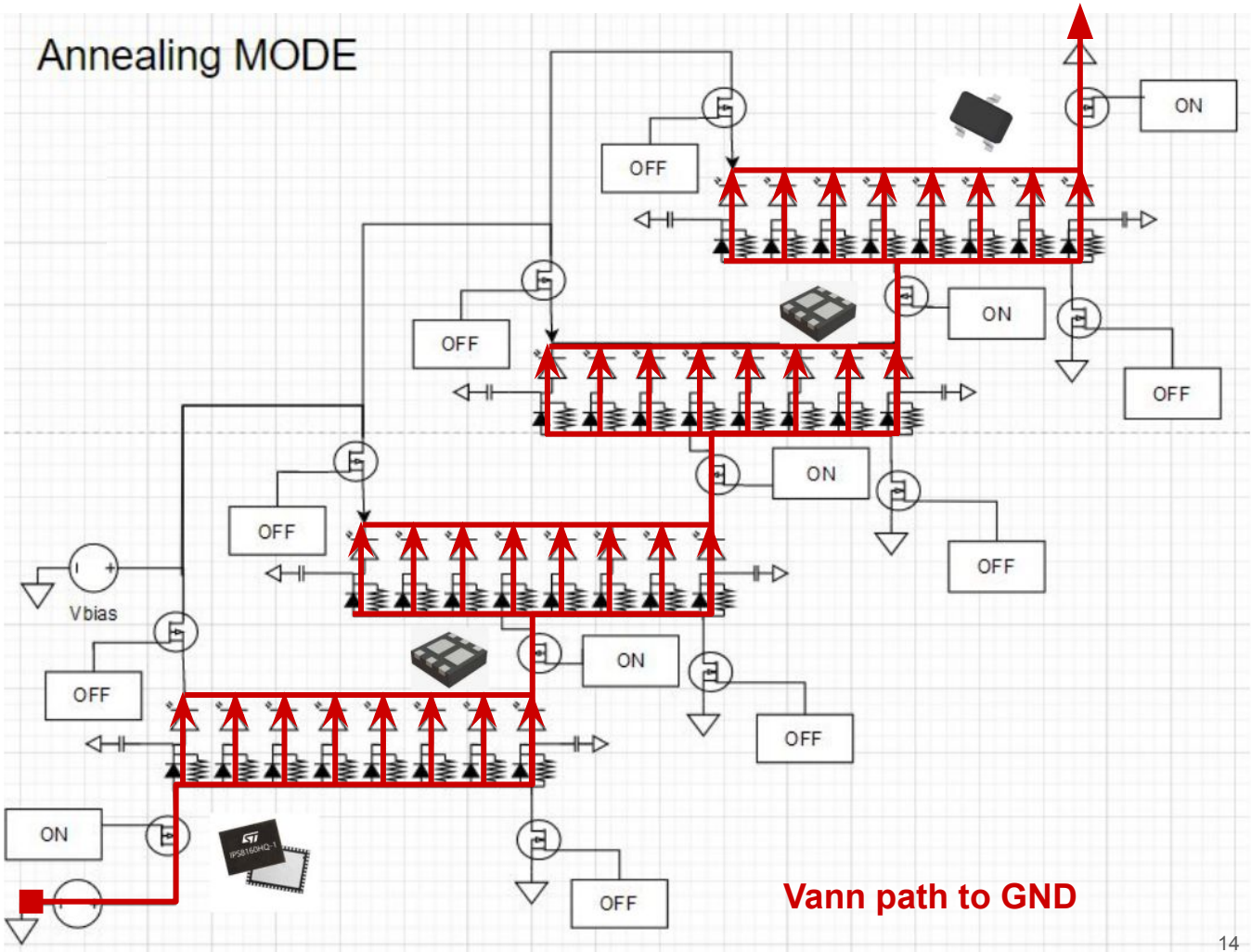


Summary

	Vbias	Vann
$N_{primary}$	6 / 312	312
$N_{primary}$ / sector	1 / 52	52
$V_{primary}$	60 V	48 V
$I_{primary}$	1 A / 1 mA	8 A
analog grouping voltage regulation	256 / 1024	1024
digital grouping capability to turn OFF	8	32
T dependence	yes measured and regulated	no
stability	< 20 mV	< 100 mA
noise ripple	< 3 mVpp	not critical

PDU voltage services

the **SiPM grouping** is composed of 4 strings of 8 SiPM each

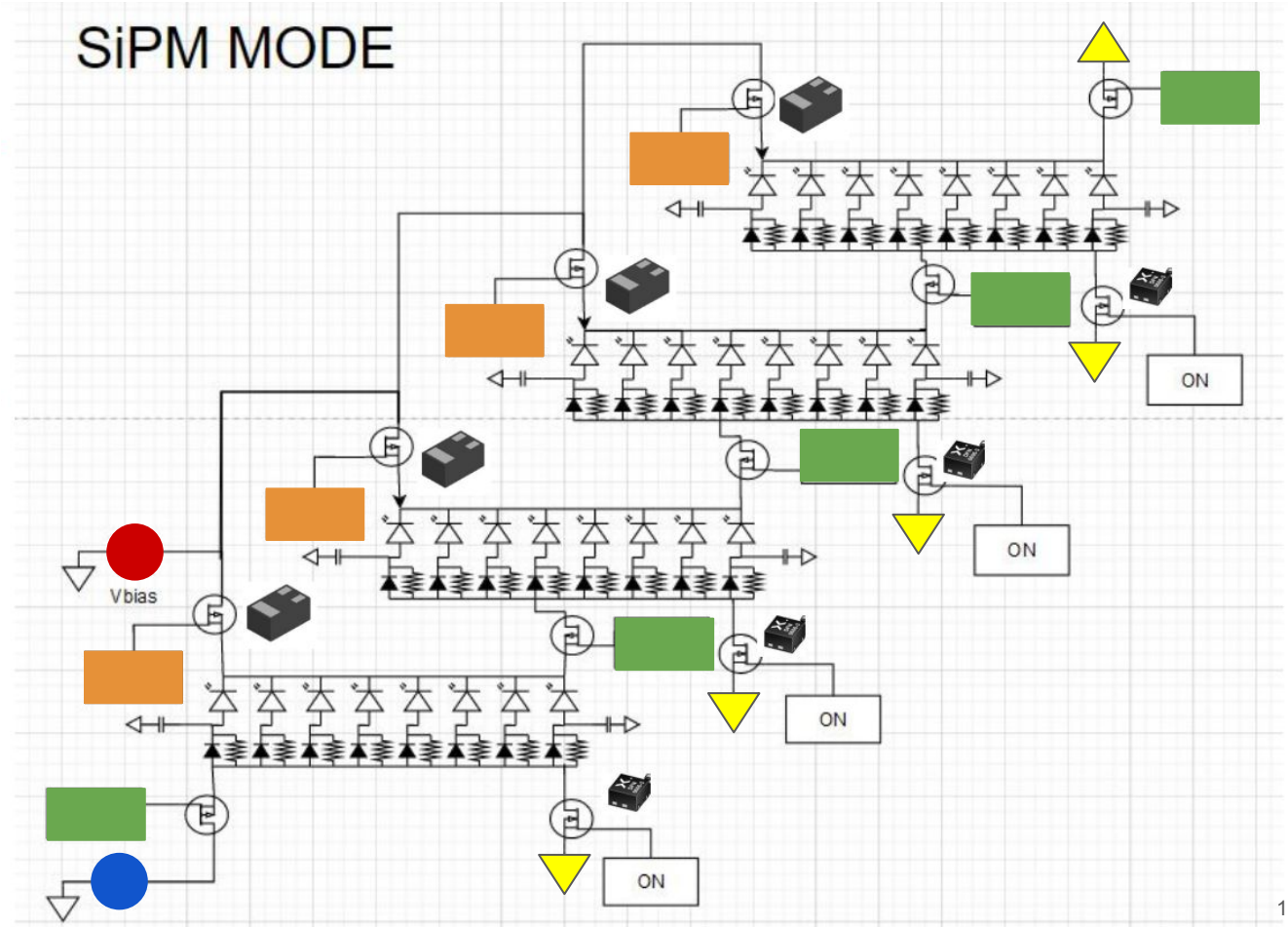
one **SiPM matrix** is composed of two SiPM groupings

the **dRICH PDU** is composed of four SiPM matrices

for each SiPM grouping we foresee the following external services (via RDO)

- **1 V-bias**
- **1 CTRL-bias**
- **1 V-ann**
- **1 CTRL-ann**
- **1 GND**

This is a total of 5 wires for each SiPM grouping, namely a total of **40 wires for one PDU**. The 40 wires enter on the RDO from the readout box patch-panel.



PDU voltage services

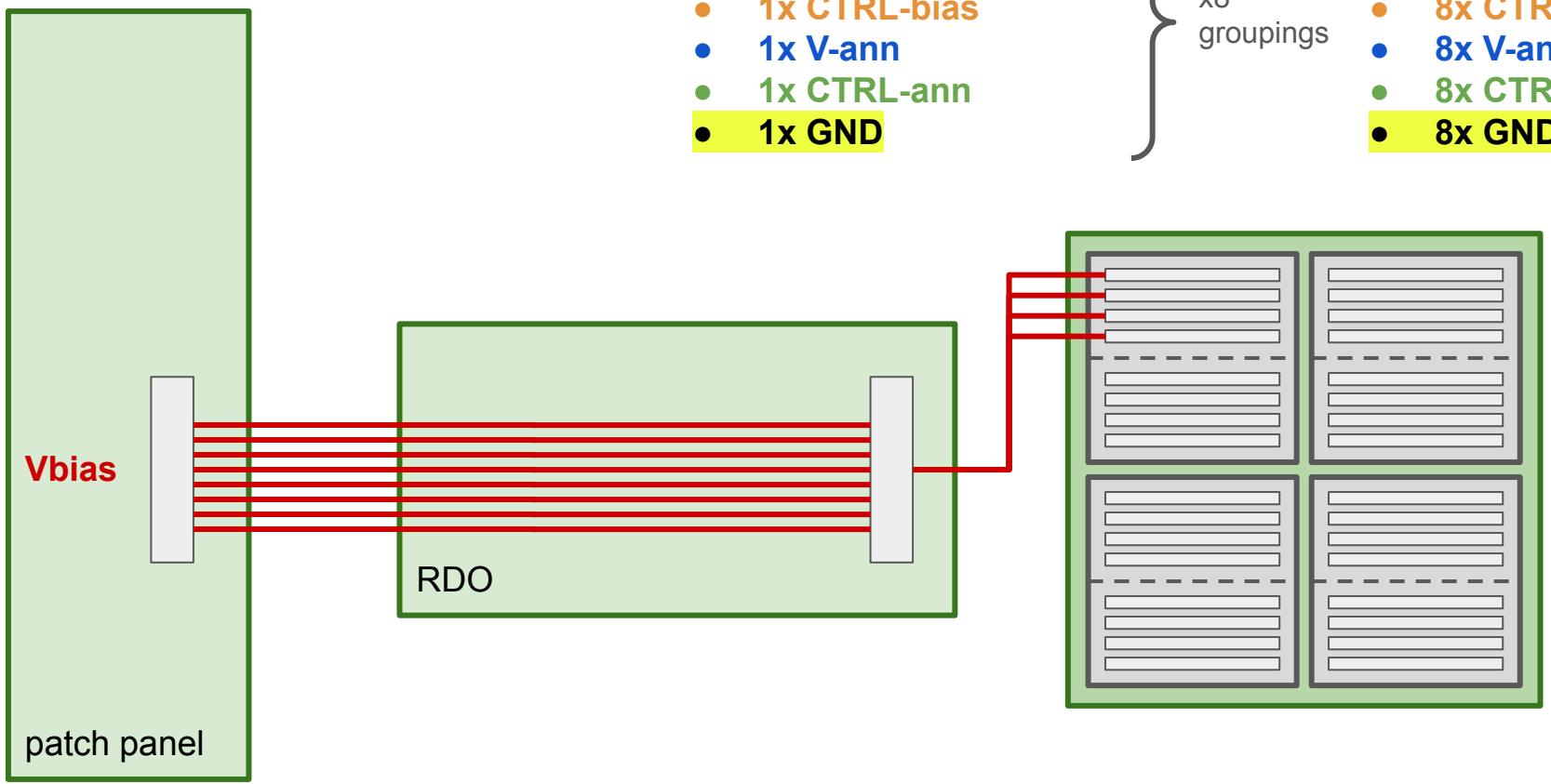
for each SiPM grouping we foresee the following external services (via RDO)

- **1x V-bias**
- **1x CTRL-bias**
- **1x V-ann**
- **1x CTRL-ann**
- **1x GND**

x8 groupings

for each PDU we foreseel services (via RDO)

- **8x V-bias**
- **8x CTRL-bias**
- **8x V-ann**
- **8x CTRL-ann**
- **8x GND**



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