Electronics design of the Muon Entrance Trigger

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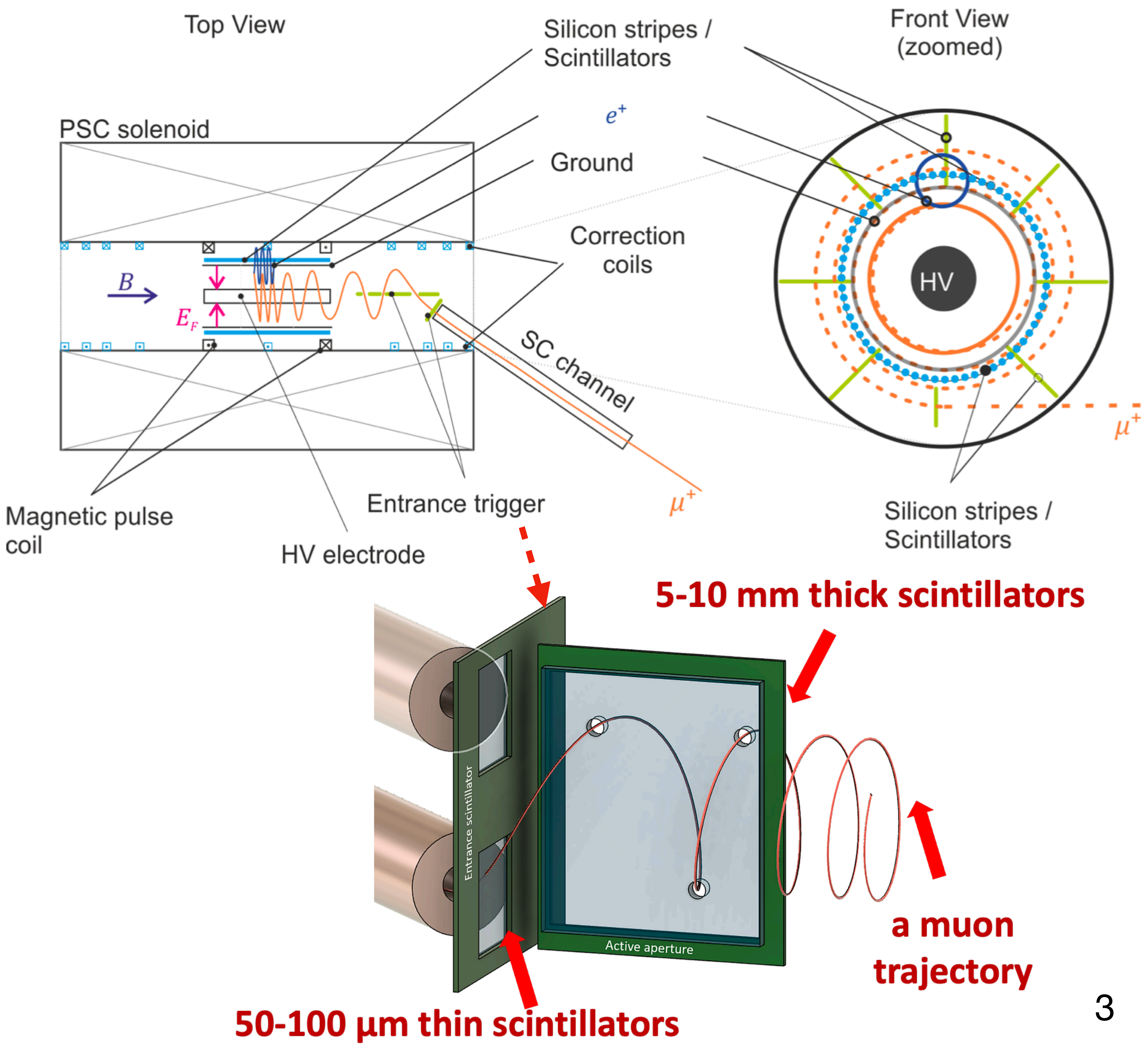
Outline

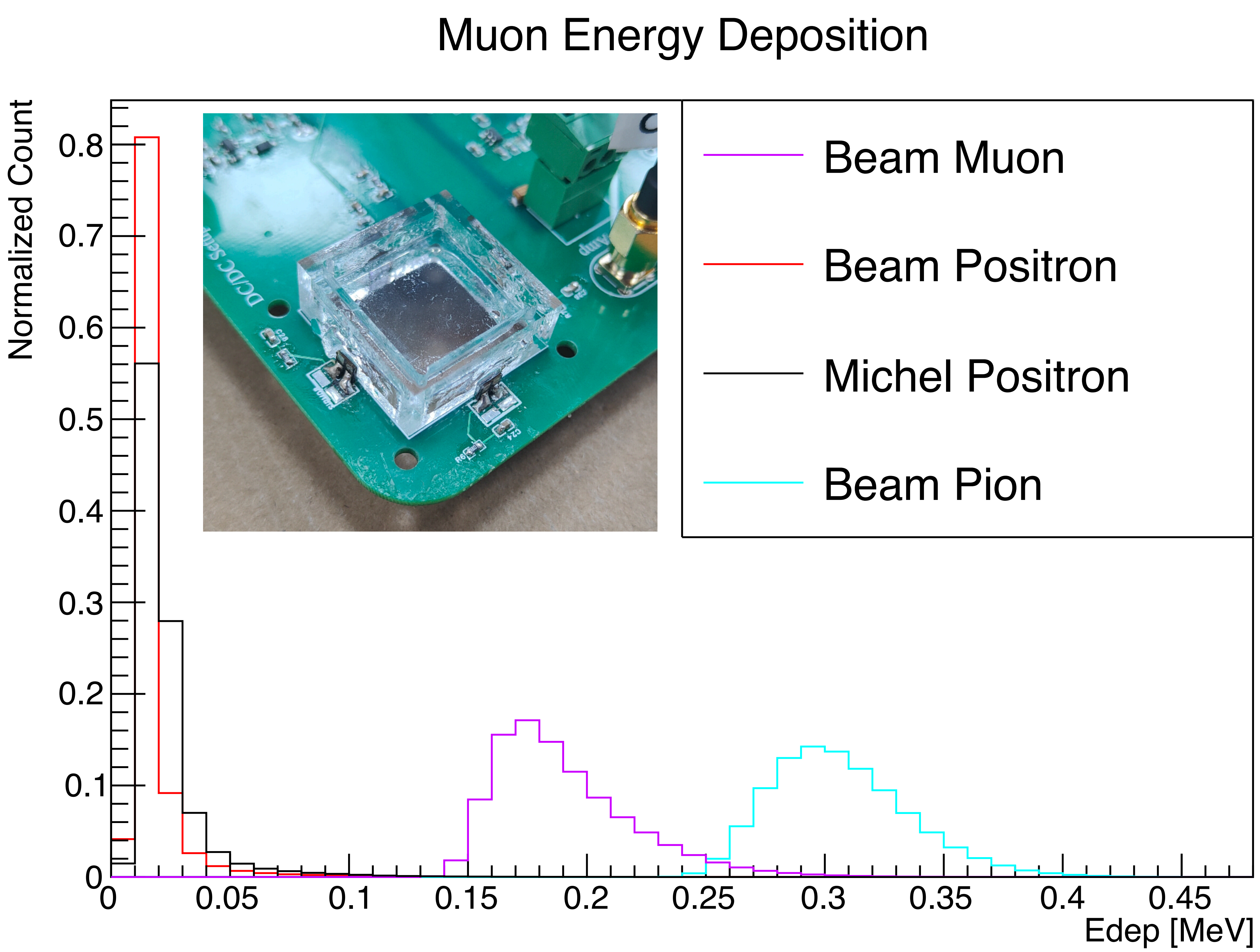
- **Review**
- **Updated work on the Gate detector**
    - The ability to discriminate the beam electron, muon, and pion
    - Kicker-activated time influence, the fast electronics requirements
    - The electronics prototype and its performance
    - Dynamic ranges for the electronics output
- **Next plan for the aperture and coincidence logic**

Review



- We are developing an entrance detector
  - To store the muons in a stable orbit, a pulsed magnetic field needs to be triggered.
  - Match the phase space between the beamline and solenoid
- Requirements
  - To be fully efficient while keeping at the minimum the multiple scattering of the detected muon
  - Short propagation delay
  - Discriminate the secondary particles in the beamline
- EJ-200 (OR GNKD) Scintillator + SiPM

Gate: light yield and Energy deposition



The range of deposition energy for these particles is different

The expected dynamics range for the outputs of SiPM

Particles	Average Energy deposition(MeV)	Photons per SiPM GNKD	Photons per SiPM EJ200
Positron	0.017	<3	< 7
Muon	0.190	5~9	9~20
Pion	0.307	8~12	15~26

Note:

- the GNKD scintillator results were confirmed in both the simulation and experiment,
- the EJ-200 scintillator, results were obtained by the scale with the photon yield

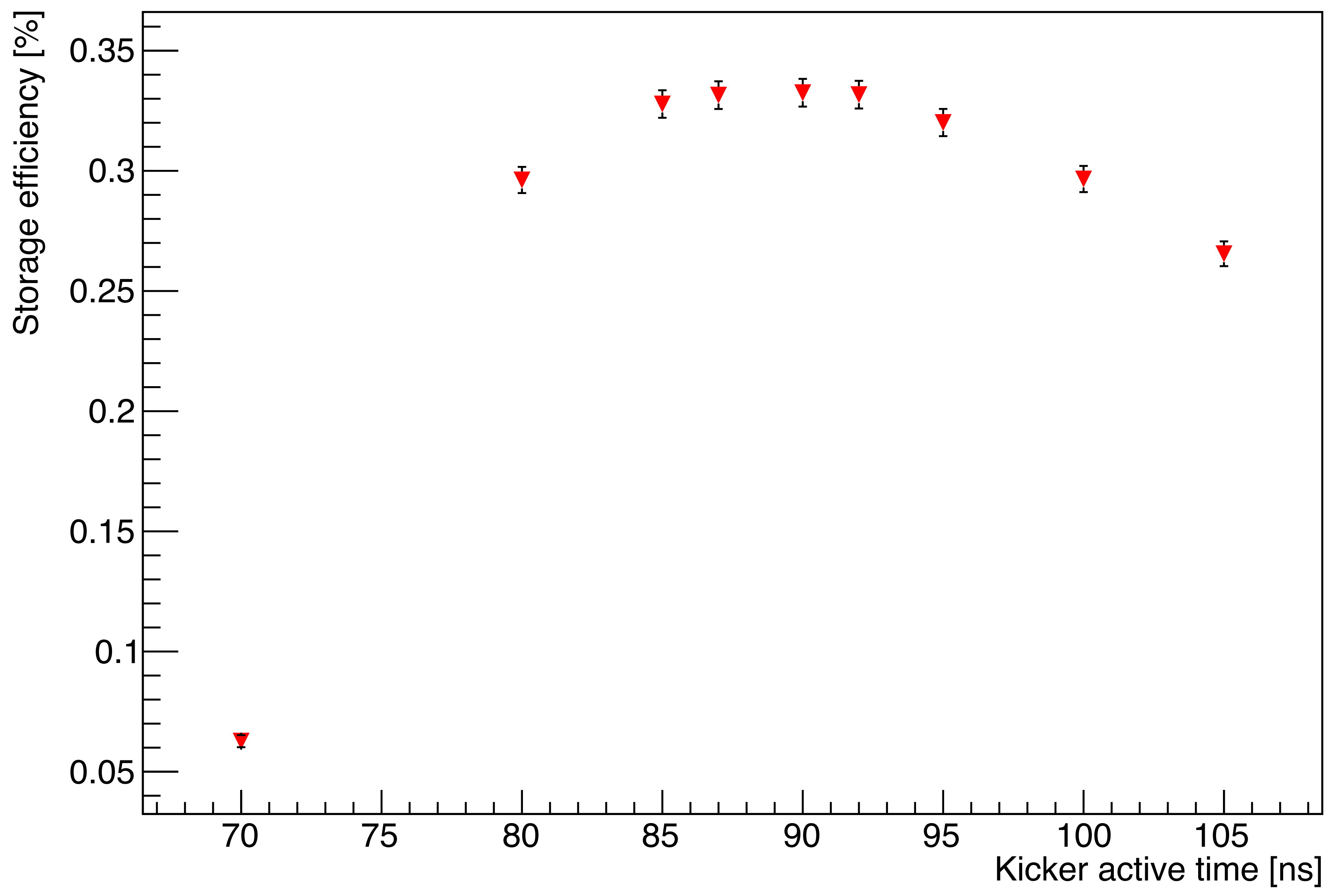
Kicker pulse time scan

- With G4bl, the muon storage efficiency varied with the kicker time
- For maximum storage efficiency
- The time fluctuation in the kicker-activated time should be limited to ± 5 ns.

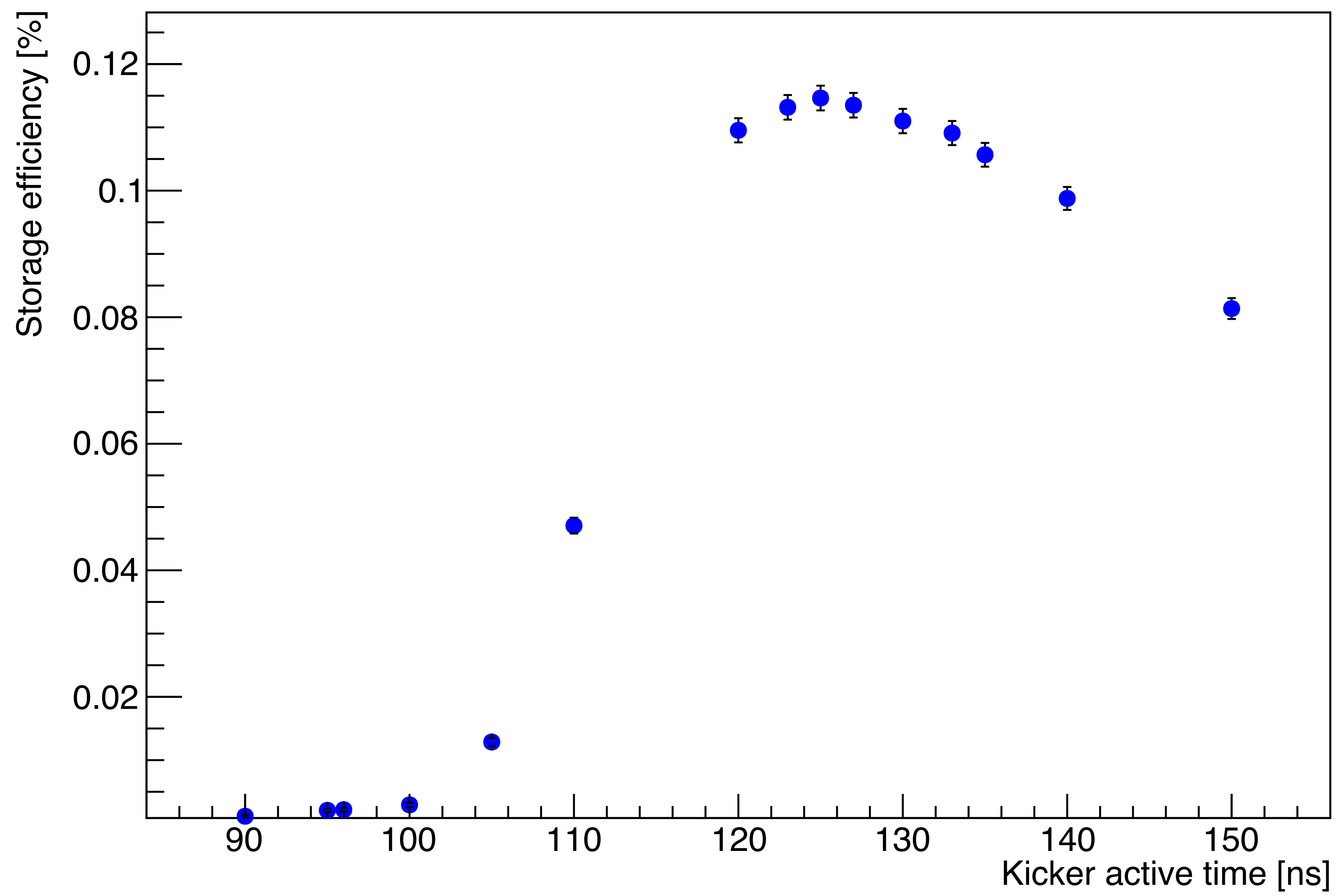
Parameter Settings

Ver.	1.0	2.0
injR, mm	45.561	47.087
mZ, mm	-443.836	-454.609
Theta, deg	-45.022	-42.317
Phi, deg	9.244	10.581
PFfilename	PulseCoilB_simPuls_107_35.txt	SplitCoilArray_largeVolumeGrid.txt
WeakCurr, Amps/mm	1.5	1.5
InputDistFile	InputDistAfterCollimator_R75mm.txt	Inputdist_3M.txt
SplitPair, Amps/mm	2.5	1.6

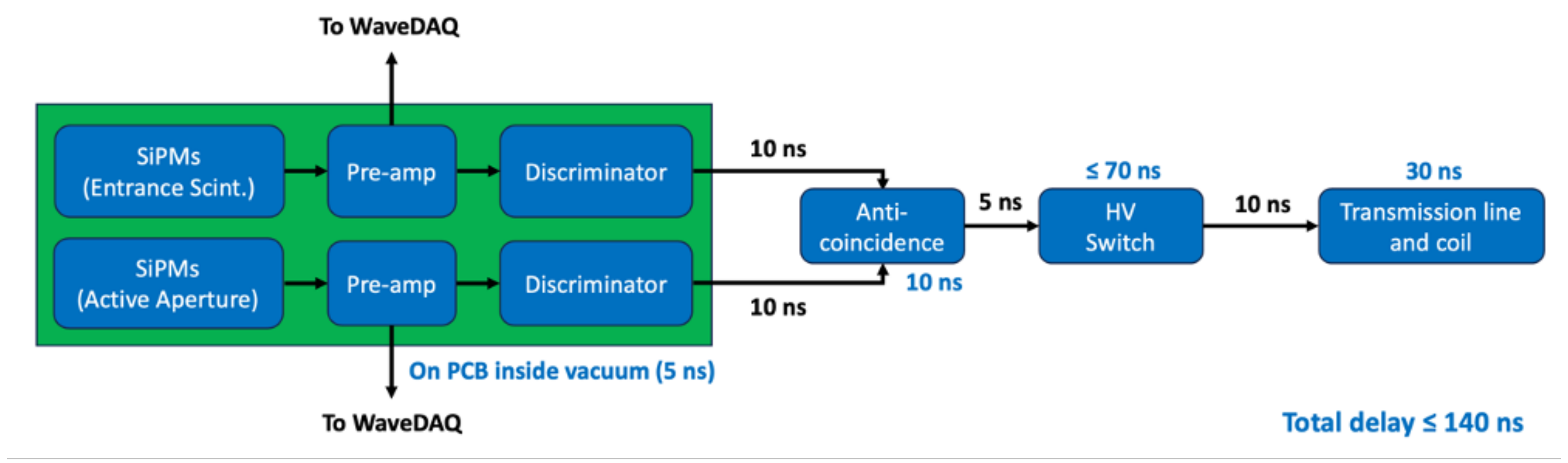
Muon storage efficienct affected by Kicker (V1 Pars)

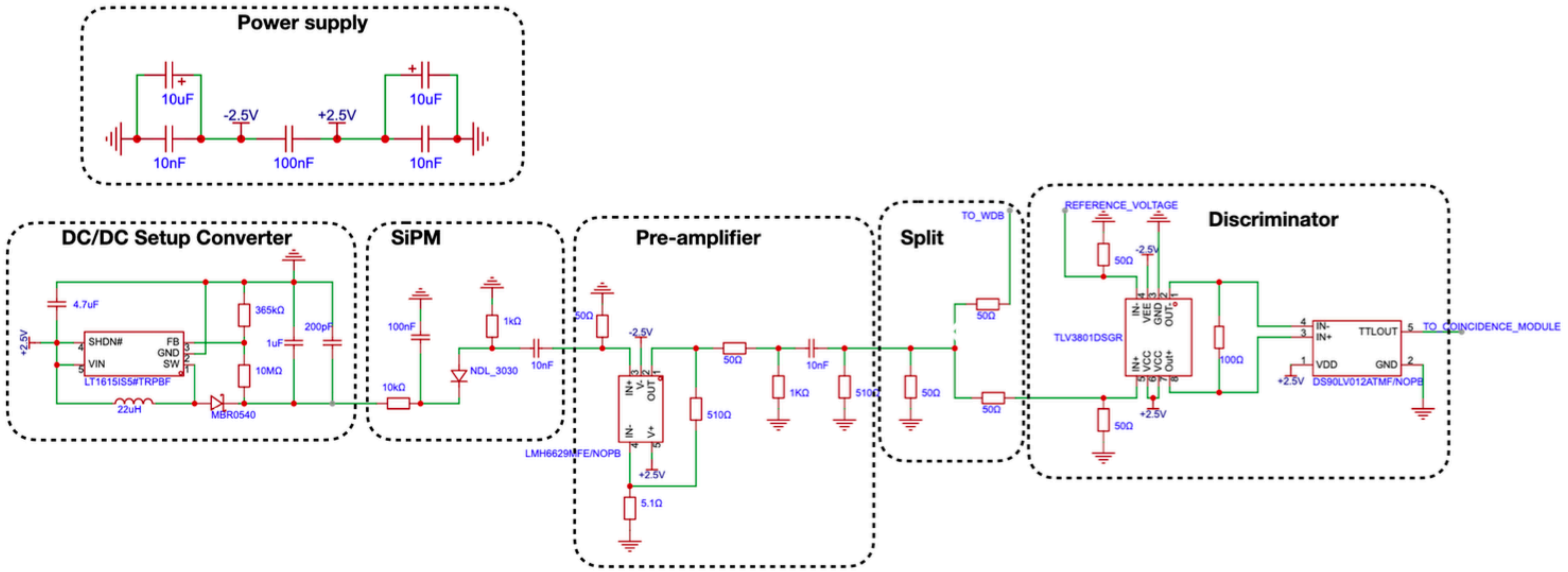


Muon storage efficienct affected by Kicker (V2 Pars)

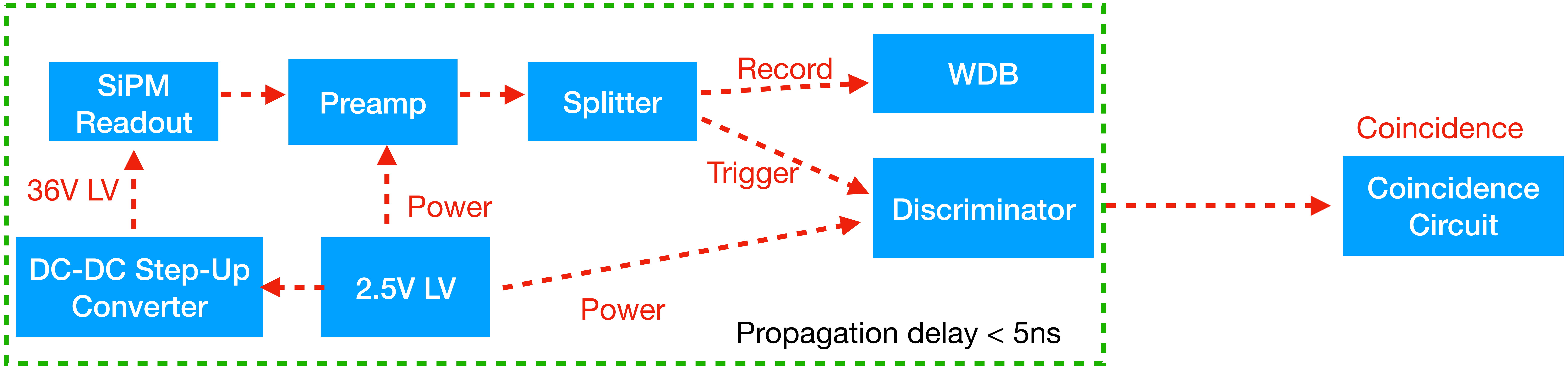


Fast electronics design of gate



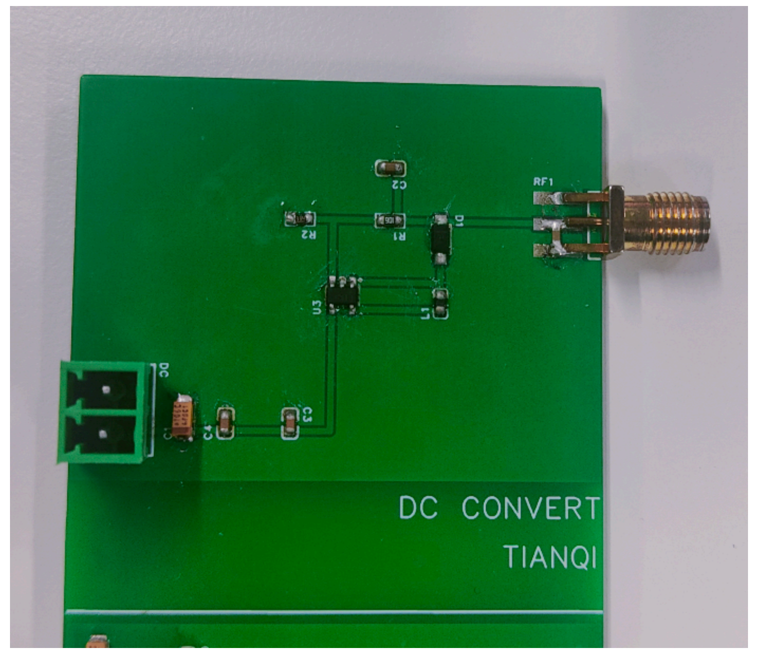


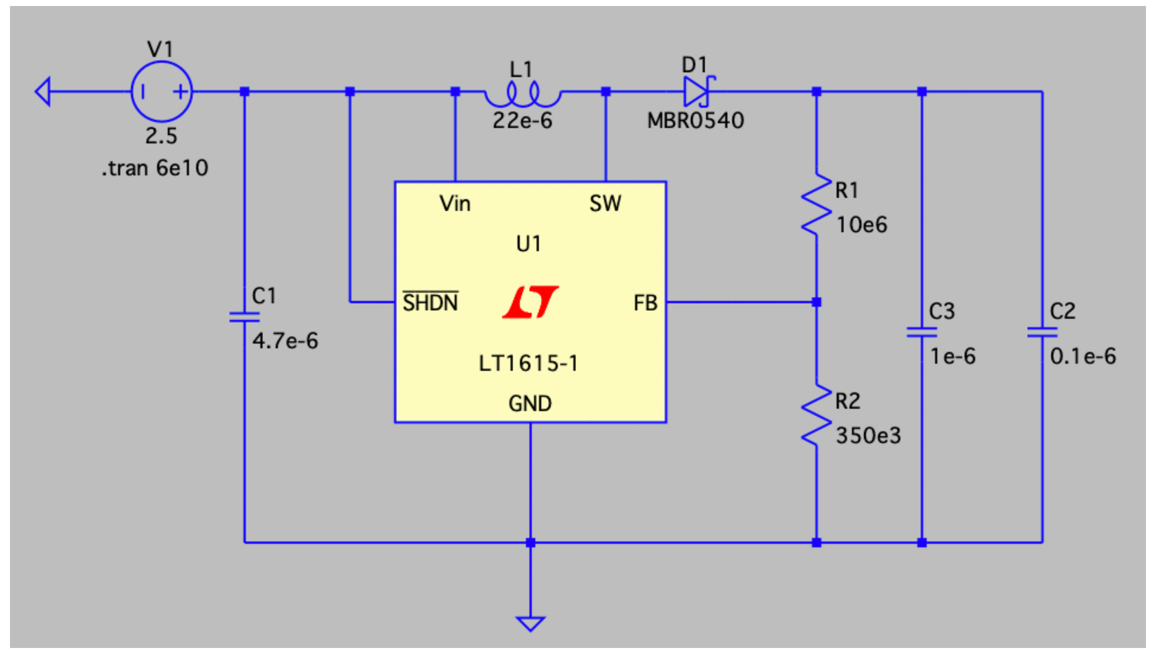
The propagation delay of ~ 100ns between the gate and HV switch to maximize the storage efficiency



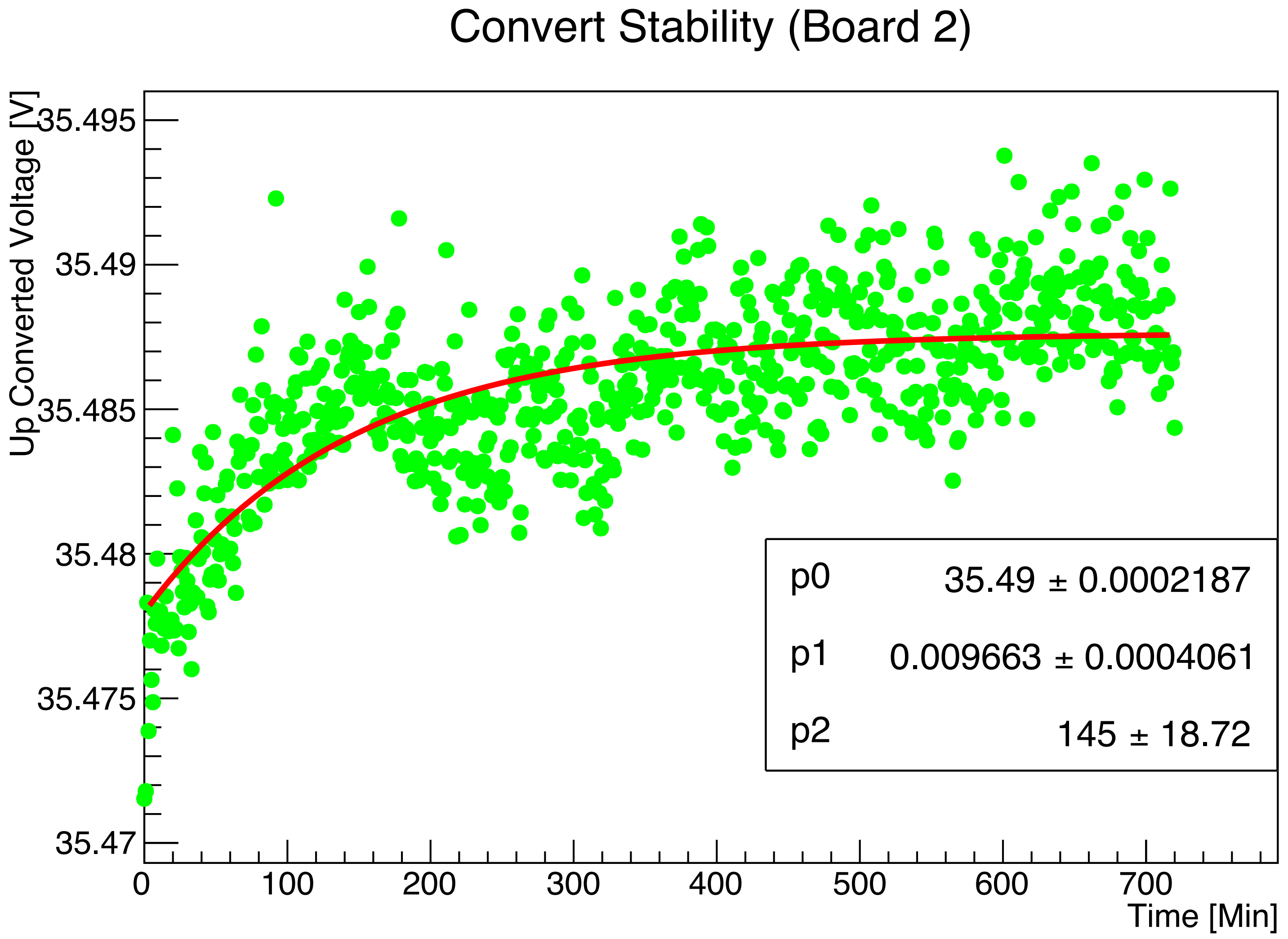
DC-DC Step-Up Converter

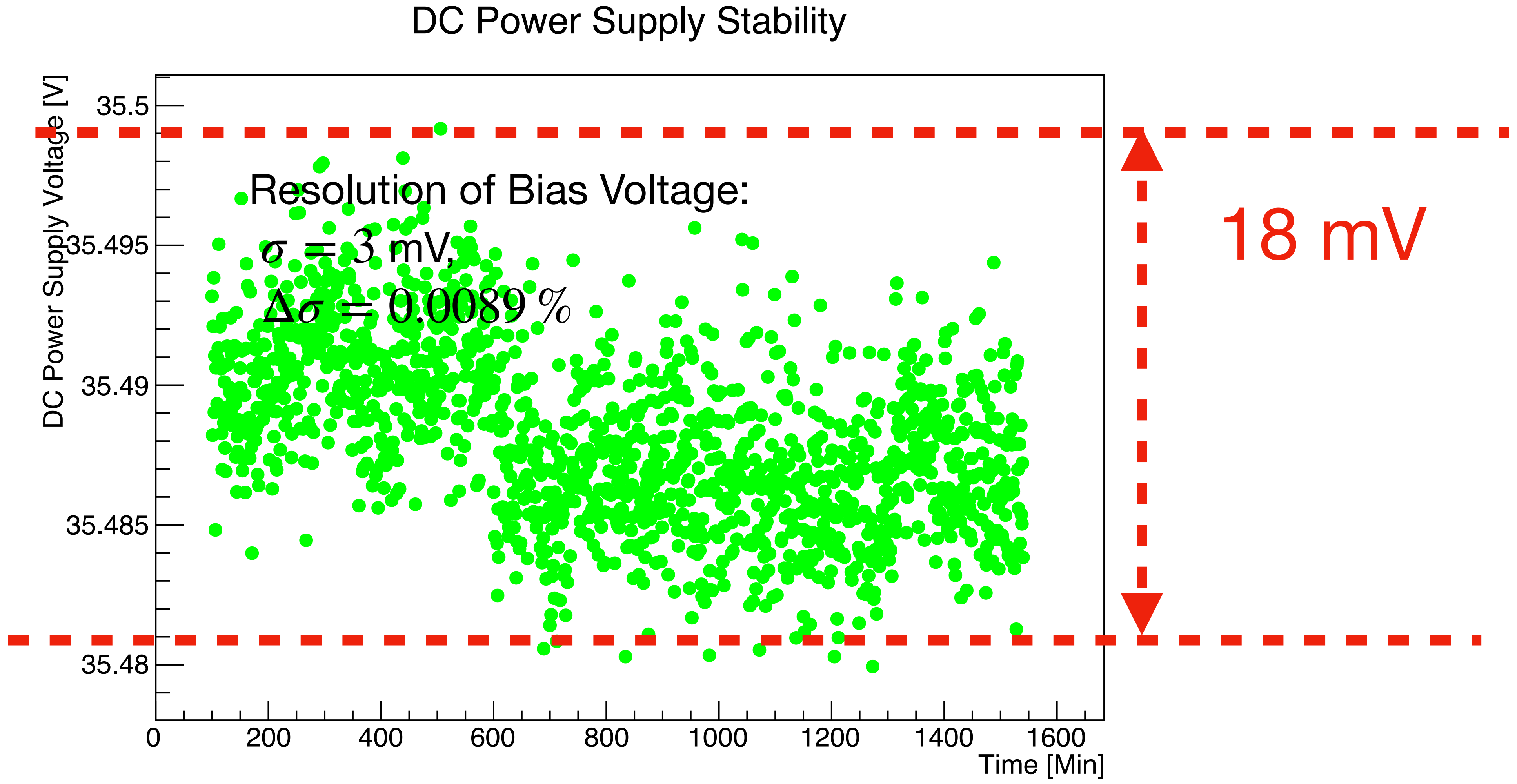
Up-Convert





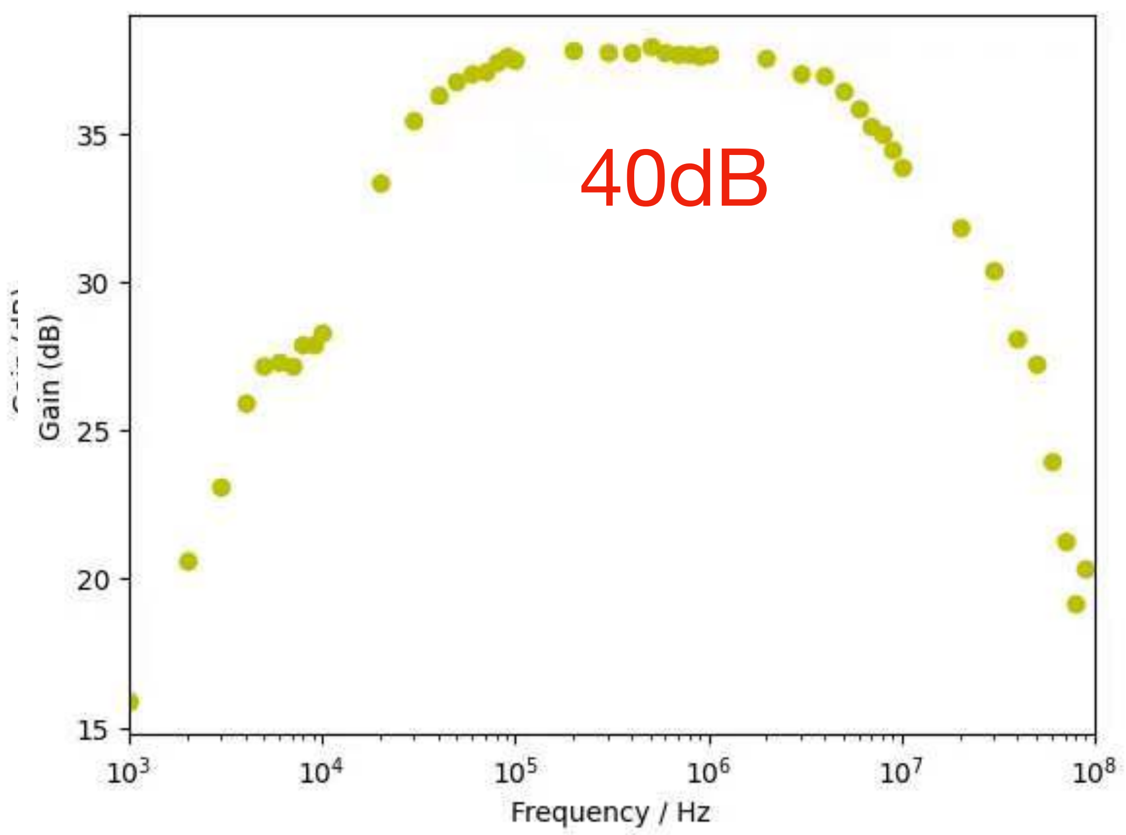
- DC-DC Step-Up Converter:
  - Output is about 35V
  - With a resolution of Bias Voltage < 4 mV, $\Delta\sigma < 0.010\,\%$
  - The output voltage fluctuation is 18 mV,
  - SiPM Gain is $\sim 3.5 \times 10^5$, and the corresponding fluctuation in the SiPM gain is evaluated $\sim 0.26\,\%$, and also ~ 0.26% fluctuation in P.E. count

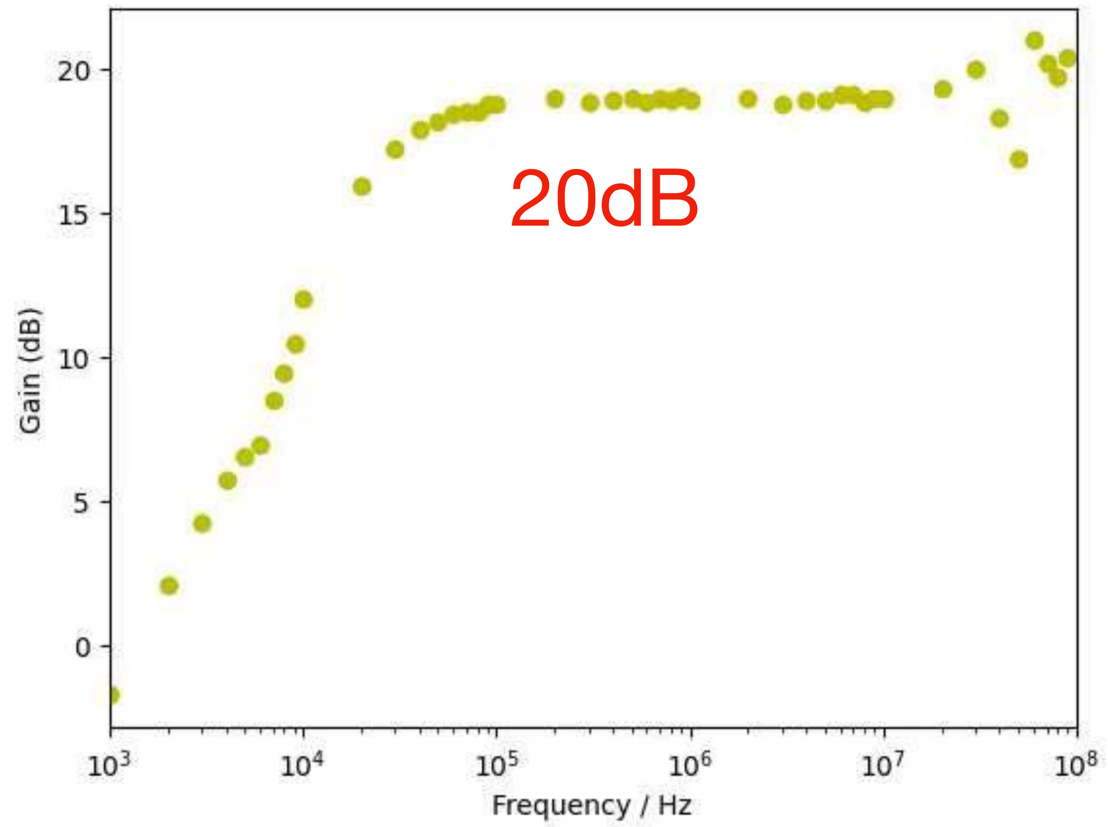




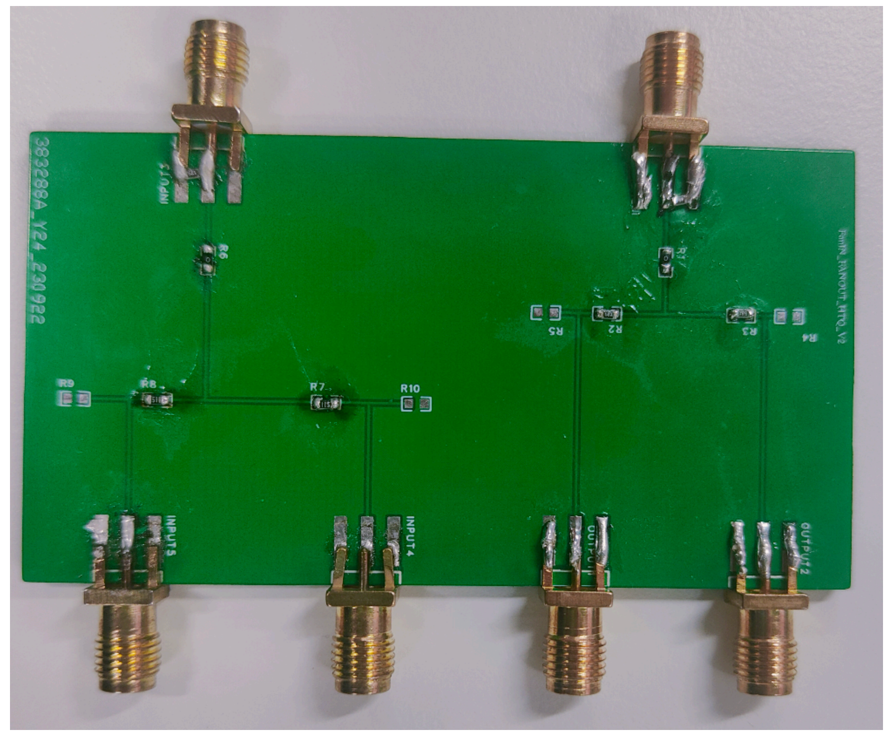
PreAmp+Splitter component

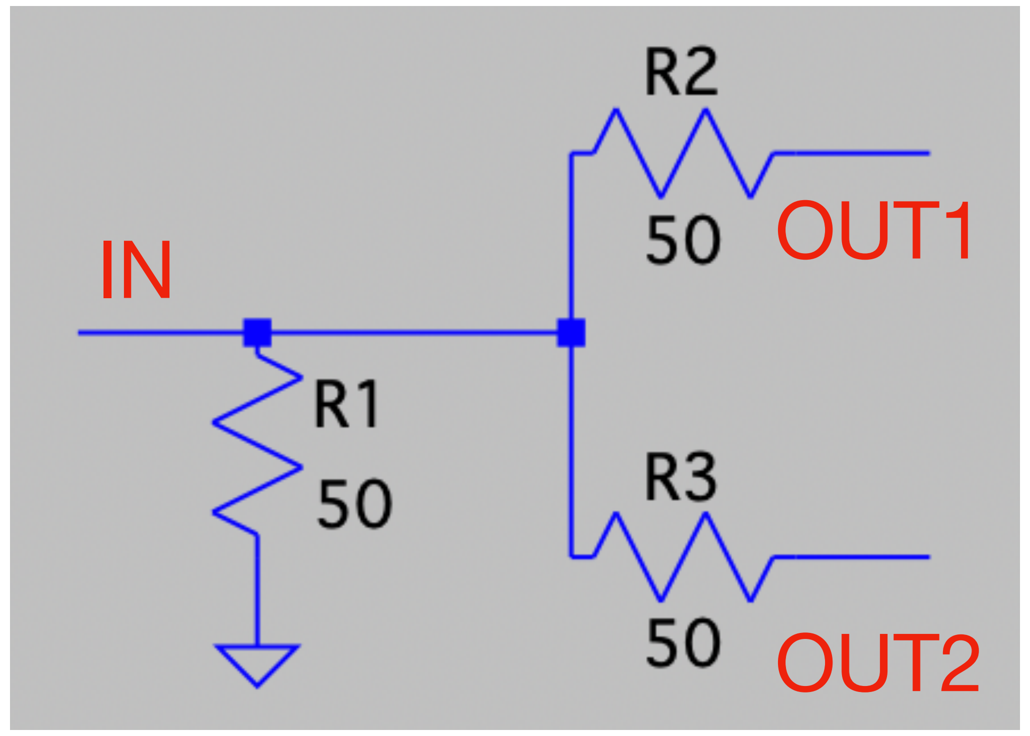
Frequency response





Split

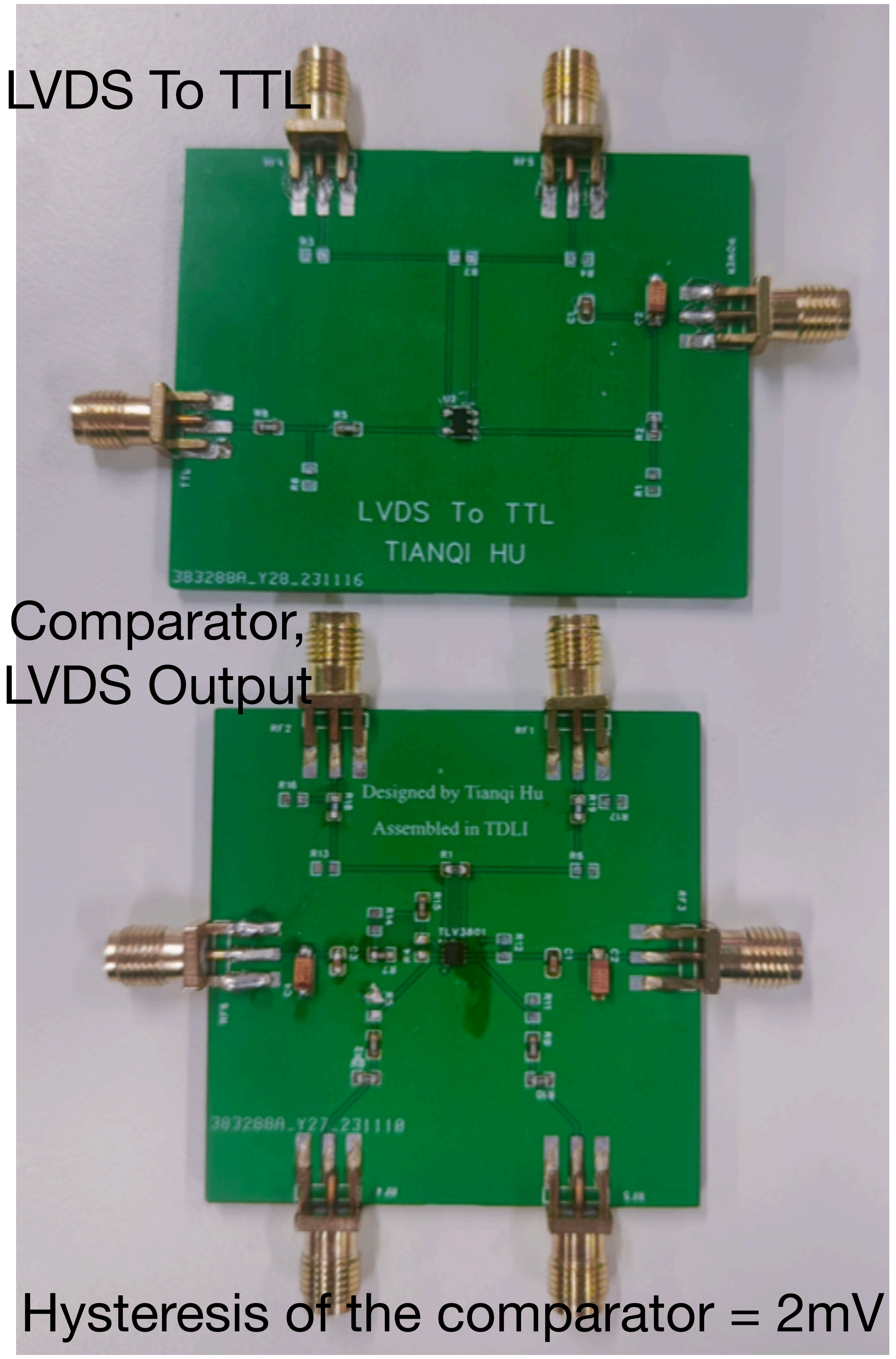


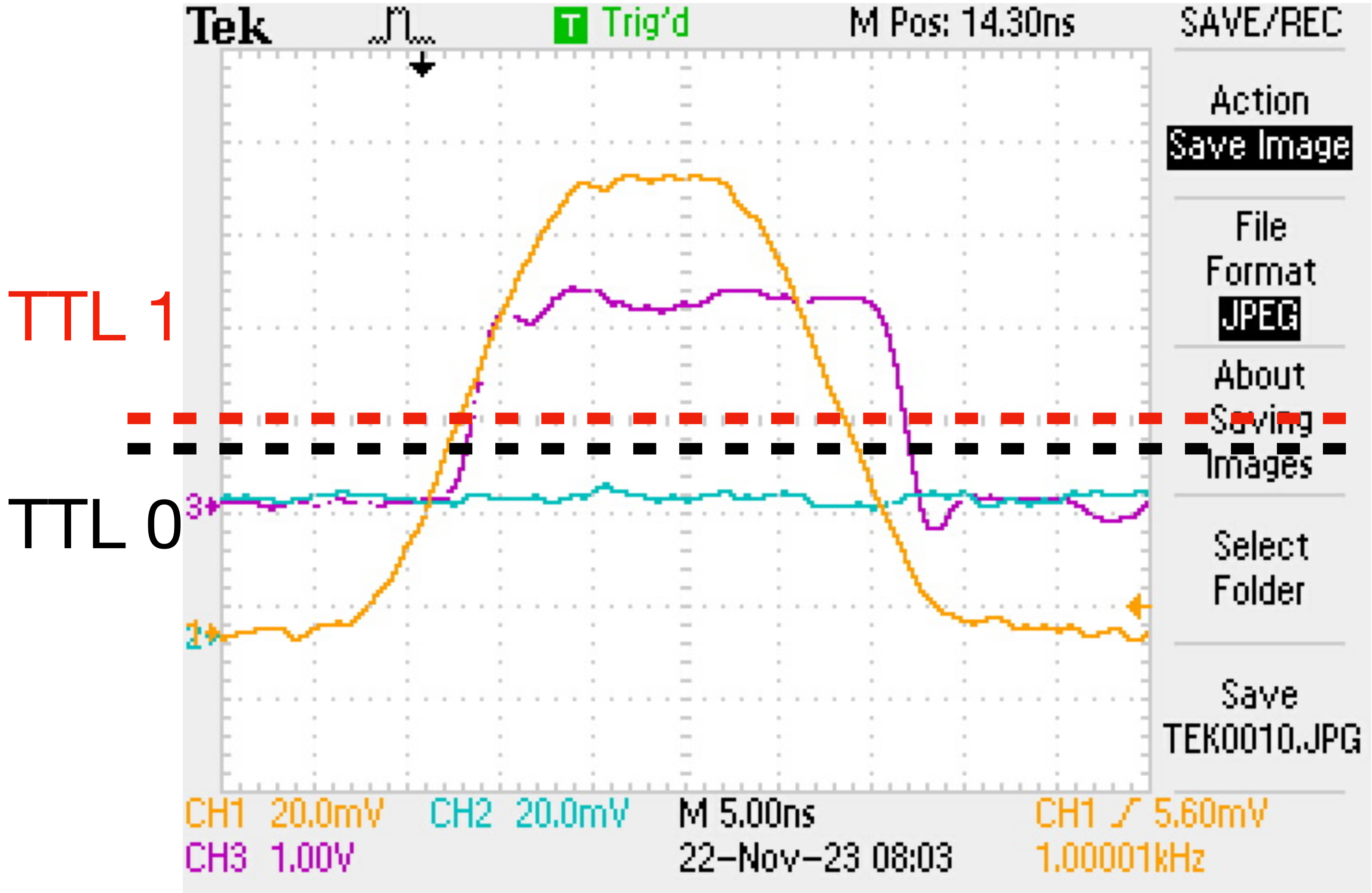


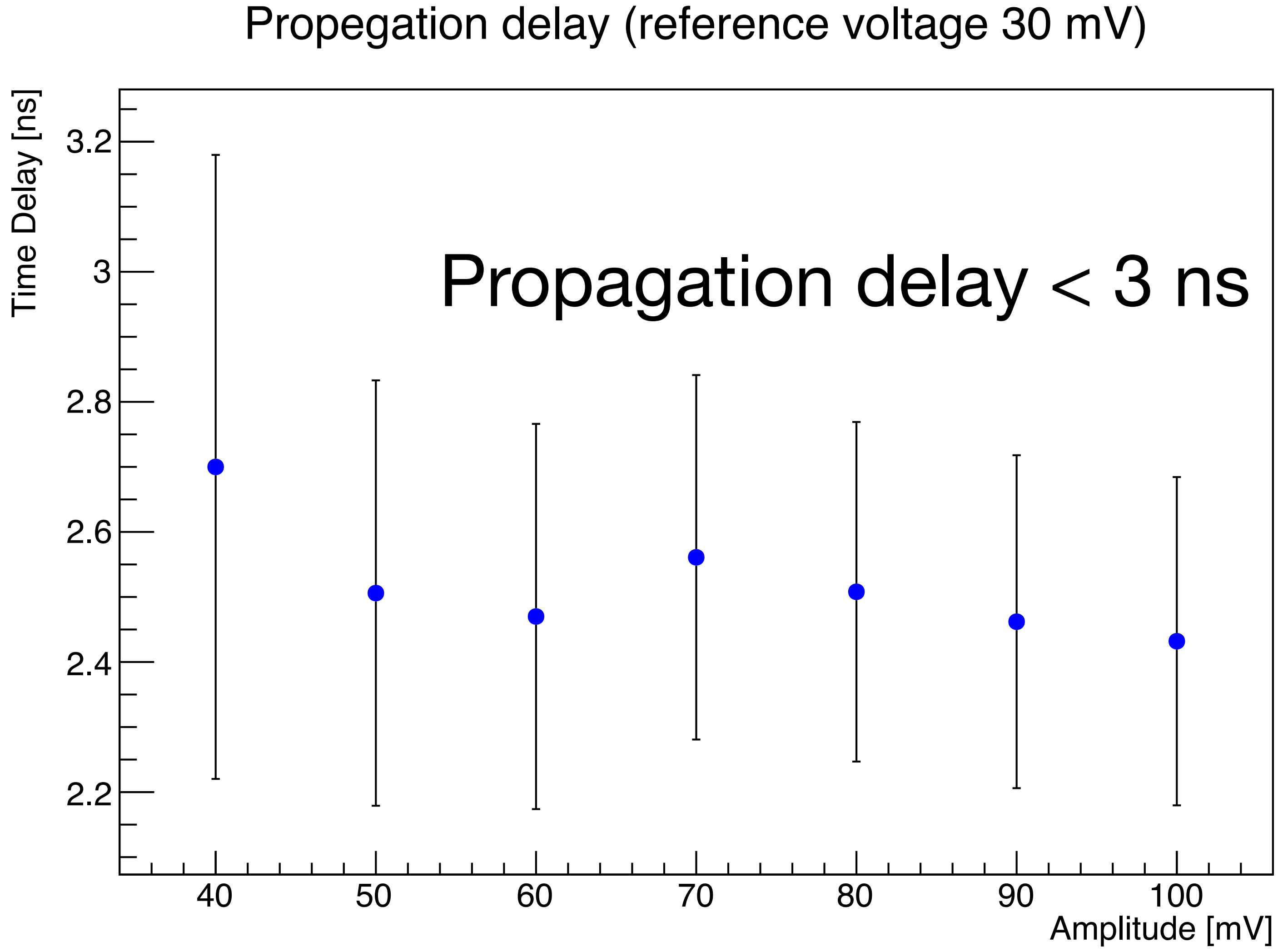
$$V_{OUT1} = V_{OUT2} = \frac{1}{3} V_{IN} \approx 0.33 V_{IN}$$

- Pre-amp:
  - 1GHz bandwidth
  - Amplifier amplification is adjusted to 50x
- Splitter:
  - Three resistors used
  - The output from the splitter is about 10x the input SiPM signal, after impedance matching

Discriminator component





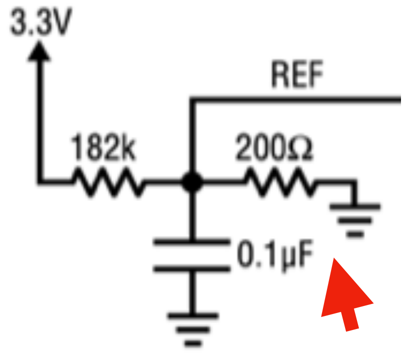


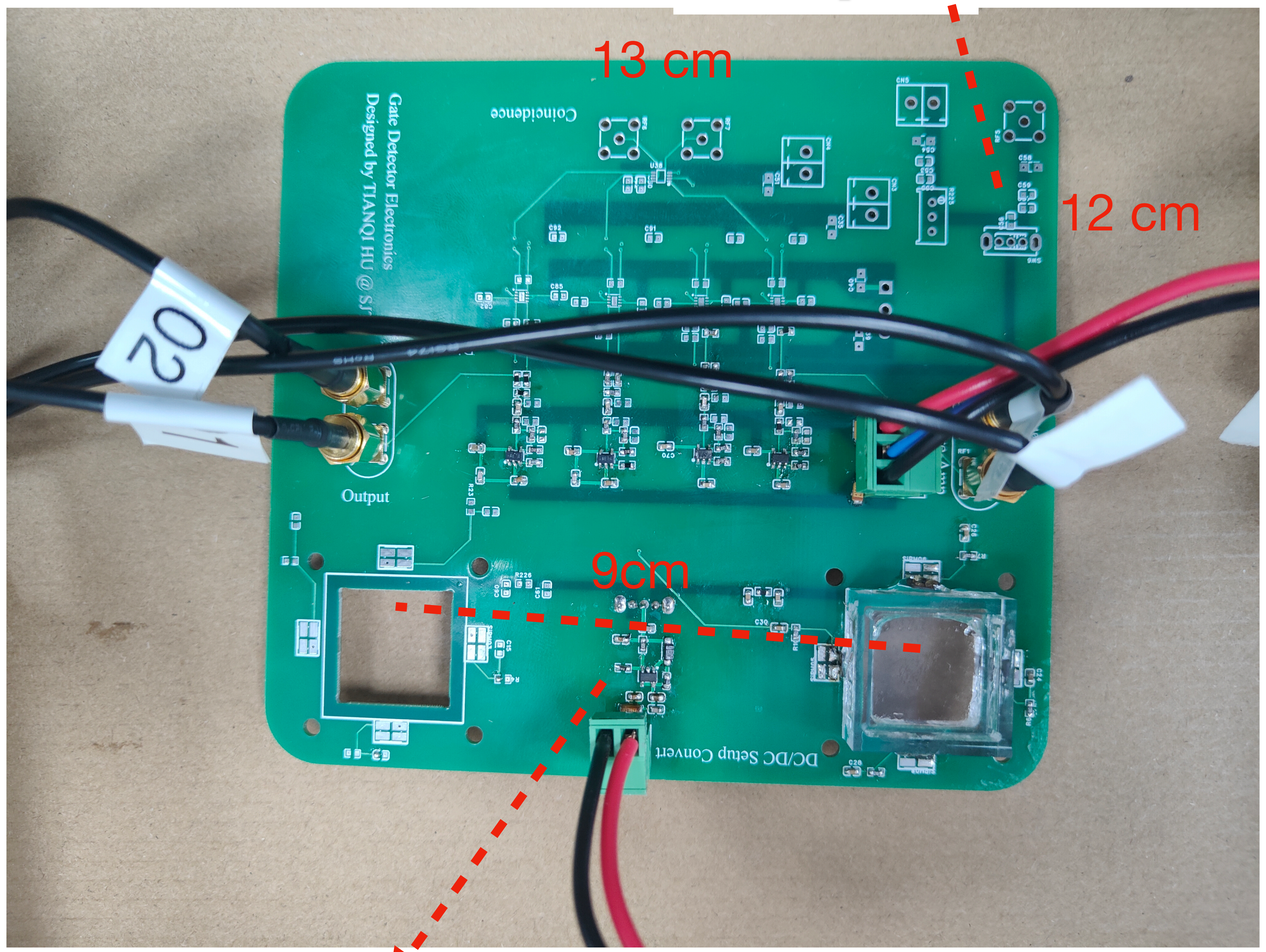
Components	Delay (ns)
Preamp	< 1
Split	~ 0
Discriminator	<3

- The discriminator module outputs LVTTL to the coincidence
- The total propagation for the electronics within the gate below 5 ns is expected

Electronics Board Prototype

Flexibly adjust the threshold of the comparator





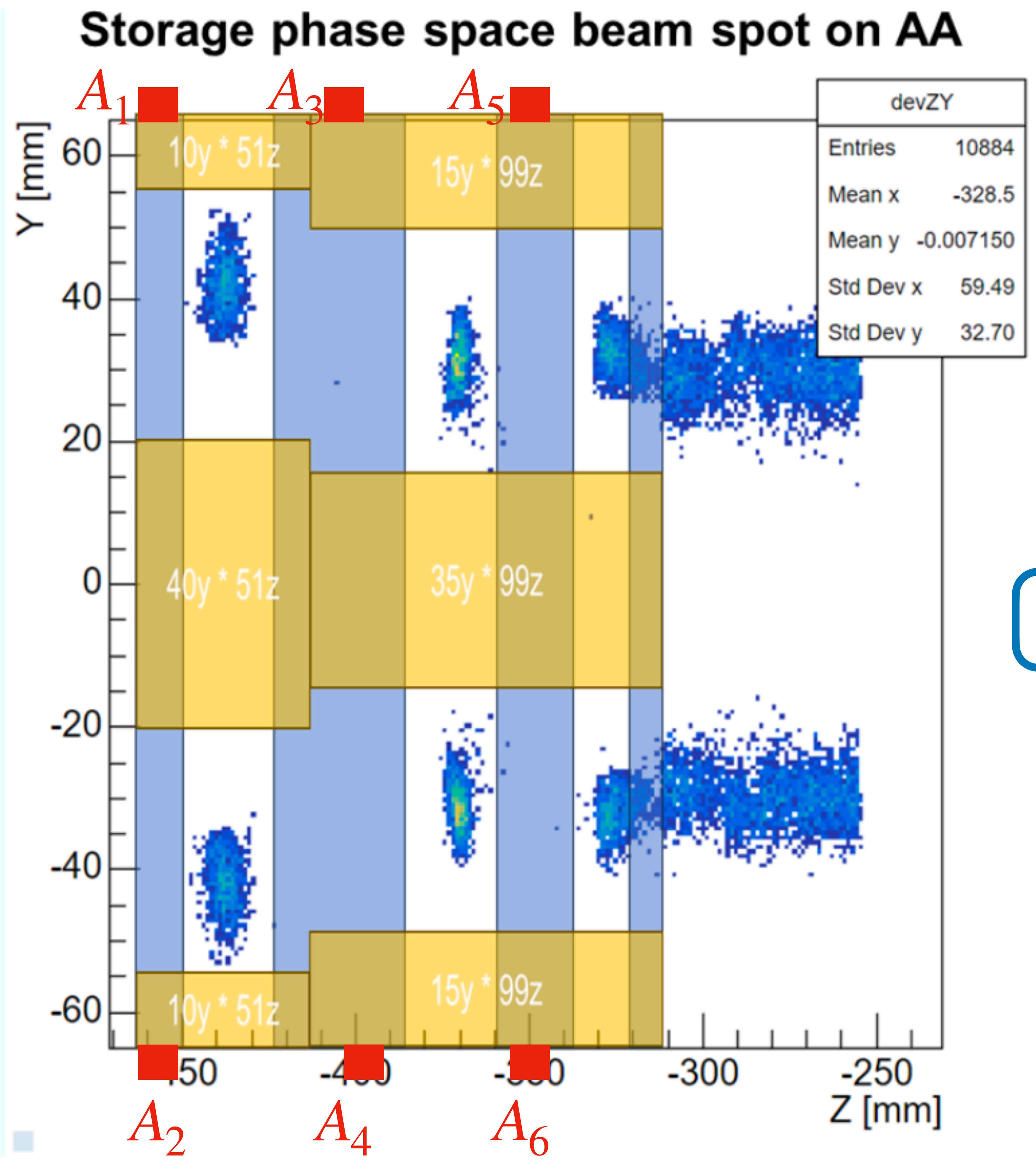
A switch of power supply, for selecting the up/bottom SiPMs work

- The electronics board prototype
  - Design two methods for the reference voltage in the discriminator
  - Outputs the coincidence logic of the gate SiPMs to the Aperture.
  - The expected dynamic ranges for the electronics are shown

Particles	Average Energy deposition(MeV)	Photons per SiPM GNKD	Pre-amp(mV) (20dB)	Split Output (mV)
Positron	0.017	<3	<12	<4
Muon	0.190	5~9	20~36	7~12
Pion	0.307	8~12	32~48	11~16

Expected dynamics range for the electronics

Electronics Design Concept for Aperture

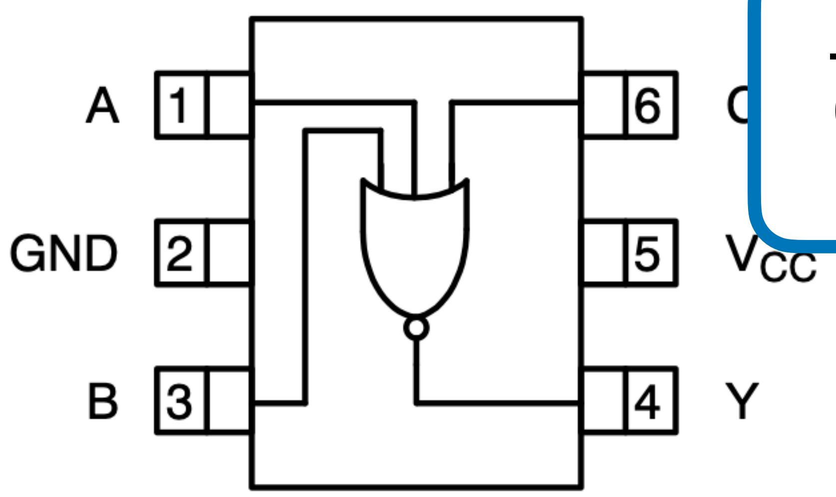


- For aperture
  - The electronics used are the same as those of the gate detector
  - The following coincidence logic, we plan to use AND and NOR

A_1~A_6 → $A_1 \,\&\, A_2$, $A_3 \,\&\, A_4$, $A_5 \,\&\, A_6$, →

NOR Logic (NC7SZ27)

- $V_{cc} = 2.5V$
- $V_{IL\_MAX} = 0.75V, V_{IH\_MIN} = 1.75V$
- $V_{OH\_MIN} = 0V,\ V_{OH\_MAX} = 2.5V$
- $t_{pd\_MAX} = 4.9ns$



$$\overline{(A_1 \,\&\, A_2) + (A_3 \,\&\, A_4) + (A_5 \,\&\, A_6)}$$

Coincidence Logic Plan

$G_1 \sim G_4$

AND Logic(SN74AUC2G0)
- $V_{cc} = 2.5V$
- $t_{pd\_MAX} = 1.6ns$

G_1 & G_2, G_3 & G_4

AND Logic(NC7SZ11)
- $V_{cc} = 2.5V$
- $t_{pd} = 4.9ns$

$V_{OUT} = 2.5V$

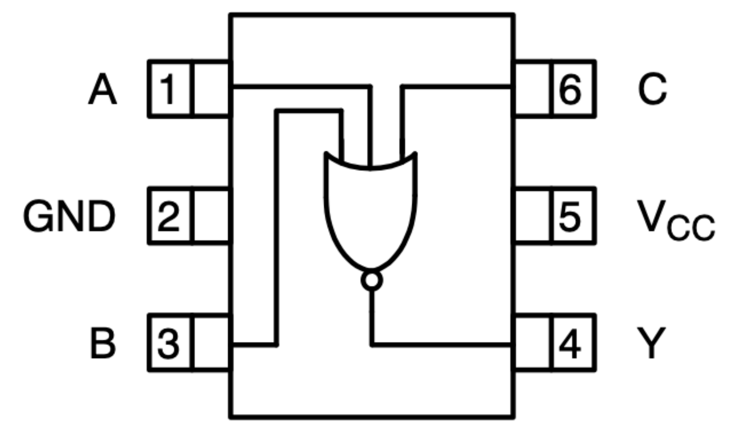
HV Switch

$A_1 \sim A_6$

AND Logic(SN74AUC0)
- $V_{cc} = 2.5V$
- $t_{pd\_MAX} = 1.8ns$

A_1 & A_2, A_3 & A_4, A_5 & A_6,

NOR Logic(NC7SZ27)
- $V_{cc} = 2.5V$
- $t_{pd} = 4.9ns$



$$\overline{(A_1 \,\&\, A_2) + (A_3 \,\&\, A_4) + (A_5 \,\&\, A_6)}$$

Propagation delay: 11.6 ns

However: if we set 5V for NC Chip, 6.9 ns PD totally

Summary

Gate detector:

- The ability of the gate to identify particles is evaluated
- The influence of the different activated times for kicker on the muon storage efficiency is evaluated
- The electronics prototype of the gate detector was produced, and the propagation delay was evaluated to 4ns within the gate detector
- The Expected dynamic ranges for the particles are evaluated

To-do:

- Aperture electronics and detector design and produce
- Optimize the electronics layout for the entrance detector
- The stability of the fast electronics within the magnet field environment
- Entrance Prototype test with radioactive sources

Thanks

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