ASIC developments in MiTo

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HASPIDE collaboration - MiTo group

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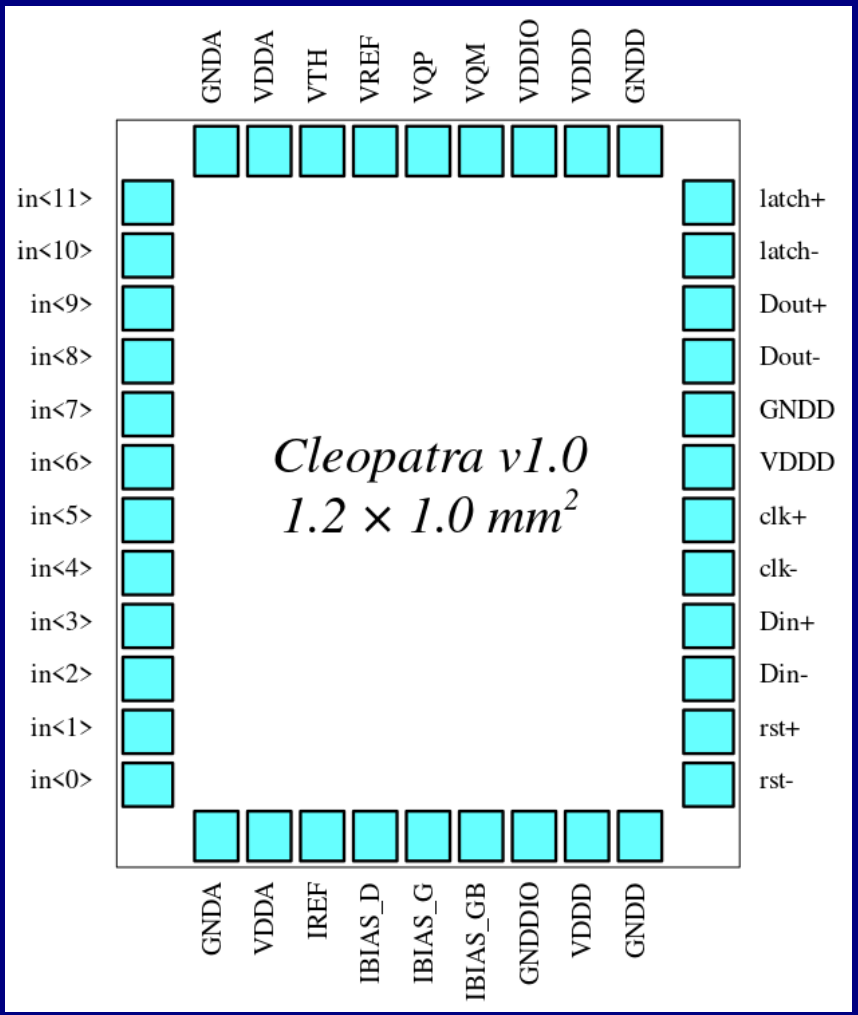
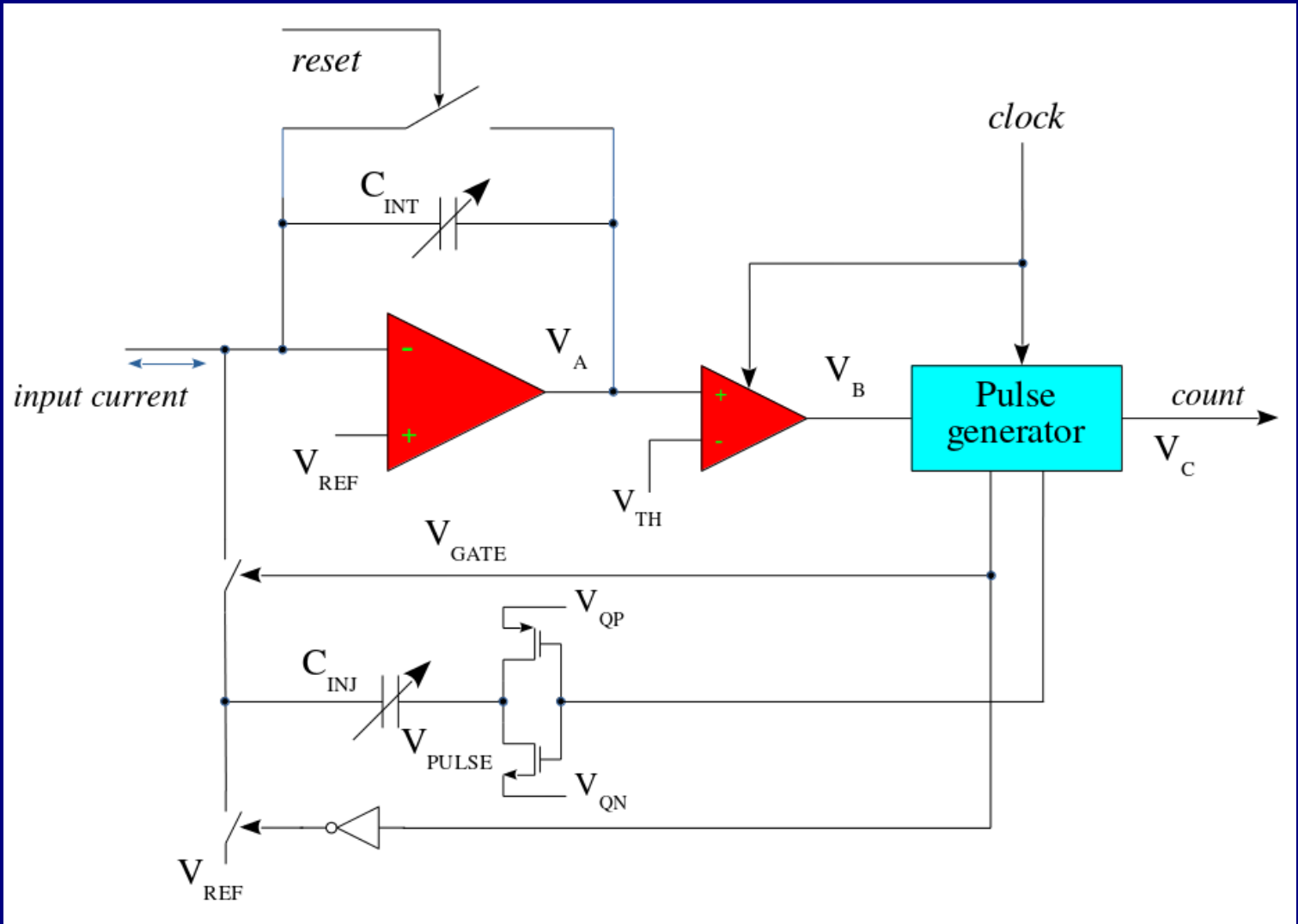
Cleopatra v1.0

Test ASIC pinout



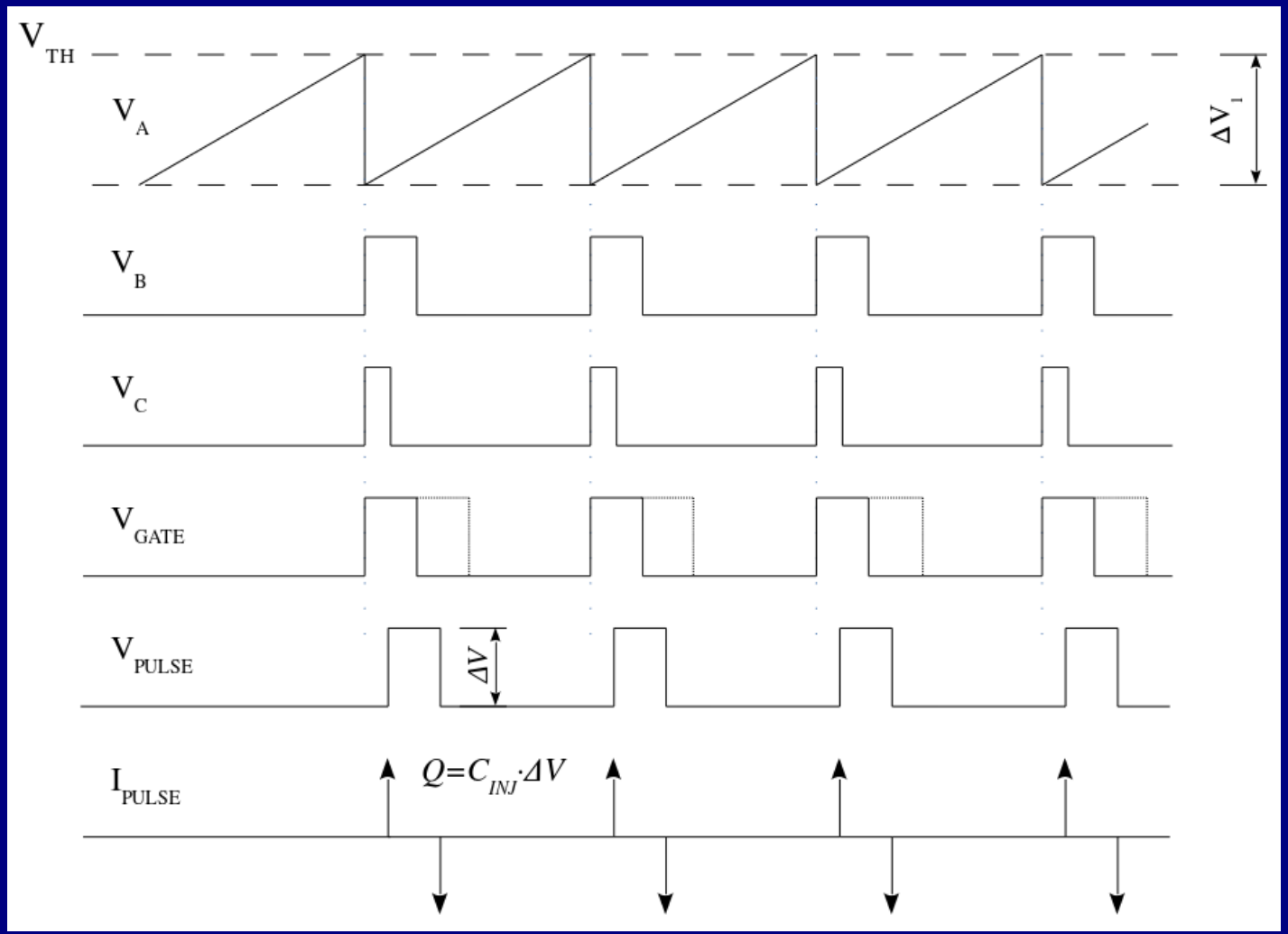
- Technology : CMOS 28 nm
- 12 channels recycling integrator
- Simple serial interface (pad limited die)
- Submitted on April 26^{th} 2023
- Received back on August 2023
- Test ongoing

Channel scheme



$$f_{out} = \frac{I_{IN}}{Q_{INJ}} = \frac{I_{IN}}{C_{INJ} \cdot (V_{QP} - V_{QN})}$$

Waveforms



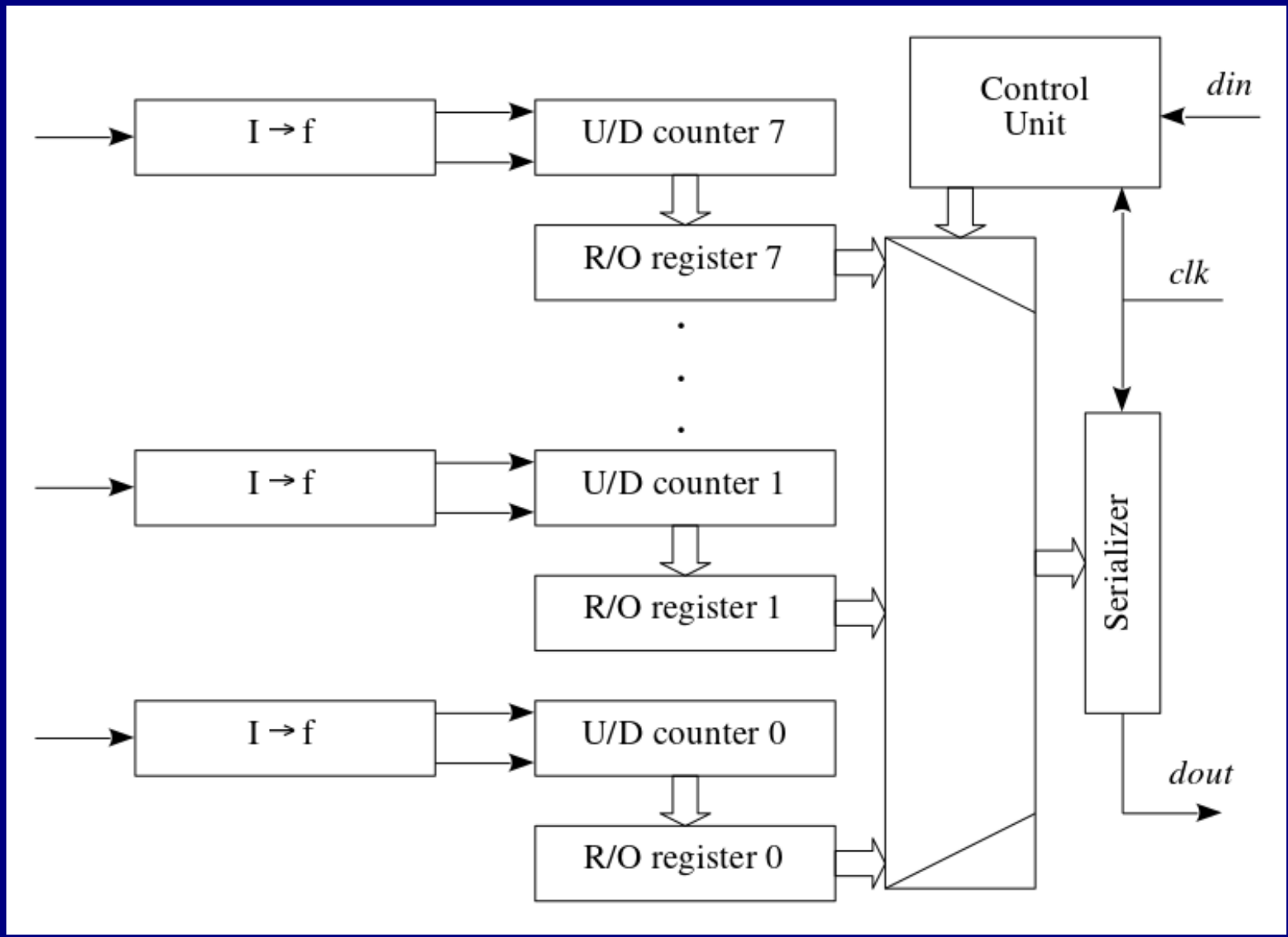
$$C_{INT} = 20\ fC \cdot N_1$$

$$C_{INJ} = 20\ fC \cdot N_2$$

$$\Delta V_1 = \frac{C_{INJ}}{C_{INT}} \cdot \Delta V$$

$$\Delta V = V_{QP} - V_{QN}$$

Cleopatra block diagram



Prototype features

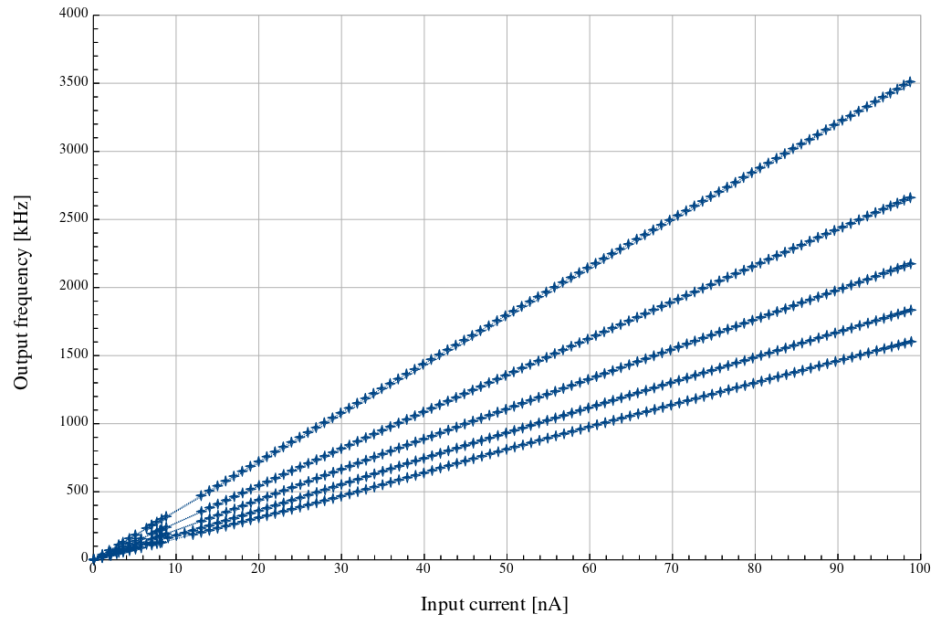
- 12 channels
- Three opamp configurations
  - Zero cancellation (ZC) - channels 0-3
  - Cascoded (G) - channels 4-7
  - Cascoded with gain boost (GB) - channels 8-11
- Serial interface for configuration and data
- 7 configuration registers

Data output format

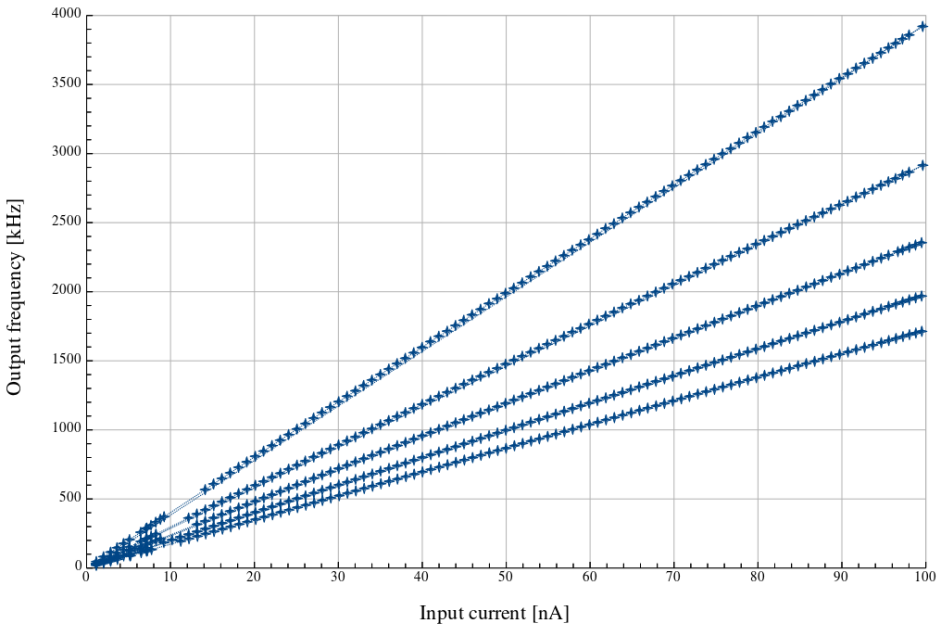
GCR06		**Output word**				
4	3:0	31:28	27:20	19:16	15:4	3:0
0	n	1001	*ReadOutReg(n)*			0110
1	m	1001	11001100	m	*GCR(m)*	0110
0	$n > 11$	1001	1100 1010 1100 1100 1100 1010			0110
1	$m > 6$	1001	1100 1010 1100 1100 1100 1010			0110

Transfer function (0-100 nA)

Channel 4



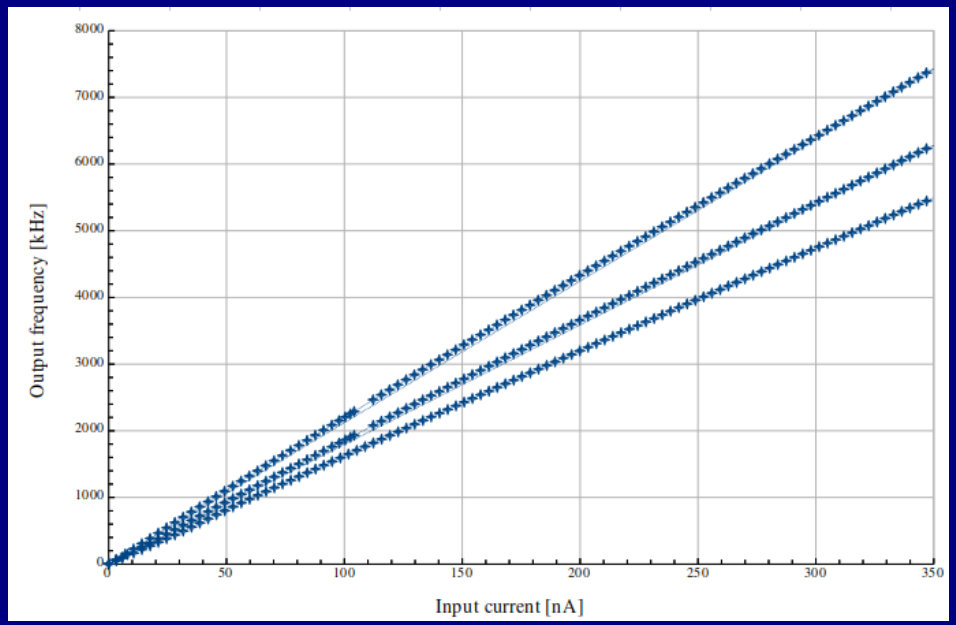
Channel 8



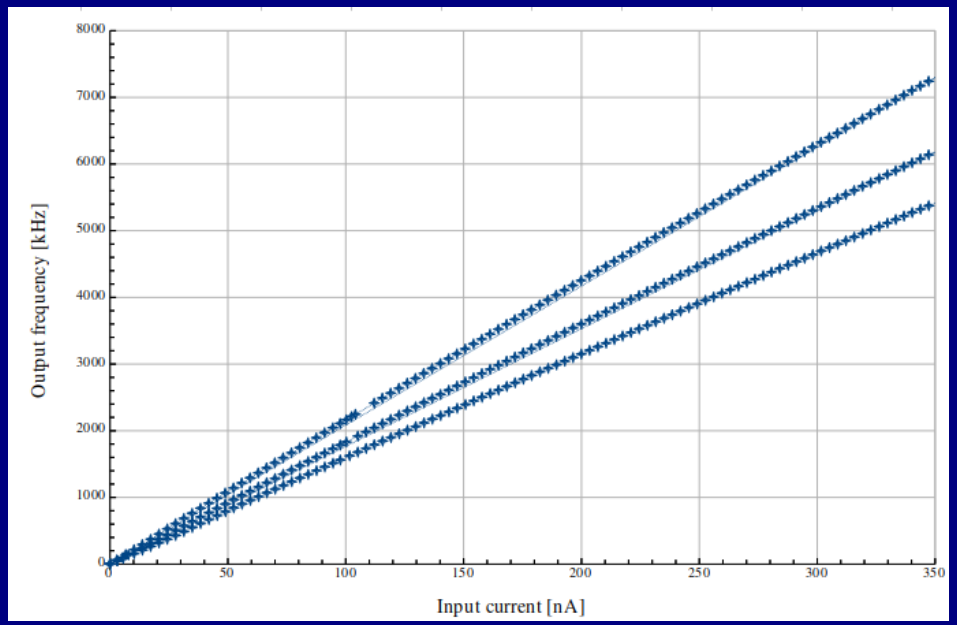
- Frequency vs input current for C_{INJ} between 3 and 7
- Clock frequency 200 MHz
- Channel 0 not responding (to be understood)

Transfer function - more measurements

Channel 4, range 0-350 nA

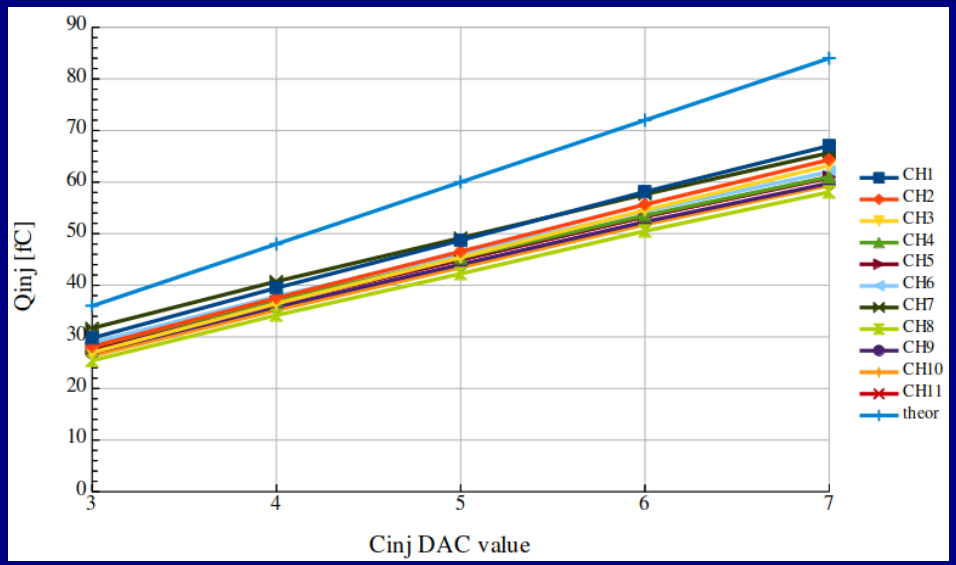


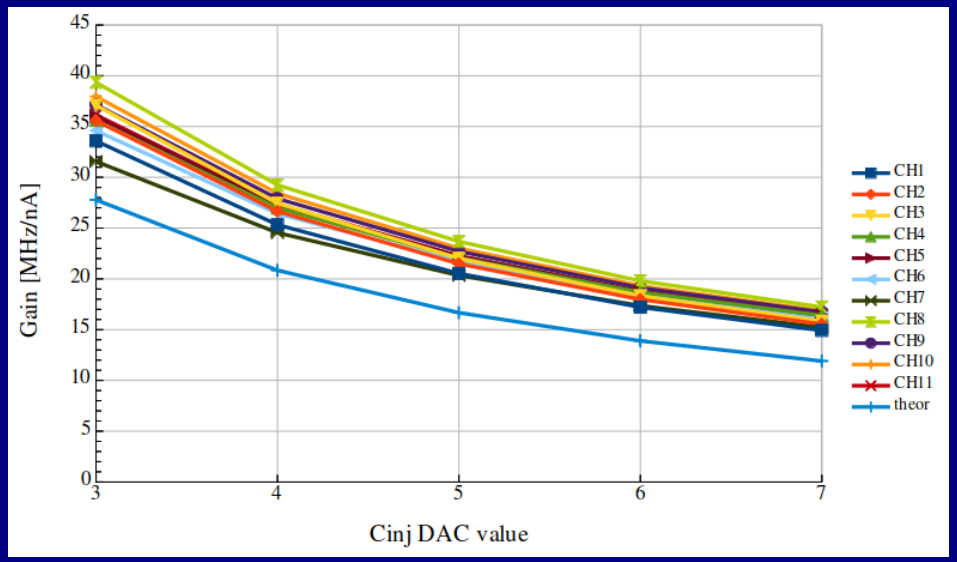
Channel 8, range 0-350 nA



- More measurements ongoing - *some setup modification needed to explore lower and upper range*
- Modification of FPGA code to increase clock speed from 200 MHz to 350-400 MHz ongoing.

Gain

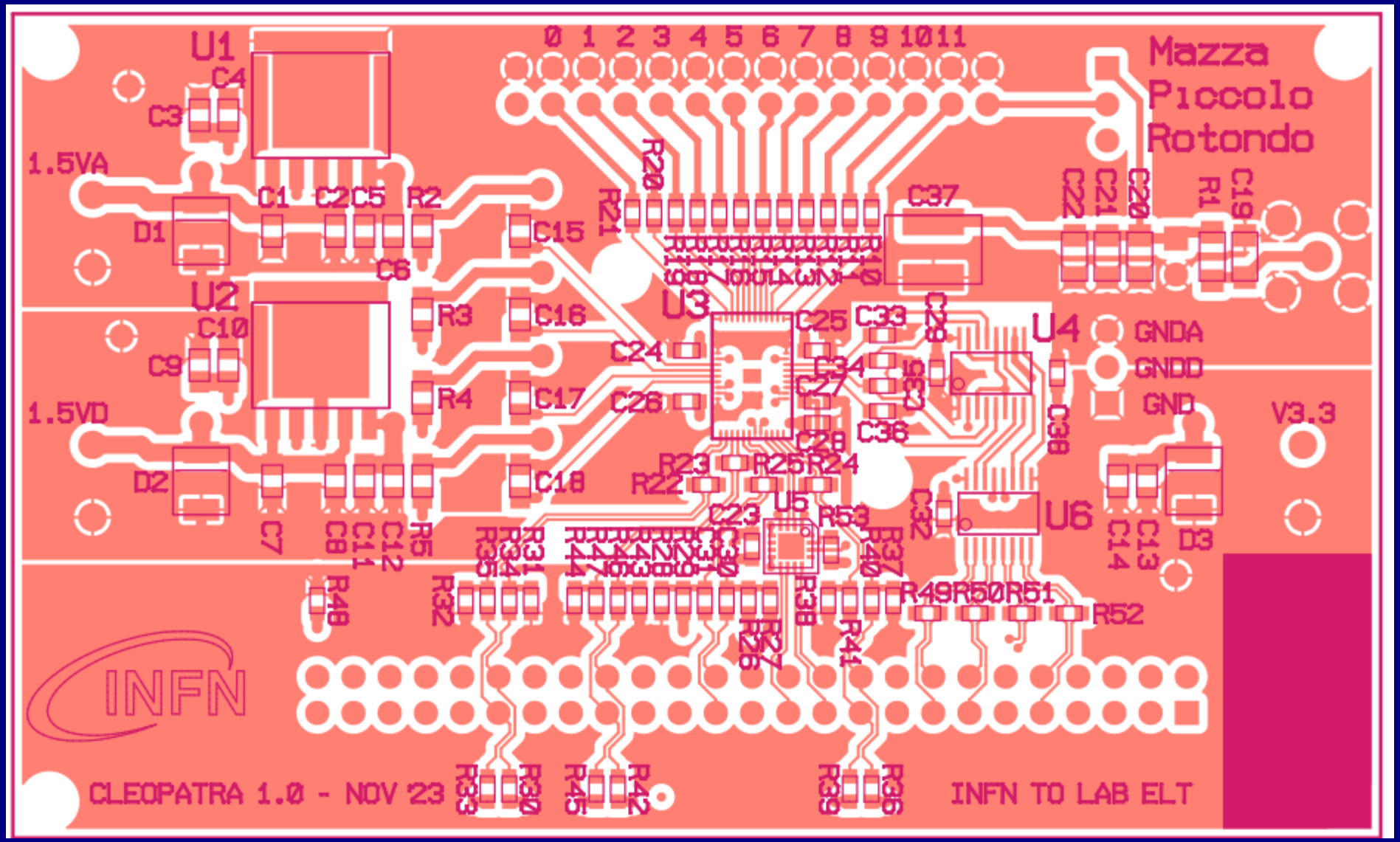




Difference between measured and theoretical values due to parasitic capacitance

	avg	σ	theor.	Unit
slope	8.514	0.419	12.0	fC/Cinj_DAC
offset	2.772	1.807	0	fC

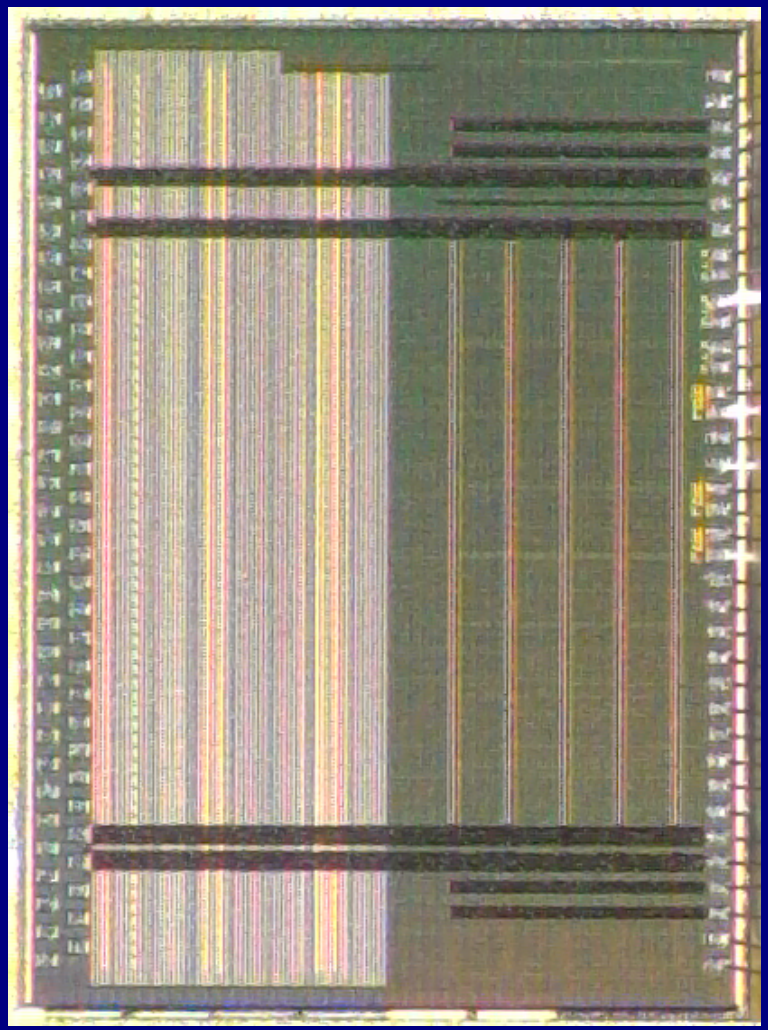
Test board layout



Cleopatra v2.0

- Based on v1.0, 32 or 64 channels
- 32 channels
  - Estimated size : 1.5×2 mm^2
  - Possible package : QFN64 9×9 mm^2 €163/pkg
- 64 channels
  - Estimated size : 2.8×2 mm^2
  - Possible package : CERQUAD FP 128, 11.6×11.6 mm^2, €194/pkg
- Submission in 2H2024

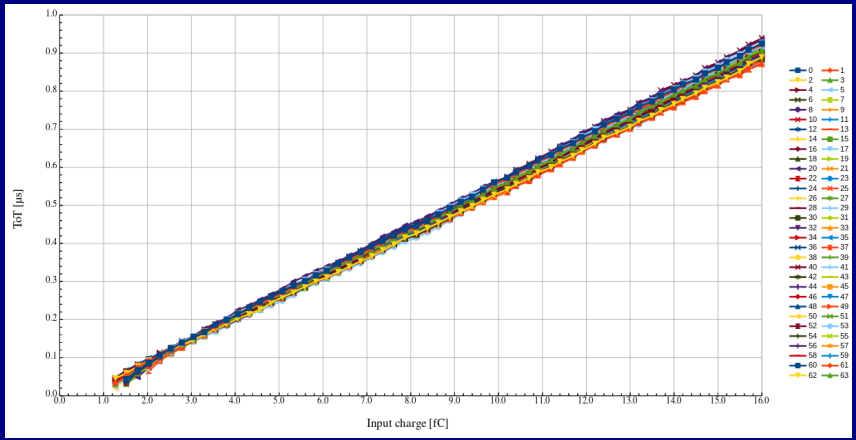
Chip for single particle detection



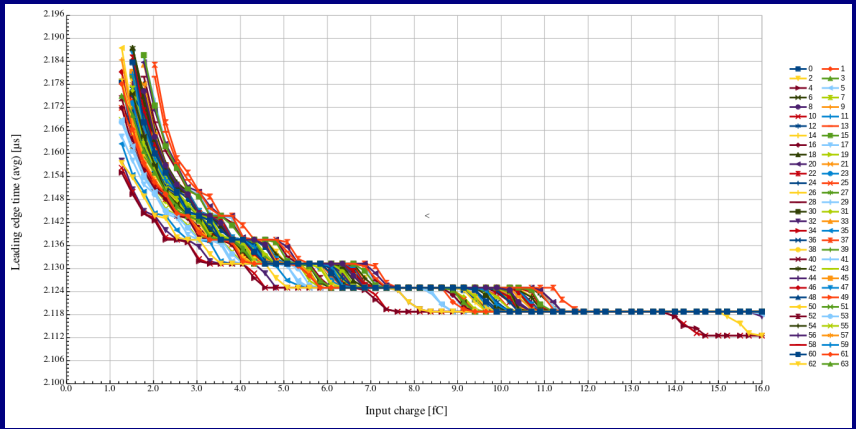
- Designed for the PANDA MVD
- 64 channels ASIC for strip readout
- Detector capacitance 2÷17 pF
- ToA and ToT measurement
- Input charge up to 50 fC
- Reference clock 160 MHz
- Time resolution (rms) 1.8 ns
- CMOS UMC 0.11 μm technology
- ToASt v2 submitted to foundry
  - same functionality, improved radiation tolerance

Test results

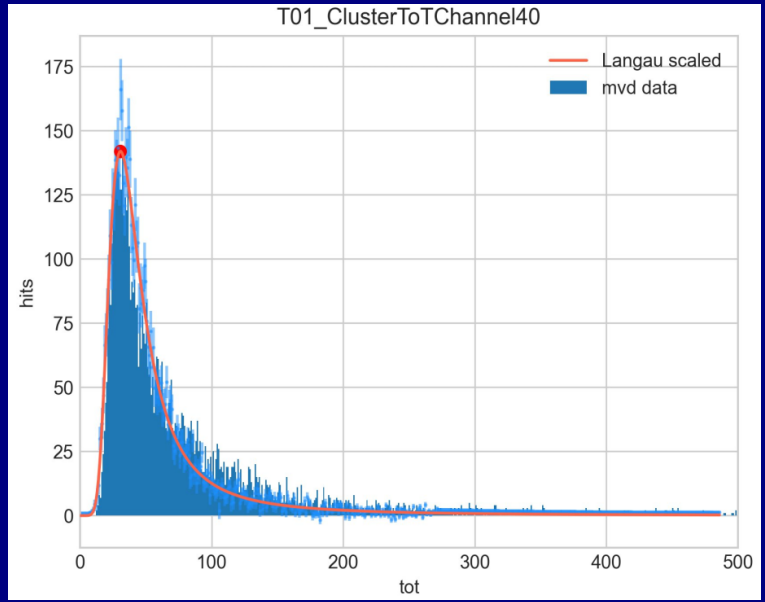
Linearity after calibration (Gain 60ns/fC)



Time resolution (before ToT correction)



Beam test at COSY (Juelich)



Proton beam, 2-3 GeV/c, $10^7 \div 10^8$ p/s

Summary

- Test of the Cleopatra prototype ongoing
- First results shows very good linearity
- Fairly large space of parameters
  - 3 amplifier configuration
  - 7 charge injection setting (+ voltage pulse height analog control)
  - positive and negative currents
  - Clock frequency range
  - Analog parameter tuning
- ToASt ASIC successfully tested on a beam test with SSD
- Preliminary work started in Torino to test ToASt with aSi:H