HASPIDE WP2: Electronics and DAQ

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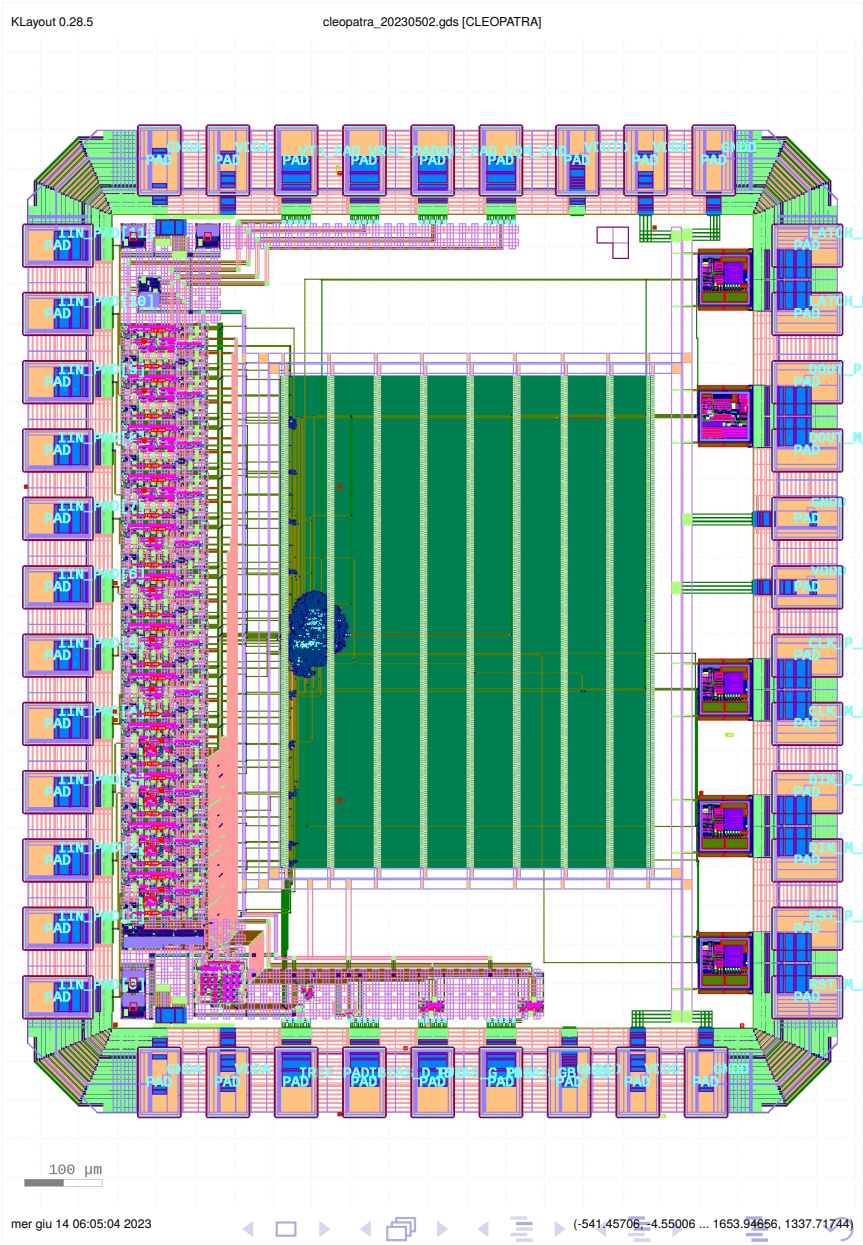
HASPIDE WP2 Activities

Two targets:

1. Clinical dosimetry and radiation flux measurement
   - Current signal from the detector, to be converted in frequency, then digitized (counting pulses) and acquired by an FPGA-based DAQ board
2. Single particles and neutron detection
   - Single charge pulse read-out solution (based on a previosly designed chip); data acquisition by an FPGA-based board

1. Clinical dosimetry

- First miniAsic in 28 nm CMOS received (cleopatra), and assembled on the test board – Torino
  $\longrightarrow$ Characterization ongoing – see Gianni's presentation for first results
- No need for the second miniASIC; we will design the final chip
- 128-channel data acquisition system – Wollongong – see Marco's presentation
- modified board and control software for TERA 08 – LNS – see next slides



2. Single particle detection

- ToASt chip (110 nm) tested for the PANDA experiment – Torino
- new version of the ToASt chip designed, to improve radiation hardness – Torino
- ongoing activities to adapt or redesign the ToASt board, to accommodate the Haspide sensor – Torino

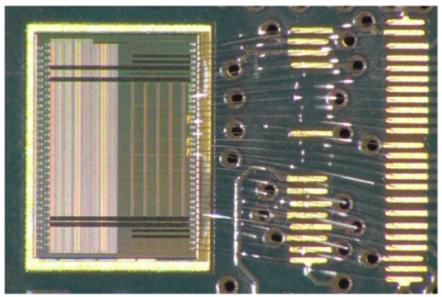


Figure 4. ToASt microphotograph.

ToASt : A 64 Channels Readout ASIC for Silicon Strip Detectors in 0.11 μm CMOS Technology

Giovanni Mazza, *Member, IEEE*, Fabio Cossio, Daniela Calvo, Marco Mignone, and Richard Wheadon

***Abstract*—A 64-channel Application-Specific Integrated Circuit (ASIC) has been designed for the readout of the Silicon Strip Detectors that will equip the Micro Vertex Detector of the PANDA experiment. The ASIC, named ToASt, provides both time of arrival and released energy measurement of the particle crossing the detector.**

The ASIC is synchronous to a 160 MHz master clock, which also sets the time resolution. The time of arrival of both the rising and the falling edge of the preamplifier outputs are recorded and transmitted, togheter with the channel address, via two serial links. A programmable discharge current is used to reset the front-end amplifier integrating capacitor in order to provide a linear ToT measurement.

The ASIC is implemented in a commercial CMOS 0.11 μm technology. The Triple Modular Redundancy technique has been implemented in most of the digital logic to protect the circuit from Single Event Upsets.

***Index Terms*—Analog-digital integrated circuits, Silicon radiation detectors, Radiation hardening.**

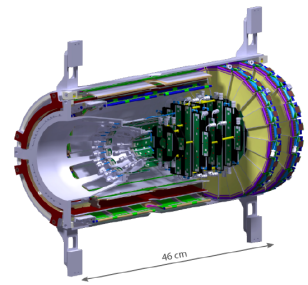


Fig. 1. PANDA Micro Vertex Detector.

G. Mazza, F. Cossio, D. Calvo, M. Mignone and R. Wheadon, "ToASt: A 64 channels readout ASIC for silicon strip detectors in 0.11 µm CMOS technology," *2021 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, doi: 10.1109/NSS/MIC44867.2021.9875549.

G. Mazza et al., "A 64 channels ASIC for the readout of the silicon strip detectors of the PANDA micro-vertex detector," *JINST*, vol. 18, C01020, 2023.

Activities at LNS (1/3)

Haspide Project at INFN-LNS

1

Main goal

Realize an electronic chain based on the TERA-08 chip, modified for laser-driven applications, able to work in two different configurations: continuous and pulsed proton beams.

- **TERA-08 chip was realized by INFN-TO and available on the market through DE.TEC.TOR. s.r.l. company**
- **It was designed for continuous beams**
- **LNS-INFN group modified it for pulsed beams (laser-driven applications)**
- **Acquisition by means of a PXIe FPGA 782x board**

- **1-year post-doc position (Bando INFN N. 25885/2023)**
  "Development and characterization of front-end electronics for a-Si detectors in the framework of the HASPIDE call"
- **Dr. Mariacristina Guarrera (from january 31st, 2024)**
  (hardware assembling, software developing, electronic read-out characterization, experimental runs with pulsed beams)

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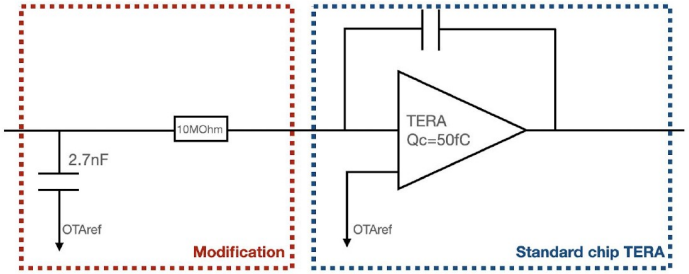
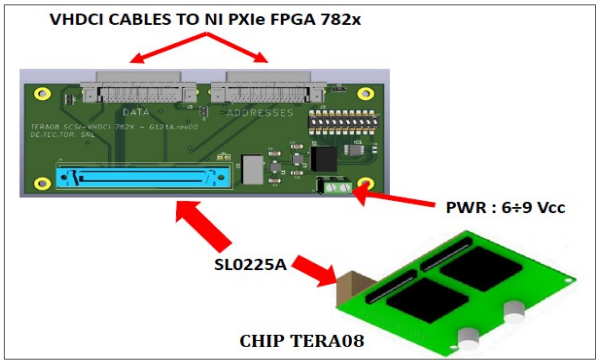
Electronic chain for pulsed beams



Thanks to: Antonino Amato (INFN-LNS)



SETUP CONFIGURATION FOR ACQUISITION
WITH NI PXI CRATE AND PXIe FPGA 782x BOARD

- NI PXIe-1071 chassis
- NI PXIe-7821R → Digital I/O

The Digital I/O module include a FPGA (Kintex-7 160T type, National Instruments)

We will use LabView to configure the FPGA and set the characteristics of the acquisition system. In addition, LabView enables on-line data processing, resulting in a significant spare of time.

We will use an electronic board to connect the chassis I/O modules to the TERA08. The board was specifically designed by DE.TEC.TOR. s.r.l. to allow the connection between the two devices, which have different binning characteristics.

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Time schedule (2024)

Time schedule

- **Hardware assembling – within March 2024**
- **Realization and optimization of the software control system – within April 2024**
- **Read-out characterization (background current, linearity of current-to-frequency conversion, charge conversion efficiency, gain uniformity, channel cross-talking) – within June 2024**
- **Detector characterization with pulsed proton beams accelerated by laser-matter interaction at ELI-Beamlines (Prague, Czech Republic) – from July-August 2024**

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Activities and resources for 2024

Activities in 2024

- complete the characterization of the cleopatra prototypes
- choice of the best front-end architecture (the first prototype has 12 channels: 4 inputs for each type of front-end)
- design of the final chip (easy task if cleopatra works well): Milano + Torino
- design (adaptation) of the test board for ToASt + HASPIDE sensor

Milestones: complete these tasks and submit designs before end of 2024

Financial resources for 2024

Funding for 2024

- 75 k€ for consumables (second chip in 28 nm) and boards – SUB IUDICE, probably to be unlocked in Sepember
- 25 k€ for services ("Assegno di ricerca" – 1 year)
  - 1 candidate in Milano, will graduate in Apr. 2024
  - funds for AdR have been unlocked and are available
    $\longrightarrow$ we can start the procedure for the call
  - very last deadline for the call: July 31, 2024

Papers

A conference paper describing the cleopatra chip will be submitted to the MOCAST conference: **http://www.mocast.eu**
4 pages, IEEE conference format; Final deadline: March 15

A Front-End Circuit in 28 nm CMOS for Hydrogenated Amorphous Silicon Detectors in Clinical Dosimetry

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