Reconfigurable Electronics for Experimental Physics

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Outline

- FPGA-embedded Hadron Fluence Sensors
  - PHI experiment CSNV (INFN NA + JSI)
- Beyond-CMOS Hardware for Machine Learning

FPGA-embedded Hadron Fluence Sensors

Motivation

- SRAMs used as fluence sensors at LHC [1] and in proton therapy [2]
- Hadrons with energy>few MeV and thermal neutrons may indirectly induce SEUs in SRAMs

hadron fluence

upset count

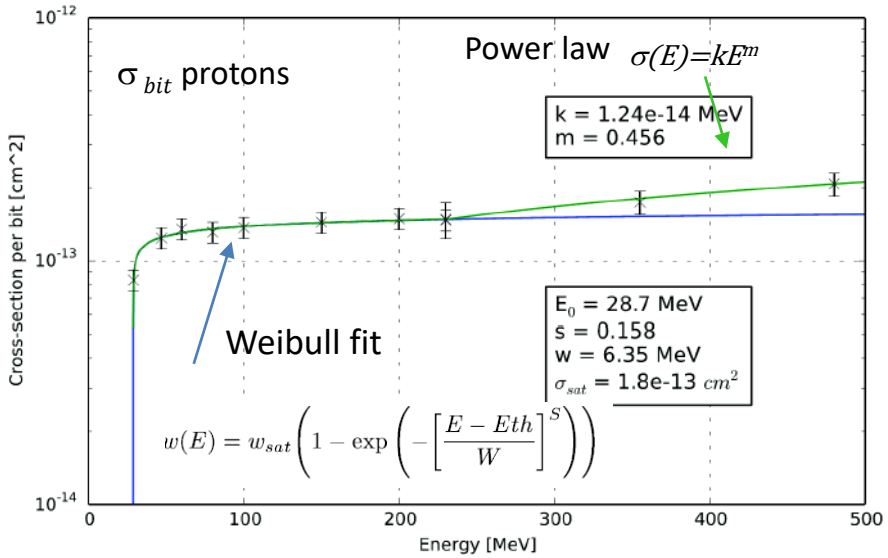
$$\Phi = \frac{N_{upsets}}{\sigma_{bit}\, N_{bits}}$$

cross section per bit

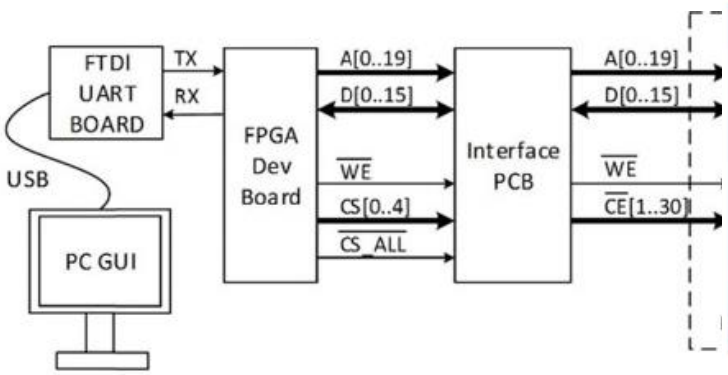
memory size

- $\sigma_{bit} = \sigma_{bit}$(device, V_{DD}, hadron, E)
- Sensor SRAM + readout device (FPGA [3])
  - Complex interface and PCB
  - Radiation hardening issues related to the readout circuitry

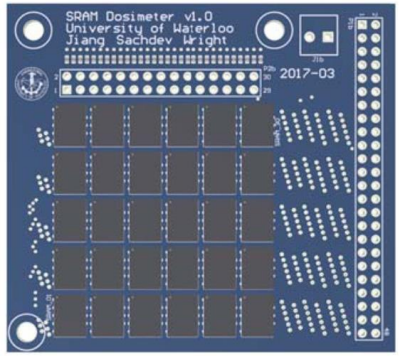
SRAM Cypress CY62157EV30 8Mb (90nm) [1]



SRAM readout chain [3]



SRAM array

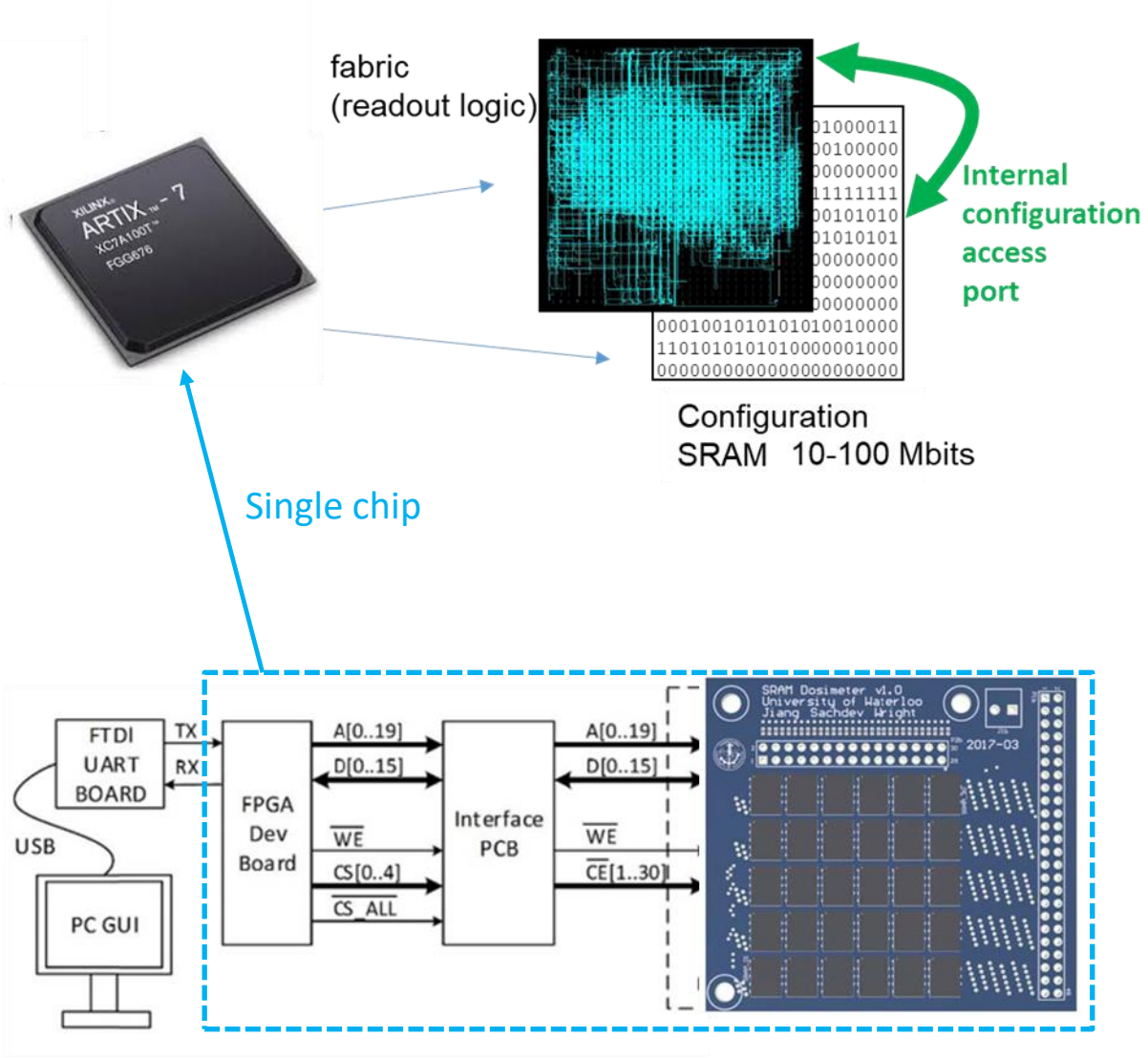


Radiation beam

[1] S. Danzeca et al., 2014, doi: 10.1109/TNS.2014.2365042
[2] K. S. Ytre-Hauge et al., 2019, doi: 10.1016/j.radmeas.2019.01.001
[3] E. Blackmore et al., 2019, doi: 10.1109/TNS.2018.2884148.

SRAM-based Field Programmable Gate Arrays

- FPGAs embed programmable fabric and configuration SRAM (CRAM) [1]
- Programmable fabric can access CRAM via dedicated internal ports (ICAP for AMD/Xilinx)
- Many devices are TD-tolerant (>few kGy) and latch-up free
- FPGA as a compact hadron fluence counter
  - CRAM as sensitive element + fabric programmed as readout
- Opposite requirements
  - CRAM as sensitive as possible to SEUs (sensor)
  - firmware as robust as possible against single event effects (readout)

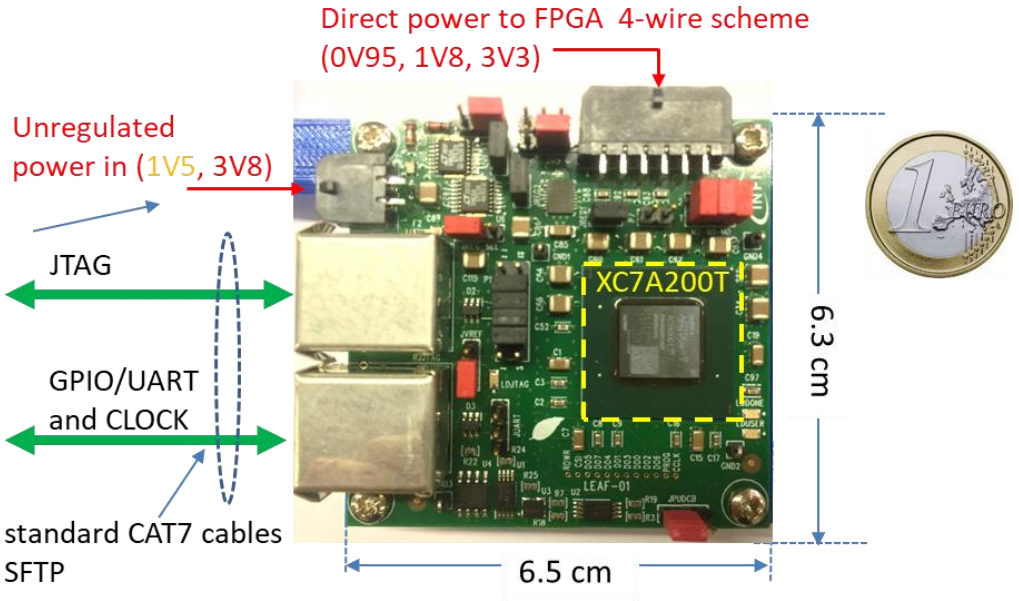


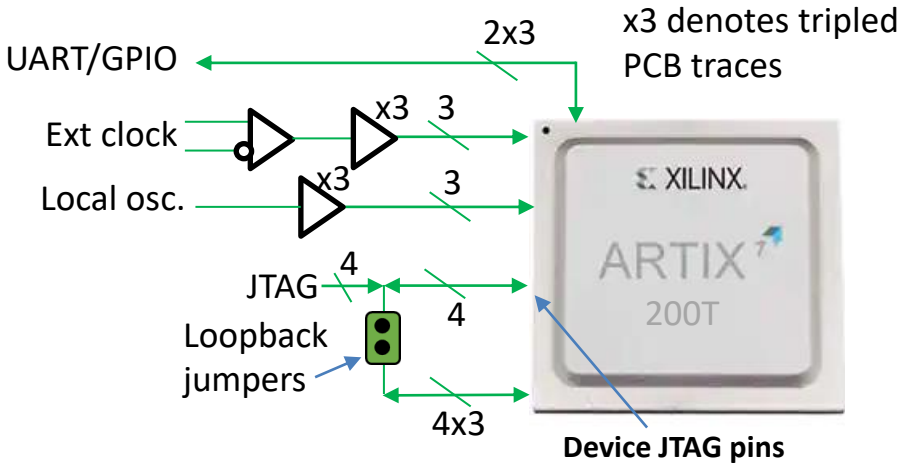
Early study on correlation between fluence and upsets

[1] V. Bocci et al., 2001, doi: 10.5170/CERN-2001-005.137

FPGA-Embedded Hadron Fluence Sensor

- Compact PCB
  - Only COTS components, radiation tolerance studies in [1,2]
  - Low power consumption (~0.7 W)
- AMD/Xilinx Artix-7 FPGA
  - 28nm CMOS
  - 59 Mb CRAM + 18 Mb BRAM
  - Expected proton-SEU σ_{dev} = $5.5 \cdot 10^{-7}$ cm^2 (CRAM)
- Radiation-Hardening by Design on PCB and firmware
  - Triple traces for clock, UART, JTAG self-scrubbing (loopback)



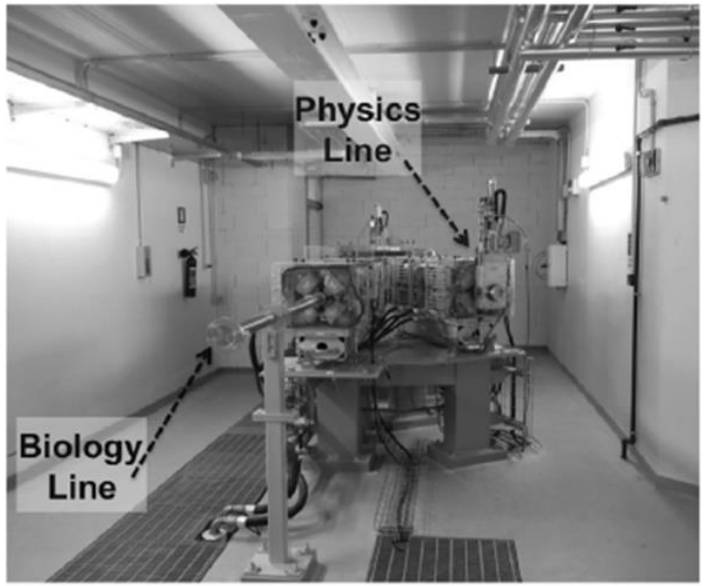


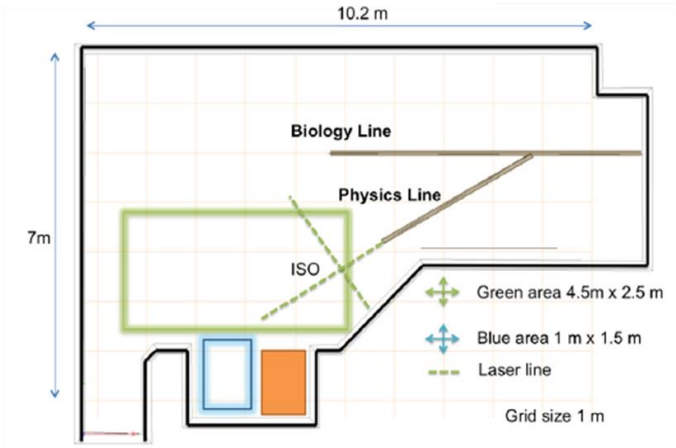
[1] T. Higuchi et al., 2012, doi: 10.1088/1748-0221/7/02/C02022
[2] Y. Yu Nakazawa et al., 2020, doi: 10.1016/j.nima.2019.163247

Proton Irradiation Facility

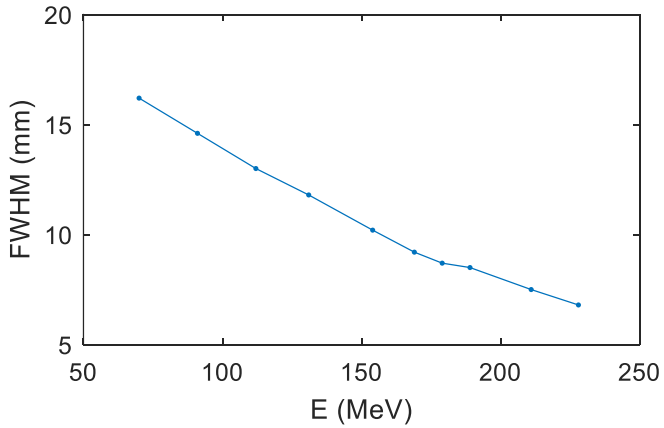
- INFN facility: Trento Institute for Fundamental Physics and Applications (Trento, Italy)
- Cyclotron provides monoenergetic protons from 70 MeV to 228 MeV (energy degraders)
- Intensities 10^6 to 10^8 p/s
- Gaussian beam
- Beam spot size depend on energy
- Real-time proton counting provided by the facility (ionization chamber)

TIFPA's Experimental Room



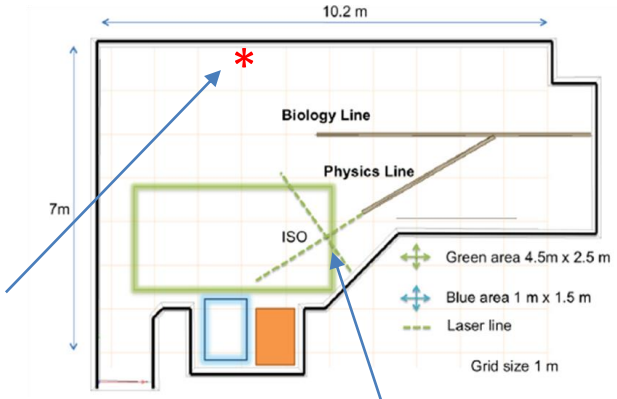


Beam spot @ ISO center



Test Setup

- DAQ Personal Computer
  - FPGA configuration and readback w/ SEU logging
  - Power supply management and logging
  - Functionality test between irradiation runs



Nearly 5m away from sensor

Keysight N6705A Power Supply

Ethernet

To FPGA

12

4-wire sensing scheme
1.0V, 1.8V, 3.3V

Remote terminal to DAQ computer in control room

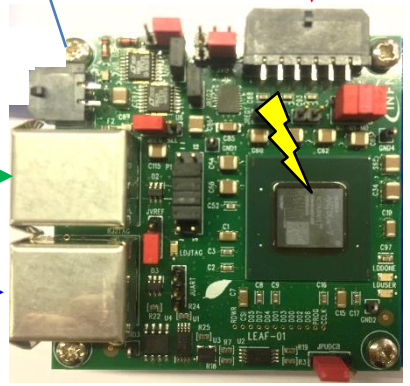
Ethernet

Ethernet

Interface Board

JTAG

GPIO & clock



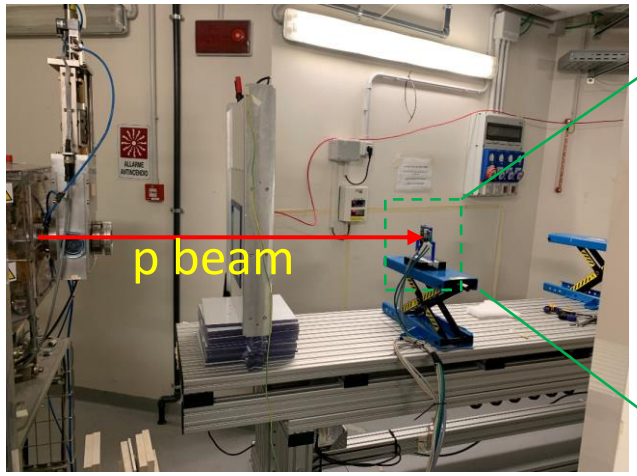
Custom Ethernet-enabled JTAG programmer

Irradiated sensor at ISO center

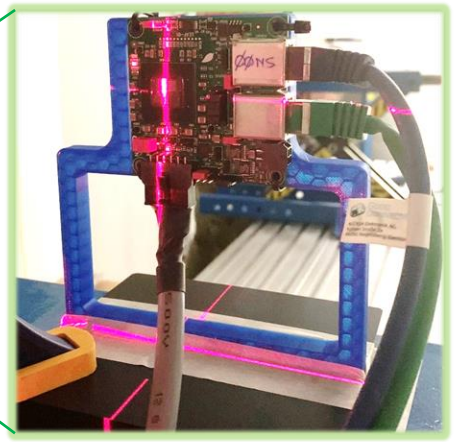
Test Conditions

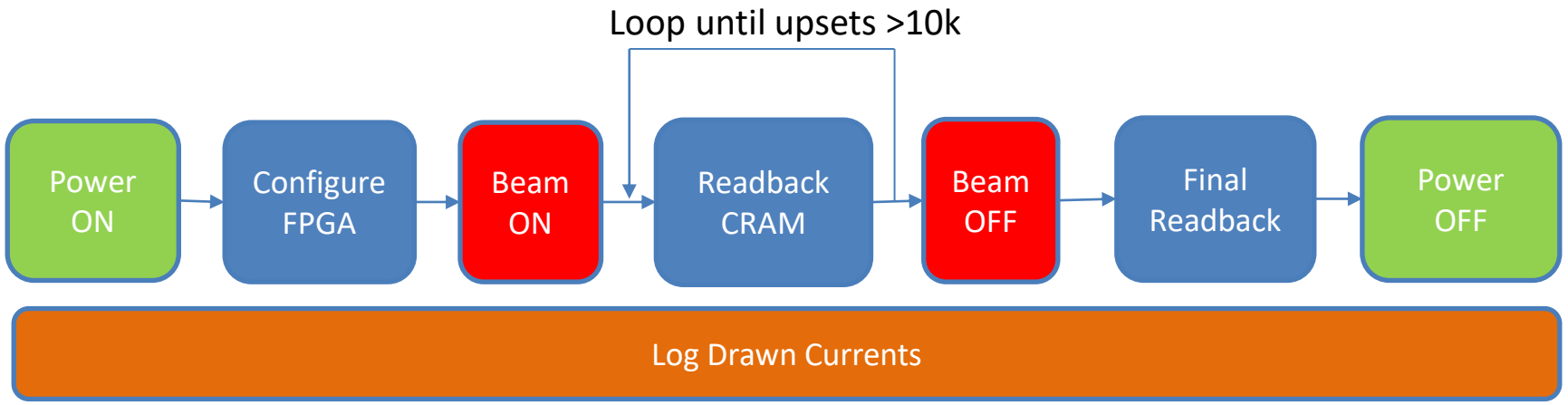
- Total proton fluence delivered over six units $1.3 \cdot 10^{13}$ p/cm^2
  - i.e., average $2.1 \cdot 10^{12}$ p/cm^2 per sample
- Average flux $6.7 \cdot 10^{8}$ p/(cm^{2}s)
- Test partitioned in runs with more than 10k upsets each (count uncertainty < 1%)
- Average temperature of chip stable within 2°C in a run
- Test run procedure

Physics line



Sample positioned at ISO center

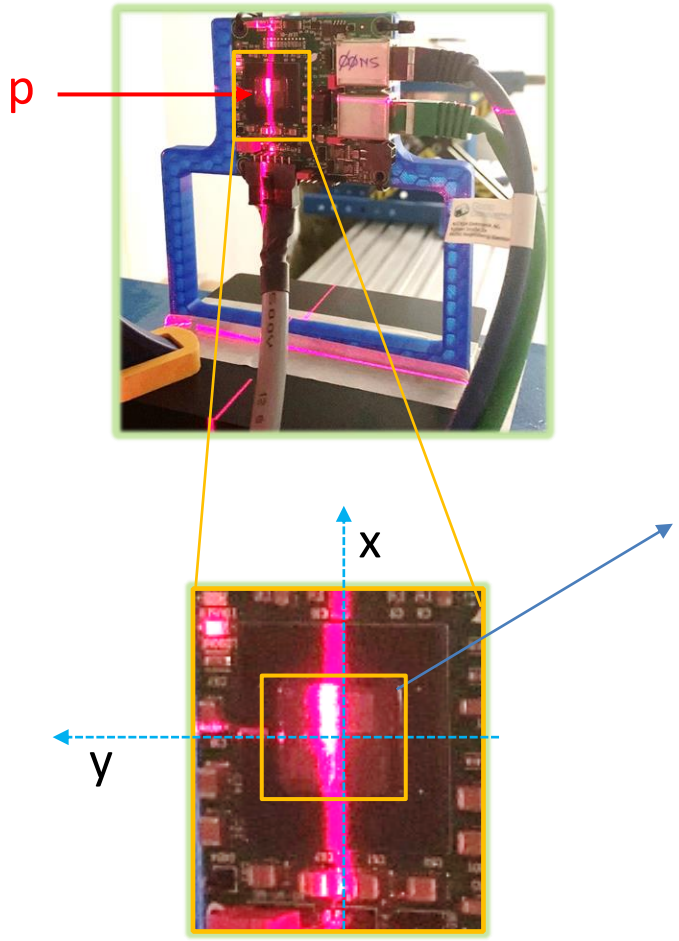


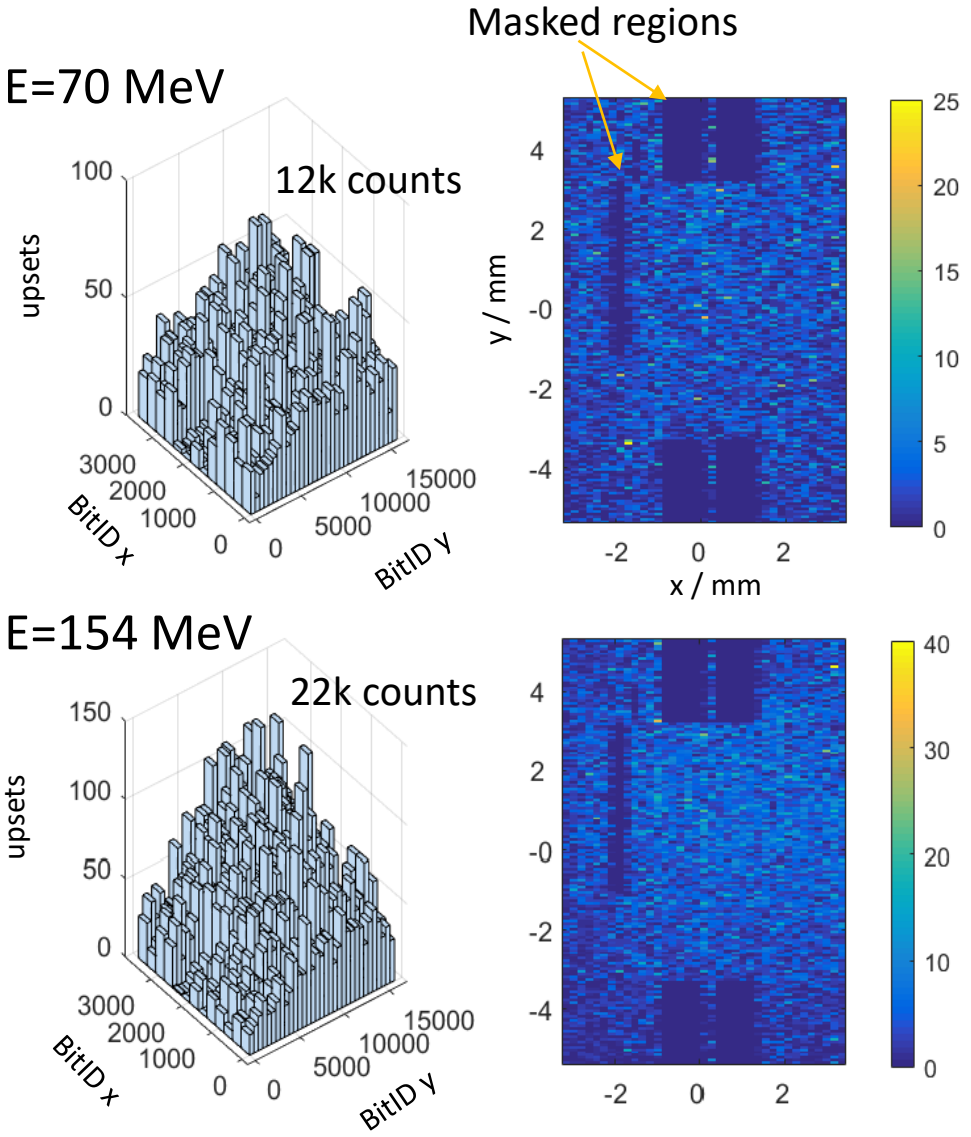


Total fluences on samples	
Sample code	Φ (10^{12}p/cm^2)
SN03	4.7
SN04	2.5
SN05	1.1
SN06	1.9
SN07	1.3
SN08	1.2

Imaging the Beam with an FPGA

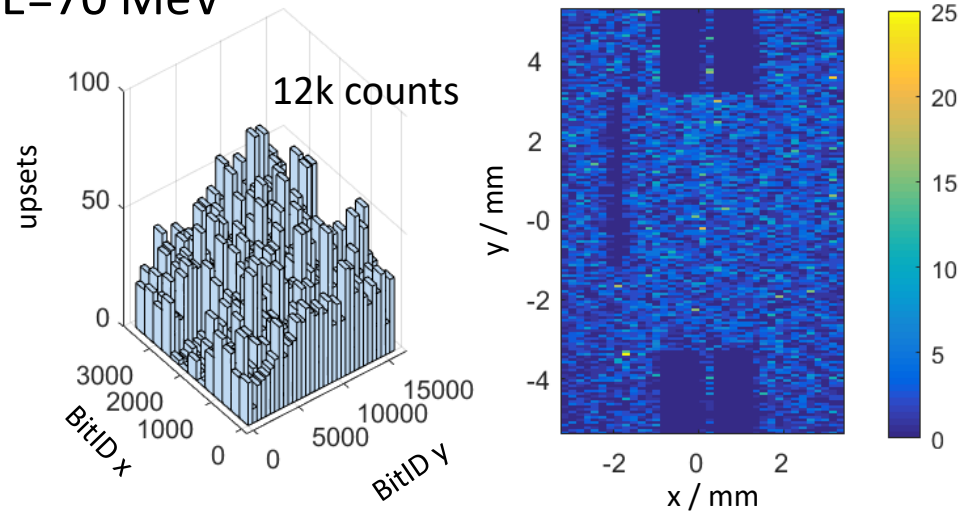
- Readback CRAM bitmap
- Cluster adjacent bits, 1 cluster = 100 bits x 100 bits
- Upsets per cluster => histogram and density map
- Approximate proton beam image
- Masked regions



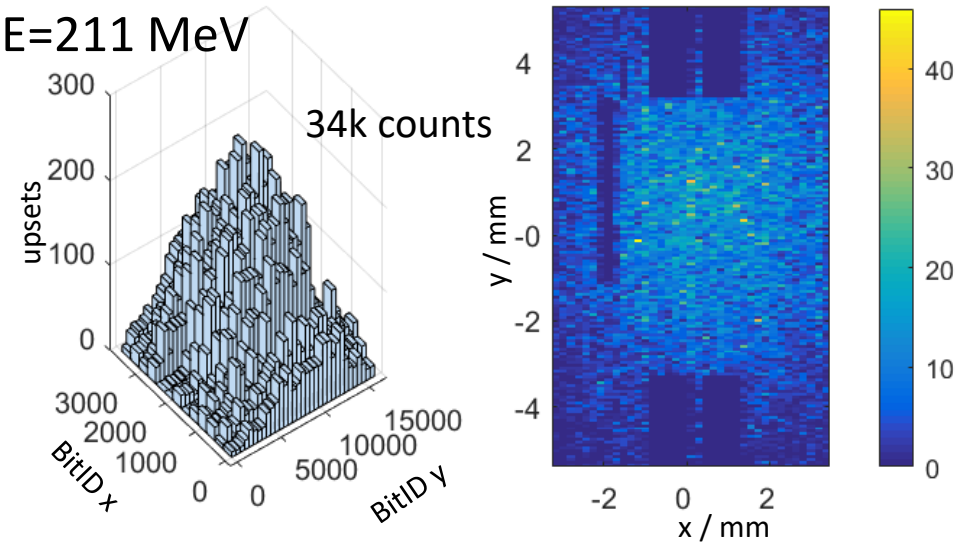


Beam Image Vs Proton Energy

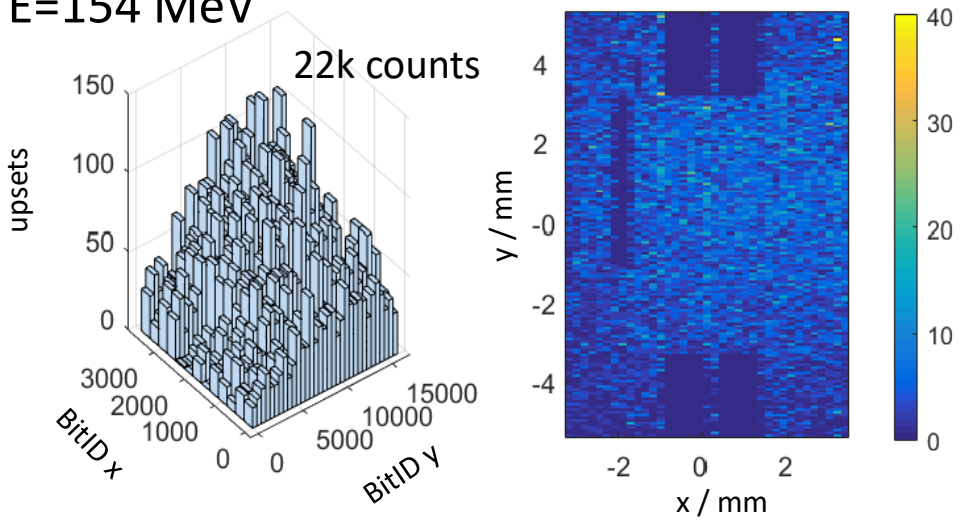
E=70 MeV



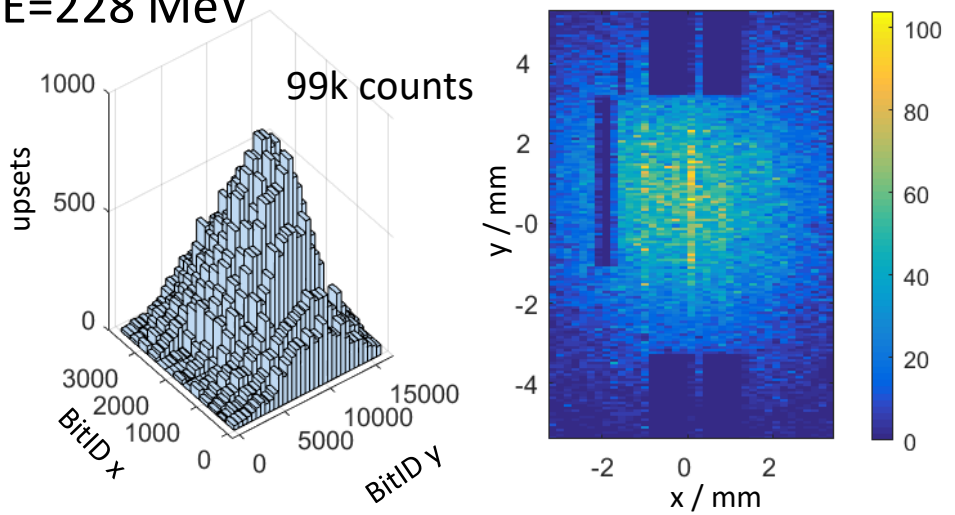
E=211 MeV



E=154 MeV

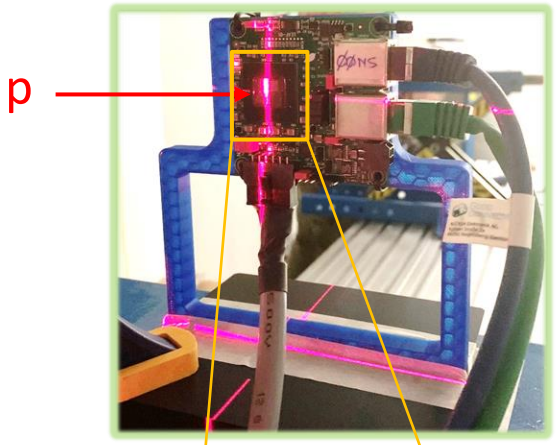


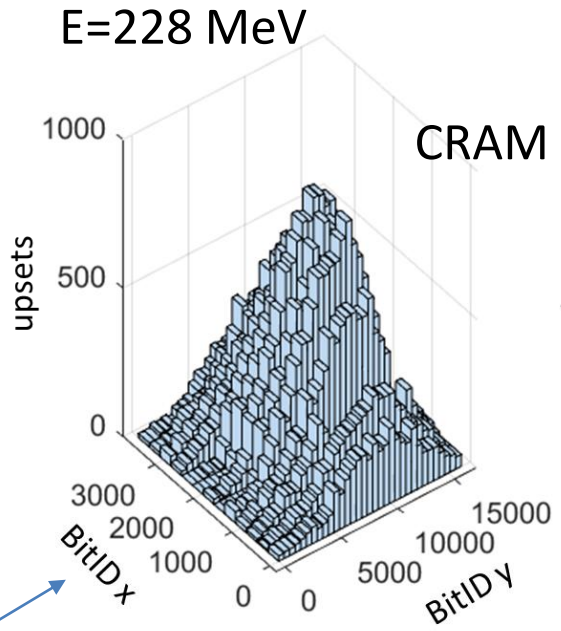
E=228 MeV

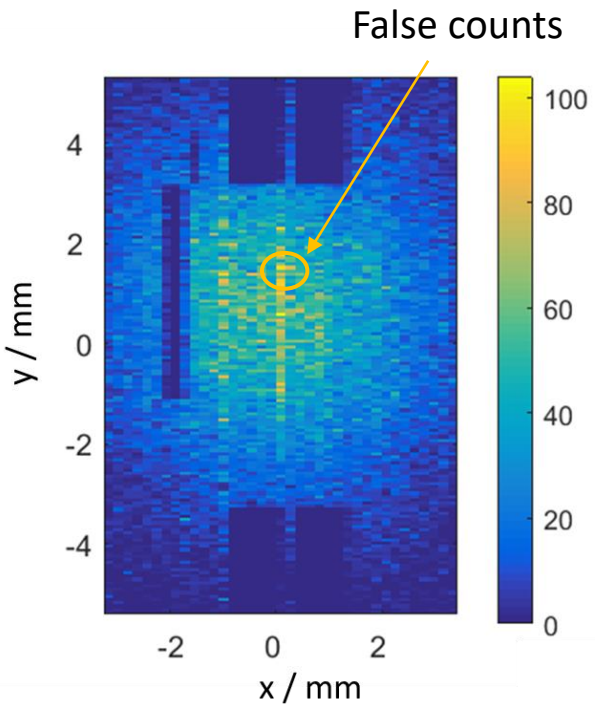


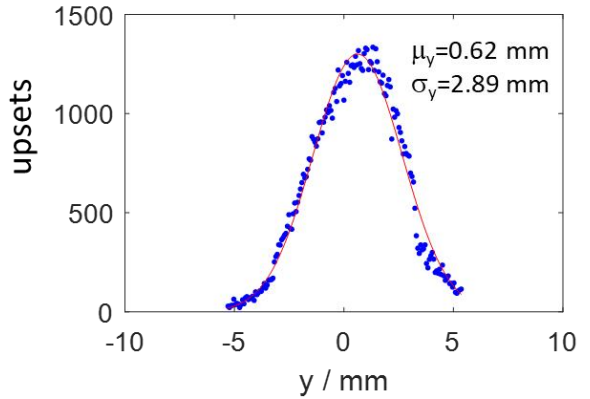
Imaging the Beam with an FPGA (2)

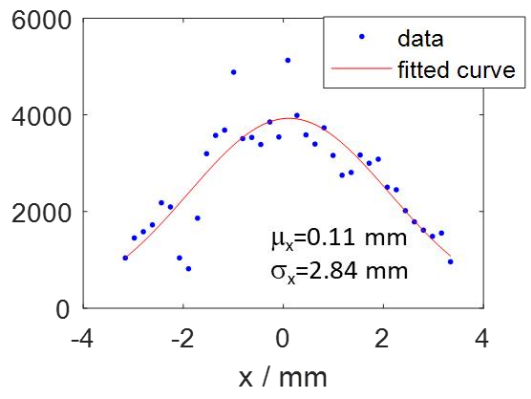
- Useful to check sample alignment and estimate proton fluence
- CRAM access logic SEFIs => false counts
- JTAG failed (13 times), but very reliable
  - $\sigma_{JTAG} = 1.0 \pm 0.2 \cdot 10^{-12}\ cm^2$







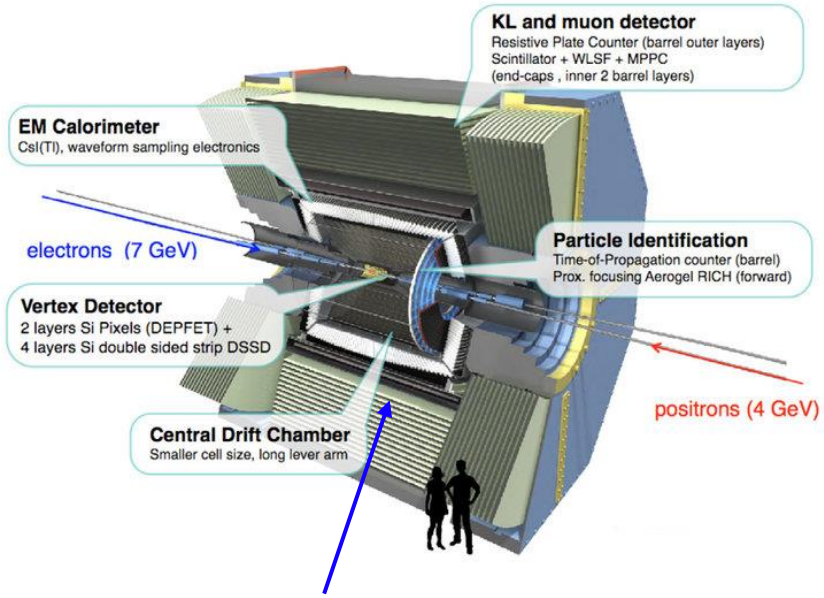


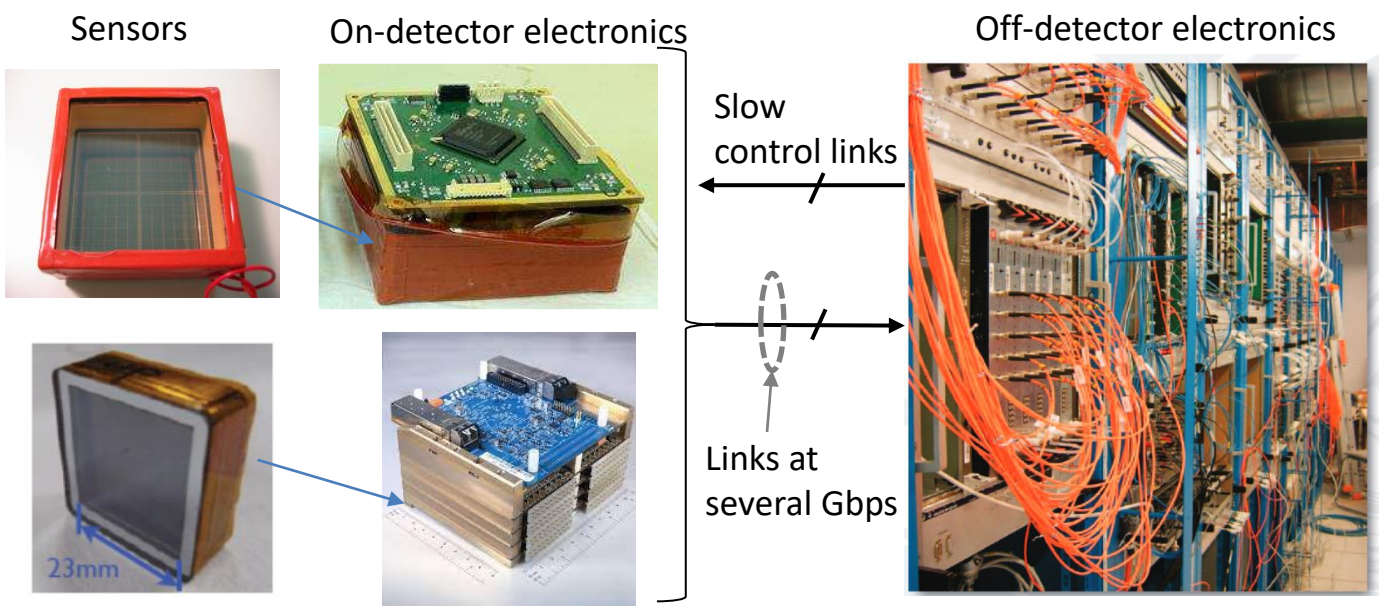


Outlook:
Beyond-CMOS Hardware for Machine Learning

Motivation

- Trigger and data acquisition systems in HEP are complex
  - Many heterogenous (fast) sensors, ~10-100 millions of electronic channels
  - ~1-10 Petabyte/year raw data rate
- Complexity will grow even more, power consumption too
- on/near-sensor processing for reducing data rates and triggering
  - ECFA recommendation [1]
- Reconfigurability required
  - e.g. search for different physics processes, change of collider conditions





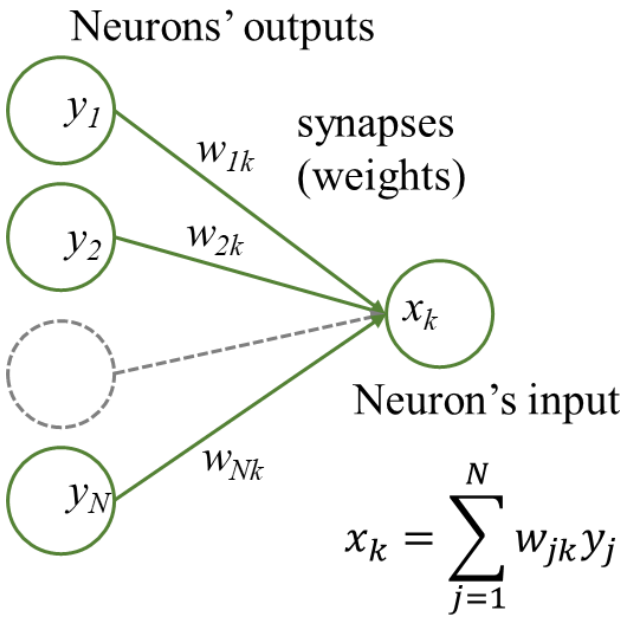
[1] www.doi.org/10.17181/CERN.XDPL.W2EX

Digital-Circuit-based Machine Learning

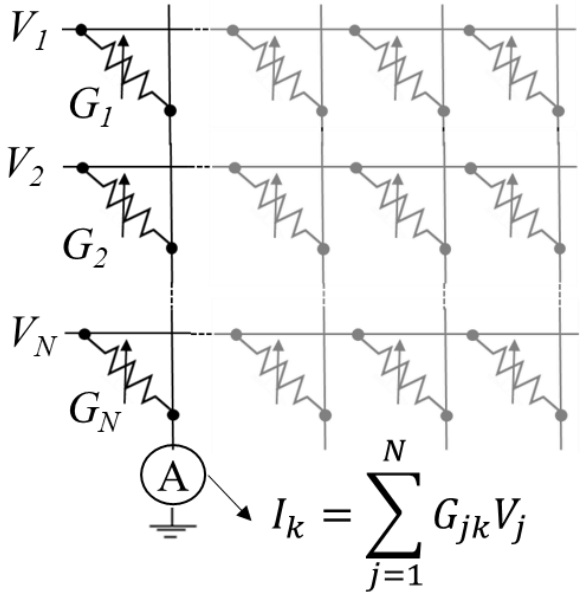
- ML today widely used in off-line data processing
- Fast (i.e. on-line) ML increasingly being used, even on detector
  - Mostly FPGA and ASIC-based implementations
  - Examples of trigger [1,2] (off-detector) and data compression [3] (on-detector)
  - Latency: tens of ns (ASIC) to microseconds (FPGA)
- CMOS digital hardware designed for logic and arithmetic
  - not optimized for Neural Networks

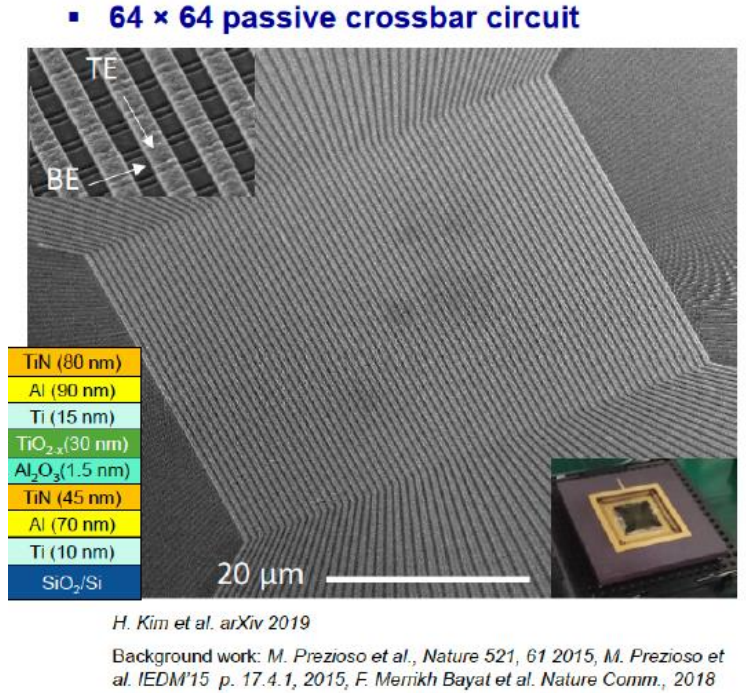
[1] www.doi.org/10.48550/ARXIV.1910.13679
[2] www.doi.org/10.1051/epjconf/202024501021
[3] www.doi.org/10.1109/TNS.2021.3087100

Beyond-CMOS Hardware for Machine Learning



Memristor crossbar





H. Kim et al. arXiv 2019

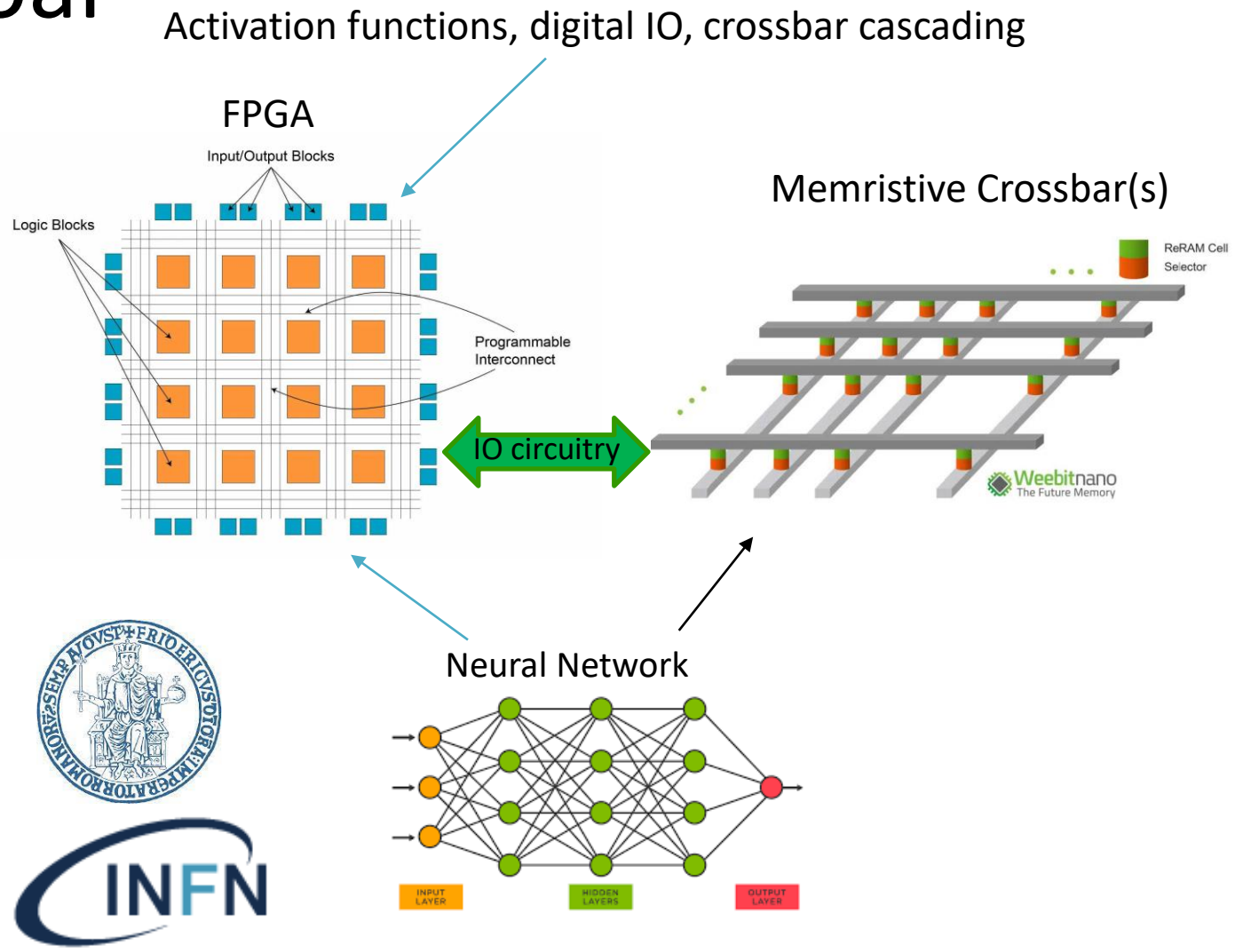
Background work: *M. Prezioso et al., Nature 521, 61 2015, M. Prezioso et al. IEDM'15 p. 17.4.1, 2015, F. Merrikh Bayat et al. Nature Comm., 2018*

https://doi.org/10.1038/s41467-021-25455-0

- Emerging hardware represents directly neurons and synapses
  - Memristors: CMOS-compatible, high circuital density (Tb/cm^2) and low power consumption (fJ 100x100 VMM at 6b)
  - Computing in memory
- R&D required to leverage new hardware, PRIN at Unina (PI) + INFN

Goal

- Demonstrate fast hybrid digital-neuromorphic computing with FPGAs interfaced to memristive crossbars
  - Perform analog-grade IO with compact circuitry
  - Study of performance and limiting factors (e.g. memresistance granularity)
  - Compare with full digital ML implementations
- Case Study
  - Graph-based Neural Networks for anomaly detection



NA - RM1

Conclusions

- Reconfigurable electronics is pervading physics experiments
  - Can be used for computation but also for radiation detection
- Beyond-CMOS Hardware available for artificial neural networks
  - Need to investigate novel hybrid digital-neuromorphic systems