HASPIDE WP2: Electronics and DAQ

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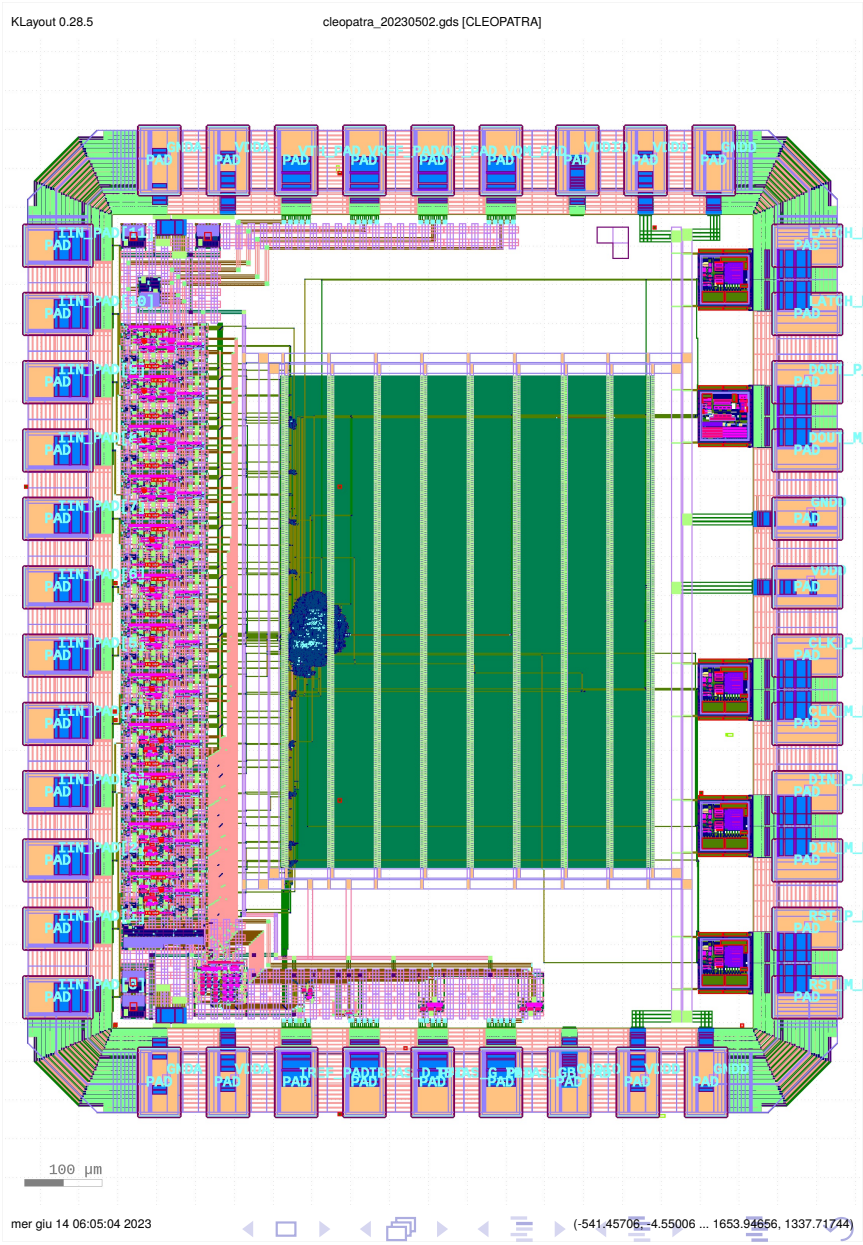
HASPIDE WP2 Activities

Two targets:

1. Clinical dosimetry and radiation flux measurement
   - Current signal from the detector, to be converted in frequency, then digitized (counting pulses) and acquired by an FPGA-based DAQ board
2. Single particles and neutron detection
   - Single charge pulse read-out solution (based on a previosly designed chip); data acquisition by an FPGA-based board

1. Clinical dosimetry

- First miniAsic in 28 nm CMOS received (cleopatra)
- Test board produced (5 boards), but not received yet – Torino
- TO DO:
  - test of the prototypes
  - choice of the best front-end architecture (12 channels: 4 inputs for each type of front-end)
  - design of the final chip (easy task if cleopatra works well; **personpower needed if front-end redesign is required**)
- 128-channel data acquisition system – Wollongong – see Marco's presentation
- modified board and control software for TERA 08 – LNS – see Mariacristina's presentation



2. Single particle detection

- ToASt chip (110 nm) tested for the PANDA experiment – Torino
- new version of the ToASt chip designed, to improve radiation hardness – Torino
- TO DO:
  - design the test board for ToASt + HASPIDE sensor (**no personpower !**)

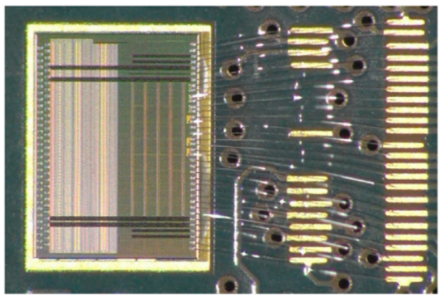


Figure 4. ToASt microphotograph.

ToASt : A 64 Channels Readout ASIC for Silicon Strip Detectors in 0.11 μm CMOS Technology

Giovanni Mazza, *Member, IEEE*, Fabio Cossio, Daniela Calvo, Marco Mignone, and Richard Wheadon

***Abstract*—A 64-channel Application-Specific Integrated Circuit (ASIC) has been designed for the readout of the Silicon Strip Detectors that will equip the Micro Vertex Detector of the PANDA experiment. The ASIC, named ToASt, provides both time of arrival and released energy measurement of the particle crossing the detector.**

The ASIC is synchronous to a 160 MHz master clock, which also sets the time resolution. The time of arrival of both the rising and the falling edge of the preamplifier outputs are recorded and transmitted, togheter with the channel address, via two serial links. A programmable discharge current is used to reset the front-end amplifier integrating capacitor in order to provide a linear ToT measurement.

The ASIC is implemented in a commercial CMOS 0.11 μm technology. The Triple Modular Redundancy technique has been implemented in most of the digital logic to protect the circuit from Single Event Upsets.

***Index Terms*—Analog-digital integrated circuits, Silicon radiation detectors, Radiation hardening.**

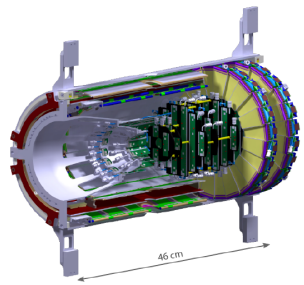


Fig. 1. PANDA Micro Vertex Detector.

G. Mazza, F. Cossio, D. Calvo, M. Mignone and R. Wheadon, "ToASt: A 64 channels readout ASIC for silicon strip detectors in 0.11 µm CMOS technology," *2021 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, doi: 10.1109/NSS/MIC44867.2021.9875549.

G. Mazza et al., "A 64 channels ASIC for the readout of the silicon strip detectors of the PANDA micro-vertex detector," *JINST*, vol. 18, C01020, 2023.

Financial resources for 2024

Funding for 2024

SUB IUDICE:

- 75 k€ for consumables (second chip in 28 nm) and boards
- 25 k€ for services ("Assegno di ricerca" – 1 year)
  - no candidates availble in Milano, nor in Torino
  - deadline for the call: July 31, 2024

Papers

A conference paper describing the cleopatra chip will be submitted to the MOCAST conference: **http://www.mocast.eu**
4 pages, IEEE conference format; deadline: Feb. 15
Preliminary measurements needed on cleopatra chip!