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Study of SEU effects in readout circuits of silicon micro-strips detectors developed in 110 nm UMC technology.

At INFN-Torino, ASICs for readout of several detectors were designed and are under development using the 110 nm CMOS UMC. This technology has been chosen for its lower cost even if there was not a systematic characterization for what concerns the radiation tolerance. Total Ionizing Dose and Single Event Upset (SEU) effects measurements are important studies to characterize ASICs and then also this new technology. Proton beams with different current intensities can be used to investigate the SEU effects as a function of particle flux and to study the dependence of the upsets rate to the clock frequency applied to the circuits. Ion beams of different energies allow the measurement of the cross section for SEU. However, the two techniques are correlated (H. Hutinen and F. Faccio, NIMA, 450, 2000). Among others, the development of full-size prototypes for the custom readout circuit of silicon double-sided microstrips of PANDA Micro Vertex Detector is a good tool to know the behavior of this technology under radiation. Some years ago, the development of this readout started with a full-size prototype named PAStA. It is a triggerless circuit and implements the Time over Threshold (ToT) technique to determine the charge and time information, it features 64 channels and presents a global controller that is common to all channels, it collects the data from the channels and distributes the configurations to the registers. The clock frequency was limited to 120 MHz. Two techniques (TMR-Triple Modular Redundancy and HE-Hamming Encoding) are applied in the configuration registers, and they were tested with ion beams at the SIRAD facility (INFN-LNL) and with proton beams in the experimental room of INFN-TIFPA, in Trento. Results from these measurements shown the robustness of these two techniques against SEU effects and collect information on the 110 CMOS nm technology under radiation (D. Calvo et al. https://doi.org/10.22323/1.370.0126). Recently a new full-size prototype named ToASt_v1 has been designed and produced. ToASt has 64 channels, grouped in 8 regions with local buffering, then the corresponding FIFOs outputs are stored in the Global Readout FIFO. Each channel provides the event timestamp and implements the ToT. The master clock frequency is 160 MHz, the circuit can work at different clock frequency (up to 200 MHz) anyway. A configuration serial link running at 80 Mb/s provides access to the channel and global configuration registers. In this new ASIC configuration registers the TMR is implemented. Evaluation of the cross section for SEU has been performed with ion beams detecting only upsets from logic 1 to logic-0. The motivation is connected to a triplication error in the Verilog code that was corrected in the ToASt_v2 submitted to the foundry the past February. The characterization with proton beams become more interesting to provide information for different clock frequencies also in anticipation of use of ToASt in other experiments.

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