

PSD firmware status

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For the IFAE-HERD group

PSD meeting, 30th January 2024

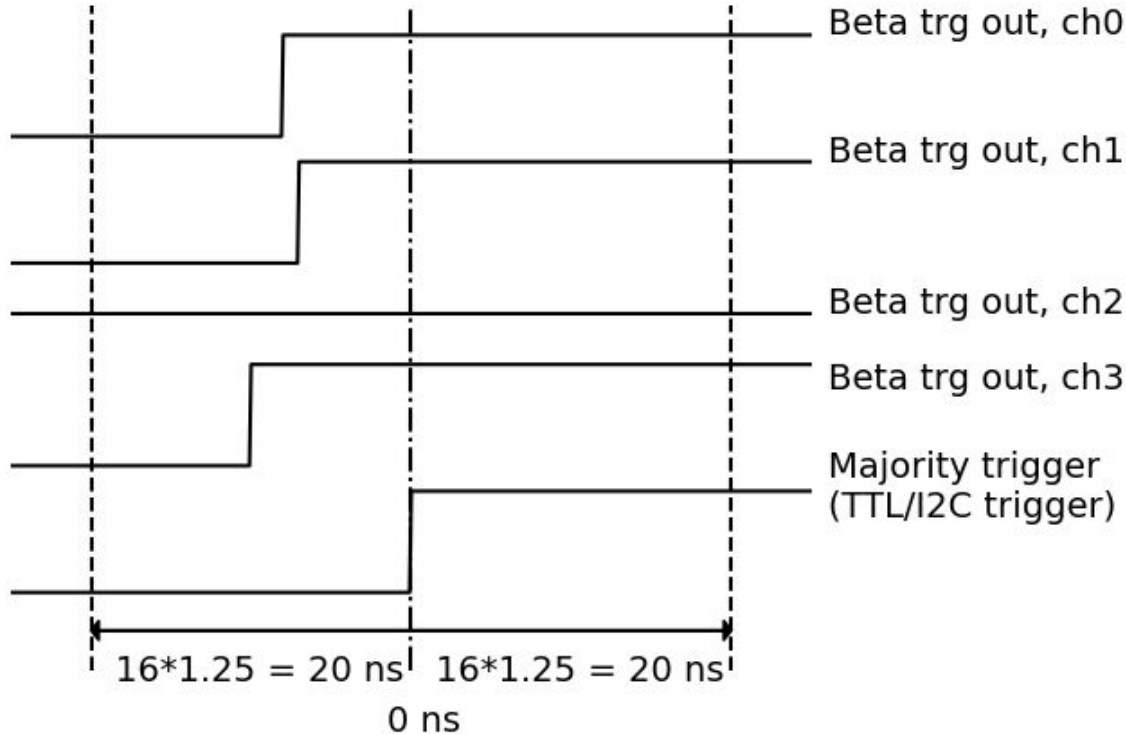


Working on the implementation of missing features, and fixing the problems encountered during the beam tests:

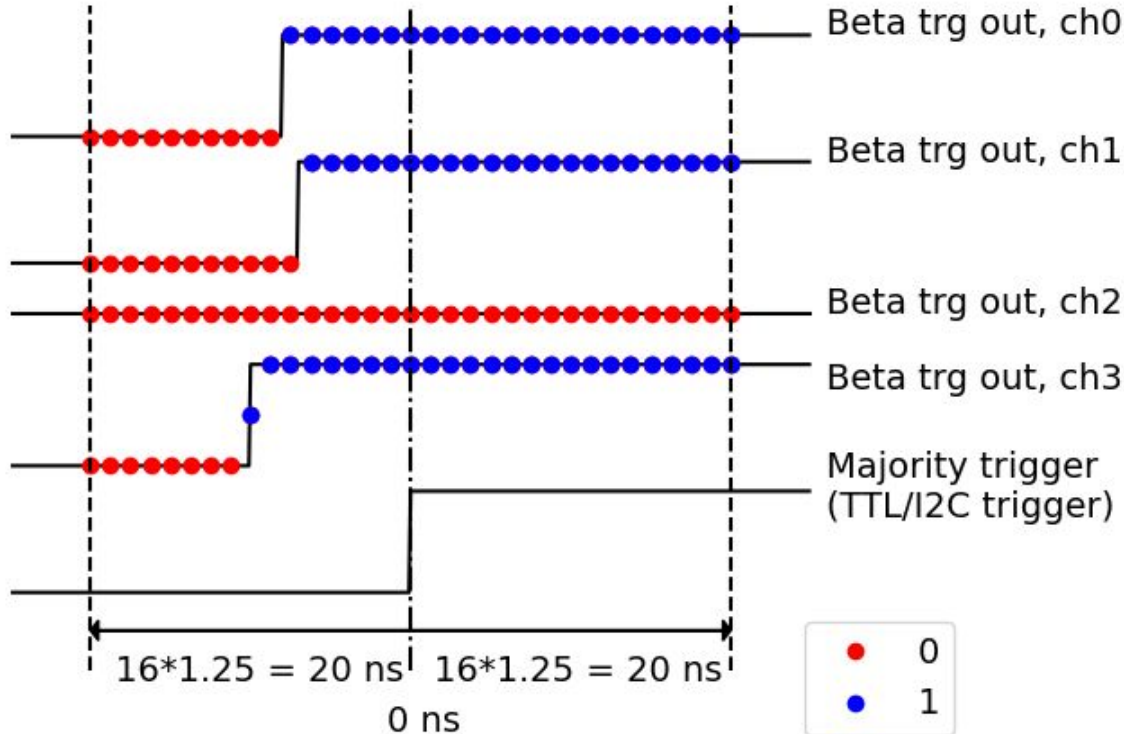
- ❑ **Implementation of the timing information for the Beta channels pre-triggers**, with a resolution of 1.25ns.
Status: implemented in the current version of the firmware and under testing.
- ❑ **Data acquisition problems during the beam tests:**
 - ❑ Shift in ADC channels information and trigger map/I2C information.
Status: should be solved with the current version of the firmware, but we need to test it extensively.
 - ❑ Majority trigger not working properly (only working as 4over4).
 - ❑ Data corruption after 23k events.
 - ❑ From *GammaMeV* beam test at SPS-H8: problems with TTL/I2C acquisitions; many events were missed (note: conflict between majority trigger and TTL/I2C trigger).
- ❑ **Implementation of CAEN modules for remote HV control, LED for calibration**
Status: not implemented yet.

Status: reproduced in the lab; to be solved with the new firmware version.

Timing resolution: implementation



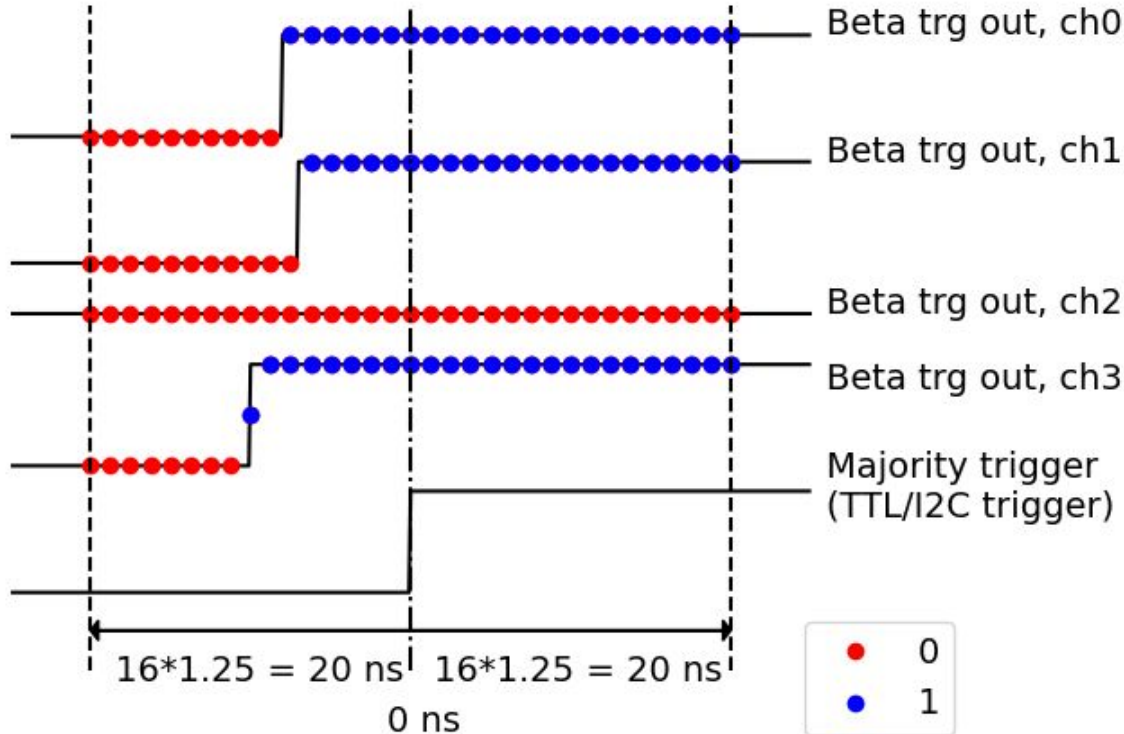
Timing resolution: implementation



Trigger defining the time window:

- If a majority is created; it is the majority trigger (no matter of what is used in the acquisition).
 If more than one majority is created, the first majority that is issued counts.
- If there is no majority, it is the TTL or I2C trigger, depending on which one is used in the acquisition.

Timing resolution: implementation



Trigger defining the time window:

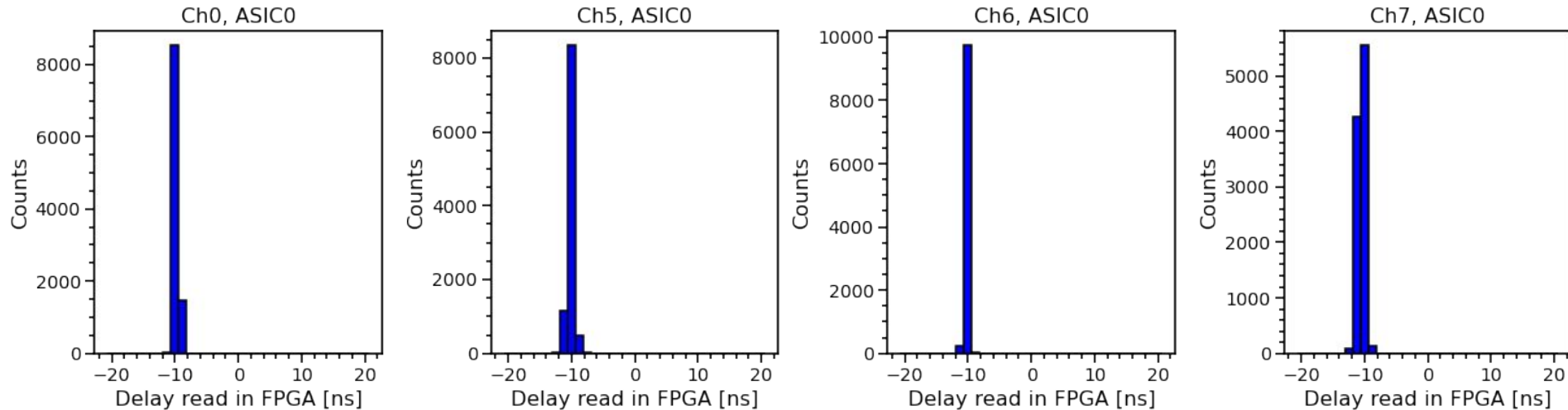
- If a majority is created; it is the majority trigger (no matter of what is used in the acquisition). If more than one majority is created, the first majority that is issued counts.
- If there is no majority, it is the TTL or I2C trigger, depending on which one is used in the acquisition.

What to do in the case the majority is not created (e.g. for PSD inefficiency)?
 What is the delay of the I2C trigger? Is the 40ns sampling window good?

Timing resolution: testing

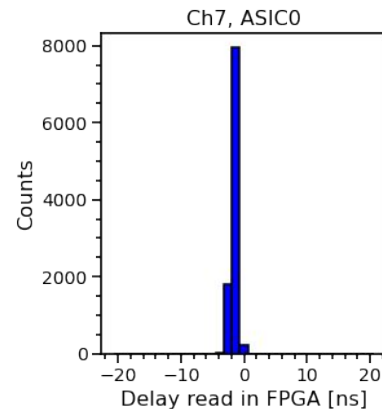
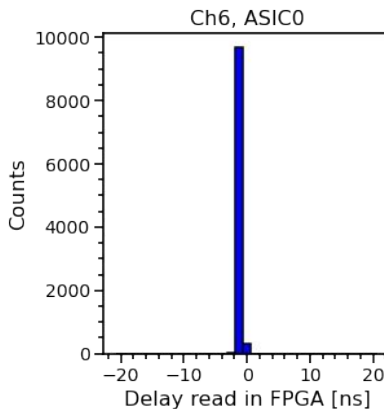
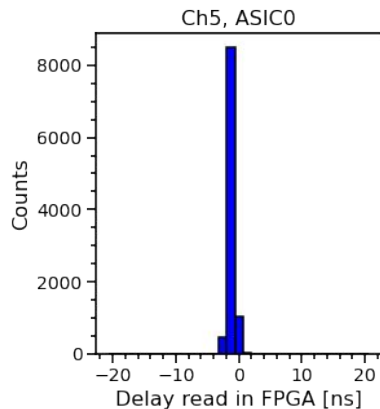
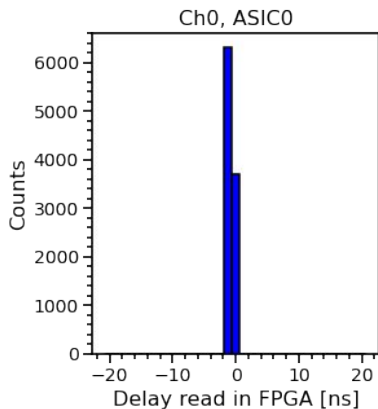
- ❑ Pulses and trigger generated with a high-precision pulse generator: *Agilent 81160A*
- ❑ Compare the delay put in the pulse generator and observed at the oscilloscope, with the timing read-out by the FPGA.

Applied delay = -10 ns

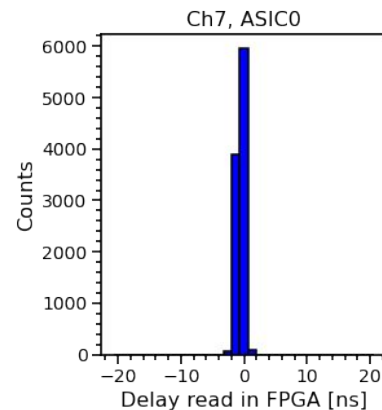
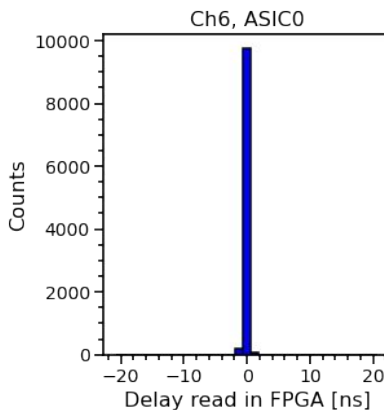
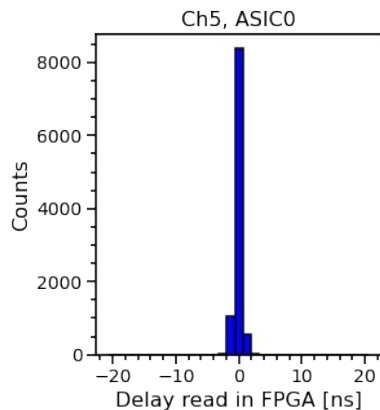
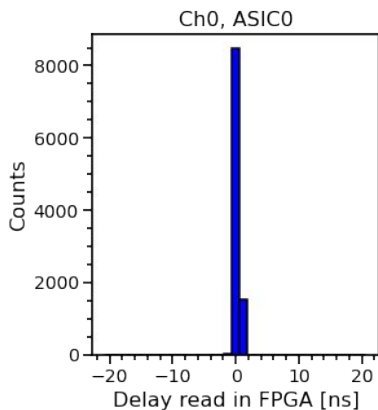


Timing resolution: testing

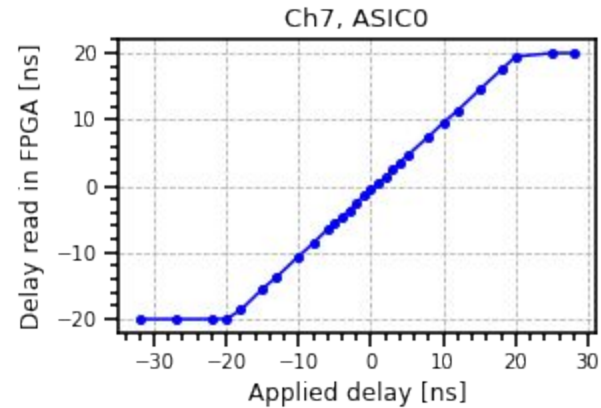
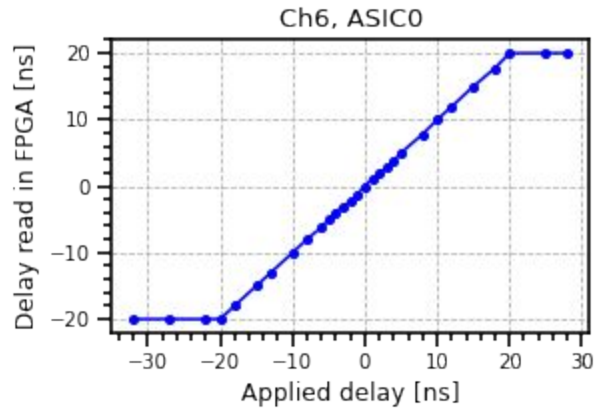
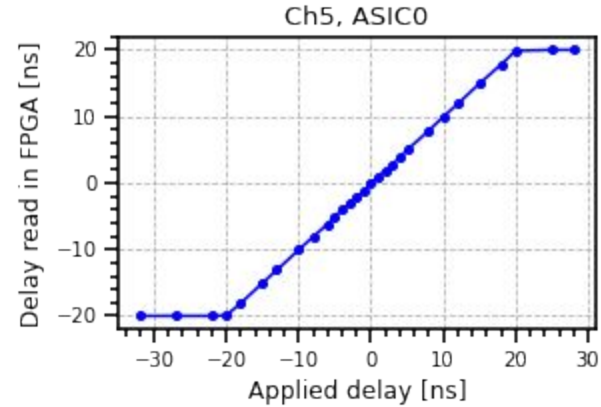
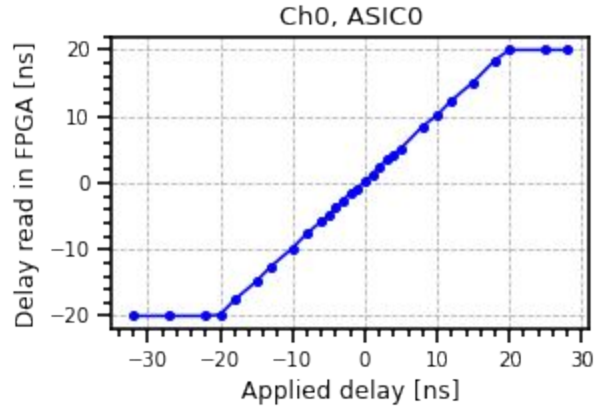
Applied delay = -1 ns



Applied delay = 0 ns

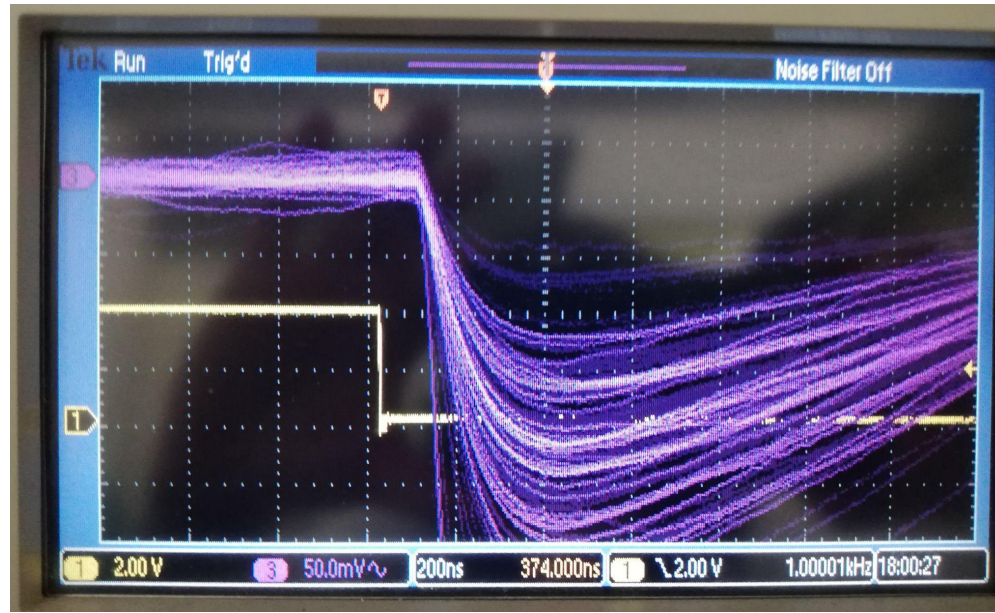


Timing resolution: testing



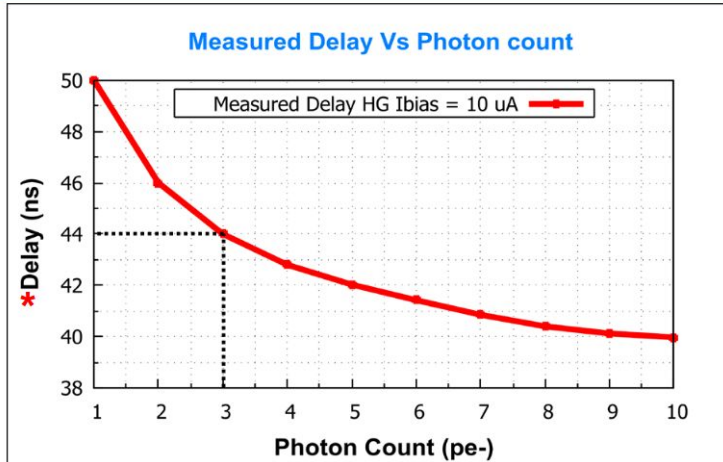
Jitter with SiPMs

- ❑ In a real-file system with SiPMs, the timing will be different for different values of produced photo-electrons.
- ❑ Since the trigger is a time-over-threshold of the pre-amplifier, the timing and the jitter will depend on the combination of signal and threshold level. The higher the signals and the lower the threshold, the lower the jitter is.
- ❑ Calibration of the system needs to be done very carefully.

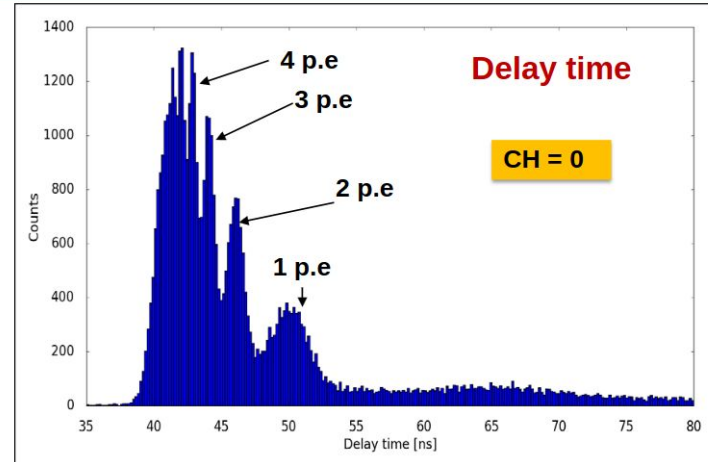


Note: this is a SiPM used in FIT, not the SiPM for PSD.

HERD Measurements : Laser n-PTR measurements



*Note: The delay measured here includes the laser setup delay which is estimated about approximately 25ns



OV = 6.5 V

- The delay introduced from the laser setup delay is ≈ 25 ns
- Delay at : 1 pe- is 25 ns
- : 3 pe- is 19 ns

Note: this is a SiPM used in FIT, not the SiPM for PSD.

Input HG preamplifier Bias current configuration = 10 uA (Maximum)

- First priority is to solve the problems related to the data acquisition (freezing for the moment the time resolution implementation).
- Implement the missing features (CAEN modules, LED...).