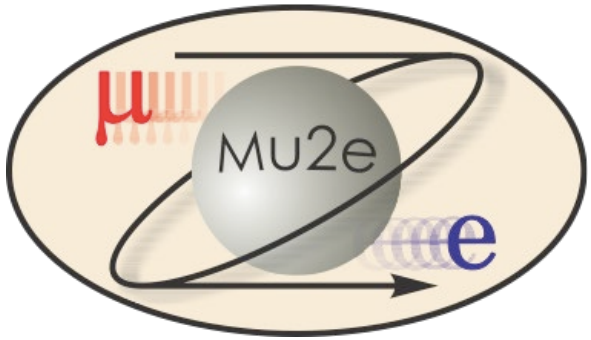


Calorimeter VST status and GR#1 plans

Mu2e Italia Meeting
January 31, 2024

L. Morescalchi, E. Pedreschi, F. Spinella

SiDet Test Stand Hardware

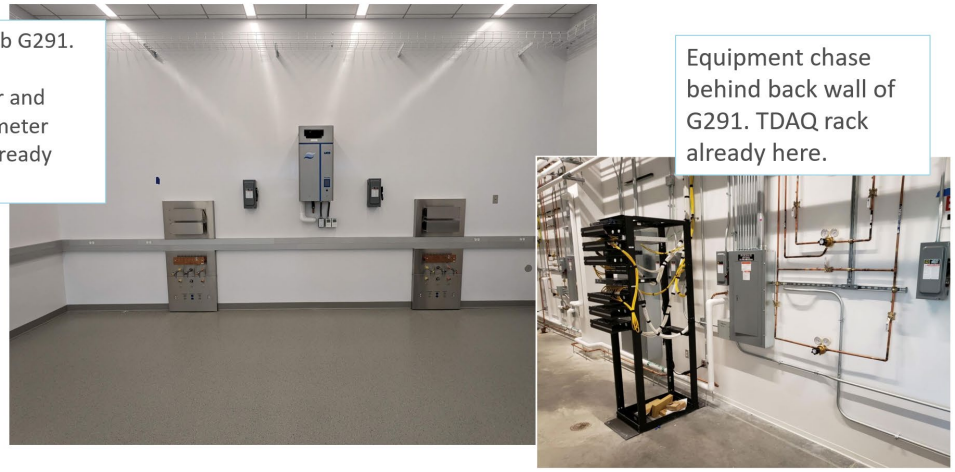
- At the moment the test stand is not active because of ROC shortage, 3 in Italy and 1 at IERC for DTC debugging
- **4 new PC servers** with **7 DTCs** have been installed in a crate outside the clean room, configured and are now reachable with ssh connection
  - **mu2edaq20** is connected directly to a lab ethernet port with a fix IP and to a switch to create a local network with **mu2edaq18**, **mu2edaq19** and **mu2edaq21**

- Another PC desktop machine (**mu2ecalo01**) dedicated for the development of the firmware and the debug has been procured and is connected to the lab network
- A list of the missing material for VST has been made and the procurement procedure started:
  - 7 MTP cables (30 m), 7 breakout cables (1 m), 15 cassettes: 8 IN calo, 7 out DTC, 1 cassettes' support for Rack and 1 power strip

Calorimeter Hardware for Global Run #1

- At the moment the location for GR#1 is IERC lab G291, with the server's rack behind the wall of the room

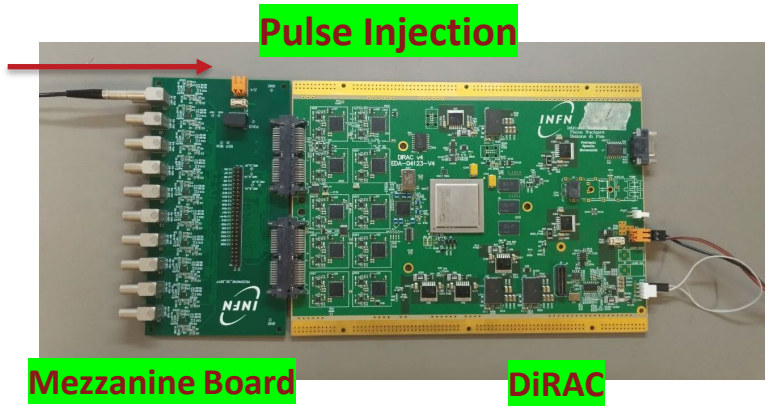
1. **mu2edaq07** has been moved from SiDET to lab G291 and then installed in the rack, now it is reachable through **mu2edaq-gateway**
2. A temporary minimal setup with a DiRAC V2, a power supply and a fan for power dissipation has been installed but **needs an ORC to stay ON overnight**



- In order to have the approval for the ORC, the setup needs to be upgraded:
  - An additional power supply (TTi CPX400SP) for the DiRAC Low Voltage has been procured;
  - The fan has to be compliant with FNAL security standards; the plan is to select a covered fan model that can be powered directly with the 5V from a DiRAC connector
- To have the possibility to program and debug the FPGA from remote, we found a dedicated PC desktop with Windows that still has to be configured with Libero SoC 2023.1 and equipped with a FlashPro 5

ROC Features for Global Run #1

- The Global Run 1 is scheduled for the week 11-15 March 2024 and has as primary goal the evaluation of the system synchronization
- The plan is to inject a synchronized analog pulse to test timestamp consistency
- From the hardware point of view we have to provide a DiRAC with the possibility to inject a pulse to the ADCs:
  1. a mezzanine board with lemo connectors as inputs that performs the single ended – differential conversion and route the analog signals to the ADCs has been developed -> **HW Ok!**



V2 or V5
(depending on new version debug)

- The needed **firmware** features are the following:
  1. Respond to DCS Requests -> **Ok!**
  2. Record noise/generated data triggered by injection pulse -> **Ok!**
  3. Deliver payload in response to Data Requests -> **Ok!**
  4. Provide loopback synchronization markers -> **NOT YET**
     - Under test by Ryan's team (implemented on Avalache demo boards)
  5. Program FPGA over fiber link -> **NOT YET**
     - Under development by tracker team

VST Software / Firmware Status

- We are experimenting some difficulties on the software side, since there isn't a stable 'official' updated working version of the DTC firmware, pcie drivers and mu2e_utils that we can use to readout the board
  - A new debugging session of the official release has been yesterday, but situation still unstable.. even if better than December
- As a temporary workaround to readout some data from the calorimeter we are using some combination of old DTC firmware/drivers/utils
  - Not trivial to understand how to configure ots to use the correct combination of old versions, took a lot of time
  - Sometimes a stable version stopped to work and needed additional work
- The main iussue is that the global run is coming but we didn't have the possibility to deeply test the DiRAC firmware

Software: art_daq

- Currently, we are focusing on understanding the tracker VST software and customizing it to support our needs. Our short-term goal is to develop:
  - A working .fcl configuration file
  - A Generator module CaloVST containing a function getNext(), which interacts with the DTC calling mu2e_pcie_utils functions and produces artdaq:: Fragments
  - An Analyzer module that decodes the Fragments received as input using the CaloDataDecoder class
- A working group with me, Antonio and Sophie started to work on this last week using the Pisa test-stand, which is not directly accessible from the outside world.
  - Switch to mu2edaq20 as soon as a new ROC will be at SiDet there
  - Can produce fragments but there is some issue in passing them to the Analyzer, need to gain experience with the code
- The idea is to start using the internal incremental counters to generate a predictable payload for each ‘event’ and to check the data integrity at each point of the chain
  - The counter can be generated in different parts of the firmware inside the board, for example before the DDR, before the DDR controller, after the DDR (useful to understand fw instabilities)
  - Counter in different ROCs can be sync