SVT - Attivita' 2012

Firenze, 8 Settembre 2011

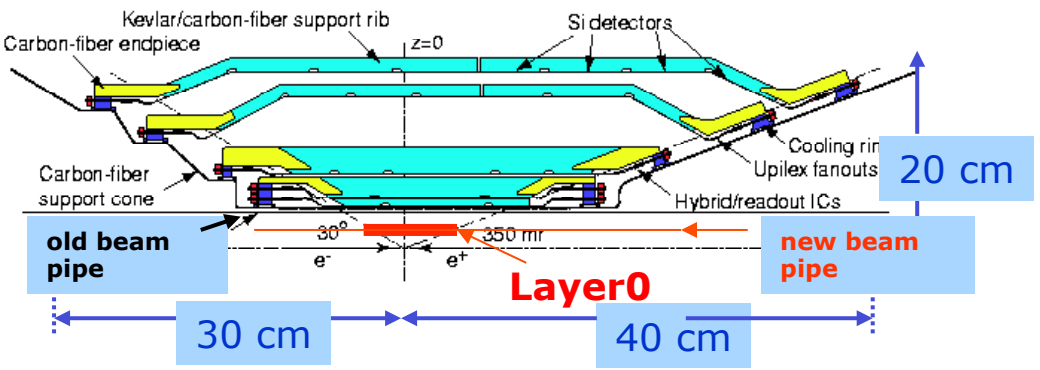
- Stato di SVT
- Attivita' 2011 per finalizzazione TDR
- Attivita' 2012 e richieste finanziarie

Giuliana Rizzo
Universita' & INFN Pisa

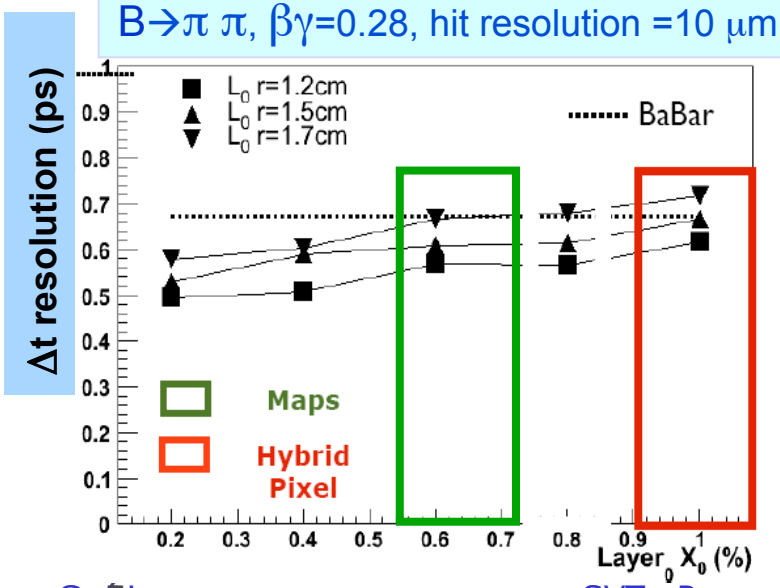
The SuperB Silicon Vertex Tracker

• SVT provide precise tracking and vertex reconstruction, crucial for time dependent measurements, and perform stand-alone tracking for low p_t particles.

• Design based on BaBar SVT: 5 layers silicon strip modules + Layer0 at small radius to improve vertex resolution and compensate the reduced SuperB boost w.r.t PEPII



B→π π, βγ=0.28, hit resolution =10 μm

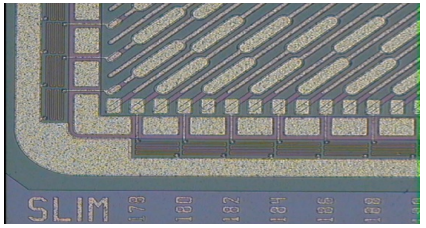


- Physycs performance and backgrounds set stringent requirements on Layer0:
  - R~1.5 cm, material budget < 1% X_0,,
  - hit resolution 10-15 um in both coordinates
  - Track rate > 5MHz/cm^2 (with large cluster too!), TID > 3MRad/yr
- Several options under study for Layer0

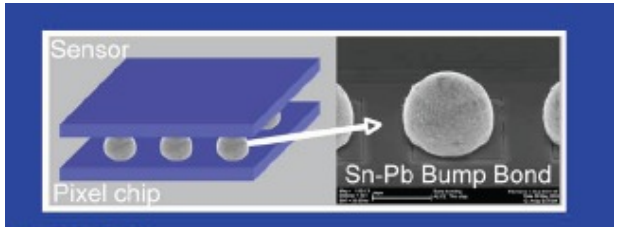
SuperB SVT Layer 0 technology options

Complexity

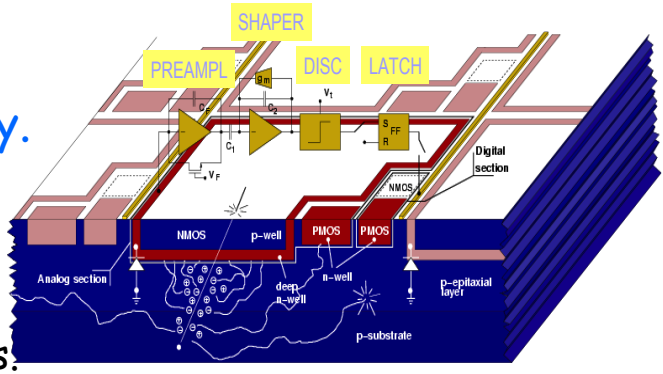
- **Striplets option:** mature technology, not so robust against background occupancy.
  - Marginal with background rate higher than ~ 5 MHz/cm^2
  - Low material budget, but module design quite complex and new FE chip development needed.



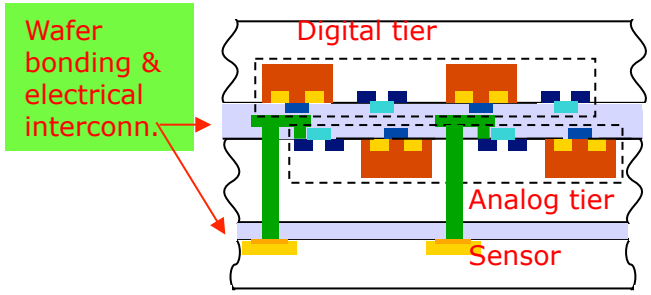
- **Hybrid Pixel option:** viable with some R&D
  - FE chip with 50x50 μm^2 pitch and fast readout architecture under development (4k pixel, ST 130 nm)
  - Pixel module deisgn with ~ 1%X_0 with present technology: further reduction of total material :FE chip, sensor, pixel bus under evaluation



- **CMOS MAPS option:** new & challenging technology.
  - Sensor & readout in 50 μm thick chip!
  - Extensive R&D (SLIM5-Collaboration) on
    - Deep N-well devices 50x50μm^2 with in-pixel sparsification.
    - Fast readout architecture implemented
  - CMOS MAPS (4k pixels) successfully tested with beams.



- **Thin pixels with Vertical Integration: reduction of material and improved performance.**
  - Two options are being pursued (VIPIX-Collaboration)
    - DNW MAPS with 2 tiers
    - Hybrid Pixel: FE chip with 2 tiers + high resistivity sensor



SVT Strategy

- SVT Baseline
  - Striplets in Layer0 @ R~1.5 cm
  - 5 layers of silicon strip modules (extended coverage w.r.t BaBar)
  - Main activities:
    - Layer0 striplets module design (quite complex in a very crowded region)
    - Front-end chips for striplets/strips need to be developed
    - Engineering design of the full detector
- Upgrade Layer0 to thin pixel for full luminosity run
  - more robust against background occupancy
  - SVT Mechanics will allow a quick access/removal of Layer0
  - Several pixel options still open & under development: R&D continue in 2012 after TDR → decision on pixel technology in 2013
    1. CMOS MAPS: continue R&D on readout speed and rad hardness (challenging for application in Layer0).
    2. Hybrid Pixels: FE chip development 50x50 um pitch with fast readout and R&D on reduction of total module material below 1% X0.
    3. Pixel 3D with Vertical Integration: can we access this technology in a (time) reliable and stable way?

SVT Institutions

Groups already working for the SVT:

- Trieste: Silicon sensors, striplets, fanout
- Pavia/BG: MAPS & Front-End chips for pixel and strip (analog cells)
- RomaIII: MAPS
- Milano: pixel bus/fanout Layer0 & peripheral electronics, SVT performance studies, SVT mechanics (HDI cooling rings, transition cards support, beam pipe)
- Bologna: SVT DAQ , MAPS & FE chips (digital architecture).
- Torino: testbeams mechanics.
- Pisa: SVT coordination, MAPS & FE chips for pixel & strip (in-pixel logic, readout architecture, chips final layout, test of prototypes), module assembly & testing, SVT mechanics and cooling, testbeams.

« New » groups getting involved:

- Trento – pixel sensors, strip sensors
- University of Insubria – Mi-B - external layers fanout
- Bari - Hybrid Pixel, Peripheral Electronics (encoder/serializer)
- Mi - C. Fiorini FE chips (analog cell external layers)
- UK: QM (SVT mechanics, sensors?), RAL (MAPS)
- Strasbourg (MAPS)

SVT Organization for TDR phase
(in place since April 2009)

System convener: G. Rizzo

- Sensors: L. Bosisio (TS)
- Front-end electronics: V. Re (PV)
- On detector electronics: M. Citterio (MI)
- DAQ: M. Villa (BO)
- Mechanics: F. Bosi (PI)
- Testbeam: S. Bettarini (PI)
- SVT SW:
  - Det Optimization/Fastsim N. Neri (MI)
  - Background simulation/Fullsim E. Paoloni(PI) /R. Cenci(Maryland)

- Layer0 coordination: G. Rizzo (PI)
- Layer1-5 coordination: L. Vitale (TS)

- Construction responsibilities could have a similar scheme, eventually with different names (institutions) attached to each item and finer splitting (like in the SVT – WBS)
  - On detector electronics → Fanouts, HDI, transition cards
  - Mechanics → Layer0, L1-L5 modules, Support structure, cooling.

Construction Responsibility & Schedule – First Attempt

- From BaBar experience ~ 5 yrs from design to data taking
- Construction phases:
  - Design & prototype: 2012 baseline,
    - 2012 R&D on upgrade to pixel L0: technology choice in 2013
  - Procure and Fabricate (+test) (2013-2014)
    - 2013-2014-2015 for pixel upgrade
  - Module Assembly & Detector Assembly (2015)
    - 2016 for pixel upgrade
  - Commissioning 2016
    - 2017 possible installation of pixel
- Main assumption for this schedule 2 main labs (baseline):

BABAR

- Silicon sensors: Pisa+Trieste
- On detector electronics:
  - FE Chips LBL+PV
  - HDI: MI
  - Transition cards: UCSC
- SVT DAQ: UCSC
- Module assembly: Pisa+UCSB
- SVT Mechanics: LBL+ IT (PI/ FE/TO)

SuperB

- Silicon sensors: Trieste/TN + QM?
- On detector electronics:
  - Pixel Chips PV/PI/BO + others?
  - FE chips strips PV/MI/PI/BO
  - Peripheral electr.: MI+others
- SVT DAQ: BO
- Module assembly: Pisa + UK?+others?
- SVT Mechanics: Pisa + QM + MI+??

Construction Responsibility – First attempt

Approx Cost (MEuro)	ITEM	Possible responsible Institute
4.5	**SVT**	
2	silicon sensor	IT(TS+TN)+Other non IT (UK-QM?)
0.5	fanout	IT(M-L0/TS-Insubria-L1-5)
1	FE chips strips	IT(PV/PI/BO+MI) +collaboration with CERN
0.5	Peripheral electronics (HDI, transition cards,	IT(MI+Ba/LNF on encoder)+non IT ?
0.5	mechanics cooling module assembly	IT(PI+MI)+other non IT (UK QM+others?)
0.5	**L0 striplets**	
0.2	silicon sensor	as for SVT
0.1	fanout	as for SVT
0	FE chips strips	as for SVT
0.1	peripheral electronics	as for SVT
0.1	mechanics cooling module assembly	IT(PI)
1.5	**L0 MAPS**	
1	MAPS chips	IT(PV/PI/BO)+non IT ? (RAL-Strasbourg)
0.2	pixel bus	IT(MI)
0.1	peripheral electronics	IT(MI)+non IT ?
0.2	mechanics cooling module assembly	IT(PI)
1.7	**L0 hybrid pixel**	
0.1	pixel sensor	IT(TS + Ba/TN)
1	FE pixel chip	IT(PV/PI/BO)
0.1	bump bonding	IT(?)
0.2	pixel bus	IT(MI)
0.1	peripheral electronics	IT(MI)
0.2	mechanics cooling module assembly	IT(PI)
0.5	**items SVT in ETD WBS**	
0.25	SVT - DAQ	IT(BO)
0.25	SVT-Power Supply	IT(?)
6.7	**TOTAL COST SVT+Striplts+L0 pixels**	

Attivita' SVT I semestre 2011

- Progressi sul design della baseline per TDR
  - Front-end chip per striplets/strip modules
  - Layer0 striplets engineering design
  - Engineering design of the full detector
- Continua R&D sui pixel per Layer0
  - Alcuni risultati nelle prossime slides

Front-end chip for strip/striplets (I)

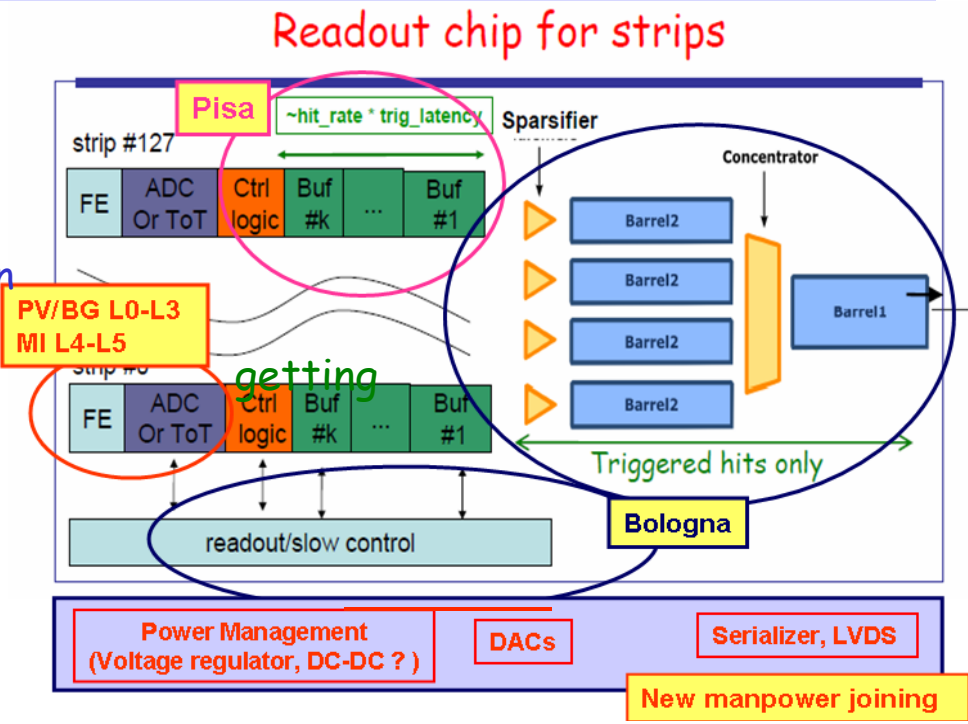
- Clearer definition of the requirements for strip modules in the last months
- Need to develop 2 new chips since existent chips do not match all the requirements : analog info, high rates in inner Layers (2 MHz/strip in L0) & short shaping time (25-100ns), long shaping time (0.5-1 us) in Layers 4-5

Current Plan:

- Adapt readout architecture developed for pixel for strip readout chips.
- First studies performed and no evident showstopper up to now. Full VHDL simulation of the chips for TDR (PV/PI/BO)
- For real chip development/construction new manpower on board.

Responsibility :

- Analog Front-end: fast channels for L0-L3 (PV/BG), slow channels L4-L5 (MI)
- Control Logic-in strip (PI)
- Readout architecture (BO)
- Auxiliary blocks (All groups + blocks developed from CERN IBM 130 nm)



Manpower = 11 designers/6 FTE=2.5PV/2MI/1 PI/0.5 BO

Front-end chip for strip/striplets (II)

L.Ratti

- First evaluation of noise performance for all layers done
- Some optimization still needed

Layer	C_D [pF]	available t_p [ns]	selected t_p [ns]	ENC from R_S [e rms]	ENC [e rms]	Channel width [μm]	Hit rate/ strip [kHz]	Efficiency 1/(1+N)
0	11.2	25, 50, 100, 200	25	220	740	3000	2060	0.890
1	26.7		100	460	940		697	0.857
2	31.2		100	590	1100		422	0.908
3	34.4		200	410	940		325	0.865
4	52.6	400, 600, 800, 1000 (or 500 and 1000)	500	490	1000	9000	47	0.947
			600	440	940			0.937
5	67.5		800	560	1090		28	0.949
			1000	500	1030			0.937

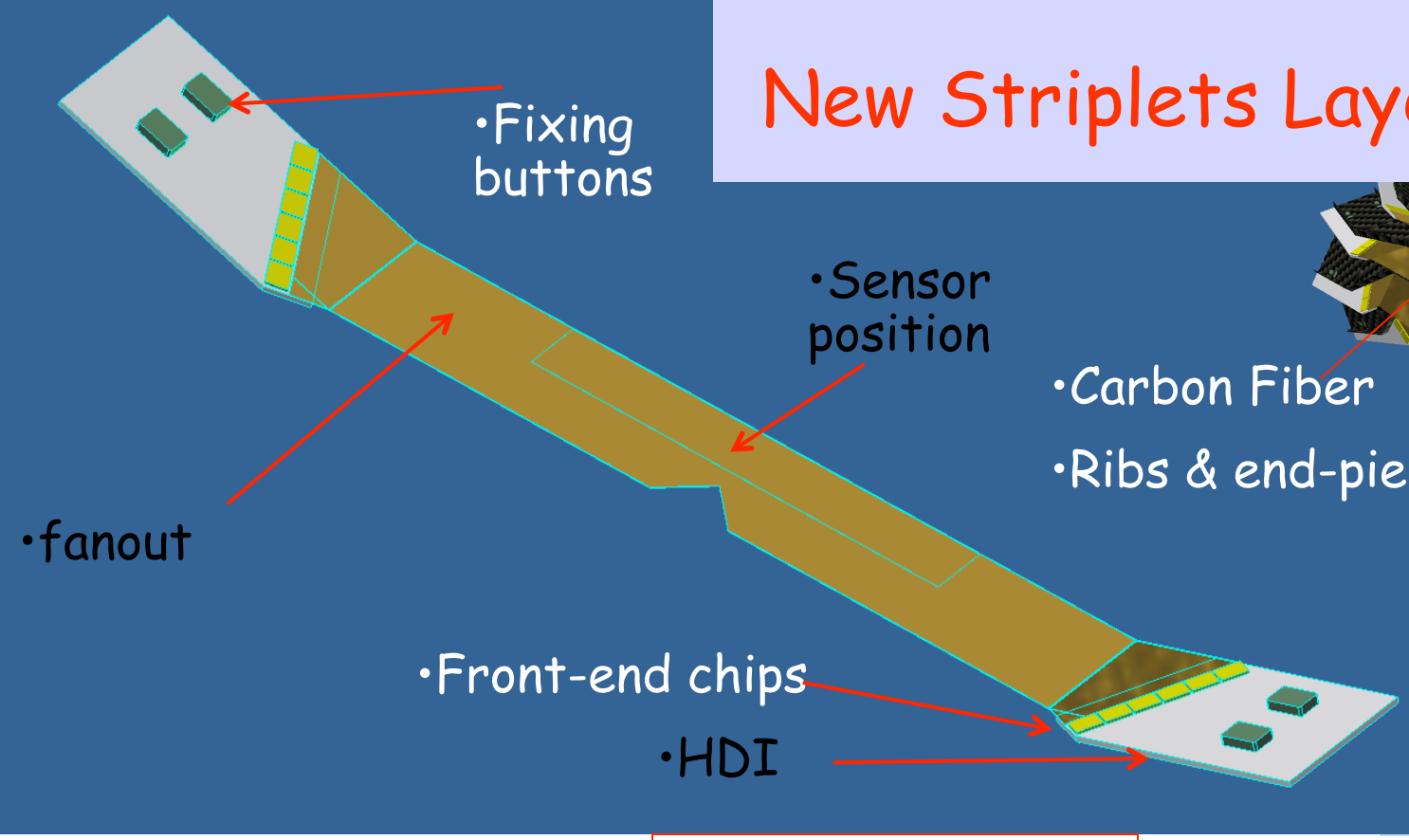
RC^2CR shaping, I_D=500 μA, L=200 nm, N-channel input device,

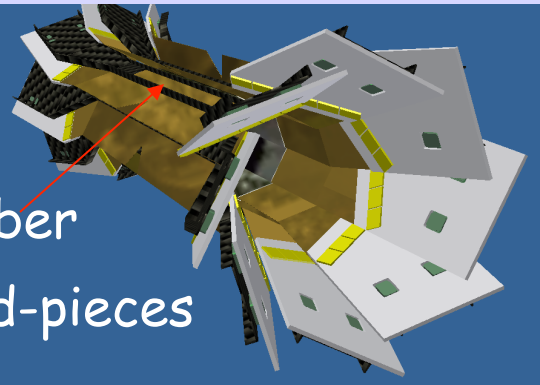
- analg dead time = 2.4 τp, assuming 1 MIP/strip (very conservative!)
- Efficiency will be higher using a reasonable charge deposited/strip (MC)

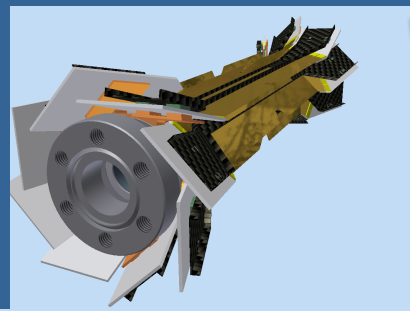
Milestones for chip development:

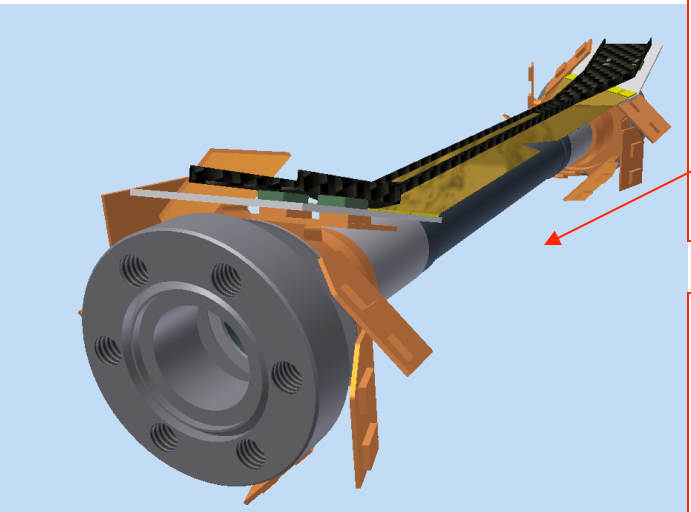
- 2012: first test structures 2x64 (fast & slow) channels, auxiliary blocks
- 2013: first fully operational prototype chips 2x128 channels
- 2104: production run

New Striplets Layer0 design



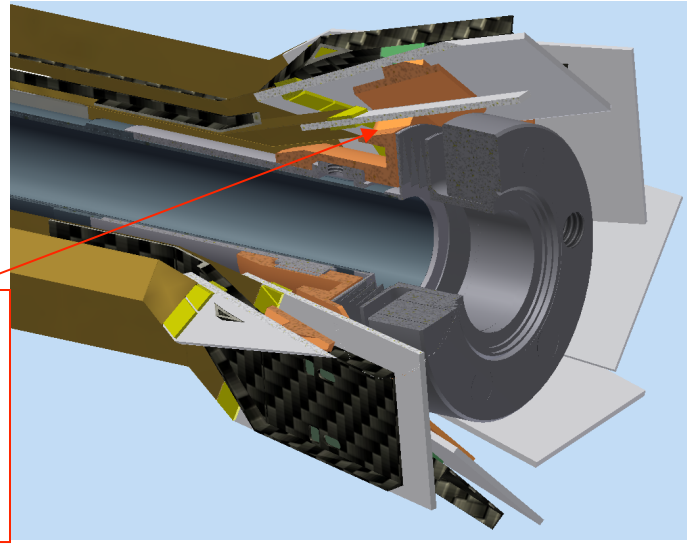






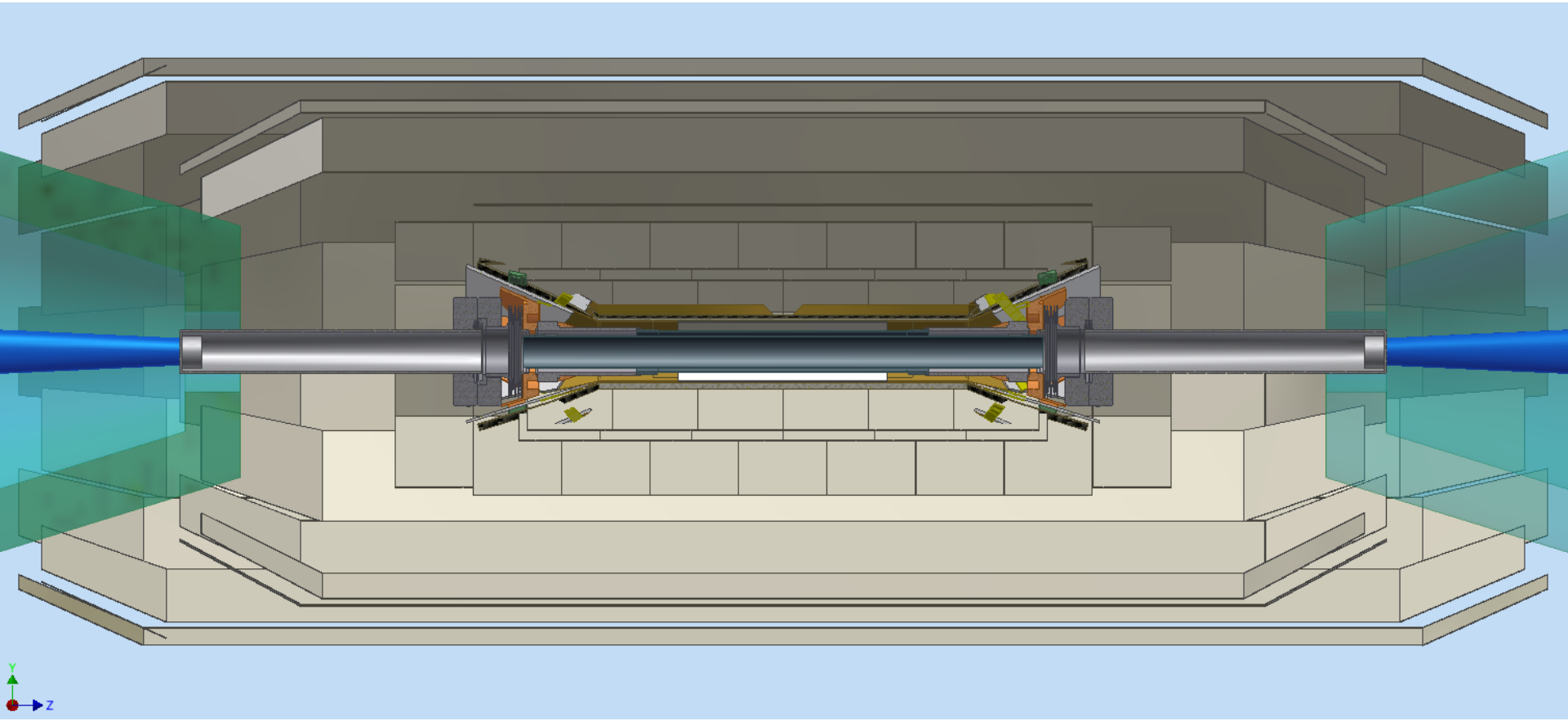
Striplet module positioned on the cold flanges with the Be beam-pipe

•Very crowded region for cold flanges and beam pipe cooling connections



F. Bosi

L1-L5 new module design started



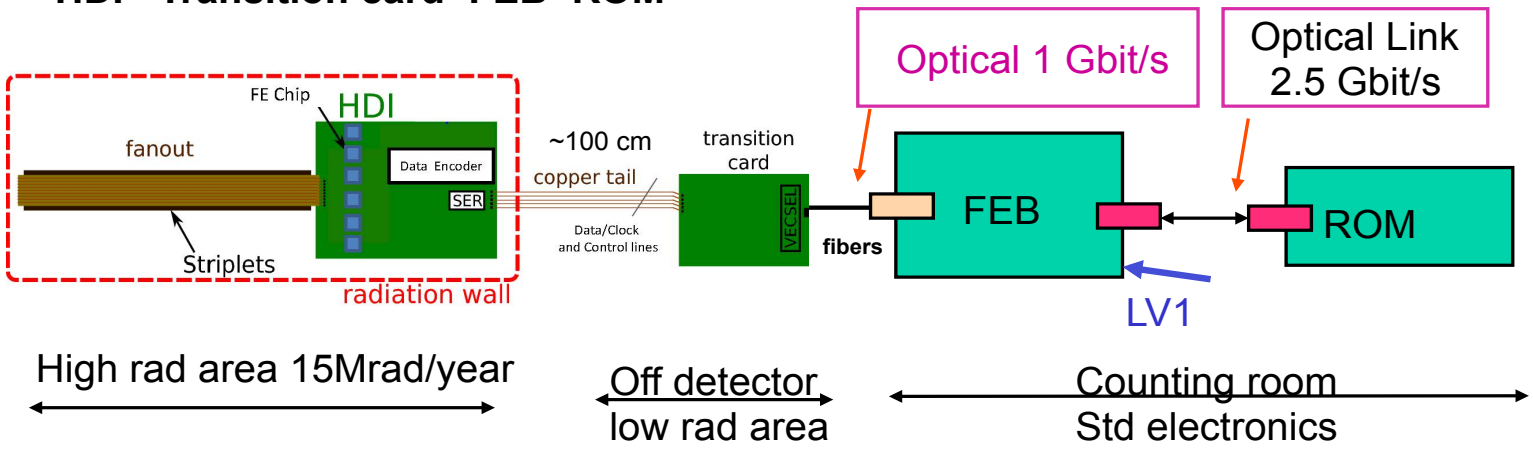
DAQ reading chain for L0-L5

M. Citterio

Design ongoing

DAQ chain independent on the chosen FE options

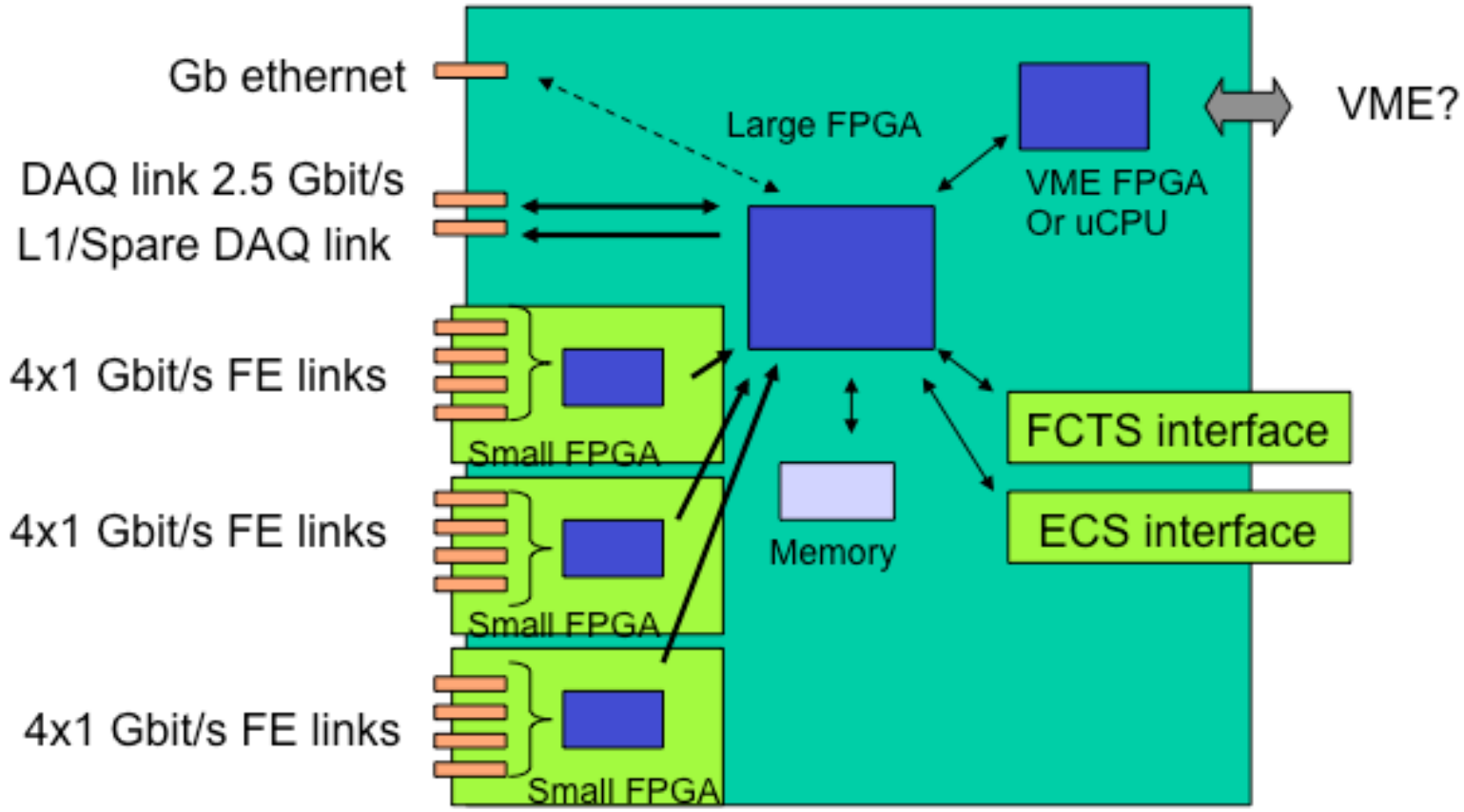
HDI +Transition card+FEB+ROM



- HDI: FE chips, passive comp. and other rad hard IC:
  1. Data encoder: needed to organize/multiplex data from FE chips to serialize 6 chips with >=4 output lines need to match serializer input (16:1). Implement on FPGA by 2012 then start prototiping on chips in 2012.
  2. Serializer (2-5 Gbs needed). LOC1 tested and could be ok. New version with low power @ 2.5 Gbs might be interested.
- Tails: some small and flexible copper cables selected and tested with LOC1.
- Transition card accomodate receiver and electr. to optical transition. Some commercial components selected (to be tested for rad. soft env.)

M. Villa

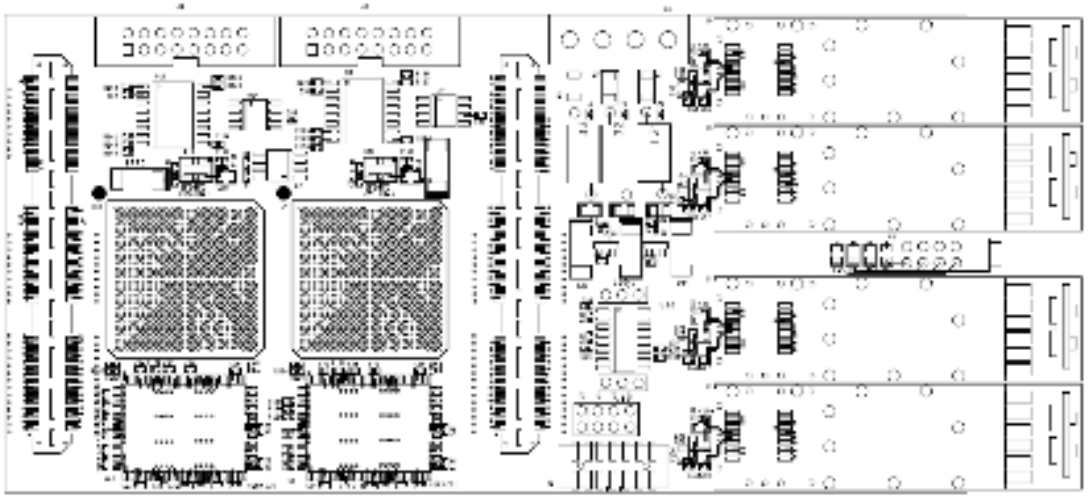
SuperB-FEB Board schematics



FCTS, ECS protocols to be decided experiment-wide
Large FPGA for data shipping and monitoring
VME FPGA or uCPU might be included in the large FPGA.

Optical link mezzanine card for EDRO

Developed as a part of ATLAS/FTK project



4 optical links at 1 Gbit/s; FPGA Xilinx, 40/100 MHz clk (programmable)

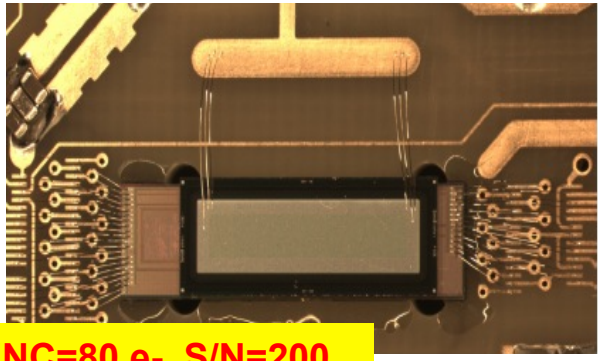
PCB realized; now mounting components on first prototype

Usable as link test mezzanine in SuperB (fall 2011)

R&D on pixel for Layer0 upgrade (I)

PV/PI/BO

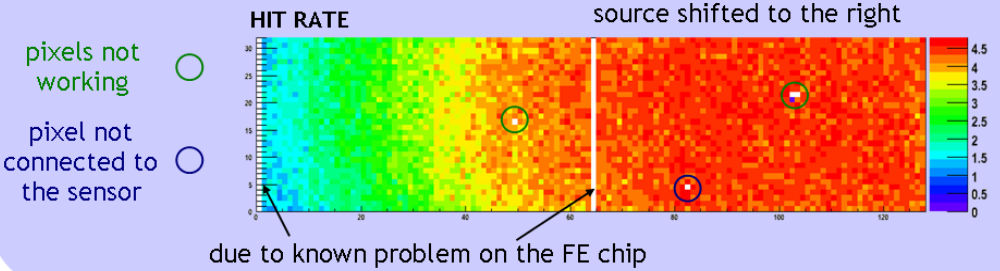
- Test Superpix0: chip di FE per pixel ibridi (32x128 pixels, 50 um pitch, ST 130 nm) interconnesso con bump-bonding a pixel n su p (FBK).



ENC=80 e-, S/N=200

Response to a Sr90 source (e-) threshold@1/4 MIP (60σ noise)

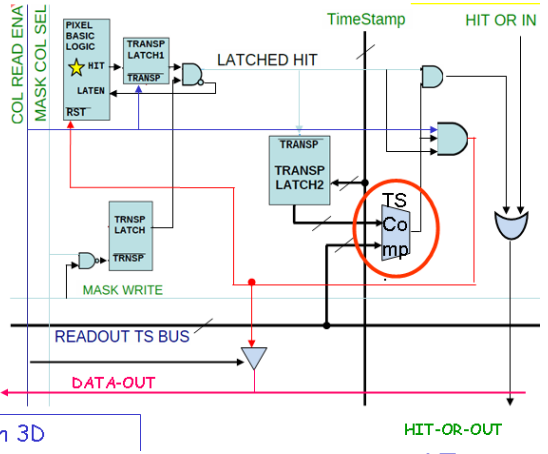
→ good quality of the interconnection @ 50x50 μm² pitch & working sensor!!



- Ottimizzazione architettura readout per pixel ad integrazione verticale.
  - Readout puo' lavorare in data push mode o triggered mode.
  - Simulazione VHDL chip con target hit rate 100 MHz/cm2 (Layer0):
    - Effi 99.9% data push
    - Effi 98.2% trigger (6 us trigger latency)

Exploiting 3D integration for next submission: in-pixel logic with time-stamp latch for a time-ordered readout

- No Macropixel
- Timestamp (TS) is broadcast to pixels & pixel latches the current TS when is fired.
- Matrix readout is timestamp ordered
  - A readout TS enters the pixel, and a HIT-OR-OUT is generated for columns with hits associated to that TS.
  - A column is read only if HIT-OR-OUT=1
  - DATA-OUT (1 bit) is generated for pixels in the active column with hits associated to that TS

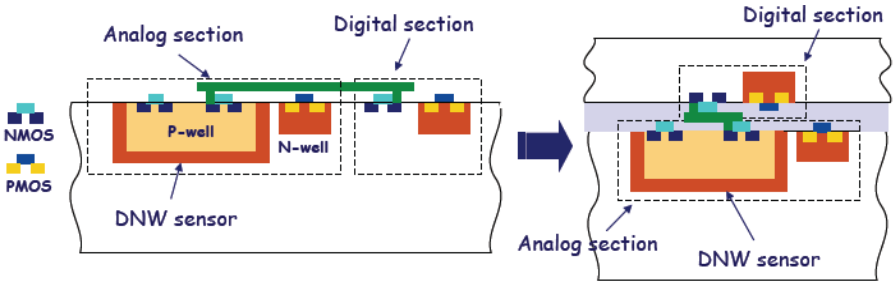


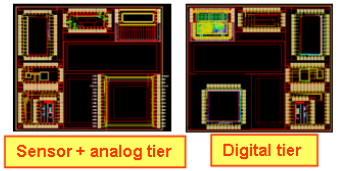
- More in pixel logic possible with 3D

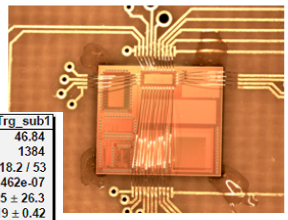
R&D on pixel for Layer0 upgrade (II)

PV/PI/BO

- Primi test su MAPS con processo Chartered/Tezzaron 130nm
  - Processo con integrazione verticale 2 layer CMOS,

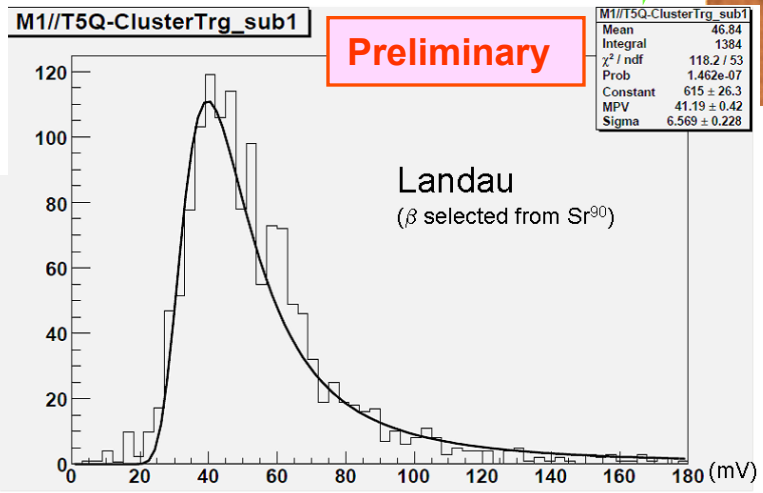




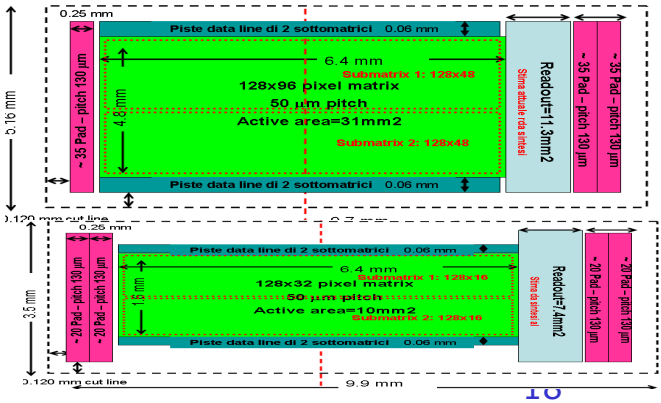


- Strutture 2D con solo layer analogico testate, strutture 3D in arrivo!
- Risultati promettenti
  - ENC ~ 45 e-
  - First estimate of MIP signal

  from test with Sr90 ~ 850 e-



- Preparazione prossima sottomissione Chartered/ Tezzaron vertical integration ~ Dic 2011 (VIPIX)
  - MAPS APSELVI (128x96) e FE per hybrid pixel Superpix1(32x128) 50 um pitch con stessa architettura di readout (data push & triggered) ottimizzata per Layer0 SuperB



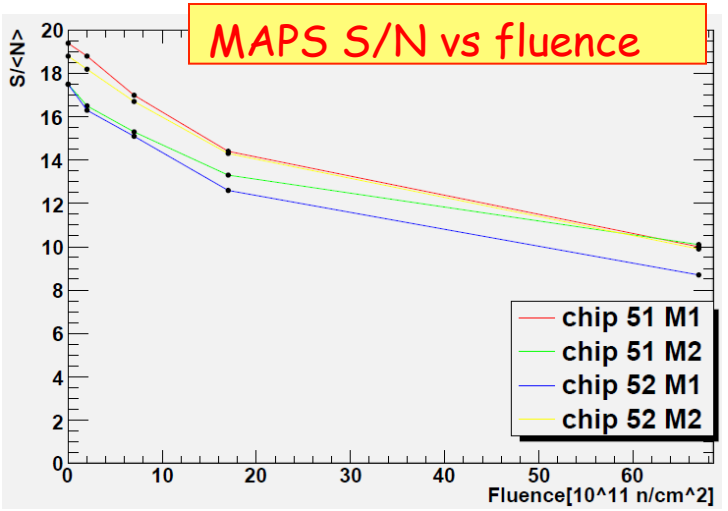
R&D on pixel for Layer0 upgrade (III)

PV/PI/BO-TS

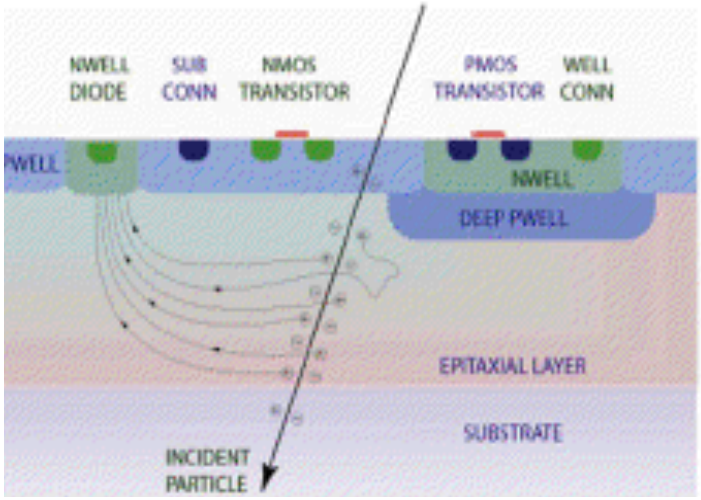
- MAPS radiation hardness: charge collection studied after neutron irradiation up to ~ $7x10^{12}n/cm^2$

  ~ eq. to 1 yr in Layer0 (no safety included!)

  - Noise and gain not affected by neutron
  - Signal degradation after each irradiation step studied with β Sr^{90} source:
    - S/N → 10 in last step
    - severe limitation for application in Layer0



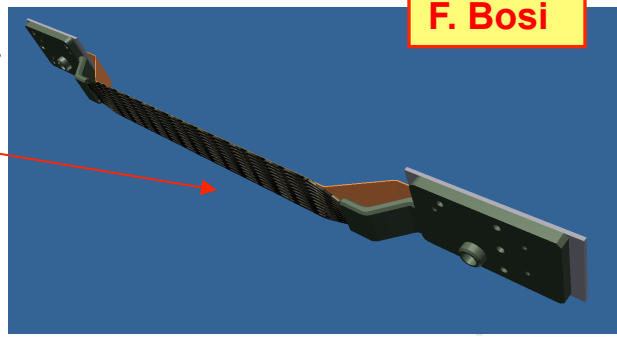
- Realizzazione di MAPS 2D con processo INMAPS (180 nm):
  - high-Ω epilayer available for improved charge collection and radiation hardness!
  - 4th well (deep Pwell), below nwells for in-pixel logic, is used to avoid charge collection in competition with sensing electrode.
  - same readout architecture optimized for 3D (more in-pixel logic thanks to 4th well)
  - Sottomesse a luglio matrici 32x32 con readout digitale e 3x3 analogiche



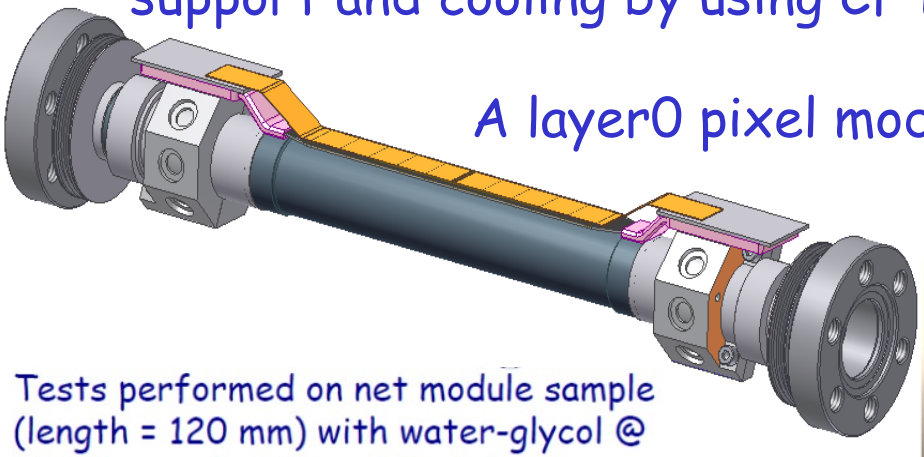
R&D on Light support & cooling

F. Bosi

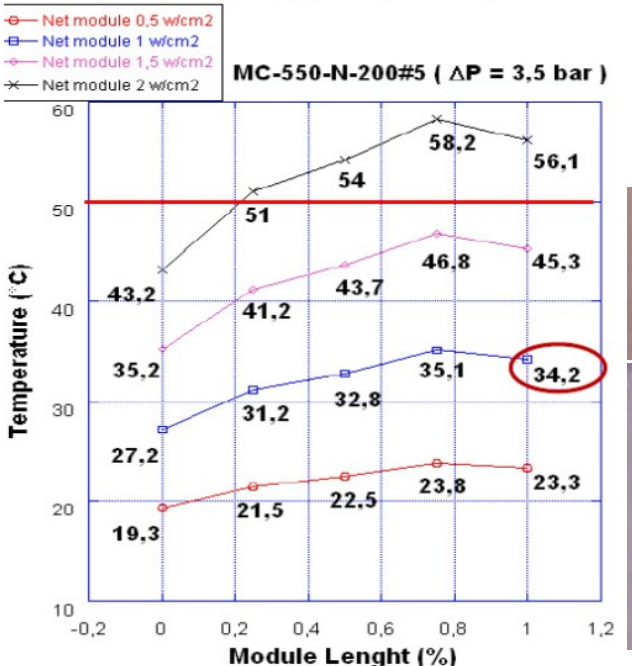
Minimize material budget for Layer0 pixel module support and cooling by using CF microchannels

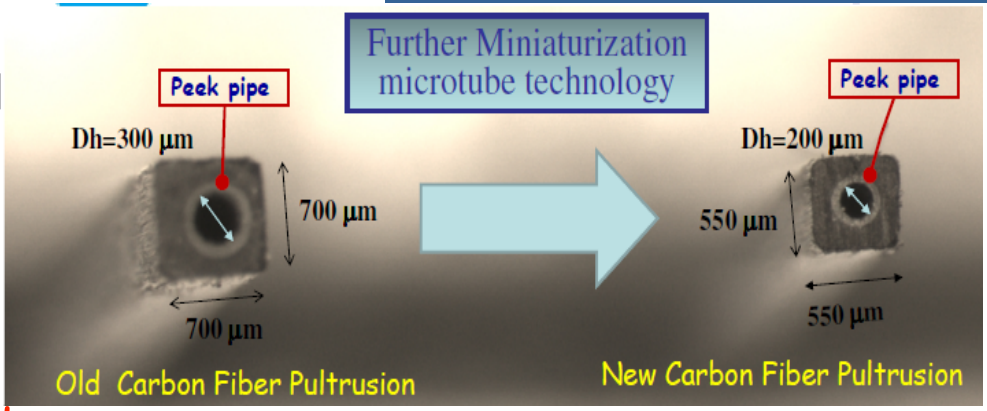


A layer0 pixel module

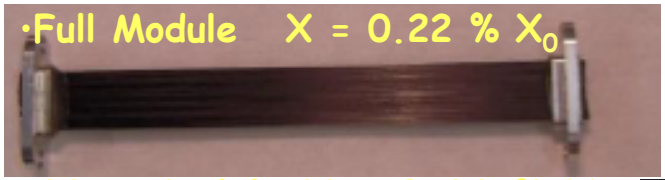


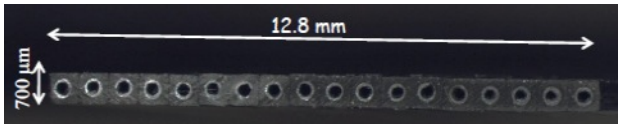
Tests performed on net module sample (length = 120 mm) with water-glycol @ 10 °C as coolant (Δp =3,5 atm).

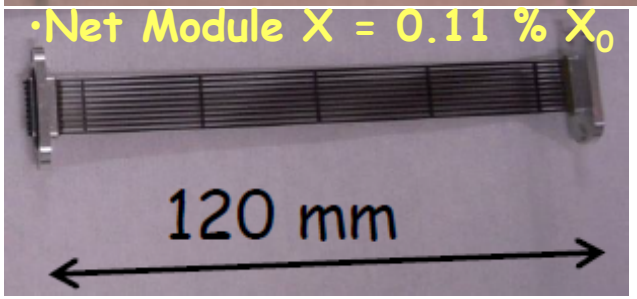


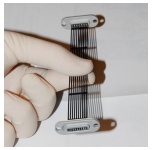


Material due to support:









Attivita' SVT II semestre 2011

- Completamento design baseline per TDR e costruzione prototipi (finanziati nel 2011)
- Continua R&D sui pixel per upgrade Layer0

Attivita ' 2011 per finalizzazione TDR → stesura finale dec 2011 – feb 2012

Baseline: L0 striplets + strip L1-L5

- Sensori: ottimizzazione geometria sensori a strip (TS)
- Fanout: Design dei fanout (dettagli Layer0, dimensioni, ganging L1-L5), produzione primi prototipi Layer0 (MI, MI-B,TS)
- FE chips per striplets/strip: (PV/MI/PI/BO)
  - simulazione VHDL architettura readout chip FE per strips
  - ottimizzazione S/N celle analogiche
  - definizione blocchi periferici FE chip: Power Management (Voltage regulators, DC-DC, LDO…), DACs, Serializer, LVDS
- Elettronica periferica: (MI)
  - definizione di tutti gli elementi della catena e produzione primi prototipi (HDI + encoder + serializer, tails, transition card + componenti optical link)
- DAQ (BO): definizione SVT FEB con componenti comuni ETD
- Meccanica SVT (PI-MI-UK/QM):
  - design moduli layer1-5 e finalizzazione Layer0 striplets con accoppiamento beampipe (produzione primi prototipi con nuovo design) (PI)
  - HDI cooling rings e meccanica di supporto/cooling transition cards (MI)
  - SVT installation procedure & quick demounting (PI)
  - SVT cones and space frame (UK/QM)

Attivita' 2011 per finalizzazione TDR → stesura finale dec 2011 – feb 2012

Pixel options

- Testbeam Sett 2011 su varie strutture a pixel (PI/TS/BO/PV/TO):
  - Pixel ibridi: chip FE Superpix0 con matrice di sensori interconnessa
  - Pixel MAPS: ST130 nm irraggiate con neutroni, Chartered/Tezz. layer analogico
- MAPS (PV/PI/BO)
- Test I Sottomissione INMAPS da ~Nov
- Test strutture 3D run pilota Chartered/Tezzaron
- Finalizzazione I sottomissione Chartered/Tezzaron
- Hybrid Pixel (PI/MI/BO)
- Assemblaggio e test multichip pixel module
- Layer0 pixel mechanics (PI)
- Produzione primi prototipi meccanici Layer0 pixel module con accoppiamento flange beam pipe

- Nel TDR: stato degli R&D sulle varie opzioni a pixel
- Nel 2012 continua R&D sulle opzioni a pixel (programma next slides); decisione sulla tecnologia per pixel upgrade nel 2013

Attivita' SVT 2012

SVT Attivita' 2012

- Dopo il TDR (meta' 2012) entriamo in fase di costruzione.

Construction phases (from BaBar experience)

- Design & prototype: 2012 baseline,
  - 2012 R&D on pixels for L0 upgrade: technology choice in 2013
- Procure and Fabricate (+test) (2013-14)
  - 2013-2014-2015 for pixel upgrade
- Module Assembly & Det. Assembly (2015)
  - 2016 for pixel upgrade
- Commissioning 2016
  - 2017 possible installation of pixel

- Per la baseline e' necessario costruire alcuni prototipi nel 2012 per finalizzare il design dell' intero rivelatore ed entrare in produzione con i vari componenti nel 2013
- Per i pixel del Layer0 nel 2012 continua R&D sulle varie opzioni per arrivare alla decisione sulla tecnologia nel 2013

SVT Activities & prototypes in 2012 – Baseline

SVT Baseline: prototypes to be built in 2012

- Sensori: meccanici per prototipi moduli (meglio se anticipati al 2011)
- FE chips per strip detector: first prototype(s) with analog cell + readout architecture (2x64 ch)+ peripheral blocks
- Fanouts: double layer for striplets (final design), prototype for arch
- Elettronica periferica: prototipi "quasi finali" della catena
  - HDI (+ submission of encoder), tails, transition cards/optical link.
- DAQ: 2 prototypes SVT FEB
- Meccanica:
  - Instrumentazione dei prototipi meccanici L0 (striplets/pixel), gia' realizzati per TDR, per test termostrutturali con raffreddamento nel lab TFD (nuove richieste 2012 + integrazione finanziamento 2011 per realizzazione L0 striplets module nuovo design TDR)
  - Prototipo arco e test termostrutturali (finanzioto nel 2011 +integrazione richieste)
  - Revisione design moduli dopo caratterizzazione termostrutturale prototipi per iniziare la produzione dei componenti dal 2013
  - Design zona di interazione

SVT Activities & Prototypes in 2012 – Pixels

- Prototypes for decision on pixel in 2013: MAPS vs Hybrid Pixels
  - Irradiation of INMAPS structures
  - Second run with INMAPS process
  - Thinner version Al Pixel bus
  - Bump bonding with thinner sensor/FE chips
    - Produce epitaxial/edgless sensors for interconnection with Superpix1 (3D)
    - Gain experience from ALICE R&D (Bari group) on FE chip thinning with IZM
    - Bump-bonding of Superpix1 (3D) with epitaxial/edgless sensors.
  - Mechanics:
    - Test continuita' supporti per pixel con cooling e test termostrutturali.
- Testbeam in Autumn 2012
  - Last testbeam before the decision on pixel technology in 2013.
  - On test:
    - INMAPS 32x32 and 3x3 matrix pre/post irradiation
    - Hybrid pixel module with 3 Superpix0 chips
    - 3D MAPS II run of Chartered/Tezzaron
    - Other pixel structures might be available

Dettaglio attivita' SVT 2012 e richieste finanziarie per Sezioni INFN

Attivita Pisa: Pixels, FE chips, Meccanica, Testbeam

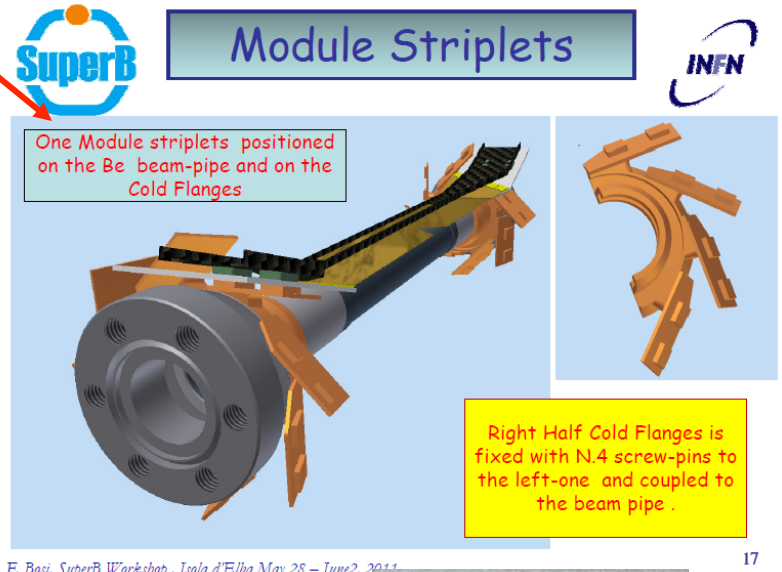
- MAPS:
  - Test strutture I sottomissione INMAPS pre/post irraggiamento (neutroni e Co60). Nuova testboard veloce con traslatori LVDS per testbeam + carriers
  - Preparazione II sottomissione INMAPS (costo chip + carriers)
- Hybrid Pixels: Assottigliamento/bump-bonding
  - Test di Superpix1 (3D) disponibile nel 2012. carriers
  - Bump bonding FE chip Superpix1 (spessore standard e assottigliato ~ 100 um) con matrice sensori (eventualmente edgless) (2 wafer ROC + 2 run a IZM). Test successivi.
- FE chips for strip/striplets
  - Adattamento architettura dei pixel per le strip e realizzazion logica di controllo "in strip" per riempimento buffer. Sottomissione prototipo FE chip (costi PV)
  - Realizzazione testboard interfacciabile con PG/LA e DAQ EDRO e test prototipo (testboard/carriers)
- Meccanica:
  - Dettagli costruzione prototipi nella prossima slide
  - Nel 2012 dopo test TFD prototipi L0 pixel/striplets e realizzazione prototipo arco con verifica "solidita' " termostrutturale del design TDR rivisitazione design dei moduli e design finali jigs per assemblaggio.
  - Nuovi prototipi dei moduli da realizzare nel 2013 con componenti classe C di dimensioni finali.
  - Costruzione mock-up zona d'interazione
- Testbeam: coordinamento e partecipazione

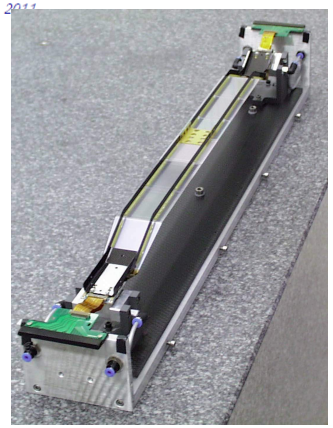
Attivita Meccanica Pisa

Meccanica: realizzazioni post TDR per entrare fase costruzione

- Modulo a striplets meccanico (per TDR) gia' finanziato nel 2011: chiediamo integrazione +4 kE Nuovo design: con HDI e supporto piu' complessi

- Instrumentazione modulo L0 striplets e pixel per test in lab TFD per verificare solidita' termostrutturale del design sotto cooling
- Test di continuita' sui supporti con cooling integrato per modulo pixel
  - Materiale per prototipi (microtubi e interfacce idrauliche)
  - Riscaldatori, termocoppie
  - Consumabili lab TFD
  - Flussimetro ad effetto coriolis per misure portata nel range 30gr/min – 70 gr/min (flussimetri per portate maggiori e minori gia' disponibili, ma nuovi microcanali con Dh=200 um non testabili in questo range)





- Arco layer esterni (costruzione nel 2012 dopo il design TDR) (gia' finanziato nel 2011) chiediamo integrazione +4KE dopo rivalutazione jigs necessari/ribs/end piece
- Metabolismo clean room

Sommario richieste SVT Pisa

consumo	testboard multipourpose (chip pixel nuova generazione) alta velocita' (150MHz) con traslatori LVDS per testbeam	5
consumo	carriers INMAPS I sottomissione	1
consumo	carriers INMAPS I sottomissione	1
consumo	carriers Superpix1 con sensore bump-bondato	1
consumo	Schede di test per FE chip per strip: testboard interfacciabile con PG/LA e DAQ-EDRO (3kE) e carriers (2kE) per 2 prototipi	5
apparati	Sottomissione INMAPS II	70
consumo	bump-bonding FE pixel chip Superpix1 spessore <=100 um con sensori (6.5 kE ROC wafer + 13.5 kE assembly IZM)	20
consumo	bump-bonding FE pixel chip Superpix1 spessore standard con sensori (6.5 kE ROC wafer + 13.5 kE assembly IZM)	20
consumo	meccanica - integrazione costi per realizzazione modulo striplets con nuovo design TDR	4
consumo	meccanica - integrazione costi per realizzazione arco con nuovo design TDR	4
consumo	materiale per instrumentazione moduli prototipi e test termostrutturali lab TFD (riscaldatori, termocoppie)	5
consumo	meccanica materiale per realizzazione prototipi supporto/cooling modulo a pixel (microtubi in fibra di carbonio 3.5kE e interfacce idrauliche relative 1.5kE)	5
consumo	consumi lab TFD per test di conitnuita' su supporti con cooling per pixel	2.5
consumo	flussimetro a effetto coriolis per range di portata 30-70 gr/min (nuovi microcanali con diametro 200 um)	4.5
consumo	mock-up zona d'interazione per studio posizionamento servizi (tails, piping,cables)	8
consumo	allestimento testbeam (meccanica + elettronica)	5
consumo	Mantenimento clean room	6
interno	Contatti ing mecc.con collaboratori e ditte (Plyform Novara)	2
interno	Contatti ing elettronici .con collaboratori per sviluppi FE chips (MI-PV-BO)	2
interno	Test di sistema Beam Test a Bologna	4
interno	Responsabilita' SVT Convener	1
estero	Test beam al CERN	14
estero	Contatti ing mecc SLAC per sviluppo interaction region	2
estero	Contatti ing mecc UK per sviluppo meccanica SVT	2
estero	Contatti ing mecc con ditte estere (Van Dijk Pulstrusion)	2
estero	Responsabilita' SVT Convener	1.5
licenze-SW	Contributo licenze Cadence, Synopsys, Mentor Graphics	3
licenze-SW	Contributo licenze ANSYS	1.5
licenze-SW	Licenza Inventor Professional (Modellatore 3D)	2

Consumi:
13 kE elttronica
40 kE bump-bonding
33 kE meccanica
70 kE Apparati

Attivita' Trieste: Sensori, Fanout, Tails

- Sensori:
  - finalizzazione del TDR con ottimizzazione geometria sensori (fine 2011)
  - Design maschere sensori per fine 2012 (collaborazione con TN, Con QM?).
  - Acquisto wafer Si per ricavare sensori meccanici per prototipi striplets e per modulo ad arco (possibile anticipo al 2011?)
  - Prototipi meccanici sensori a strip con croci di riferimento e pad di bonding per prove di assemblaggi moduli
  - Collaborazione all' attivita' sui sensori a pixel (HP option) epitassiali ed edgless.
- Collaborazione con MI e MI-B Insubria per design fanout, tails (layer 1-5)
- Collaborazione irraggiamenti con neutroni su MAPS
- Partecipazione testbeam pixel 2012 (telescopio)

consumo	Wafer di silicio 200-300um per prototipi meccanici moduli Layer0 e Layer esterni	5.5
consumo	Prototipi meccanici sensori a strip con croci di riferimento e pad di bonding per prove di assemblaggi moduli	30
consumo	Prototipi tails Layer esterni	7
consumo	Attrezzature di test per tails e fanout	3
consumo	Materiale vario per Beam Test	2
consumo	Mantenimento Clean Room (prefiltri e impianto gas e vuoto)	1.5
licenze-SW	Manutenzione annuale SW progettazione sensori (Mentor Graphics)	1.5
licenze-SW	Manutenzione annuale SW simulazione sensori (Synopsys Advanced TCAD)	2
trasporti	0.5 keuro Spedizioni per irraggiamenti a Lubiana	0.5
interno	Coordinamento con gruppo di Milano per fanout e tails	1
interno	Test di sistema Beam Test a Bologna	1
estero	Contatti con almeno due fornitori esterni di sensori (ad es. Micron, CIS)	3
estero	Beam Test CERN	6

Attivita' Milano Bicocca (Insubria): Fanout

- Collaborazione con MI e Trieste per design e realizzazione fanout.
- Prototipi fanout per layer esterni (CERN-TVR Schio)
- Test dei fanout assemblati con sensori e ASIC gia' disponibili

consumo	produzione fanout CERN + controllo e correzione corti TVR Schio	12	
consumo	produzione fanout TVR Schio sj a buona risucita test run 2011		12
consumo	assemblaggio prototipi elettricamente funzionanti con sensori e ASIC gia' disponibili (componenti e schede di test)	5	
interno	Contatti con TS per definizione fanout	3	
estero	Contatti Cern per produzione fanout	3	

Attivita' Pavia/BG FE chips, Pixels

FE chip strips:

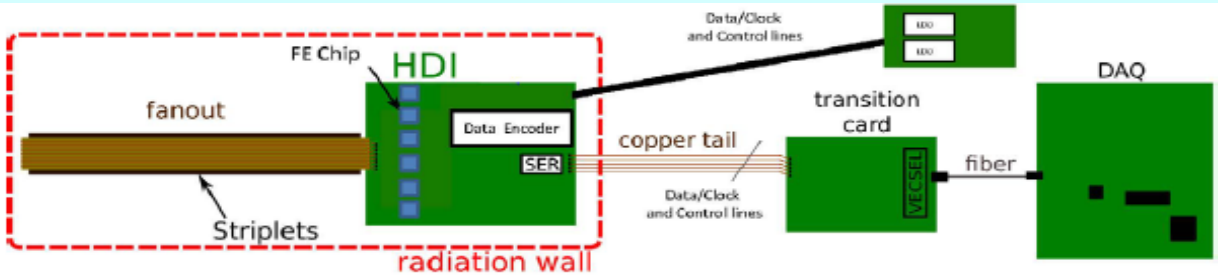
- design dei canali analogici veloci (25-100 ns) per lettura Layers 0-1-2-3.
- sottomissione IBM 130 nm: prototipi multicanale (2x64ch) con le due versioni dell' analogico e architettura di readout per strip (con MI-PI-BO) + blocchi periferici da inserire nel chip.
  - 64 channels for each front-end (fast and slow) in two separate test chips useful to fully understand power distribution problems
- Test dei prototipi

Pixel

- Test I sottomissione pixel INMAPS + irraggiamento (Co60 e neutroni) e test
- Preparazione II sottomissione INMAPS e test dei prototipi
- Caratterizzazione delle strutture MAPS e Superpix1 in vertical integration
- Partecipazione al testbeam 2012 (pixels).

apparati	Sviluppo di fast front-end e slow front-end per striplets/strips, (32 mm2 * 2.6 kEuro/mm2) + 7 % fee per supporto CERN (64 canali per prototipo + blocchi ausiliari, i.e. DC-DC converter, LDO regulator, LVDS transceiver)	90
consumo	Realizzazione di PCB per caratterizzazione di prototipi e test di radiation hardness	4
interno	Contatti sviluppi chip e test a Pisa	2
estero	Meeting con gruppi di ricerca a RAL e Strasburgo su tecnologia INMAPS (1 mese uomo)	5
estero	Meeting con IC design group del CERN su tecnologia IBM 130 nm (1 mese uomo)	5
estero	Test beam al CERN 1 mu	4

Attivita Milano: Elettr. periferica, FE chips strip, Meccanica



- Nel 2011 (→ perTDR) realizzazione primi prototipi della catena (finanziati 2011):
  - fanout layer0 (con ditta alternativa al CERN)
  - HDI (Aurel) con encoder da sviluppare/serializzatore LOC1 (5Gbs)
  - tails con cavetti, prototipo transition cards con componenti ottici
  - Al pixel bus per modulo 3 chip Superpix0 (CERN) e realizzazione interfaccia PCB per test modulo multichip (per TDR)
- Nel 2012 realizzazione prototipi "quasi finali" della catena:
  - fanout Layer0, tail Layer0, HDI (tutti layers), transition card
  - II iterazione thin Al pixel bus (thinner Al power planes and fewer layers)
- Progetto encoder (Process SoS 0.25 um – Peregrine, match LOC serializer):
  - Implement on FPGA by 2012 then start prototiping on chips in 2012.
  - I Prototype chip in 2012 4x4 mm2 36kE→ II prototype in 2013 ~50 kE
  - Production run 2013-2014 (possible sharing with SMU LOC prod) 200kE+IVA
- Progetto dei canali analogici per i layer4-5 e realizzazione del prototipo di FE chip per strip layer esterni in collaborazione con PV/PI/BO. Test dei prototipi.
- Meccanica SVT: HDI cooling rings e meccanica di supporto/cooling transition cards
- Partecipazione al testbeam 2012 (analisi dati e pixel module)

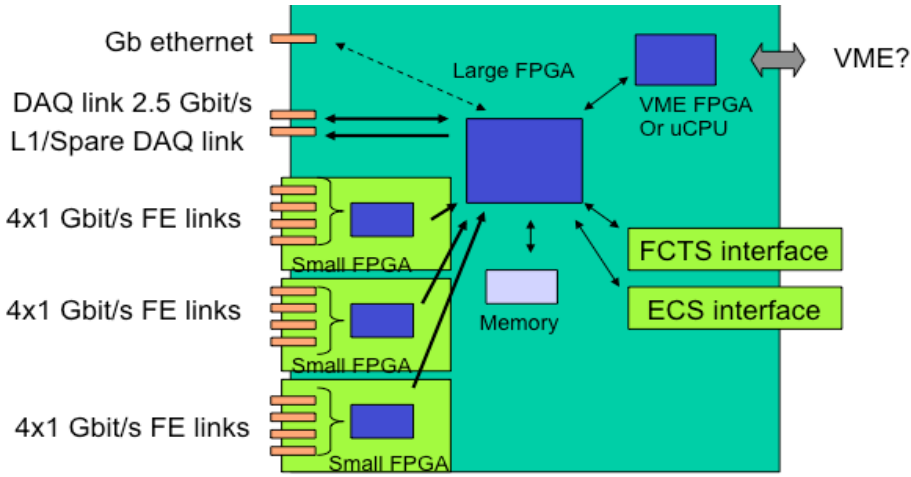
Riassunto richieste 2012 Milano

consumo	Schede e componenti per test blocchi singoli dei FE chips (carriers/testboard/componenti, probe needles and bonding wires)	7.5
apparati	HDI : 20 kE II iterazione prototipi “quasi finali” + 3kE componenti + 2kE completamento test setup	25
apparati	Sottomissione IC encoder prototipo per HDI (Silicon on Sapphire) matched con un serializzatore 16:1 a ~ 5 GBps gia' prodotto da SMU Dallas	36
consumo	Fanout Layer0 14kE II iterazione + 2 kE test setup	16
consumo	Tails: II iterazione tails “quasi finali” Layer0	7
apparati	Transition card: II iterazione transition card	4
consumo	Consumi laboratorio elettronica	2
consumo	Materiale per prototipi meccanici (cooling rings e supporto per transition card)	8
apparati	II iterazione THIN Al pixel bus (thinner Al power planes and fewer layers)	9
licenze-SW	Microwave Office per la progettazione di circuiti stampati ad alta frequenza	3
licenze-SW	Contributo licenze software per Moduli Aggiuntivi Cadence	4.5
inventario	Pattern generator PG3A necessari per arrivare a frequenze di clock di 200 MHz su bus paralleli	21
interno	Contatti ing ele per sviluppo chip FE con PV/PI/BO	3
interno	Contatti con TS per fanout/tails layers esterni	2
interno	Contatti con PV per power distribution	0.5
interno	Contatti con NA per optical link	2
interno	Contatti con Aurel per HDI	1
interno	Contatti con BO per data link	0.5
interno	Contatti con Bari per lo sviluppo chip di encoding	2.5
interno	Contatti con PI per il progetto della meccanica	2.5
estero	Contatti CERN per AL bus development & link	4
estero	Contatti con Dallas per sviluppi serializer/driver/receiver + test	13
estero	Contatti IC designer group CERN per IBM 130 nm	5
estero	Partecipazione Test Beam CERN	2.5

Consumi:
32 kE elttronica
8 kE meccanica
74 kE Apparati

Attivita' Bologna: SVT DAQ, FE chips strip, pixels

- DAQ boards (FEB) for SuperB
- DAQ Maintainance for beam tests
- FE chips per strips: sviluppo architettura readout
  e sottomissione prototipo chip FE multicanale.
- MAPS: II sottomissione INMAPS
- Partecipazione testbeam pixel 2012 (DAQ, pixels)



FCTS, ECS protocols to be decided experiment-wide
Large FPGA for data shipping and monitoring
VME FPGA or uCPU might be included in the large FPGA.

consumo	Prototipo scala reale FEB board	14
consumo	Metabolismo laboratorio	2
licenze-SW	Licenze sw per microelettronica: licenze floating Europractice per CAD Cadence, Synopsys e Mentor Graphics	2.5
inventario	PC categoria server per DAQ	3
trasporti	Trasporti per testbeam	2.5
interno	Contatti Pisa per test prototipi chip pixel/strip	2
estero	Testbeam CERN	8

Clear roles of these boards:

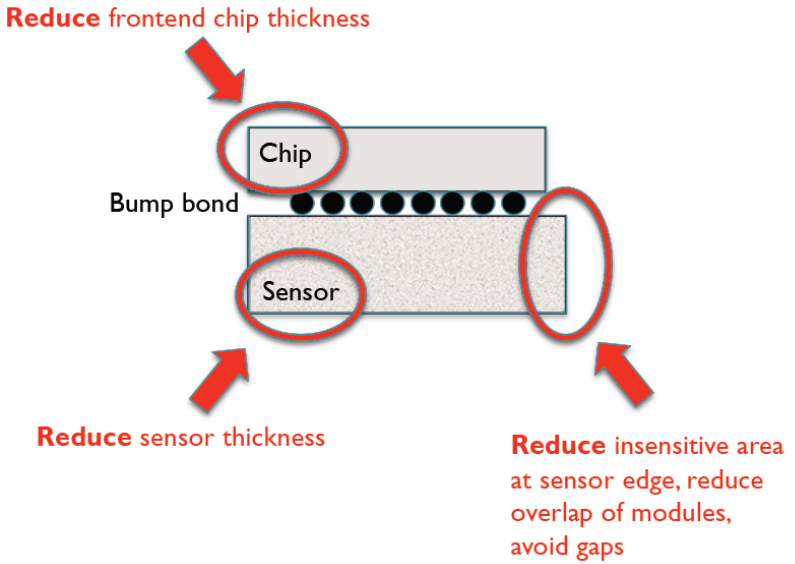
- Provide an interface for chip programming
- Data reading (push/pull modes)
- Handling of trigger information
- Chip synchronization SVT-wide

Known pieces to implement:

- Clock reception and distribution (details?)
- 12x1 Gbit/s and 2x2.5 Gbit/s optical links
- Storage memory (>128 Mbytes) for event handling

Attivita' Bari: Hyprid Pixel, chip encoder

- Collaborazione attivita' design/ assottigliamento sensori a pixel epitassiali ed edgless. Sinergia con attivita' upgrade di Alice. Run a FBK in collaborazione Alice/SuperB (BA-TN-TS)
- Programma di interconnessione bump-bonding (IZM) con chip FE e sensorsi (ALICE upgrade)



- Collaborazione con MI al progetto per il chip di encoding per HDI
- Possibile interesse anche su meccanica/costruzione moduli a strip

consumo	Testboard/componenti per test funzionali chip pixel assottigliati connessi con bump-bonding	5
consumo	Setup per test funzionali dell'encoder	6
interno	contatti con collaboratori TS/TN sensori a bordo attivo	2
interno	contatti con collaboratori MI elettronica - sviluppo/test encoder / serializzatore	2
interno	contatti con collaboratori PI meccanica SVT	2
estero	Test Beam al CERN	2
estero	Contatti con Dallas per sviluppi serializer/driver/receiver + test	4
consumo	Manutenzione camera pulita (quota parte)	2

Attivita' Trento: Sensori pixel, strip

- Collaborazione all' attivita' sui sensori a pixel (HP option) epitassiali ed edgless. Design di sensori con geometria adatta all' inteconnessione con chip Superpix1 32x128.
- Design delle maschere dei sensori a strip per produzione da meta' 2012 (collaborazione con TS, Con QM?).

consumo	Consumi Laboratorio: PCB, componenti, connettori per test elettrici ed elettro-ottici sui sensori con bordo attivo	2
inventario	Workstation per simulazioni sensori TCAD 3D	4
interno	contatti con collaboratori TS/BA design sensori pixel/strip	1
estero	Contatti IZM per bump-bonding	2

Attivita' Torino: Meccanica testbeam

- Continua a collaborare per testbeam SVT con la responsabilita' del tavolo movimentato per supporto del telescopio e dei DUT's

consumo	Aggiustamenti tavolo testbeam	1
interno	Preparazione testbeam a Bologna allestimento tavolo	2
trasporti	Trasporto tavolo al CERN per testbeam	1.5
estero	Partecipazione testbeam CERN	4

Attivita' RomaIII: MAPS

- Collaborazione alla II sottomissione INMAPS e partecipazione al testbeam (pixel INMAPS)

consumo	Sistema test schede MAPS	5
interno	Riunioni SVT	1
estero	Test Beam CERN	2

SVT sommario richieste

			MI-SVT(kE)			ME-SVT(kE)			Consumi (kE)			Apparati (kE)			Lic. SW (kE)			INV (kE)			Trasporti (kE)		
Sistema	Sede	FTE	Rich	Ass	s.j.	Rich	Ass	s.j.	Rich	Ass	s.j.	Rich	Ass	s.j.	Rich	Ass	s.j.	Rich	Ass	s.j.	Rich	Ass	s.j.
SVT	BO	2.5	2			8.0			16.0						2.5			3			2.5		
	Milano	5.4	14			24.5			40.5			74			7.5			21					
	Mi B - DTZ	1.5	3			3.0			17.0		12												
	Pavia	4.3	2			14.0			4.0			90											
	Pisa	6.0	9			21.5			97.0			70			6.5								
	RM3-DTZ	0.2	1			2.0			5.0														
	Trieste	3.6	2			9.0			49.0						3.5						0.5		
	Torino		2			4.0			1.0												1.5		
	Trento	2.1	1			2.0			2.0									4					
	Bari	2.0	6			6.0			13.0														
TOT		27.6	42.0			94.0			244.5		12.0	234.0			20.0			28.0			4.5		

+ 7 FTE w.r.t 2011

42 kE Testbeam

- 35 kE sensors
- 40 kE bump-bonding
- 30 kE FE electr
- 65 kE peripheral elect.
- 15 kE DAQ

IC submissions: 196 kE
- 90 kE FE chip strips (PV)
- 70 kE MAPS INMAPS (PI)
- 36 kE Encoder SoS (MI)

backup

Pixel for Layer0

- Clearer definition of requirements for Layer0 pixels:

Physics:
- Resolution of 10-15 um in both coordinates
- Total material budget <= 1% X_0
- Radius ~1.3-1.5 cm

Background (x5 safety included)
- Rate ~100-300 MHz/cm2 depends on radius and sensor thickness
  - Timestamp of 1 us → 5-10 Gbit/s link
- TID ~ 15Mrad/yr
- Eq. neutron fluence: 2.5 10^{13} n/cm^2/yr
  - Standard CMOS MAPS marginal

Several options still open & under development → decision on technology in 2013

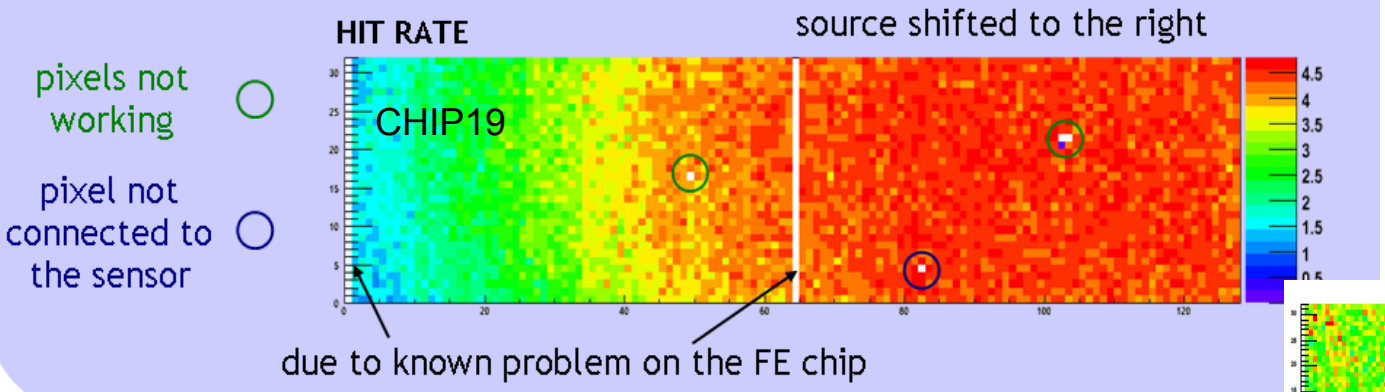
- Hybrid pixels: more mature and rad hard but with higher material budget
  - R&D on FE chip 50x50 um pitch with fast readout ongoing (INFN – SuperB SVT group)
  - Pixel module design with ~ 1% X0 with present technology
  - Evaluate reduction of material in silicon & pixel bus: ALICE ITS upgrade (Bari interest)
- CMOS MAPS: newer technology potentially very thin, readout speed and rad hardness challenging for application in Layer0.
  - R&D on DNW MAPS with sparsified fast readout well advanced (INFN – SuperB SVT group)
  - New submission in July with INMAPS CMOS process with high resistivity substrate & quadruple well→ to improve radiation hardness & charge collection efficiency.
- Other groups interested in MAPS option for Layer0: RAL + Strasbourg

Results on Superpix0

- Gain(by C_{inj} scans):
  - 38.0 mV/fC with sensor (6 % dispersion), 40.9 mV/fC w/o sensor (5 %)
- Noise (ENC= RMS_{noise}/Gain):
  - 66 e- w/o sensor , 81 e- with sensor → S/N = 200!
- Threshold dispersion ($RMS_{baseline}$/Gain):
  - 478 e- w/o sensor - 482 e- with sensor
  - Pixel threshold tuning circuit implemented in the next design

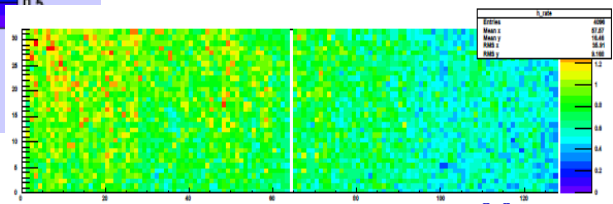
Response to a Sr90 source (e-) threshold@1/4 MIP (60σ noise)

→ good quality of the interconnection @ 50x50 μm² pitch & working sensor!!

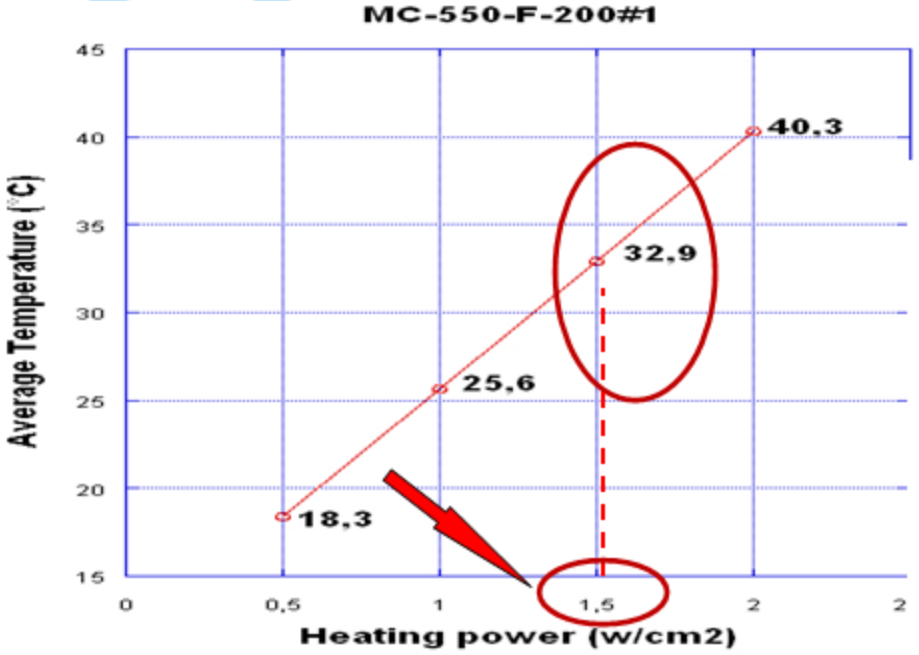


5 defects on 2 chips
6 x 10^{-4}

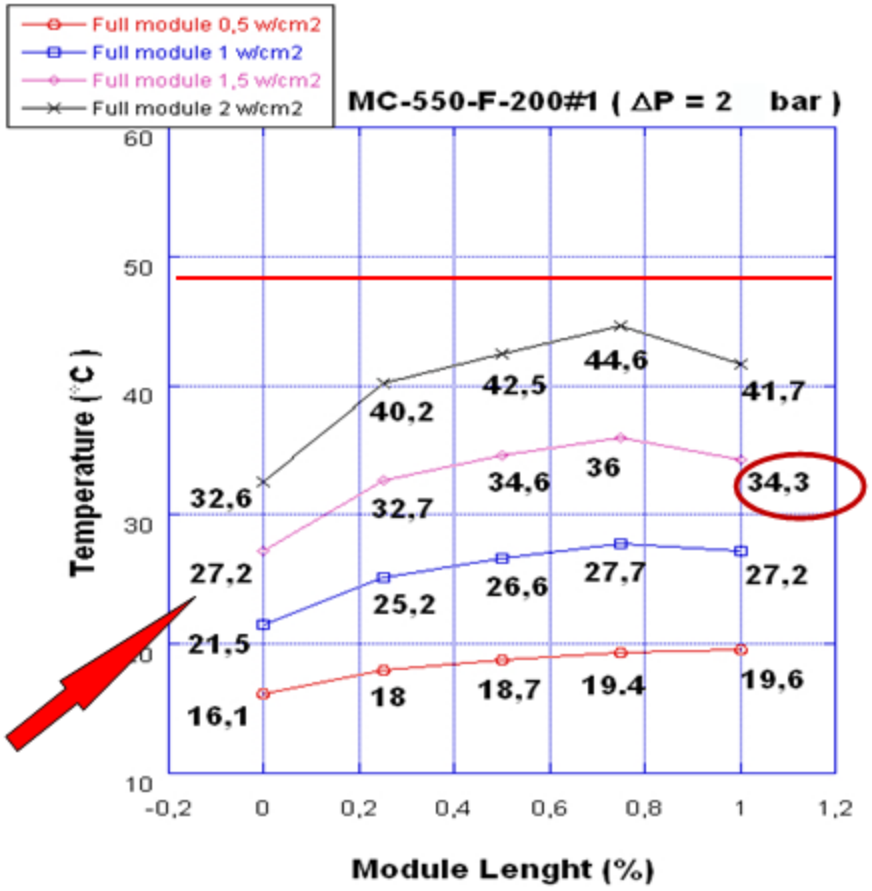
CHIP12: all ch. working



Full module H=550μm test results



Tests performed on net module sample (length = 120 mm) with water-glycol @ 10 °C as coolant (Δp =2,0 atm).

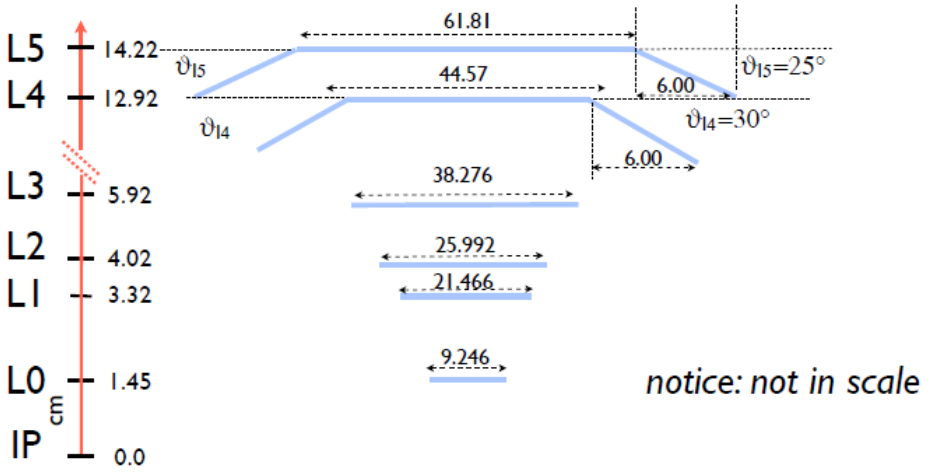


Average module Temperature vs Specific Power

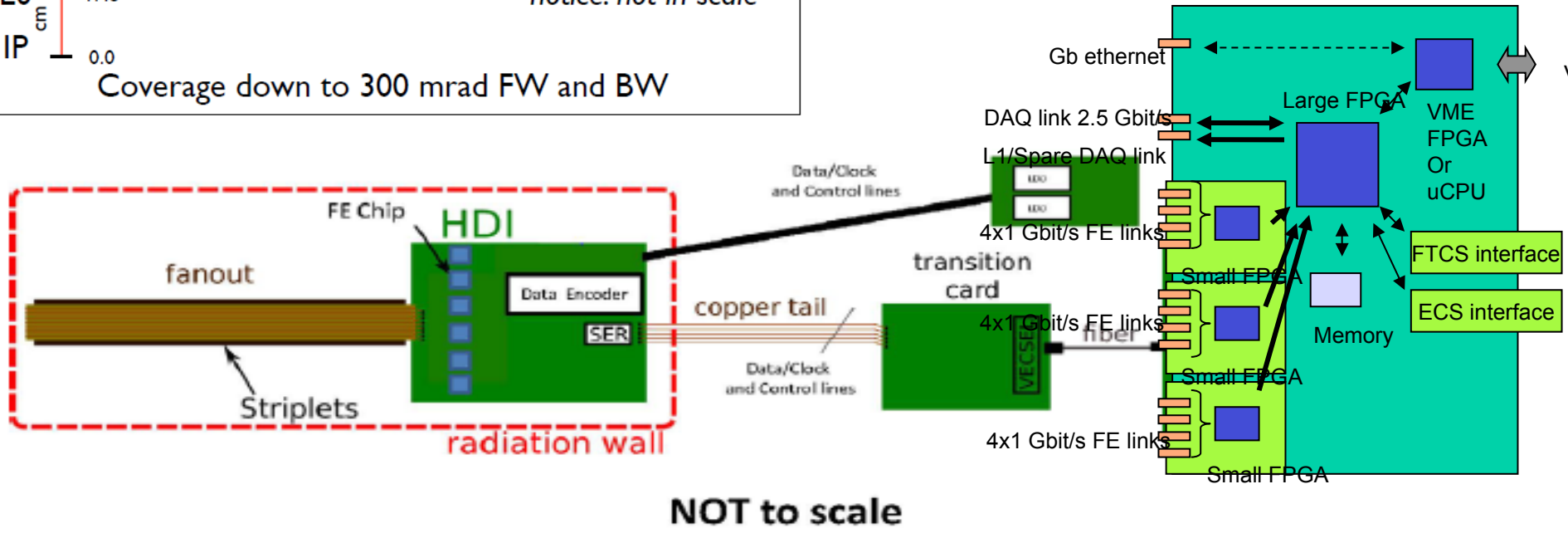
Temperature along the module: ΔT = 7,1 °C at 1.5 W/cm² and Δp =2.0 atm

SuperB SVT

SVT layer geometry for baseline

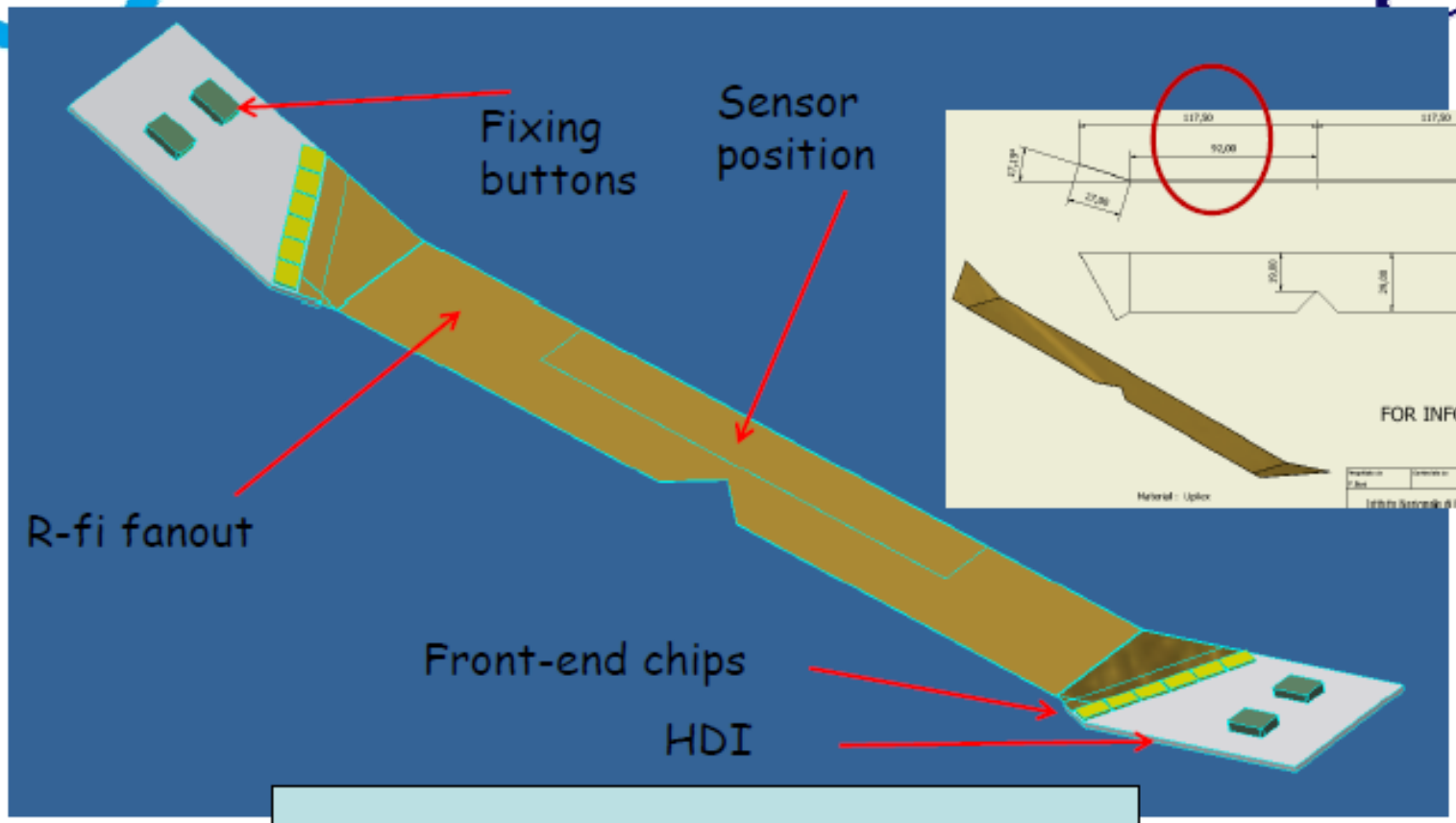


Coverage down to 300 mrad FW and BW



NOT to scale

Module Striplets

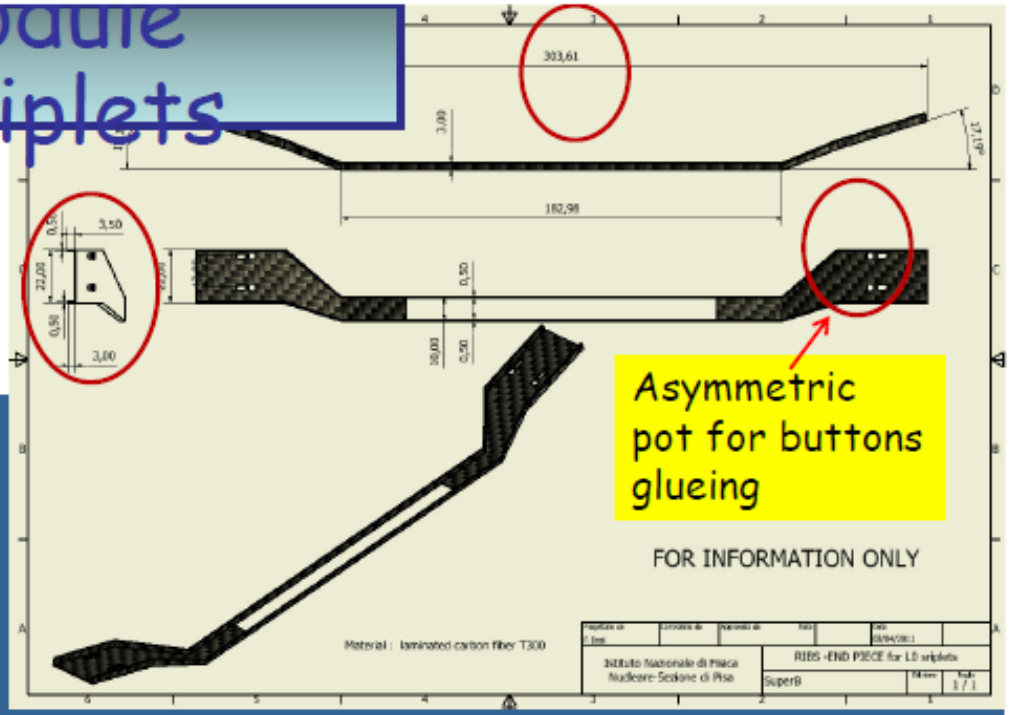


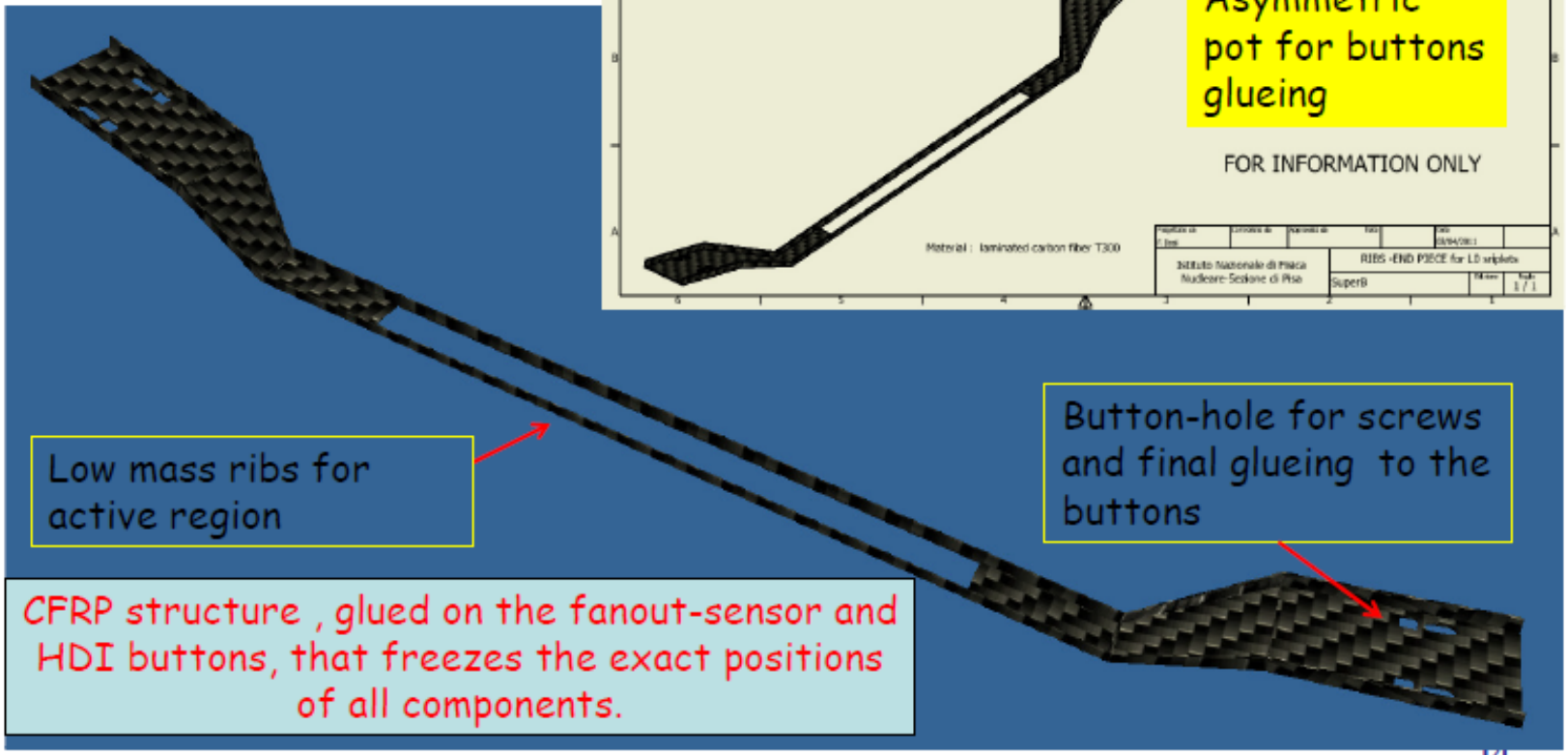
Final solution -HDI in axial direction inclinated at 300 mrad, with front-end chips 30° oriented

F. Bosi, SuperB Workshop , Isola d'Elba May 28 – June2, 2011,

12

Module Striplets





Low mass ribs for active region

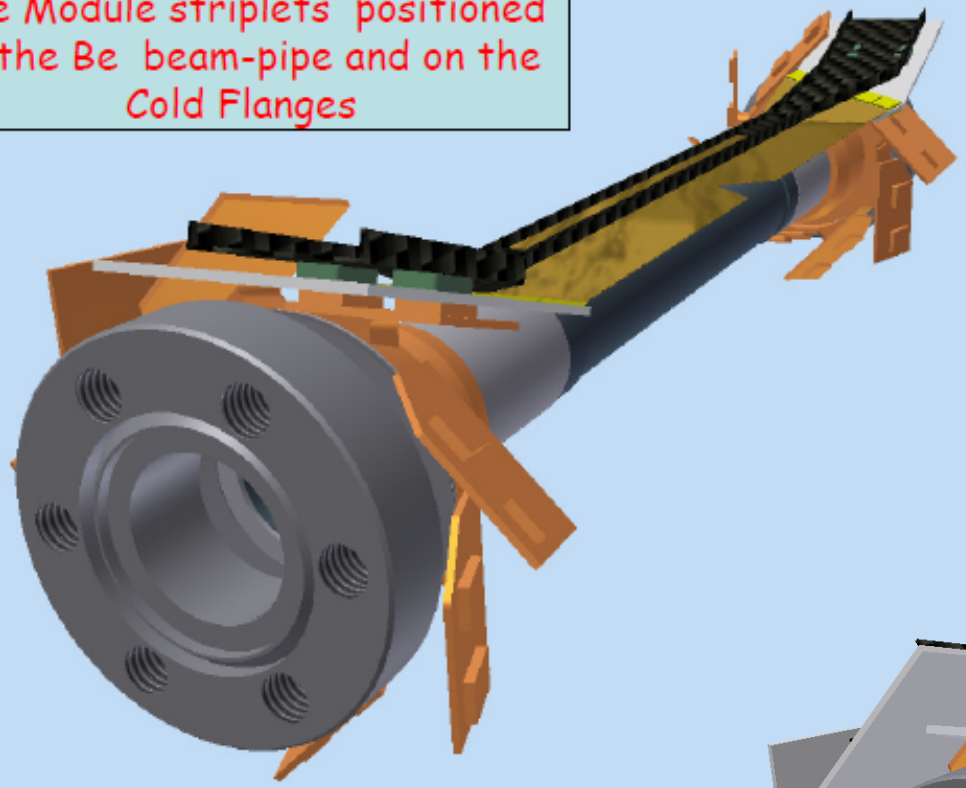
Button-hole for screws and final glueing to the buttons

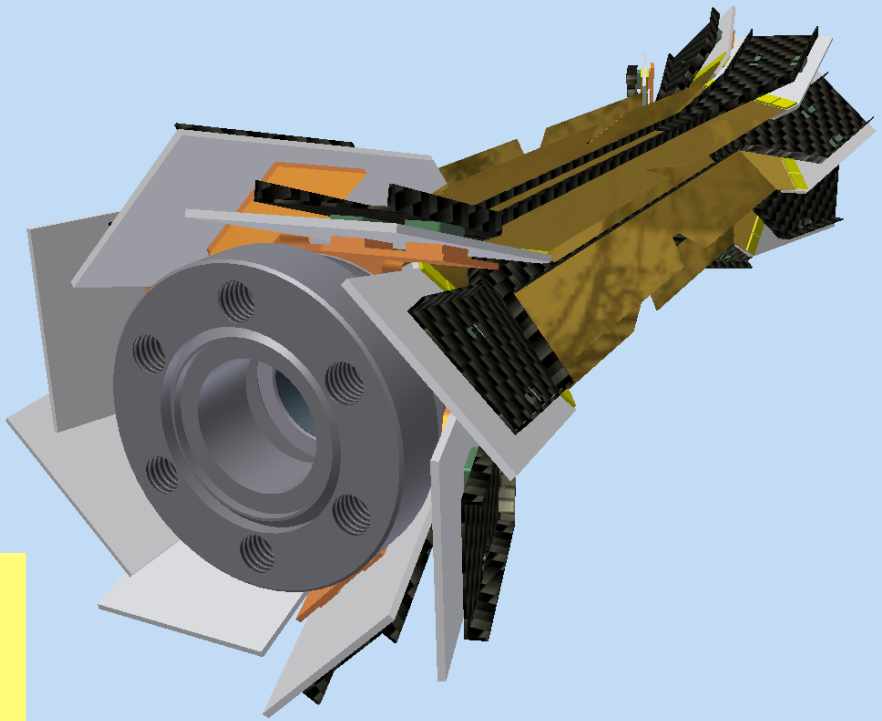
CFRP structure , glued on the fanout-sensor and HDI buttons, that freezes the exact positions of all components.

14

F. Bosi, SuperB Workshop , Isola d'Elba May 28 – June2, 2011,

One Module striplets positioned on the Be beam-pipe and on the Cold Flanges





F. Bosi, SuperB Workshop , Isola d'Elba May 28 – June2,

Complete striplets modules, supported by Cold Flange positioned on the Be beam-pipe