TRB3 - multichannel TDC and DAQ platform

G. Korcyl¹, E. Bayer², M. Kajetanowicz³, L. Maier⁴, J. Michel⁵, M. Palka¹, M. Traxler⁶, C. Ugur⁷ for the HADES collaboration

¹ Jagiellonian University, Kraków, Poland; ² Department for Digital Electronics, University Kassel, Kassel, Germany; ³ Nowoczesna Elektronika, Kraków, Poland; ⁴ Department for Physics E12, Technical University Munich, Munich, Germany; ⁵ Institute for Nuclear Physics, Goethe University, Frankfurt, Germany; ⁶ GSI Helmholtzzentrum für Schwerionenforschung, Darmstadt, Germany; ⁷ Helmholtz-Institut Mainz, Johannes Gutenberg-Universitat Mainz, Mainz, Germany

Versatile measurement solution - high precision ADC, QDC, TDC

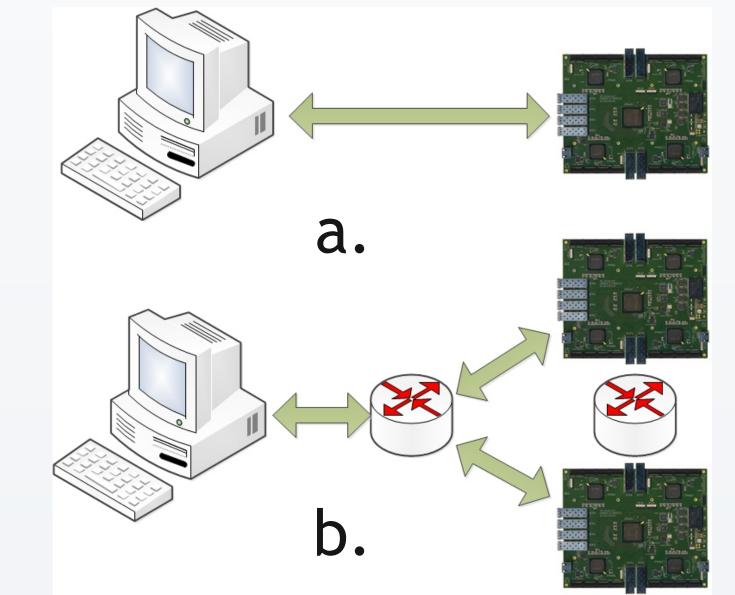
Trigger Readout Boards v3 as a new solution for any kind of charge or time measurement for modern physic experiments:

Hardware features:

- Power of 5x Lattice ECP3 150 FPGAs gives a space for implementation of sophisticated measurement mechanisms, DSP algorithms and connectivity features
- 4x 208-pin QMS connectors: high input/output channel density, act as extension ports for different kind of mezzanine cards providing power and data channels
- 106-pin Addon board connector on back for even more extendable solution

• FPGA firmware features:

- High precision time measurement (~ 14ps RMS) based on FPGA logic, up to 64 channels per FPGA
- Integrated data acquisition
- Gigabit Ethernet connectivity together with UDP stack and customizable basic protocols



Board usage scenarios: a) stand-alone measurement station or b) part of a larger system

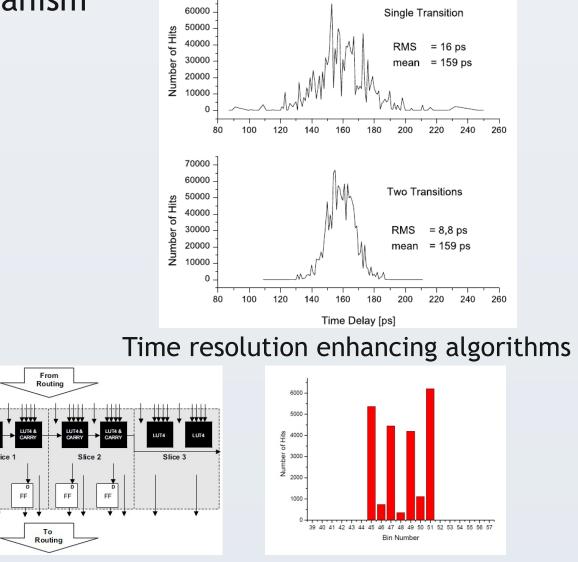
FPGA based Time to Digital Converters

• 4x edge FPGA with TDC design

Concept of using FPGA hardware structure to measure time:

- Resolution of around 14 ps
- Average binning 30 ps
- Multi-hit TDC
- ~40MHz hit rate per channel
- Configurable solution
- High channel density up to 64 per FPGA (256 per board)
- LVDS inputs
- -Temperature and power changes are compensated by online

calibration mechanism



FPGA based TDC concept - use of carry chains

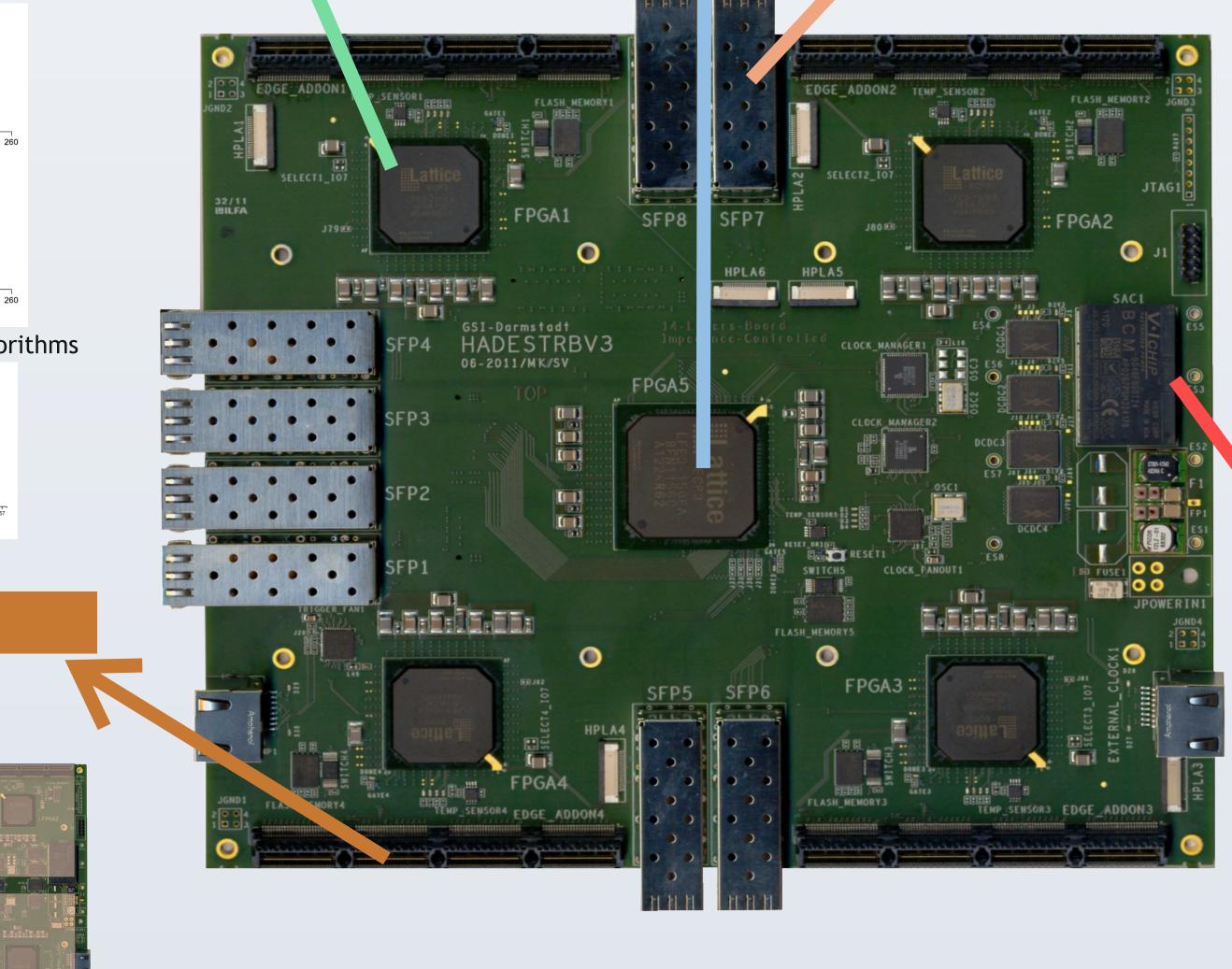
Field Programmable Gate Arrays

• Main FPGA

- High speed LVDS connections to each of the slave FPGAs
- Connectivity through 8x 3.2Gbps optical links
- Controls the operation of the board

Mounted FPGAs: Lattice ECP3 150

- 149k LUTs
- 16x 3.2Gbps SERDES channels
- 6850 Kb SRAM



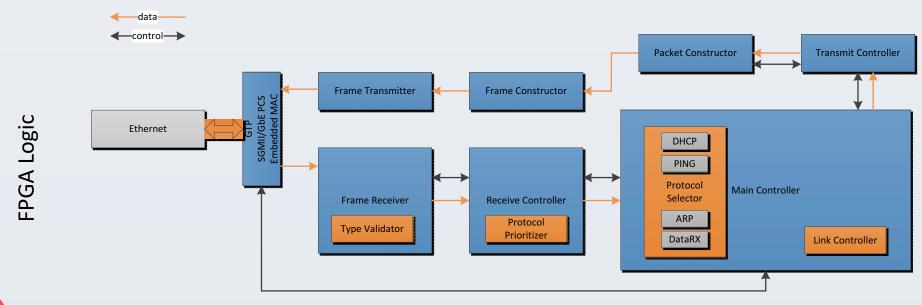
Network Features

• 8x general purpose 3.2 Gbps optical links

Variety of network protocols
Connection to larger complex systems

Gigabit Ethernet 1000BASE-X enabled links

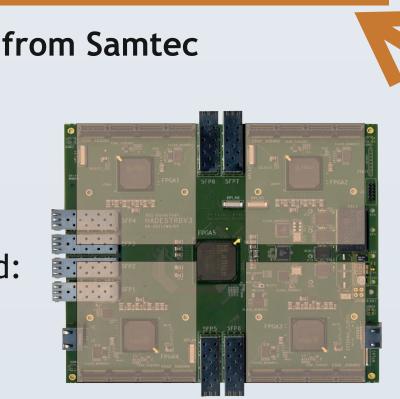
- Transport of collected data
- Slow control
- Full Duplex
- UDP stack implemented as FPGA logic
- Plug-and-Play design (DHCP, ARP)
- VLAN functionality
- Easy custom protocol implementation
- Jumbo frames



Giagbit Ethernet with higher level protocols FPGA implementation

QMS Connectors

- 208 pin high-speed connector from Samtec
 Used to transport:
 - timing signals
 - application specific data
 - power
- Slots to connect mezzanine card:
 - up to 4 cards per board
 - different apllications
 - customizable solution



Trigger Readout Board v3

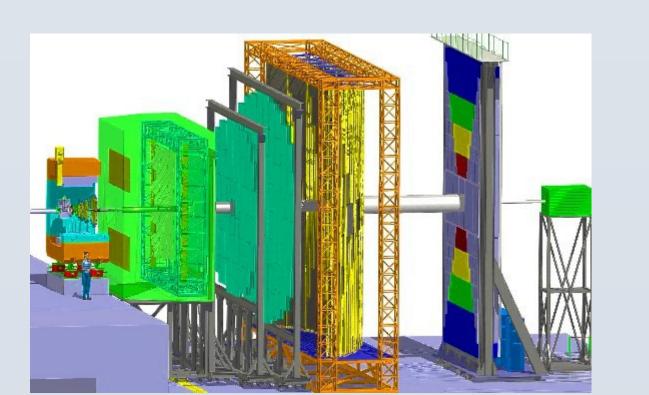
General info

- Power supply: 48V galvanically separated DC/DC
- Board size: 20cm x 23 cm
- 106 pin + power connector on back for AddOn boards
- RJ45 trigger input
- JTAG programming chain
- Flash ROM for each FPGA to store designs for quick boot-up
- External clock input for synchronous systems

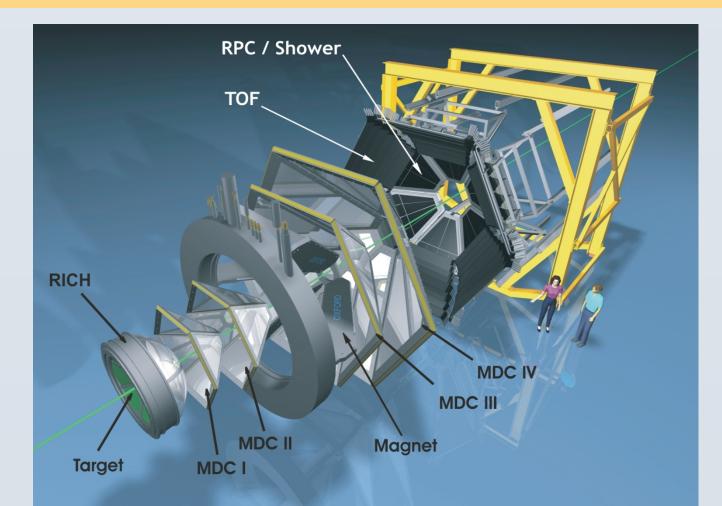
Applications

• High energy physics experiments:

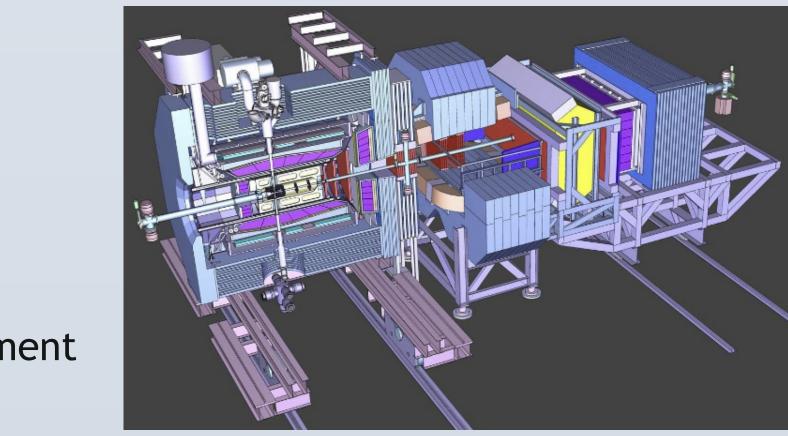
- Designed for any kind of detectors needing precise time measurement like Photomultiplier Tubes or Resistive Plate Chambers
- Can be used for charge measurement additional mezzanine Addon boards needed (development in progress)
- Network HUB 8x optical links installed on the main board can be extended by Addon boards
- Trigger system thanks to large number of input channels
- Usage scenarios:
 - The board together with a PC can be used as a stand-alone measurement station
 - Optical links provide connectivity in order to use the board in complex DAQ systems



Compressed Baryonic Matter (GSI, Darmstadt, Germany)



High Acceptance Di-Electron Spectrometer (GSI, Darmstadt, Germany)



Ongoing projects:

- Development of ADC mezzanine Addon board 4 different approaches will be tested
- Development of HUB mezzanine Addon board with 6 optical links
- Integration with HADES Data Acquisition System (GSI, DE) experiment
- Development of TRBv3 FrontEnd Boards for Barrel DIRC, Disk DIRC and Straw Tube Tracker for PANDA (GSI, DE) experiment
- Preparation for use in two Positron Emission Tomography projects at JU (Kraków, PL) and LIP (Coimbra, PT)
- Evaluation of the board for RICH, TOF and MVD detectors readout for CBM experiment (GSI, DE)
- Many more ...

HADES



anti-Proton ANnihilation at DArmstadt (future project at GSI, Darmstadt, Germany)

Contact

Grzegorz Korcyl

Faculty of Physics, Astronomy and Applied Computer Science Jagiellonian University in Cracow

Poland

E-mail: grzegorz.korcyl@uj.edu.pl