TROC EQM Architecture

December, 2023

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Outline

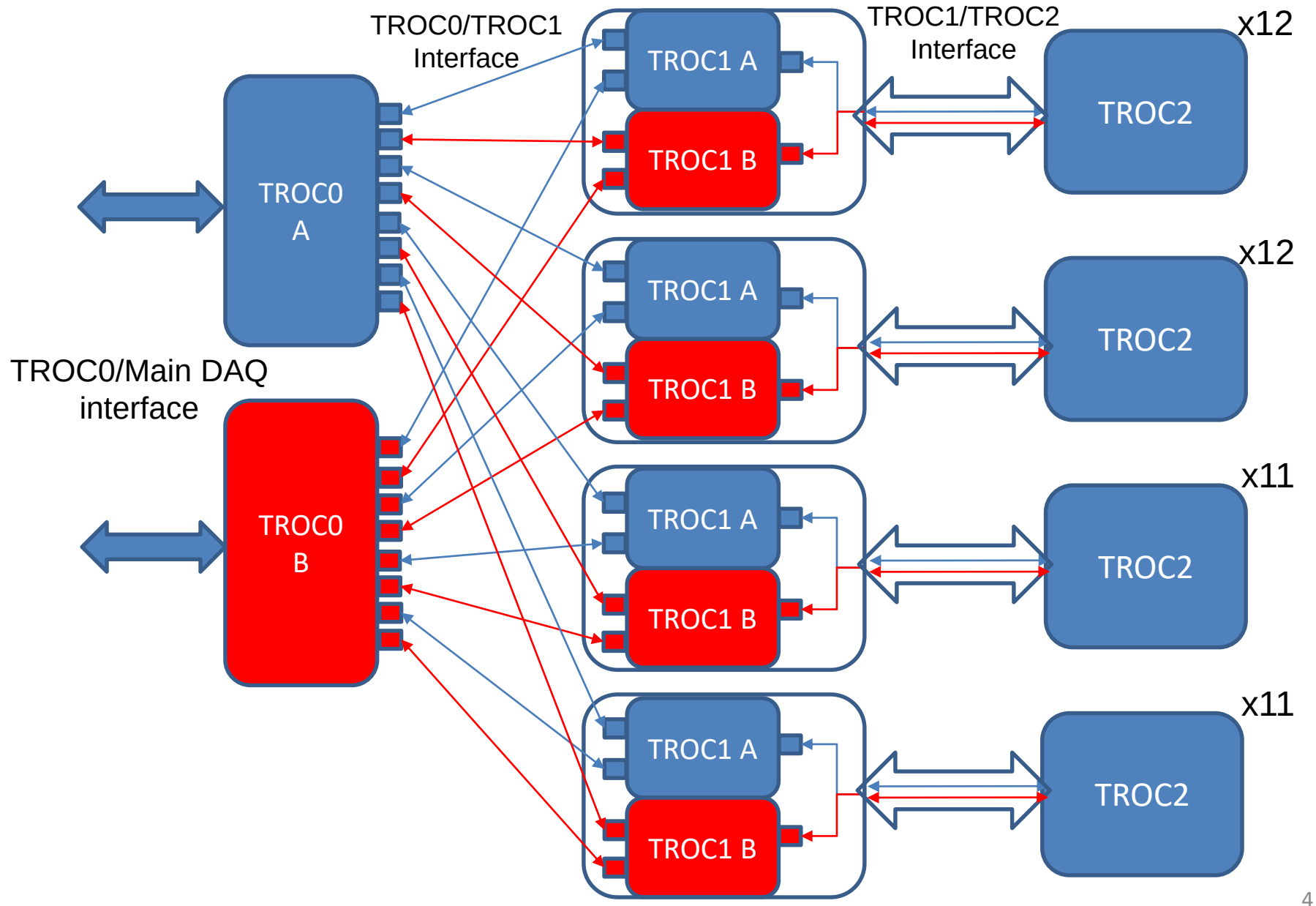
- EQM concept
- EQM System architecture
- TROC1 v2 interfaces
- Power and grounding scheme

EQM Concept

- Functionality as close as posible to final design
- Modularity and interfaces as close as posible to final design
- Redundancies as close as posible to final design
- Some electronics components may not be final
- Standard PCB construction, not suitable for space

- PCB mechanics as close as posible to final design
- PCB thermal interface not final

EQM system architecture



EQM FPGA

- TROC2:
  - Spartan 6 used so far
  - Migration to Artix 7 planned for EQM
  - Final part for QM/FM to be studied depending on radiation levels, reconfiguration methodology, export control.

- TROC1:
  - Spartan 7 used so far
  - Migration to Artix 7 planned for EQM
  - Final part for QM/FM to be studied depending on radiation levels, reconfiguration methodology, export control.

- TROC0:
  - Not defined so far
  - Final part for QM/FM to be studied depending on radiation levels, reconfiguration methodology, export control.

EQM TROC1 – TROC2 interface

- Each TROC2 has double interface with its corresponding TROC1 parts A and B
- Each "cable half" should have the following connections:

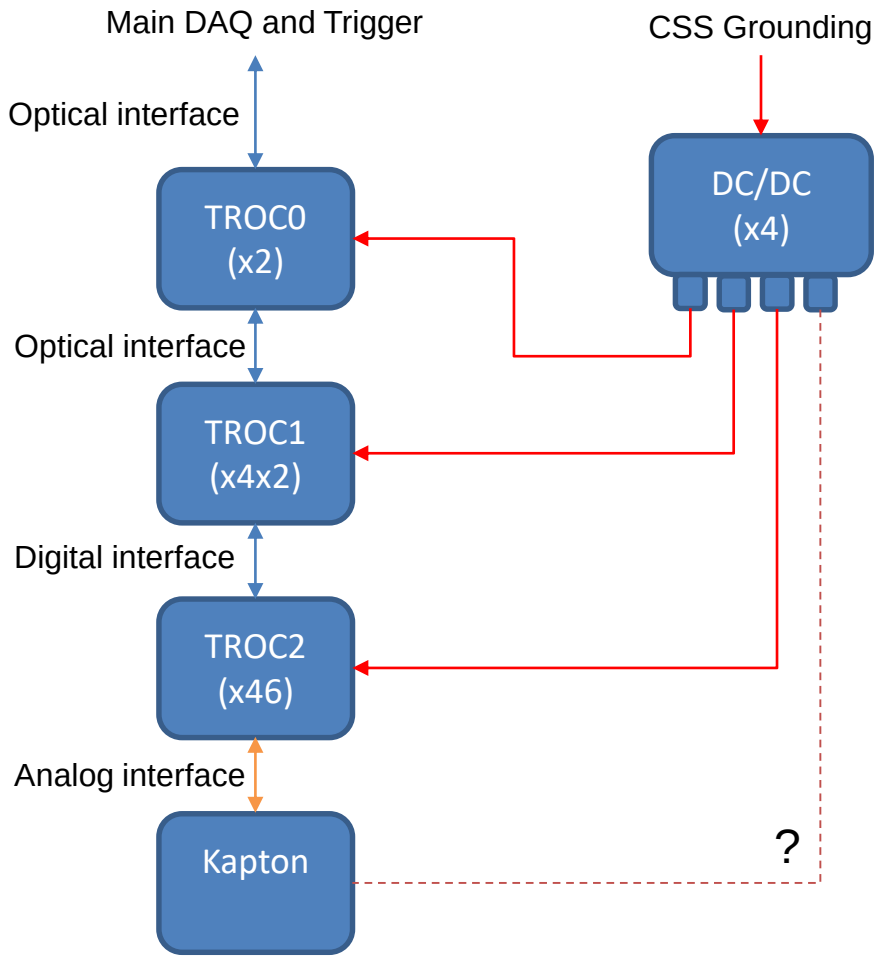
Signal name	Physical/Standard	Number of connections	Direction	Functionality
MTXSRX	LVDS	1	TROC1 TX, TROC2 RX	Slow control data link
MRXSTX	LVDS	1	TROC1 RX, TROC2 TX	Slow Control data link
CLK	LVDS	1	TROC1 TX, TROC2 RX	Clock signal
Trigger	LVDS	1	TROC1 TX, TROC2 RX	Accepted Trigger signal
Data	LVDS	1 (TBD)	TROC1 RX, TROC2 TX	ADC Data + Trigger Data link
FL_ST	LVDS	3 (TBD)	TROC1 RX, TROC2 TX	Self Trigger Data fast links
TDI	LVDS	1	TROC1 TX, TROC2 RX	JTAG, system reconfiguration in flight
TDO	LVDS	1	TROC1 RX, TROC2 TX	JTAG, system reconfiguration in flight
TMS	LVDS	1	TROC1 TX, TROC RX	JTAG, system reconfiguration in flight
TCK	LVDS	1	TROC1 TX, TROC2 RX	JTAG, system reconfiguration in flight

EQM TROC0 – TROC1 interface

- Each TROC1 "half" (either A or B) has interface both with TROC0 boards A and B
- Each interface (i.e., a bundle of fibers) should have the following connections:

Signal name	Physical/Standard	Number of connections	Direction	Functionality
MTXSRX	Optical fiber	1	TROC0 TX, TROC1 RX	Slow control data link
MRXSTX	Optical fiber	1	TROC0 RX, TROC1 TX	Slow control data link
CLK	Optical fiber	1	TROC0 TX, TROC1 RX	Clock signal
Trigger	Optical fiber	1	TROC0 TX, TROC1 RX	Accepted Trigger signal
Data	Optical fiber	1	TROC0 RX, TROC1 TX	ADC Data + Trigger Data links
FL_ST	Optical fiber	1	TROC0 RX, TROC1 TX	Self Trigger Data fast links
TDI?	Optical fiber	1	TROC1 TX, TROC RX	JTAG?, TDB
TDO?	Optical fiber	1	TROC1 RX, TROC2 TX	JTAG?, TDB
TMS?	Optical fiber	1	TROC1 TX, TROC RX	JTAG?, TBD
TCK?	Optical fiber	1	TROC1 TX, TROC2 RX	JTAG?, TBD

HERD PD Grounding Scheme



HERD PD Power Scheme