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RD50-MPW4: Design and preliminary evaluation results

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The RD50-MPW chip series are generic R&D High Voltage CMOS pixel chips aimed at boosting the performance of this sensor technology especially in terms of radiation tolerance, timing resolution and pixel size in view of the harsh requirements imposed by future physics experiments on tracking systems. The latest prototype, RD50-MPW4, demonstrates significant improvements on the current-to-voltage characteristics and pixel noise suppression with respect to its predecessor, RD50-MPW3. To achieve the current-to-voltage characteristics improvements, RD50-MPW4 uses floating p-stop style pixel-to-pixel isolation, implements an optimised multi-guard ring around the chip and has been backside processed to enable backside substrate biasing. The pixel noise suppression is the result of the strategic separation of the power and ground domains between the pixel matrix and peripheral digital readout.

RD50-MPW4 features a 64 rows x 64 columns matrix of 62 µm x 62 µm pixels with both analogue and column drain digital readout electronics embedded inside the large collection electrode. The pixel electronics incorporate logic to mask noisy pixels and an 8-bit SRAM shift register for serial configuration. RD50-MPW4 implements a double column scheme, which together with the 8-bit SRAM shift register, alleviates the routing congestion and facilitates means to minimise the crosstalk. The prototype has an advanced digital periphery for effective pixel configuration and fast data transmission, which consists of one end of column circuit per double column and a slow control system based on the I2C protocol for external communication using an internal Wishbone bus. The event data generated by the pixels is packed into frames, zero suppressed and encoded following the 8b/10b Aurora protocol. It is serialised over a single 640 Mb/s LVDS line. The RD50-MPW chip series are in the 150 nm High Voltage CMOS process from LFoundry S.r.l.

This contribution will focus on the design of RD50-MPW4 and its preliminary evaluation results.

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