RD50-MPW4: Design and preliminary evaluation results

Eva Vilella
On behalf of many people (special thanks to Uwe Kraemer, Bernhard Pilsl, Sam Powell, Helmut Steininger, Chenfan Zhang and Sinuo Zhang for providing material; see next slide for full collaborators list)
University of Liverpool
vilella@hep.ph.liv.ac.uk

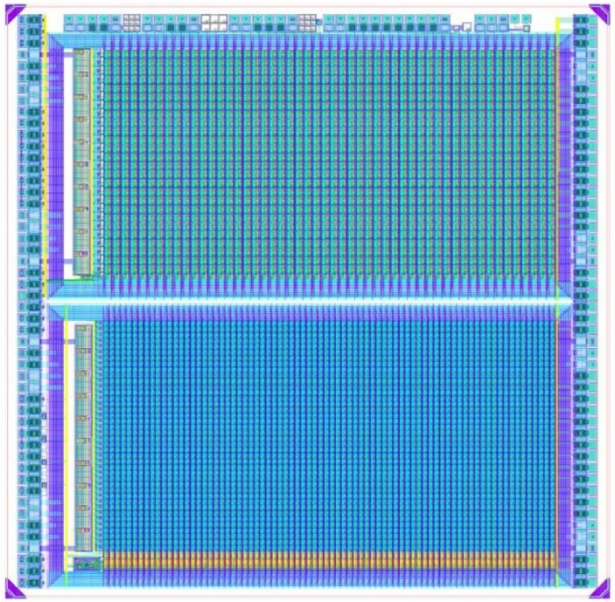
Collaborating institutes

Motivation

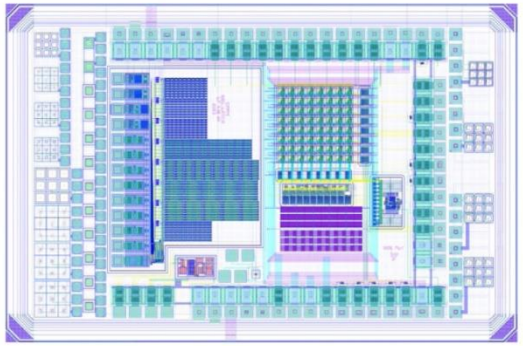
- **Generic R&D programme**
  - To boost the performance of High Voltage CMOS pixel sensors
  - In terms of radiation tolerance, timing resolution and pixel size

RD50-MPW chip series

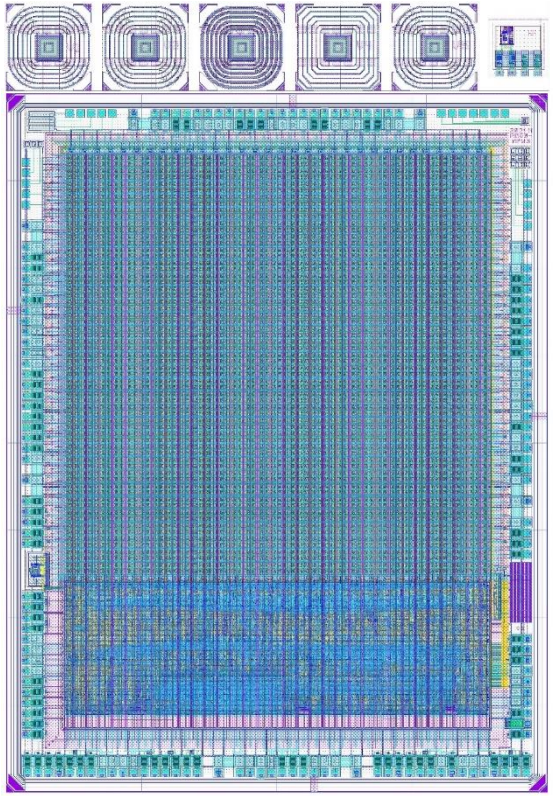
RD50-MPW1



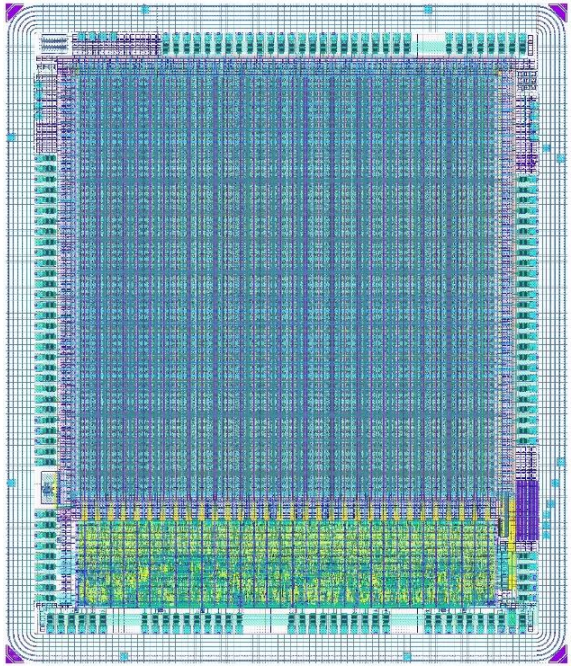
RD50-MPW2



RD50-MPW3



RD50-MPW4



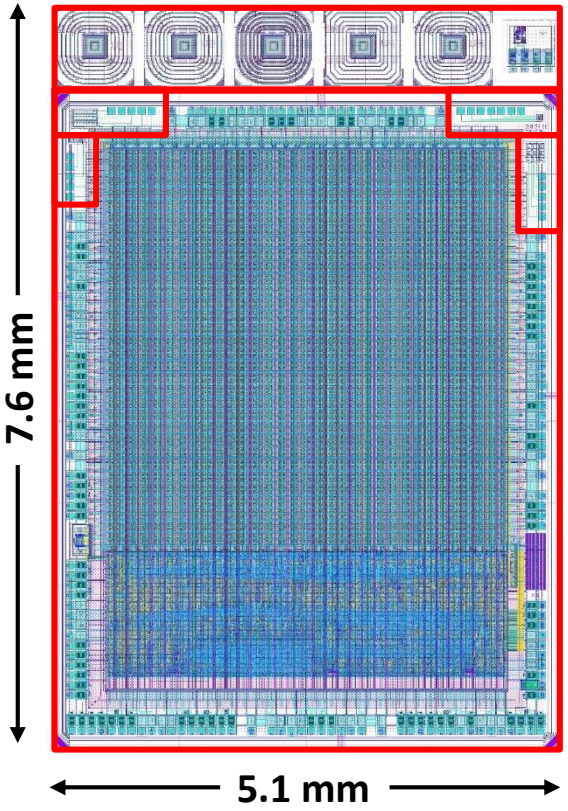
2017 2018 2019 2020 2021 2022 2023 +

RD50-MPW3

- **Main goals**
  - To extend the number of pixels in the active matrix to perform advanced measurements (e.g. test beams)
  - On-chip in-pixel column drain digital readout electronics (FE-I3 style)
  - On-chip digital periphery for effective pixel configuration and fast data transmission

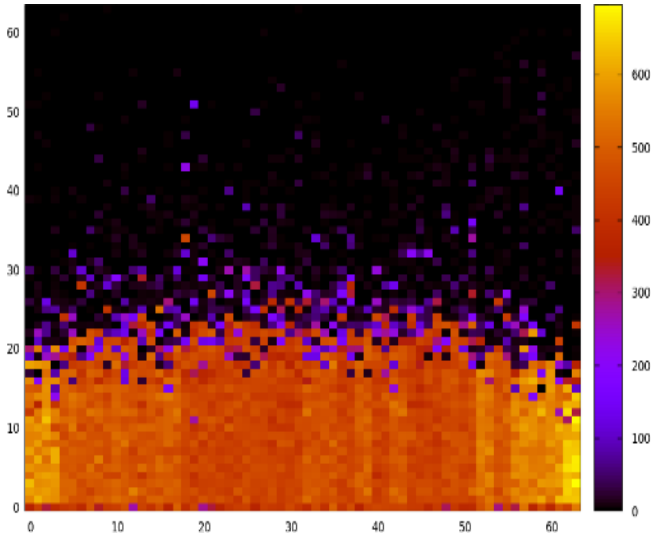
RD50-MPW3

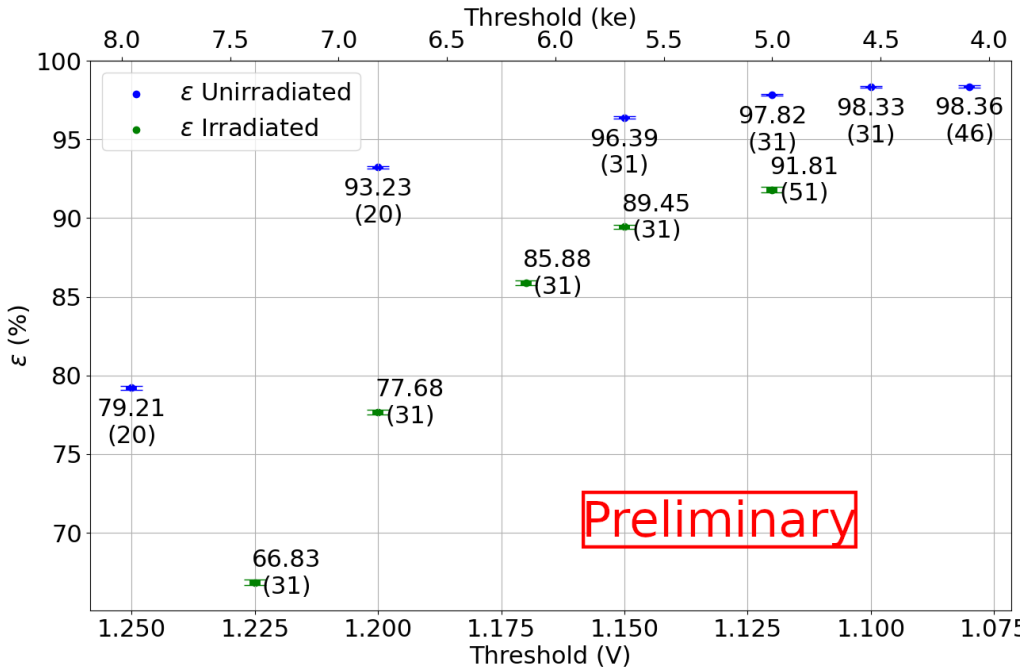
- **Chip contents**
  - Matrix of depleted CMOS pixels with FE-I3 style readout
    - 64 x 64 pixels
    - 62 µm x 62 µm pixel area
    - Analogue and digital readout embedded in the sensing area
    - Double column scheme to alleviate routing congestion and minimise crosstalk
  - Digital periphery
    - 32 EOCs, with 32-events 24-bit FIFOs
    - 128-events 32-bit TX FIFOs
    - I2C protocol, Wishbone bus and one LVDS link
  - Simple chip rings
  - Tests structures (several advanced chip rings, e-TCT, DLTS)
- **Fabrication**
  - Chip fabricated on standard, 1.9 kΩ·cm and 3 kΩ·cm wafers (150 nm HV-CMOS LFoundry)
  - Topside biasing only is possible



RD50-MPW3 – Test beam

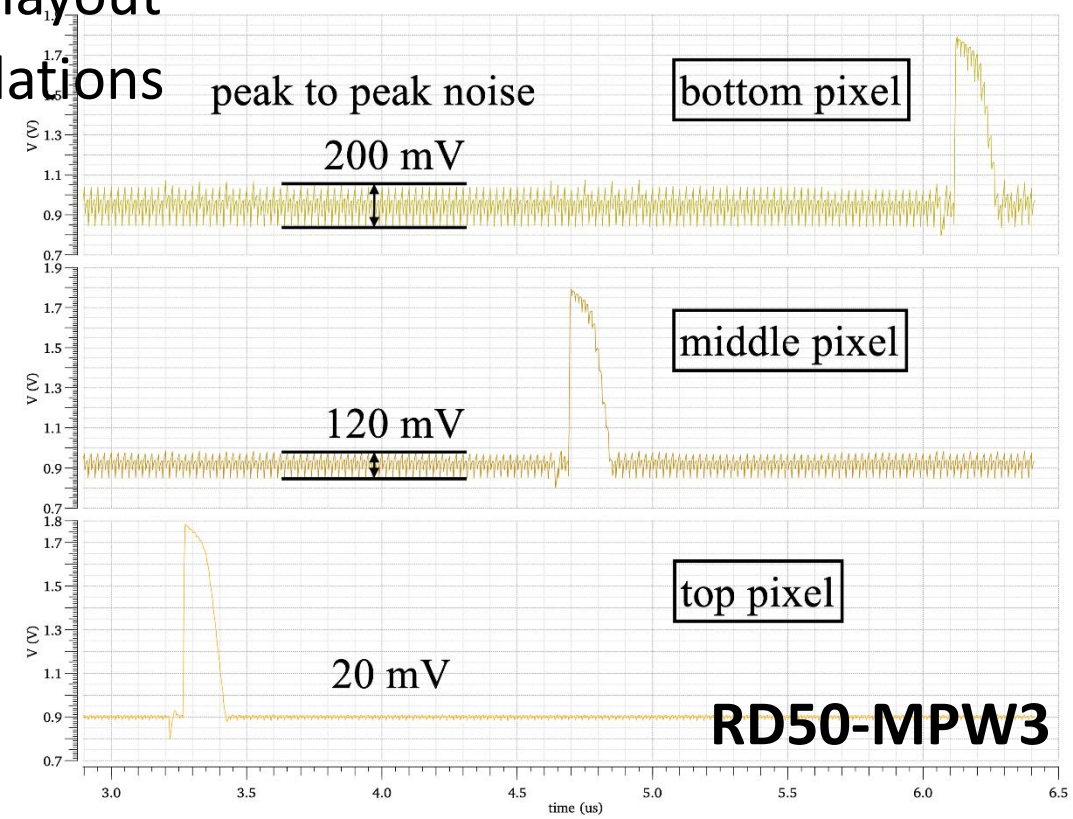
- **Methods and results**
  - *Where* DESY (4.2 GeV)
  - *When* July 2023
  - *DUT* RD50-MPW3, un-irradiated and irradiated samples
    - V_HV = 90 V
    - V_TH = 200 mV
    - Fluence = 1E14 n_{eq}/cm^2
  - *DAQ* Caribou
  - *Trigger* 2-scintillators via AIDA2020-TLU
  - *Telescope* Adenium (6 Alpide planes)
  - *Analysis* Corryvreckan
- **Results**
  - High noise half matrix was ignored
  - Average chip efficiency ~98.3% (before irradiation)

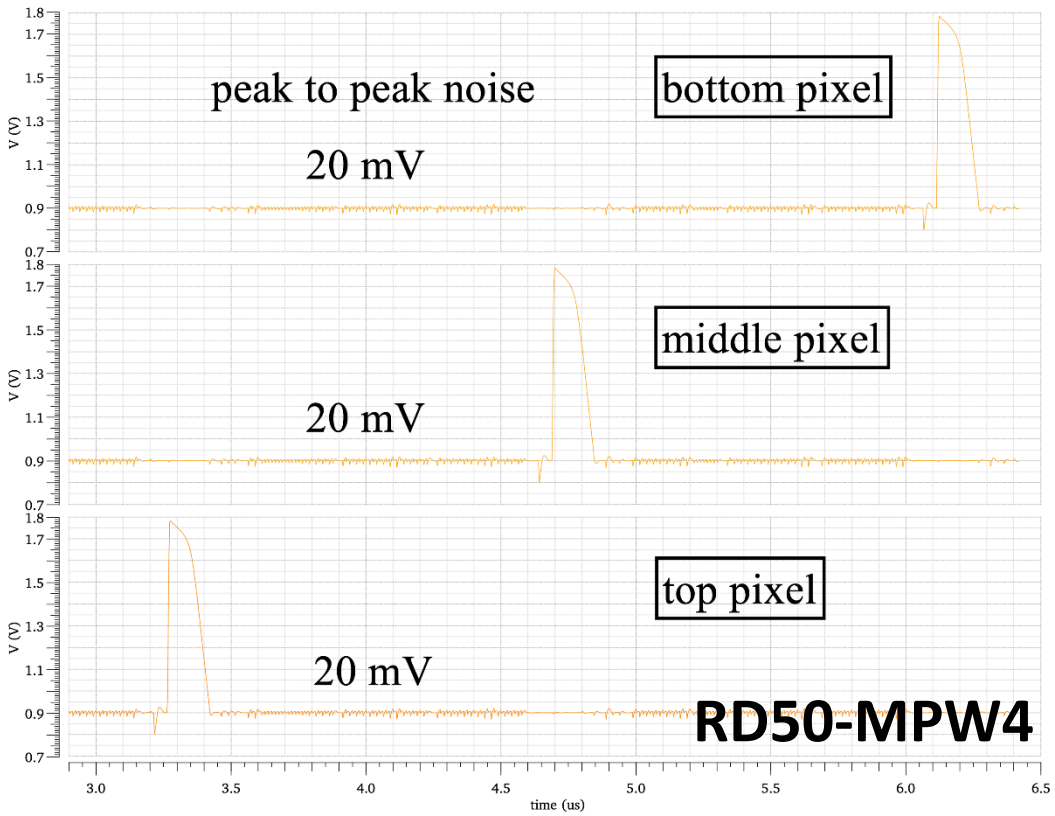




Towards RD50-MPW4 – Power and ground domains

Post-layout simulations

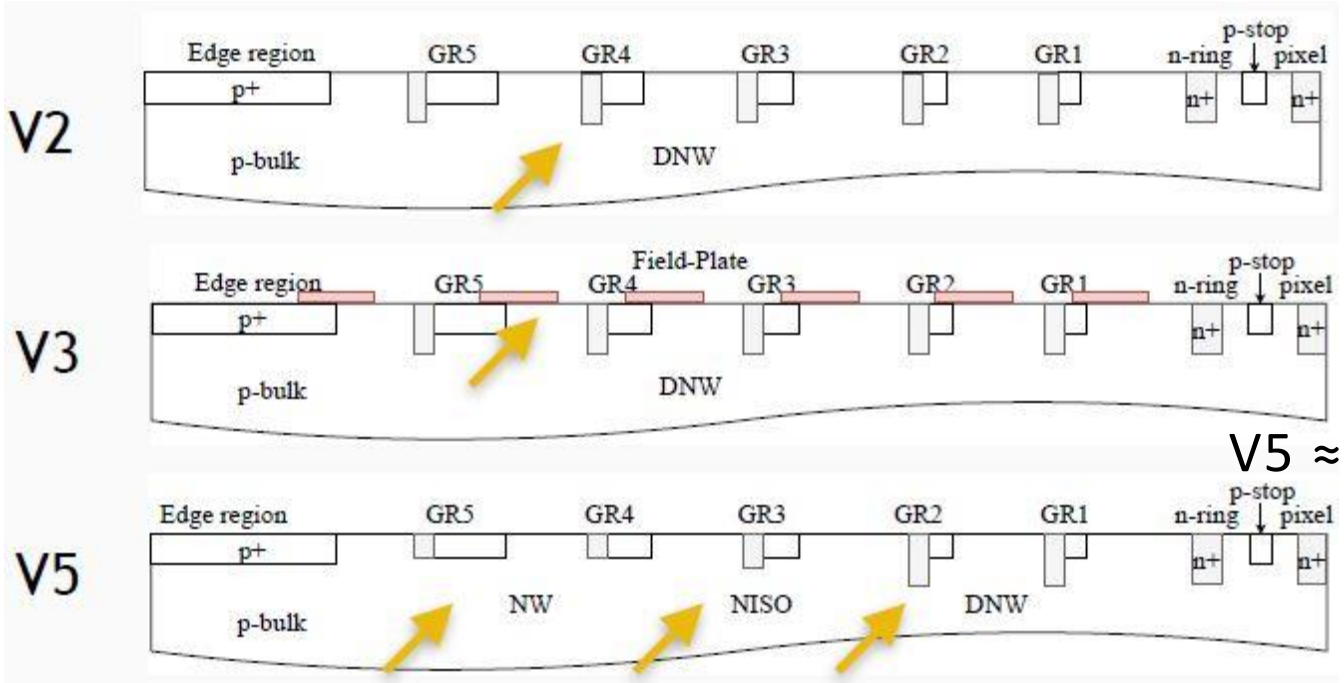




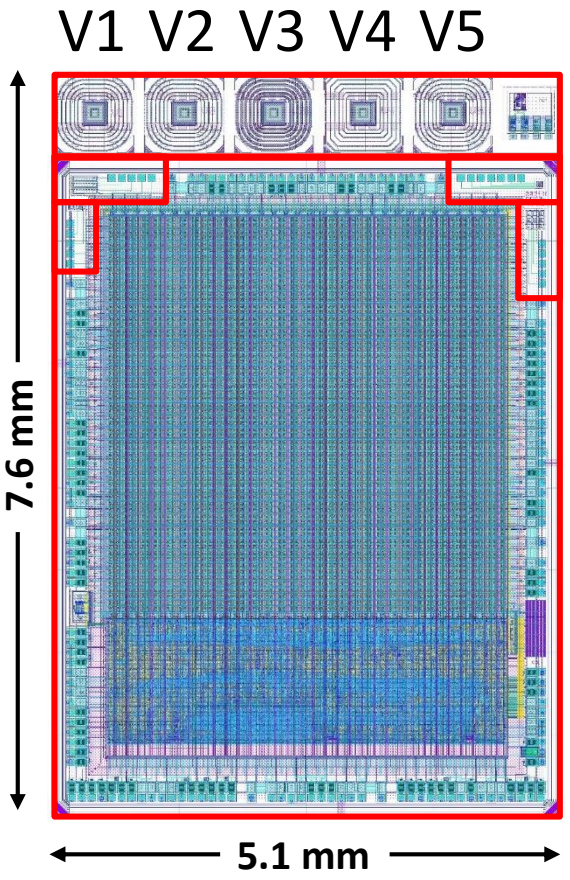
- Simulated analogue output signals of pixels from different locations
  - **Left** The pixel matrix and readout periphery share the same digital power and ground
  - **Right** The digital power and ground of the pixel matrix and periphery are separated

Towards RD50-MPW4 – Rings in RD50-MPW3

- **Guard ring types**
  - V1 old design: n+p GR, large space between n-ring and GR1
  - V2 based on V1: deep n-well replaces standard n-well at GR
  - V3 based on V2: large overhang
  - V4 based on V1: chamfer corner
  - V5 based on V1 & V2: reduced n-well depth from inner to outer GR

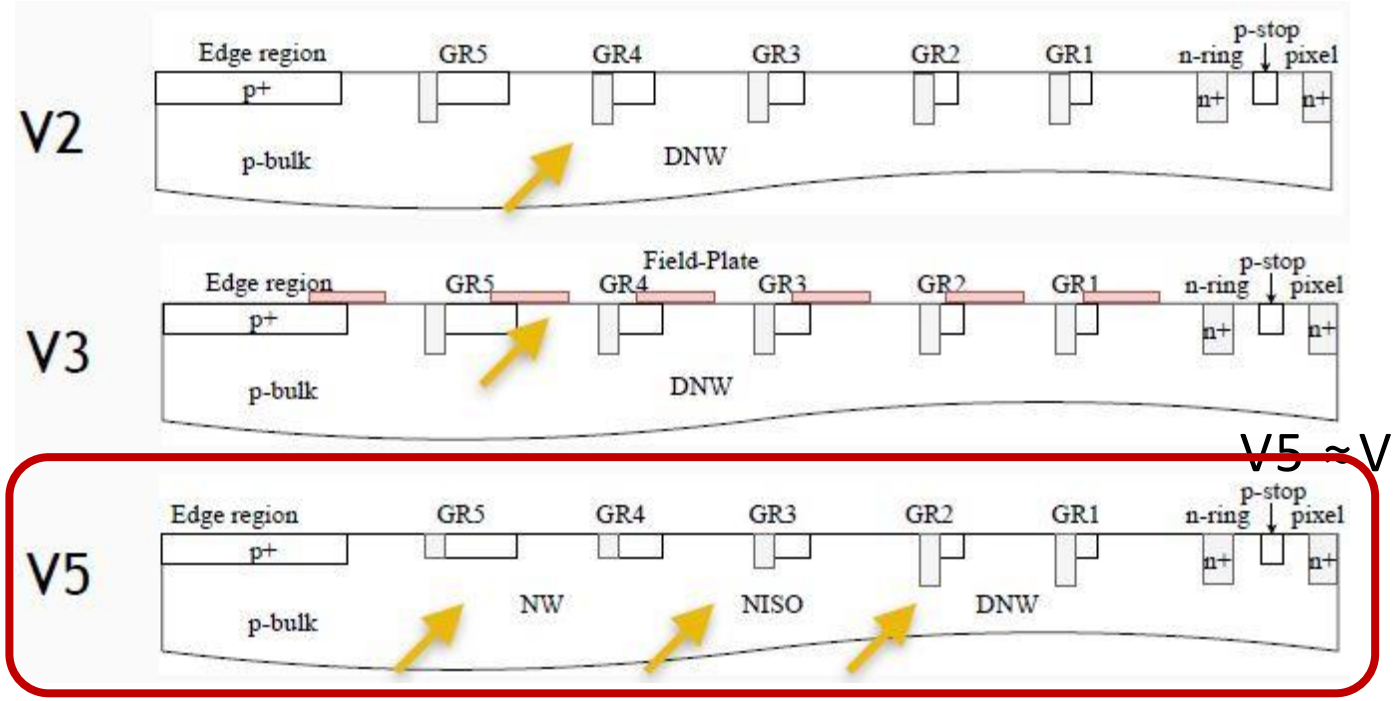


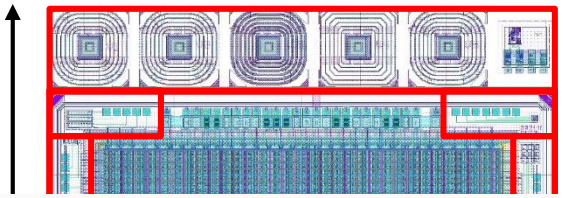
V5 ≈V2 > V3 ≈V1 > V4

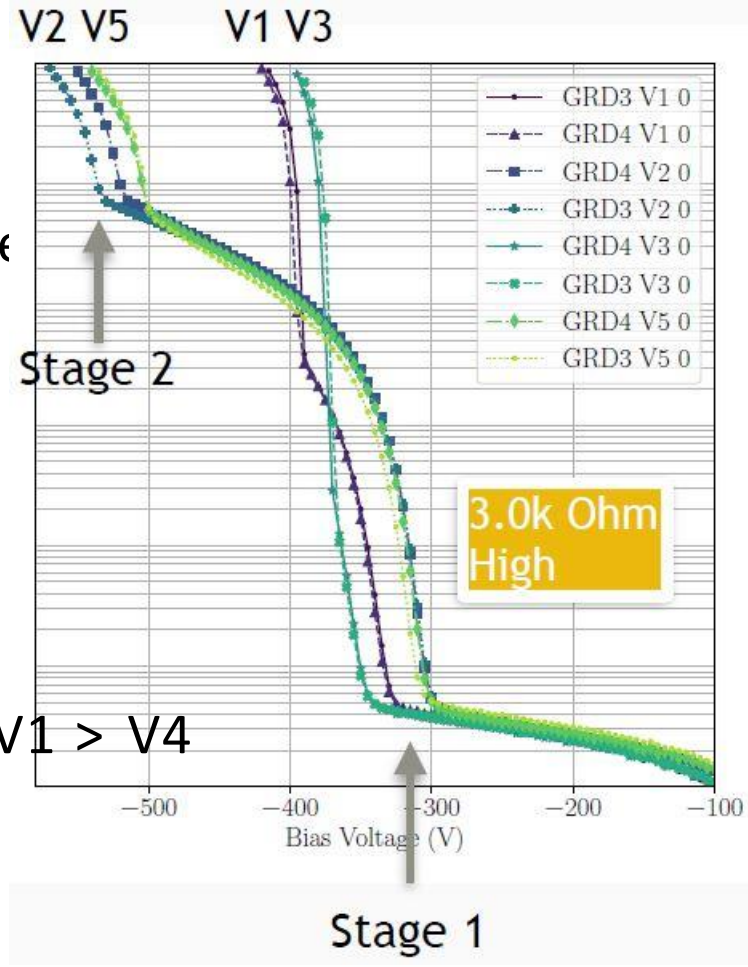


Towards RD50-MPW4 – Rings in RD50-MPW3

- **Guard ring types**
  - V1 old design: n+p GR, large space between n-ring and GR1
  - V2 based on V1: deep n-well replaces standard n-well at GR
  - V3 based on V2: large overhang
  - V4 based on V1: chamfer corner
  - V5 based on V1 & V2: reduced n-well depth from inner to oute







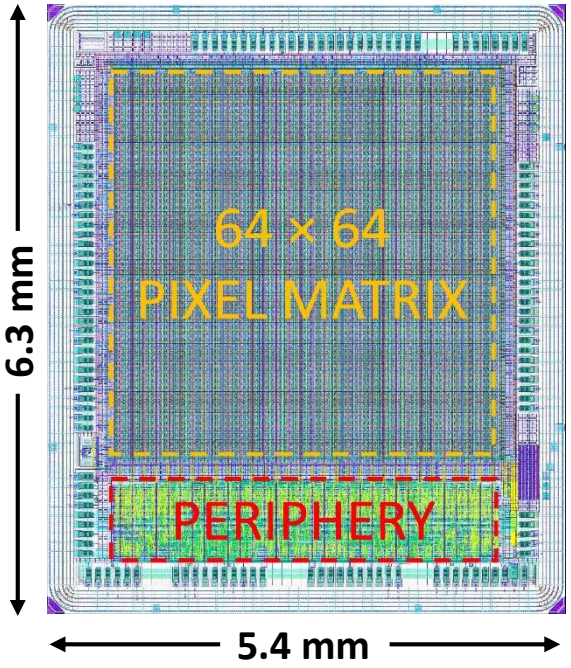
V5 ≈V2 > V3 ≈V1 > V4

RD50-MPW4

- **Main goals**
  - To further improve the current-to-voltage-characteristics
    - Much higher V_BD (and much higher radiation tolerance)
    - New chip ring frame (was a test structure in RD50-MPW3)
    - Chip substrate biasing with topside edge contacts or backside contacts
  - To achieve low-noise by separating the digital in-pixel and digital peripheral power and ground domains
  - To reduce the size of the digital periphery
  - To fix small design bugs from previous chip

RD50-MPW4

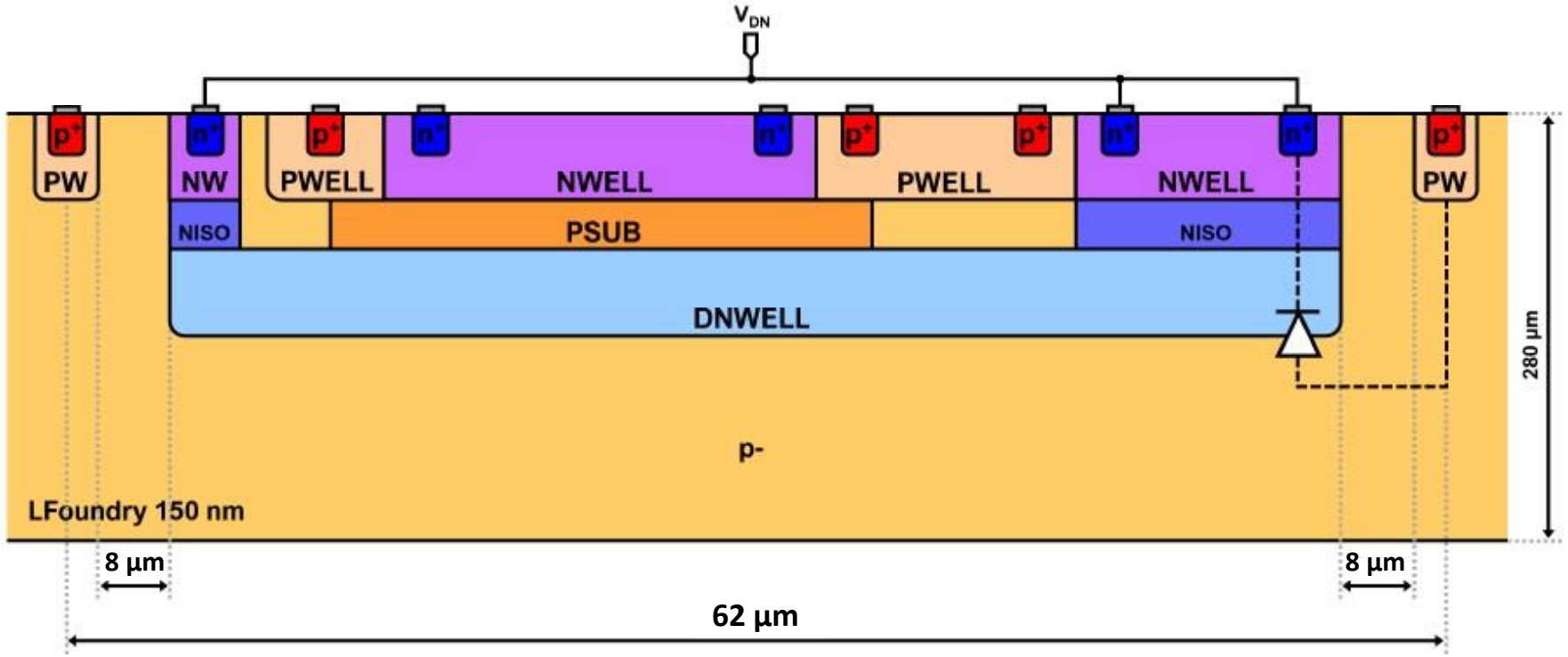
- **Chip contents**
  - Matrix of depleted CMOS pixels with FE-I3 style readout
    - 64 x 64 pixels
    - 62 µm x 62 µm pixel area
    - Analogue and digital readout embedded in the sensing area
    - Double column scheme to alleviate routing congestion and minimise crosstalk
  - Digital periphery
    - 32 EOCs, with *16-events* 24-bit FIFOs
    - *64-events* 32-bit TX FIFOs
    - I2C protocol, Wishbone bus and one LVDS link
  - *Advanced chip rings*
  - Tests structures (e-TCT, DLTS)
- **Fabrication**
  - *Chip fabricated on 3 kΩ·cm wafers* (150 nm HV-CMOS LFoundry)
  - *One wafer with topside biasing only, two wafers allow backside biasing as well*



Delivered in January ‘24 (topside biased) and February ’24 (backside biased)

Process and sensor cross-section

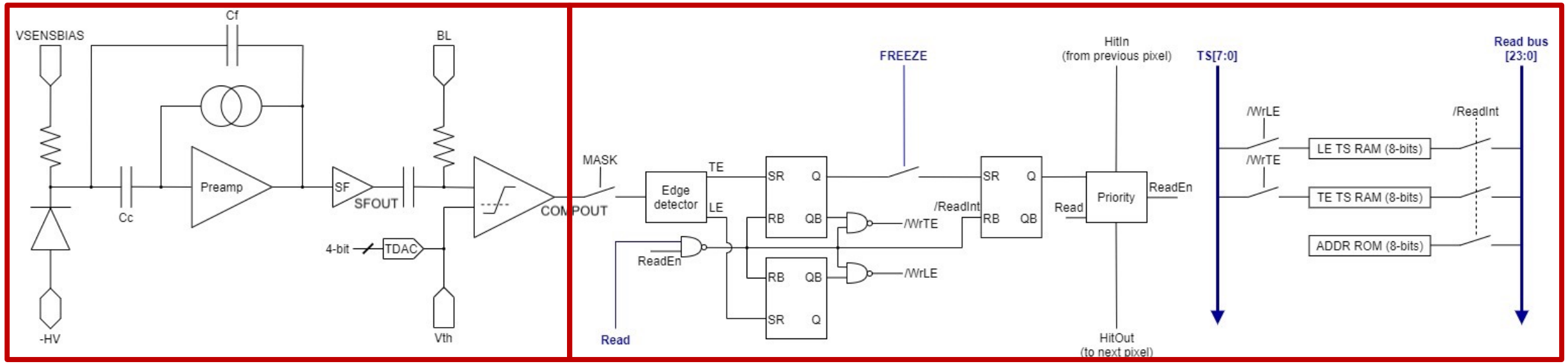
- **150 nm HV-CMOS LFoundry**
  - P-substrate/DNWELL sensing junction
  - Pixel readout electronics embedded inside DNWELL
  - CMOS electronics in sensing diode & isolated from DNWELL with PSUB



Pixel electronics

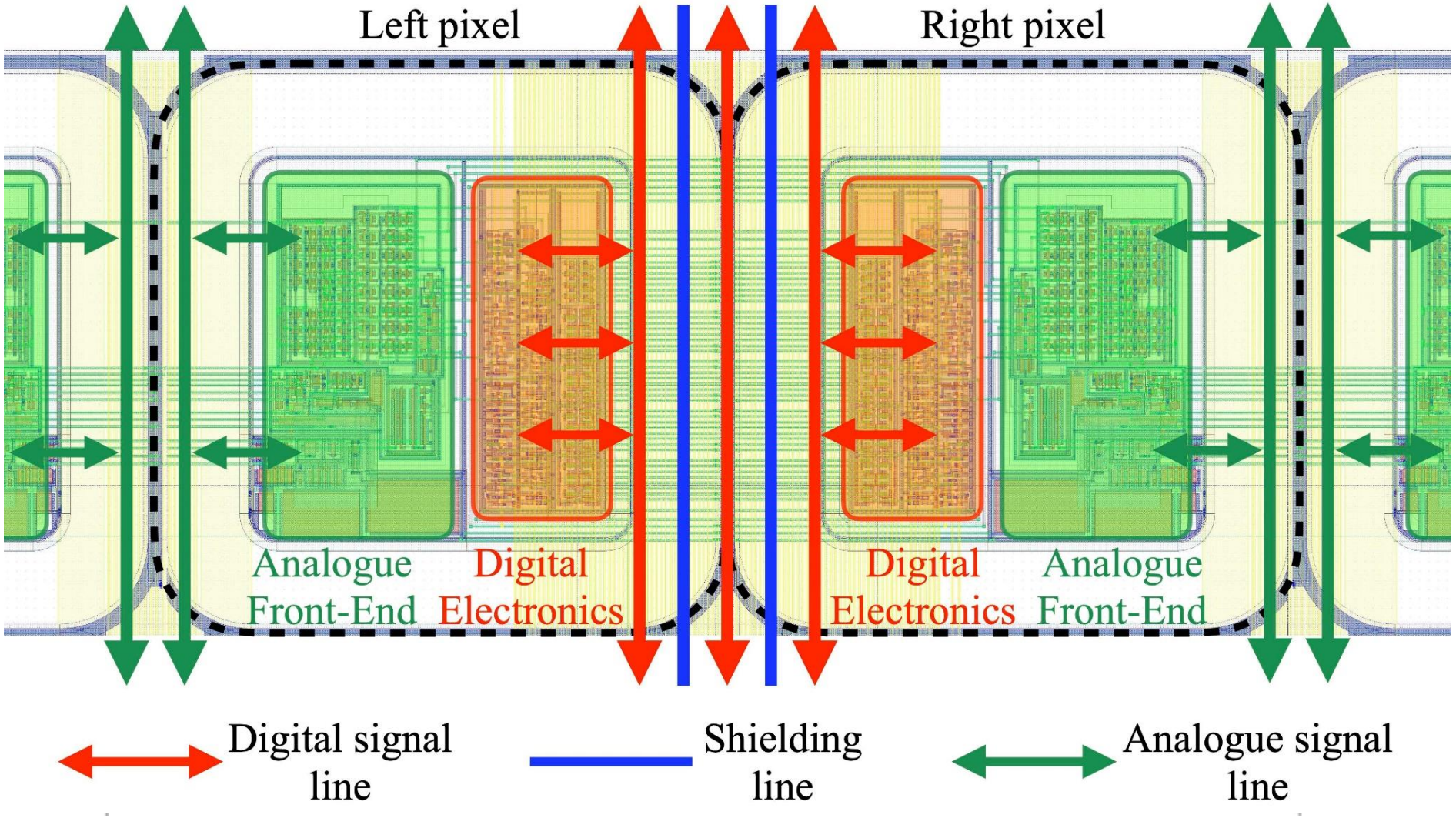
Analogue readout

Digital readout



- **Column drain architecture (FE-I3 style)**
- **Electronics to**
  - Mask noisy pixels (MASK)
  - Possibility to pause digitisation of new hits until readout is complete (FREEZE)
  - 8-bit SRAM shift register for serial configuration
    - Pixel-trimming to compensate for threshold voltage variations (4-bits)
    - Flag to mask noisy pixels (1-bit)
    - Signals to enable/disable calibration circuit (1-bit), SFOUT (1-bit), COMPOUT (1-bit)

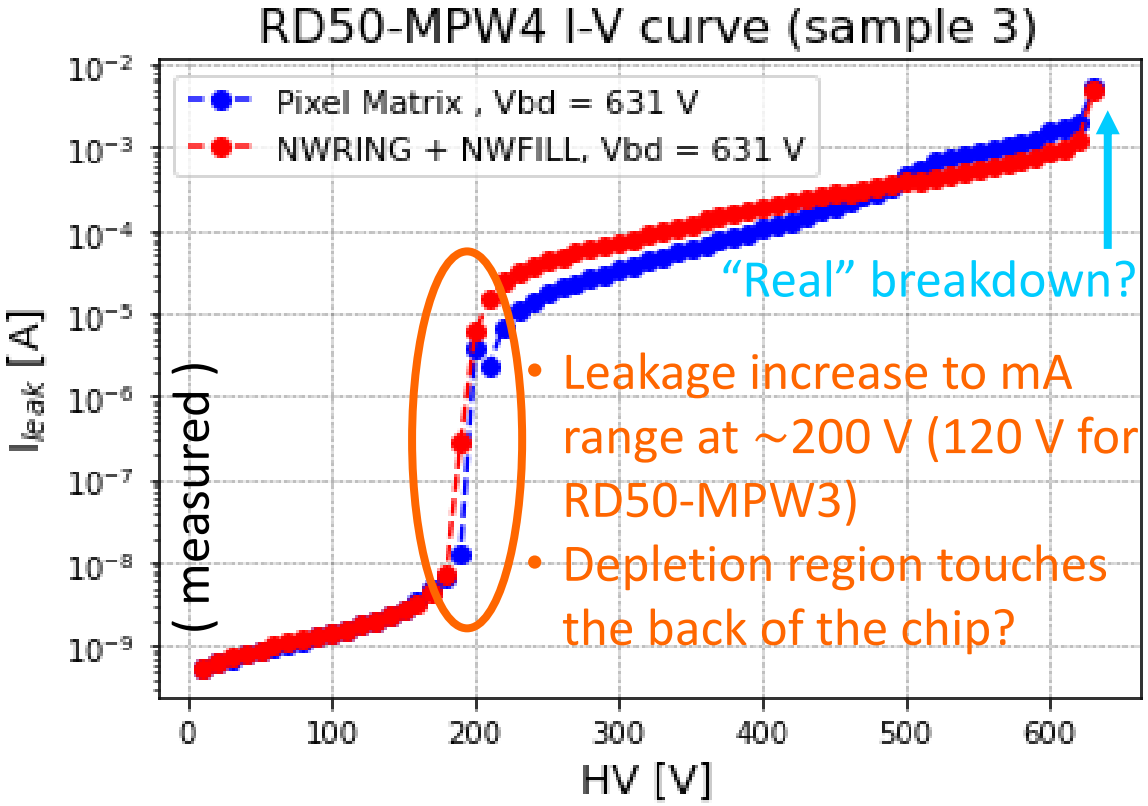
Pixel layout

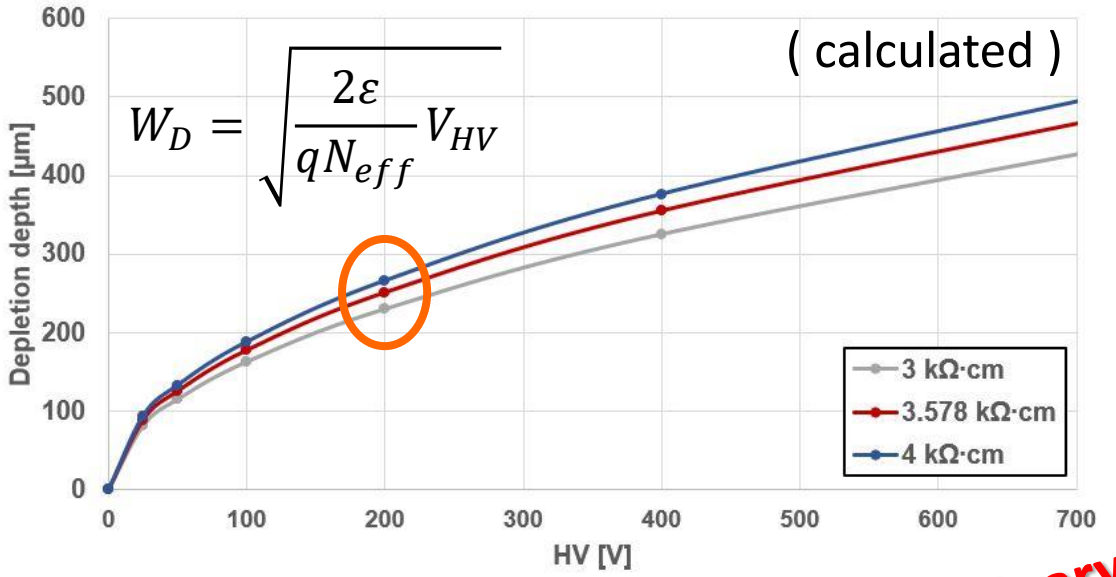


Double column scheme to alleviate routing congestion and minimise crosstalk

RD50-MPW4 – I-V measurements, topside biased

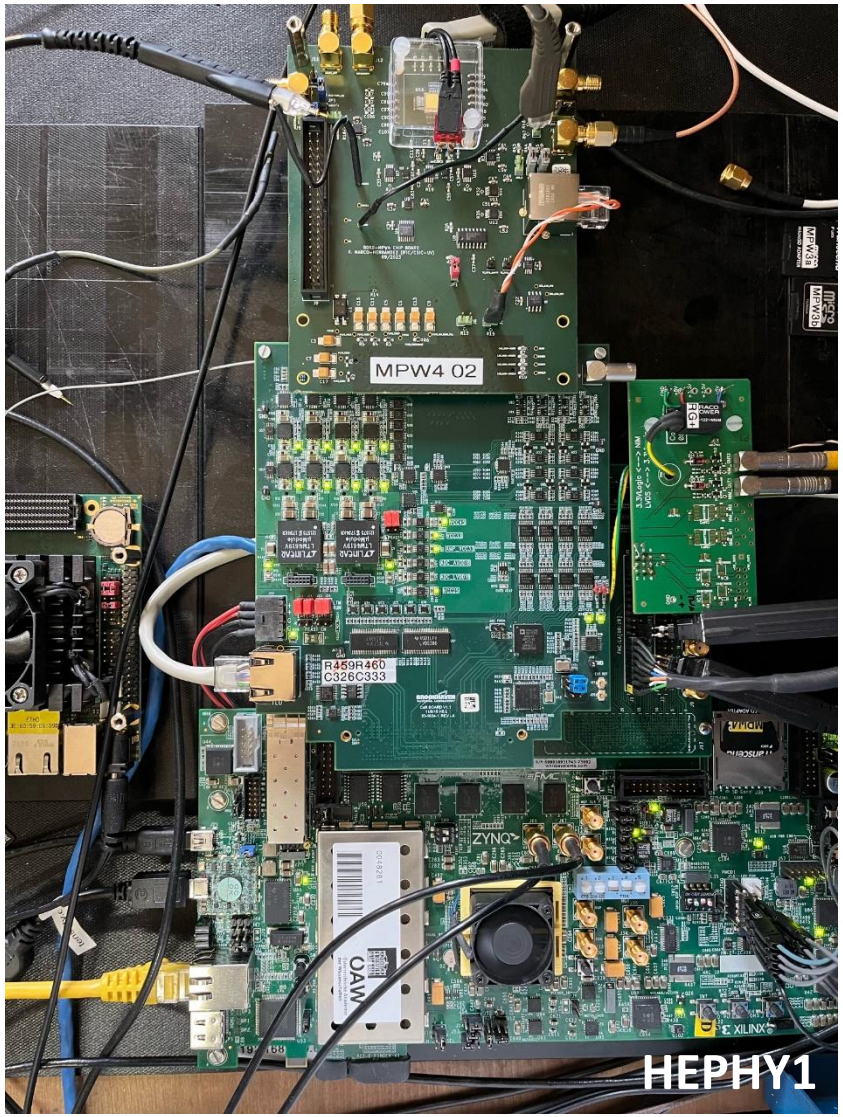
- **First set of samples without backside processing were received first (W8)**
  - Substrate biased to high voltage from top side
  - Thinned to 280 µm
  - Probe station with needles, in darkness and at room T

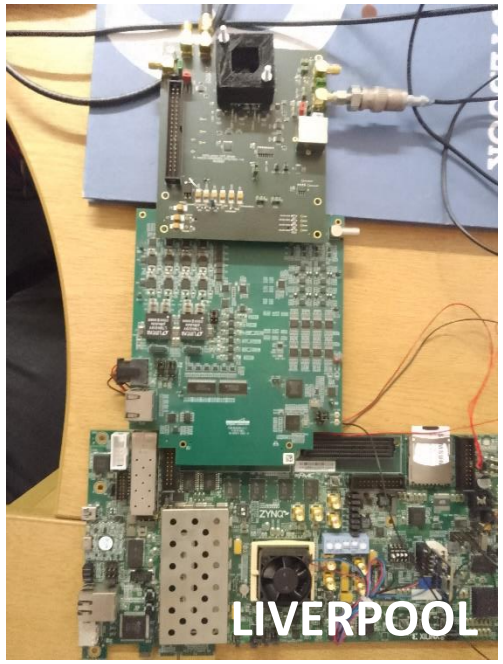


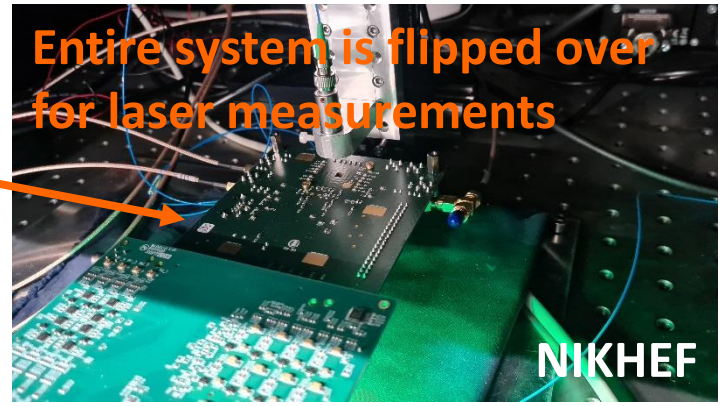


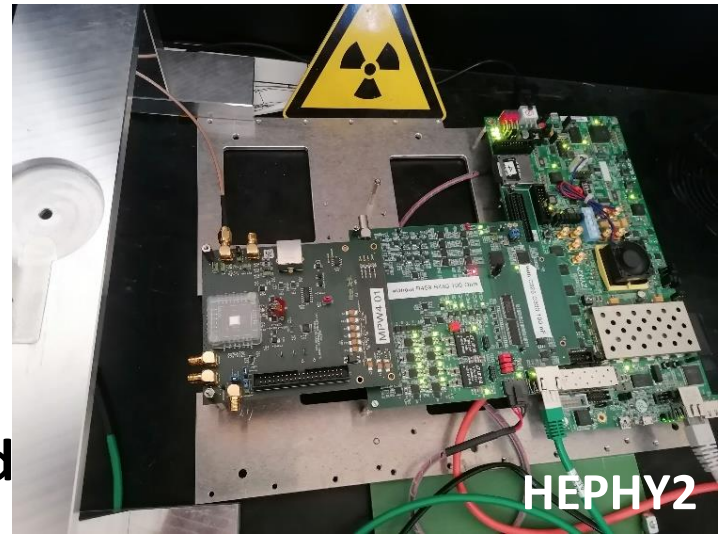
Preliminary

RD50-MPW4 – DAQ based on Caribou







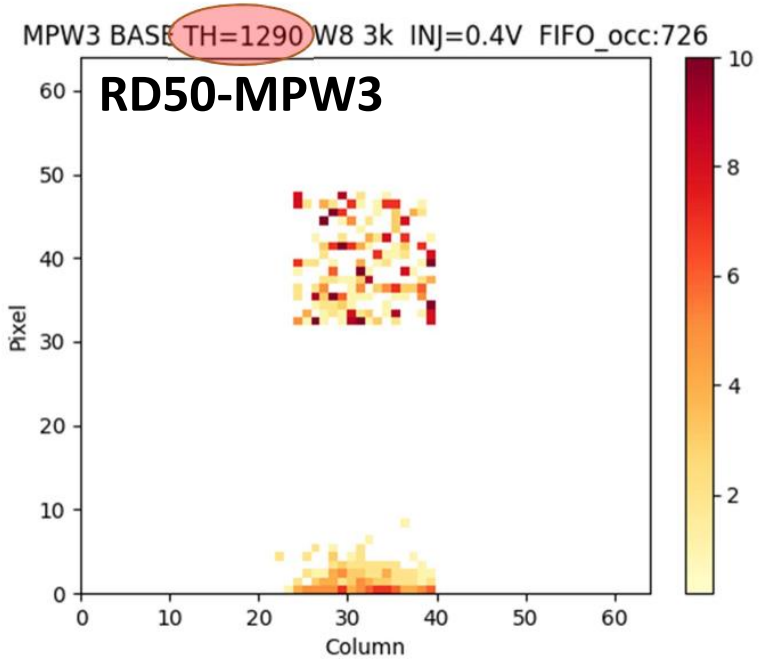


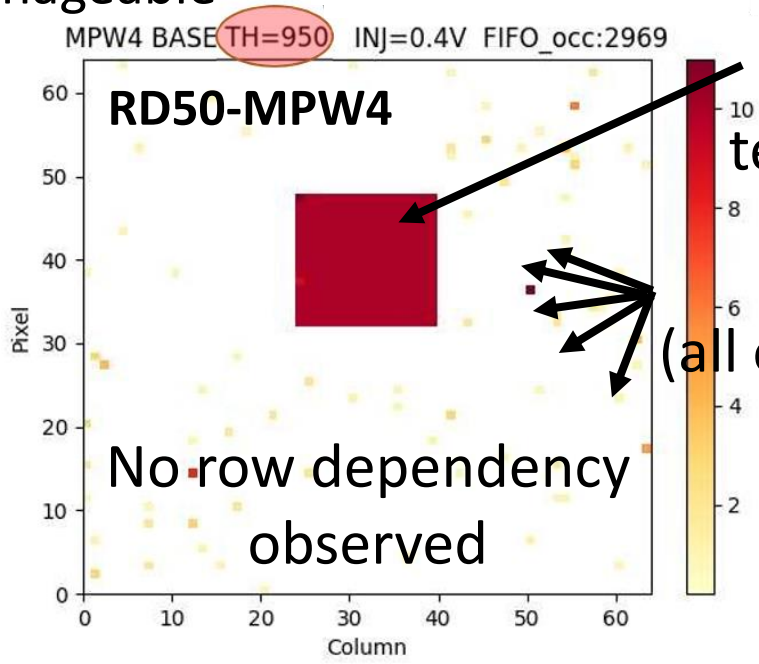
- **Xilinx Zynq-7000 SoC board**
  - ZC706 (ZC702 possible too)
- **Control and Readout (CaR) board**
  - Provides common services
- **Custom chip board**
  - Provides chip specific features

(and more sites
currently getting ready)

RD50-MPW4 – Qualitative noise studies

- **RD50-MPW3** – Reminder: Noise started at approximately V_TH = 350 mV
- **RD50-MPW4**
  - Measurements done with full matrix enabled, readout for 10 secs
  - Pixels not calibrated (VPTRIM = 0x24 and trimDAC set to 7 for all pixels)
  - V_TH = 60 mV → few noisy pixels start firing (rest of matrix still calm)
  - V_TH = 30 mV → noise is still manageable



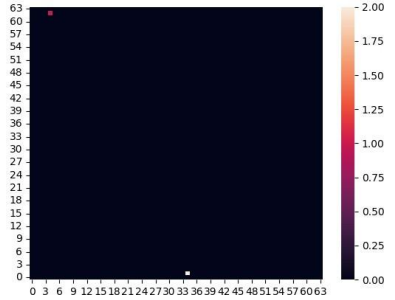


Injected test pulses

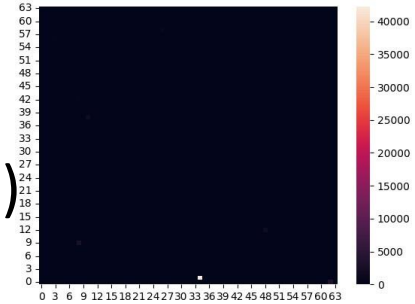
Noise (all other hits)

No row dependency observed

V_TH = 60 mV



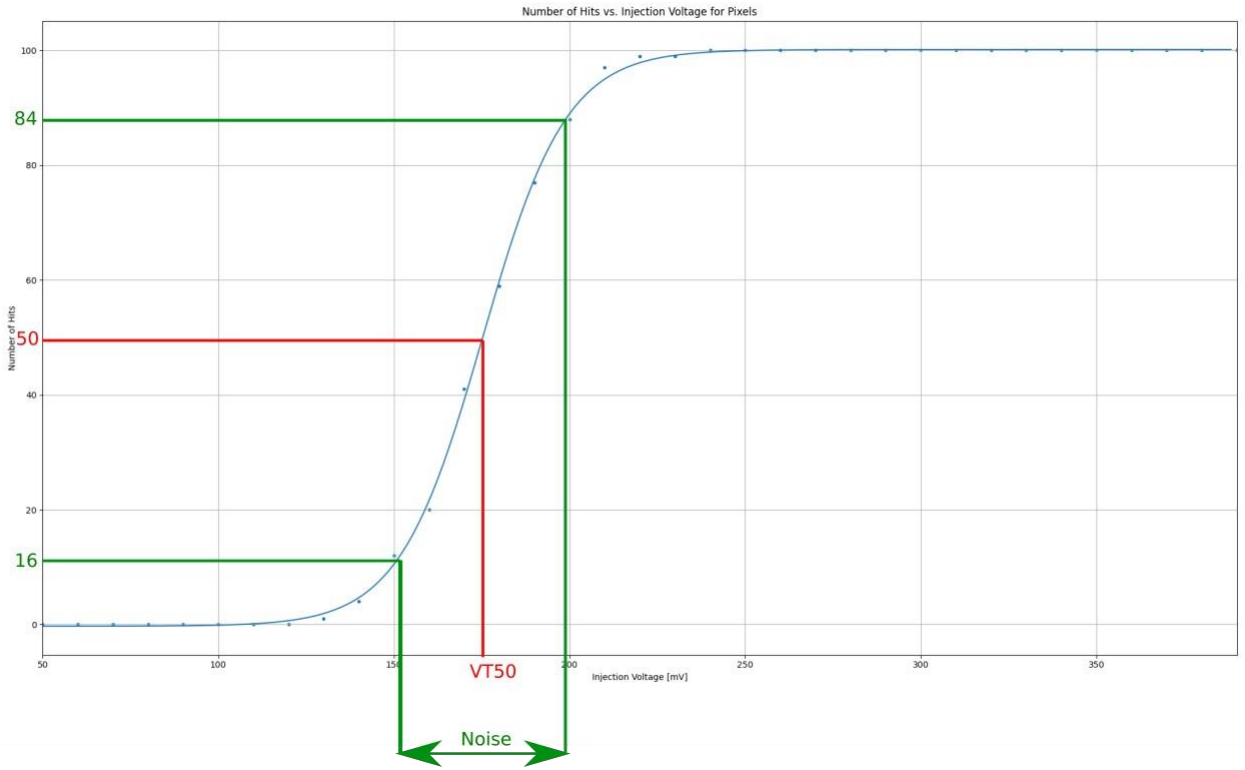
V_TH = 30 mV



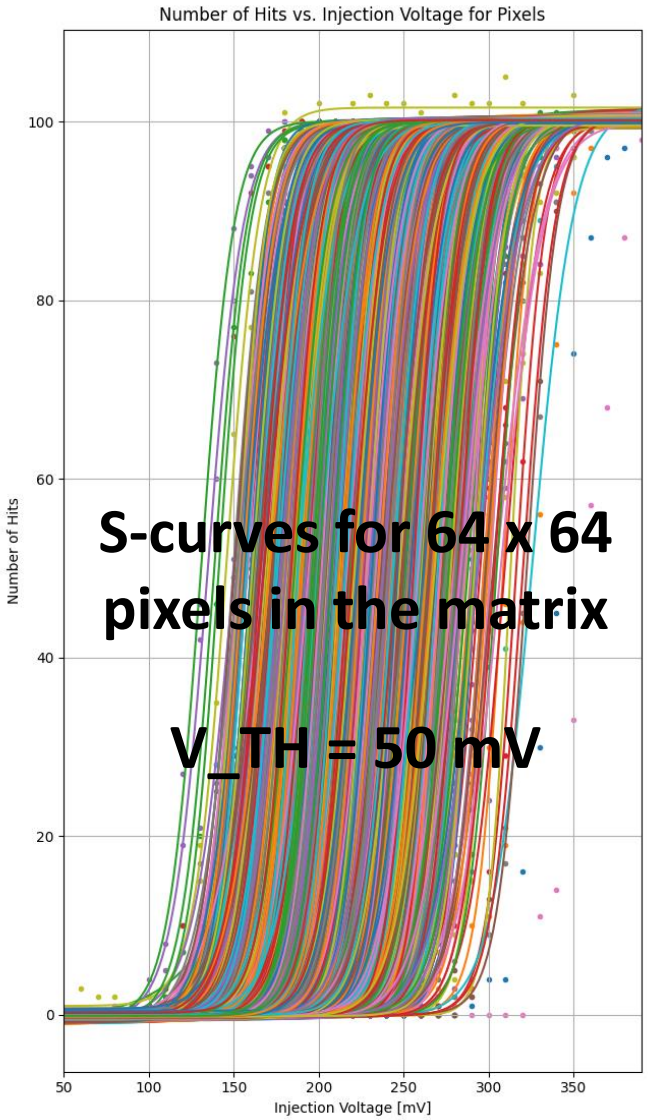
Preliminary

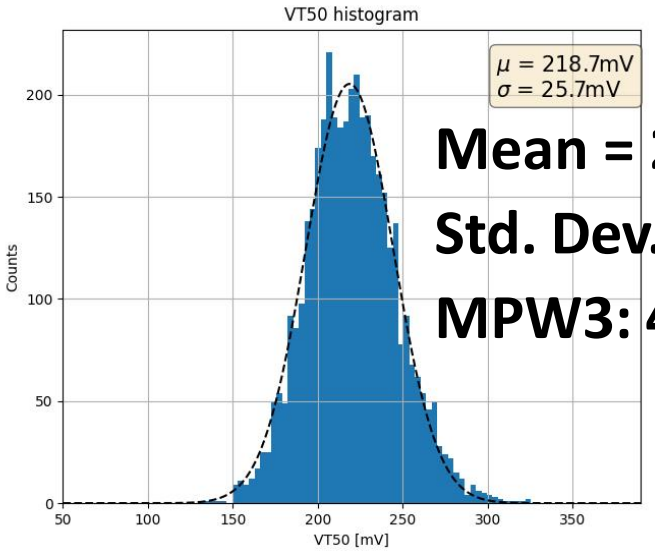
S-curves measurements

- **Method**
  - Scan injection voltage in 5 mV steps
  - 100 injections per step
  - Fit data (to “logistic function”)
    - yFit(x)
  - From yFit(x) = 50
    - evaluate x … VT50
  - From yFit(x1) = 16, yFit(x2) = 84
    - Noise = x2 - x1
  - For conversion from voltage to charge injection capacity of 2.8 fF used



RD50-MPW4 – Unbiased chip, uncalibrated pixels

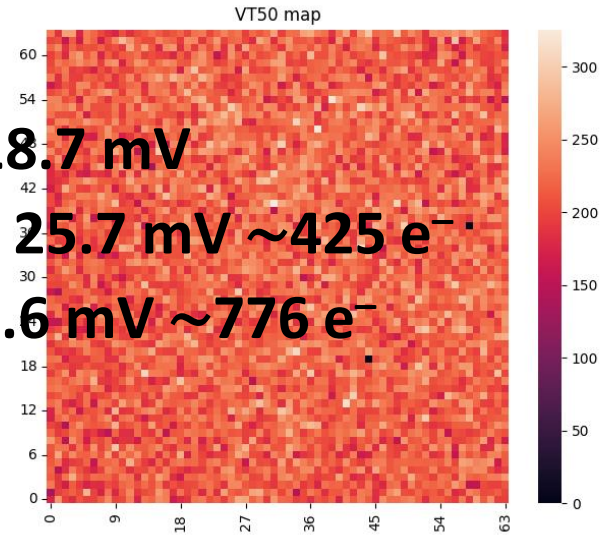


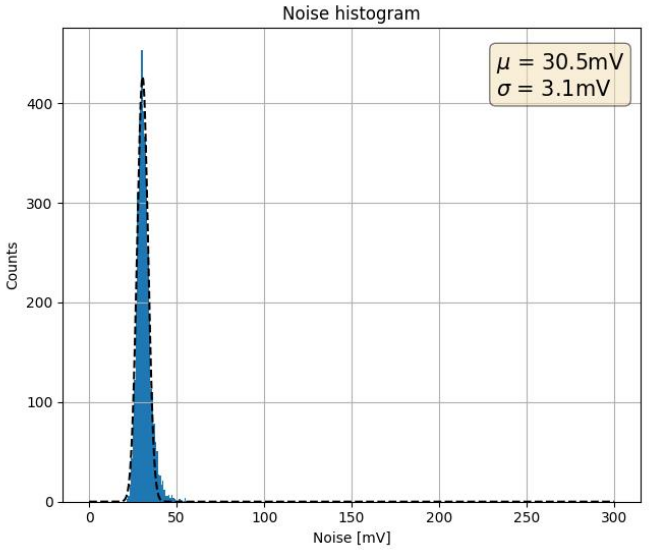


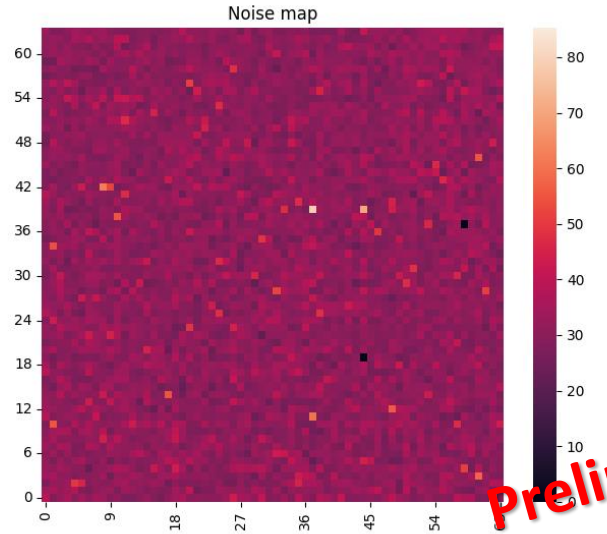
Mean = 218.7 mV

Std. Dev. = 25.7 mV ~425 e^-

MPW3: 45.6 mV ~776 e^-

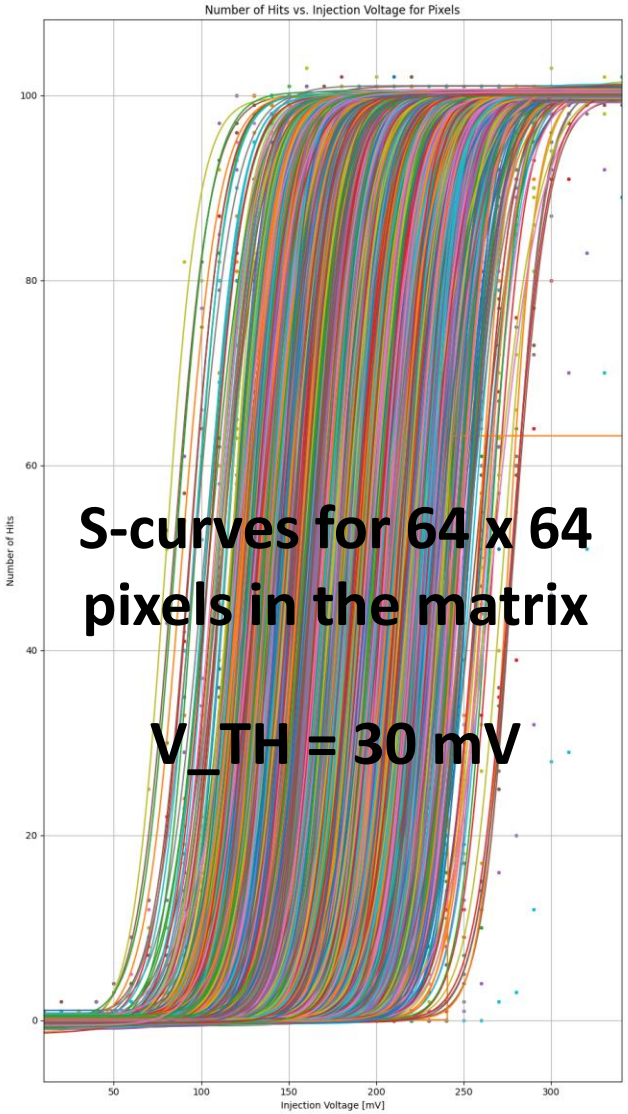






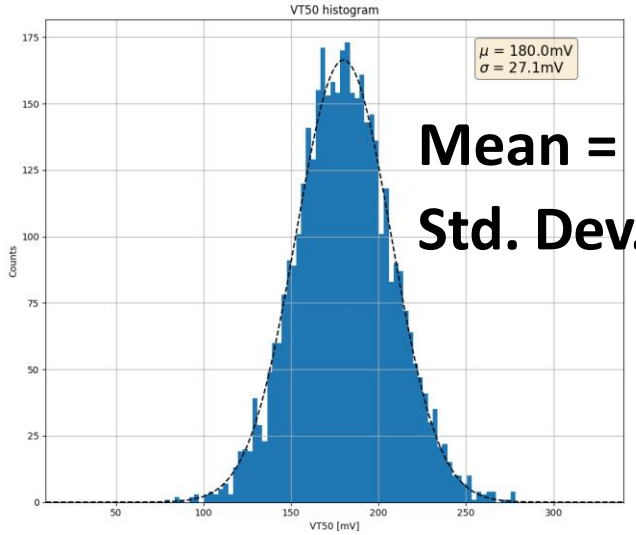
Preliminary

RD50-MPW4 – Biased chip @ 200 V, uncalibrated pixels



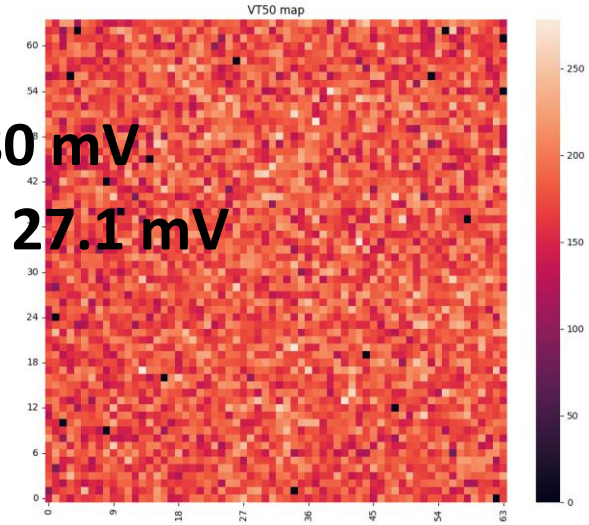
S-curves for 64 x 64 pixels in the matrix

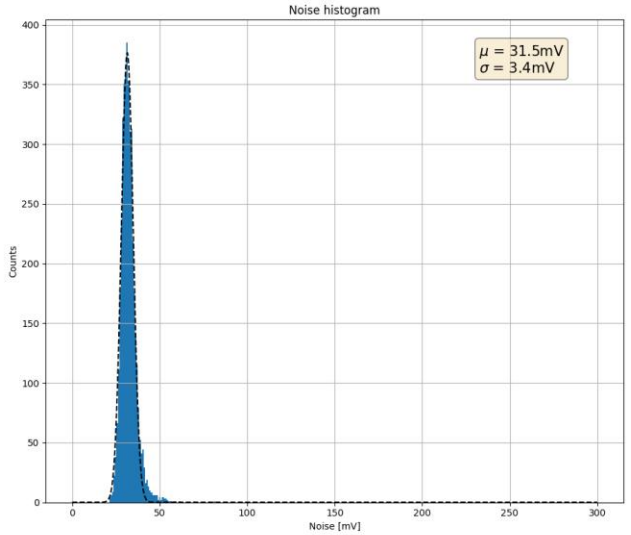
V_TH = 30 mV

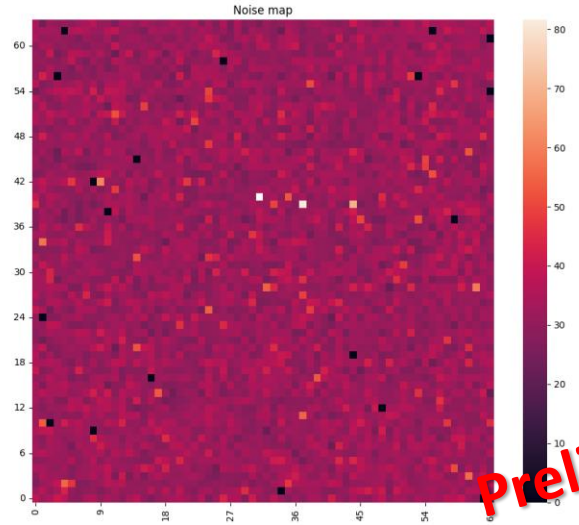


Mean = 180 mV

Std. Dev. = 27.1 mV

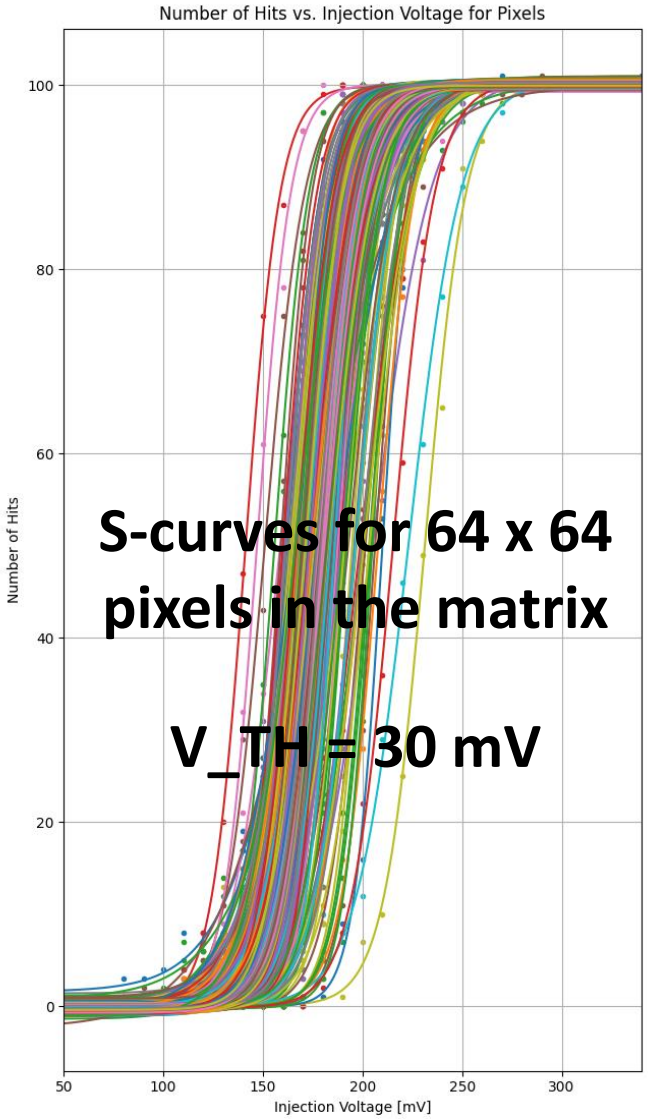






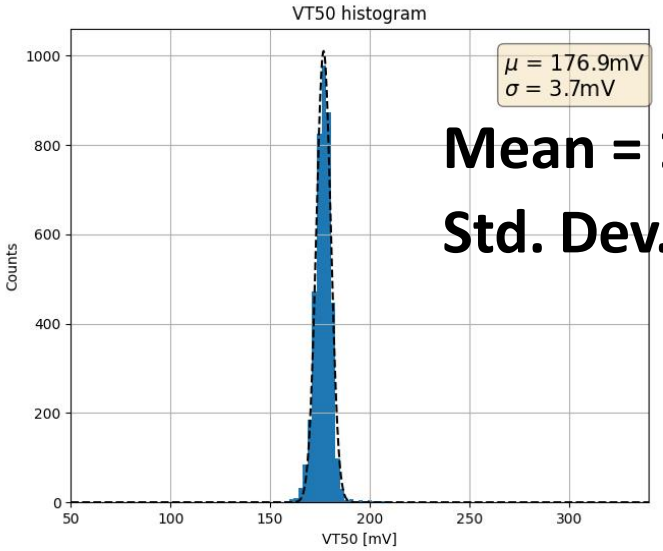
Preliminary

RD50-MPW4 – Biased chip @ 200 V, calibrated pixels



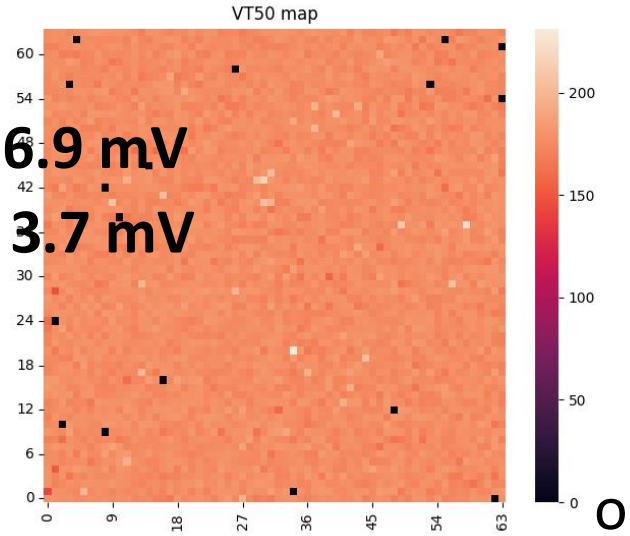
S-curves for 64 x 64 pixels in the matrix

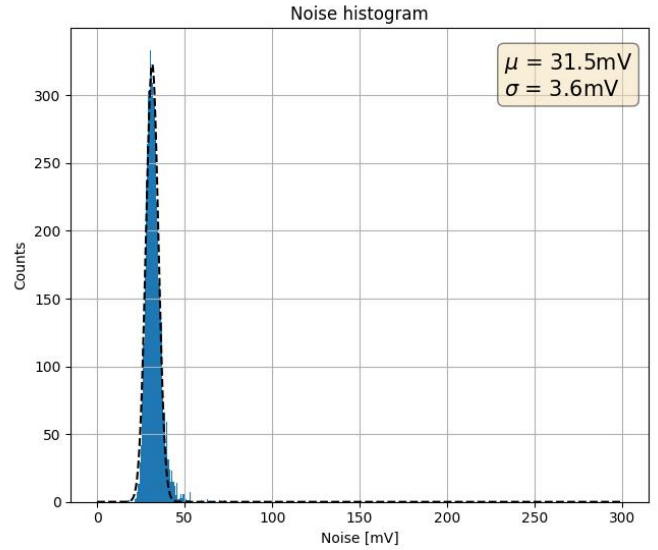
V_TH = 30 mV

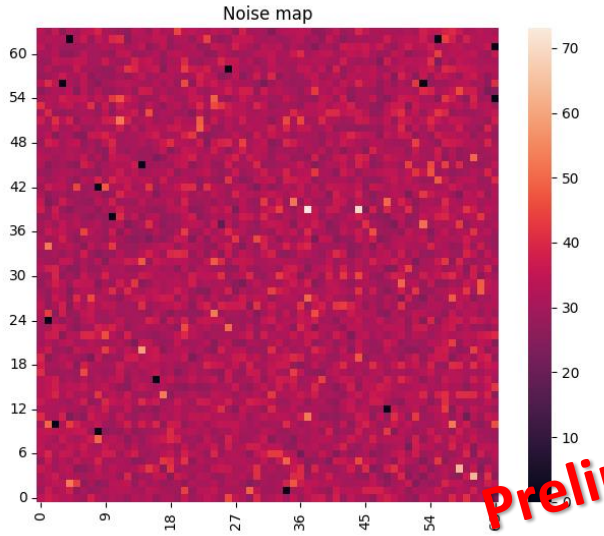


Mean = 176.9 mV

Std. Dev. = 3.7 mV







Non-optimised DAC settings

Preliminary

RD50-MPW4 – Evaluation plan

- **Laboratory measurements**
  - **I-V measurements**
    - Study V_BD, I_LEAK and their dependence with temperature
  - **Edge TCT measurements**
    - Study dependence of depletion depth with V_HV
  - **Active pixel matrix**
    - Identify optimised DAC settings for matrix bias block
    - Trade-off between pixel performance and power consumption
    - Pixels calibration and parameter extraction (gain, noise)
    - Charge collection efficiency
- **Test beam @ DESY in April (TB22)**
- **Irradiation campaign**
  - NIEL → N-fluence: 1E14, 3E14, 1E15, 3E15, 1E16, 3E16 n_{eq}/cm^2
  - TID → Evaluate pixel performance up to meaningful dose
- **Evaluate unirradiated and irradiated samples, topside and backside biased samples**

Summary

- RD50-MPW4 is a HV-CMOS pixel chip designed to have lower noise and high radiation tolerance achieved through high V_BD and backside biasing.
- The chip has been fabricated and delivered.
- The preliminary measurements suggest that the chip works according to design specifications.
- Evaluation plan will progress in the coming months.
- Irradiation campaign and test beam have been booked.

Acknowledgements

- This work has been partly performed in the framework of the CERN-RD50 collaboration.
- It has received funding from the European Union's Horizon 2020 Research and Innovation programme under grant agreement 101004761 (AIDAinnova).

Back up slides

RD50-MPWx chip series – Overview

Parameter	RD50-MPW1	RD50-MPW2	RD50-MPW3	RD50-MPW4
Device size [mm x mm]	5 x 5[(1)]	3.2 x 2.1	5.1 x 6.6	5.4 x 6.3
Pixel matrix size	40 x 78	8 x 8	64 x 64	64 x 64
Pixel size [µm x µm]	50 x 50	60 x 60	62 x 62	62 x 62
P-n spacing [µm]	3	8	8	8
In-pixel electronics	Analogue Digital	Analogue	Analogue Digital	Analogue Digital
Output data	Pixel address Time-stamp	Binary	Pixel address Time-stamp	Pixel address Time-stamp
Digital periphery	78 EOCs 2 LVDs lines	8 EOCs	32 EOCs, with 32-events 24-bit FIFOs 128-events 32-bit TX FIFOs I2C Wishbone bus 1 LVDs line	32 EOCs, with 16-events 24-bit FIFOs 64-events 32-bit TX FIFOs I2C Wishbone bus 1 LVDs line

[(1)]Half of the chip has a pixel matrix for applications beyond physics

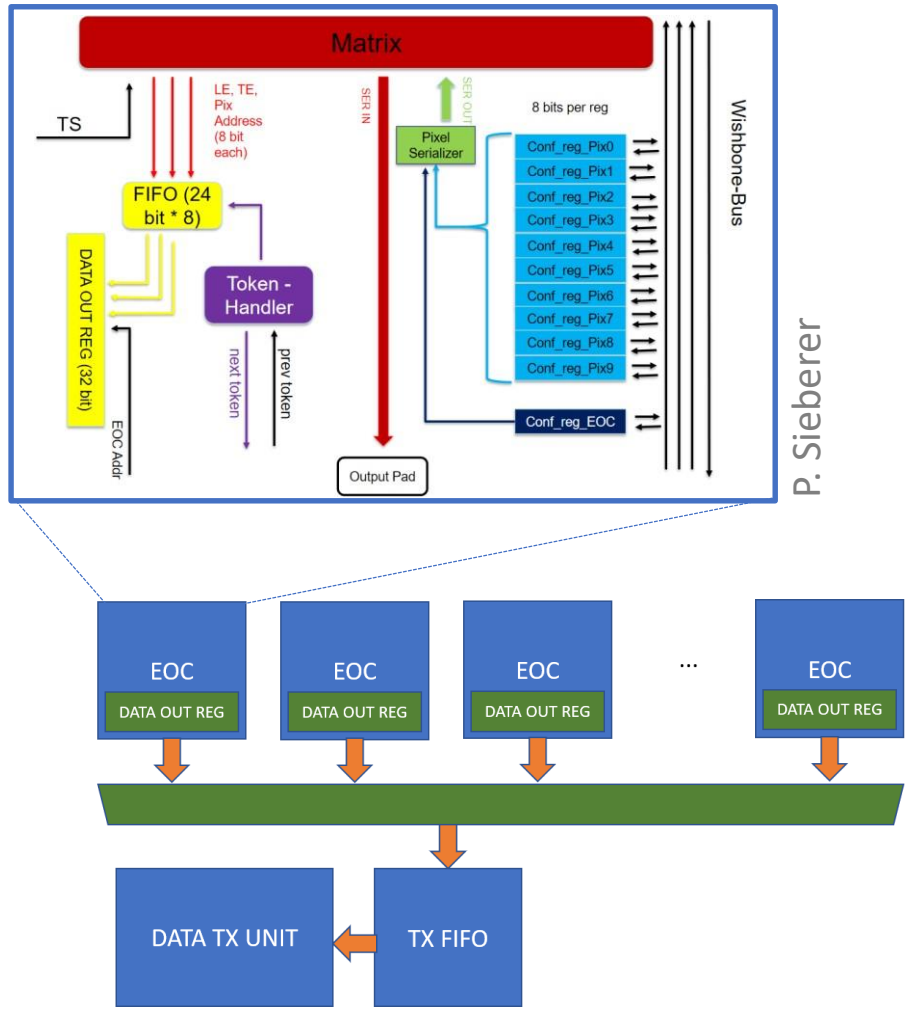
RD50-MPWx chip series – Overview

Parameter	RD50-MPW1	RD50-MPW2	RD50-MPW3	RD50-MPW4
Chip guard ring frame	None	1 n-ring 6 p-rings	1 n-ring 6 p-rings	1 n-ring 5 n-/p-rings
Substrate biasing	Through p-stop contacts	Through p-stop contacts	Through p-stop contacts	Through chip edge or backside
Substrate resistivity [kΩ·cm]	0.5 – 1.1 1.9	Standard 0.2 – 0.5 1.9 3	Standard 1.9 3	Standard 3
Device thickness [µm]	280	280	280	280
V_{BD} [V]	56	120	120	500[(2)]
I_{LEAK} [µA/pixel]	1	1E-4	1E-6	1E-6[(2)]
Depletion depth [µm]	118	110	Not tested	Fully depleted[(2)]
ENC [mV]	50	2	< 140, > 50	50[(2)]
Efficiency [%]	Not tested	Not tested	> 98	> 99[(2)]

[(2)]Anticipated values for RD50-MPW4

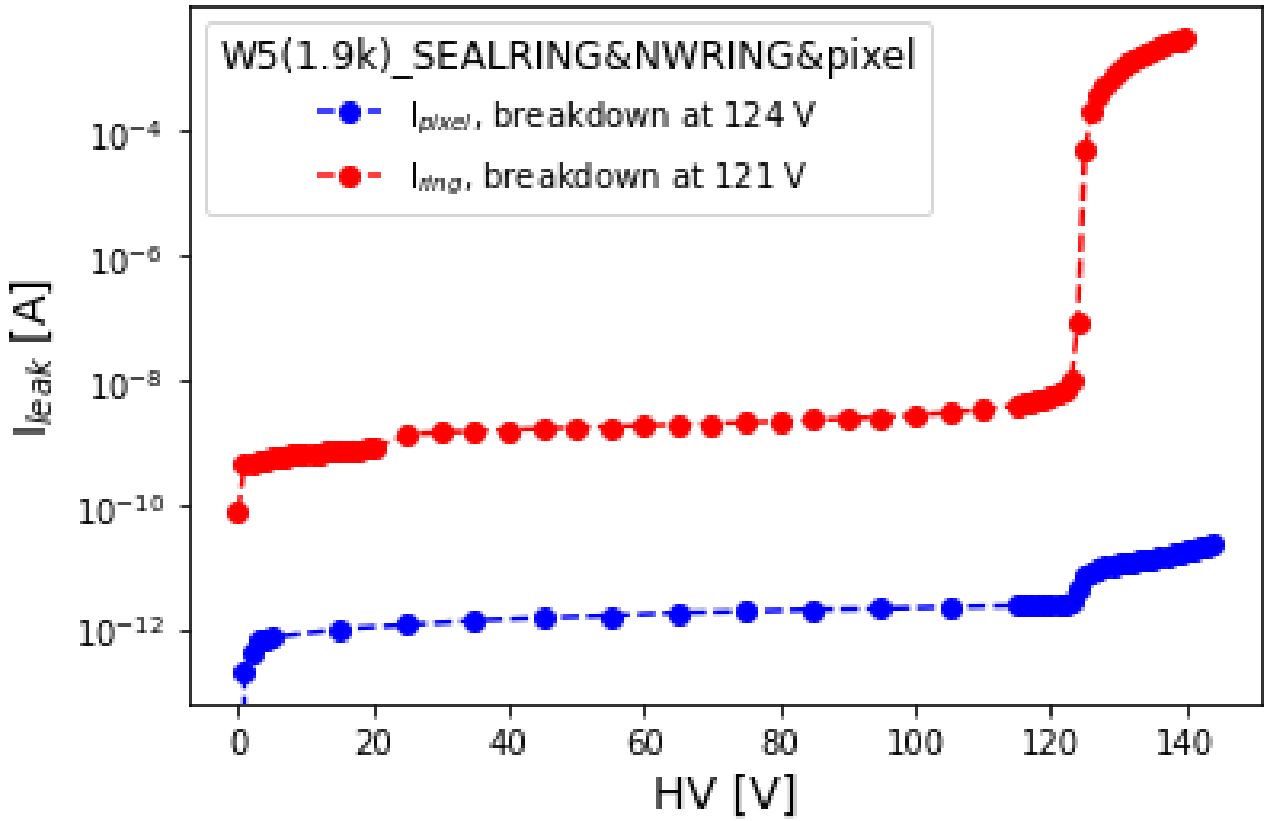
Digital periphery

- **End-Of-Column (EOC) architecture**
  - FIFO stores hit data (LE TS, TE TS and ADDR)
  - FSM reads double column
  - Token mechanism to determine which EOC is read out
- **Readout**
  - Pixel is read out immediately after hit (if FIFO is not full)
  - CU reads EOCs sequentially
  - Data stored temporarily in TX FIFO
  - Data TX unit with LVDS port @ 640 Mbps
- **Slow control**
  - Based on I2C protocol for external communication using internal Wishbone bus

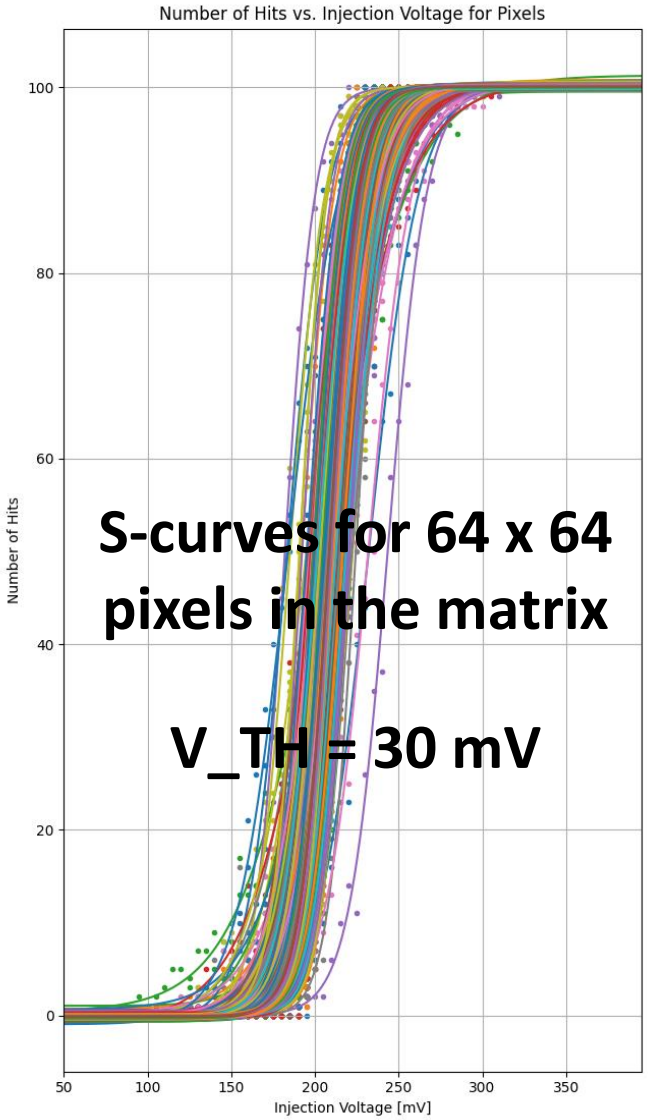


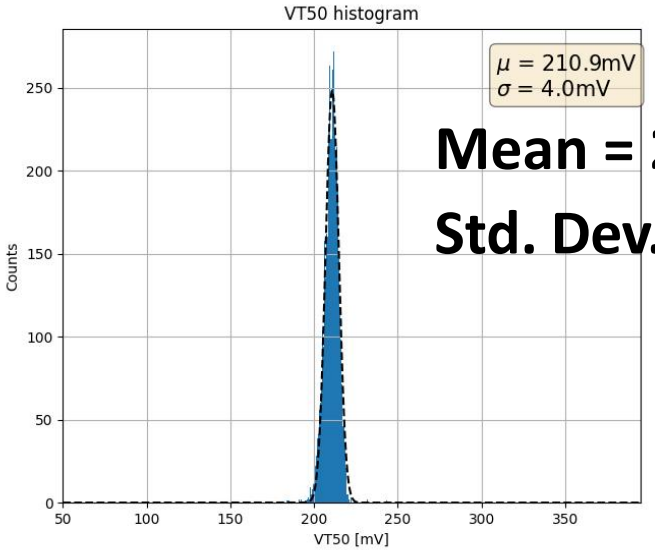
RD50-MPW3 – I-V measurements

- Measurement using probe station with needles
- V_BD > 120 V (V_BD > 300 V in RD50-MPW4)
- I_LEAK per pixel in pA range before breakdown



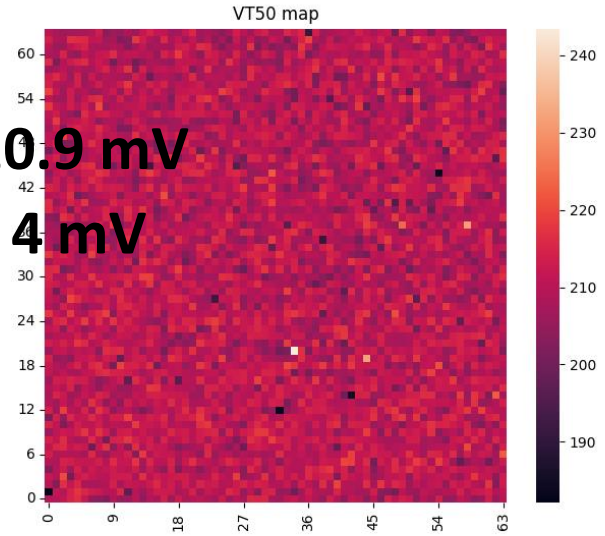
RD50-MPW4 – Unbiased chip, calibrated pixels

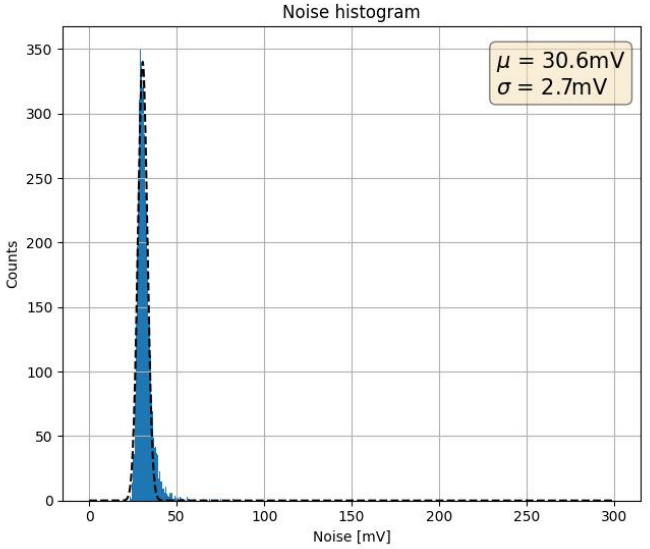


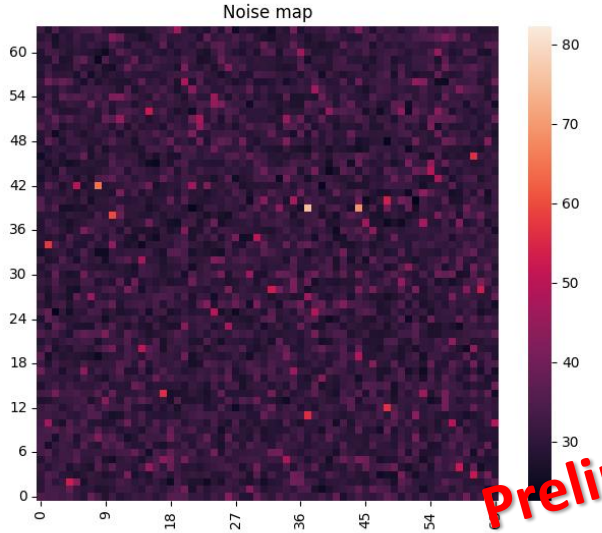


Mean = 210.9 mV

Std. Dev. = 4 mV







Preliminary