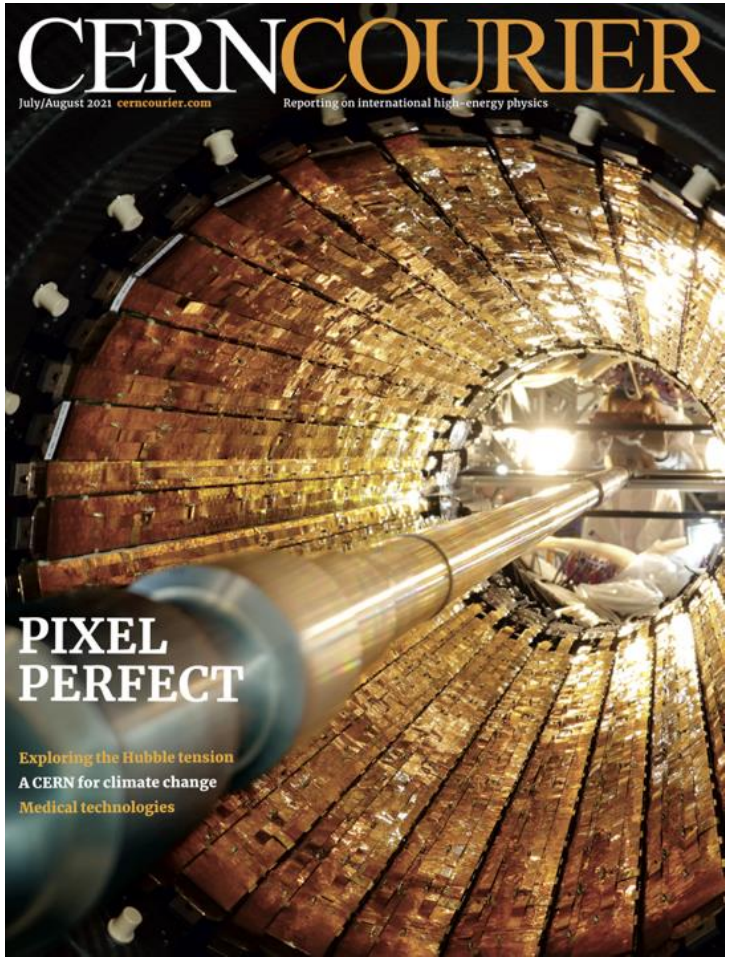
New trends in Monolithic Active Pixel Detectors

Stefania Maria Beolé

MAPS detectors state of the art



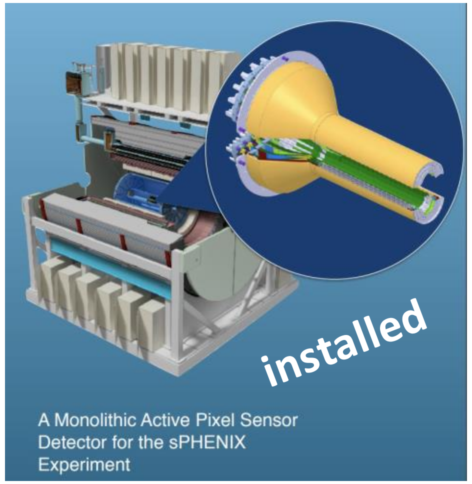
With permission. Article online

Adopted or considered for other experiments: **HADES, CBM, PANDA, NUSTAR, NA61, CSES2-Limadou, iMPACT, COMPASS++/AMBER, pCT, ePIC…**

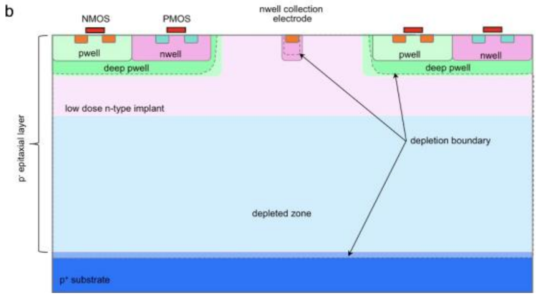
ALPIDE: Tower Semiconductor 180nm CMOS Imaging Sensor (CIS) Process

- R&D effort within the ALICE collaboration
  - excellent collaboration with foundry
  - more than 70k chips produced and tested
  - ALICE ITS pioneers large area trackers built of MAPS (EIC, ALICE 3, FCC?)

- in parallel studies to optimise process to reach full depletion and improve time response and radiation hardness up to 10^{15} 1MeV/n_{eq} :
  - **More details:** NIM **A871** (2017) https://doi.org/10.1016/j.nima.2017.07.046
  - **Now being further pursued: MALTA, CLICpix, FastPix, …**



Detector replicas for new experiments **sPHENIX MVTX @RHIC**



Modified process

MAPS detectors state of the art (ALPIDE)

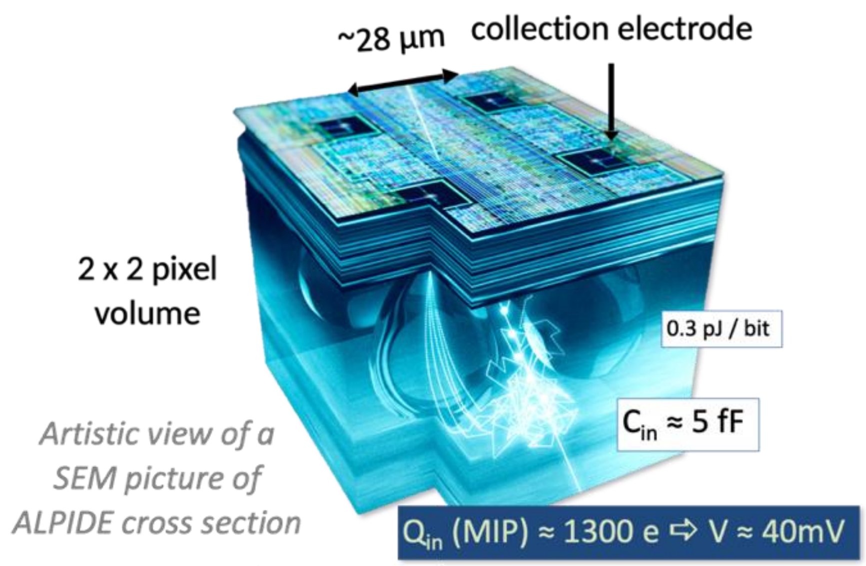
CMOS Pixel Sensor – Tower Semiconductor 180nm CMOS Imaging Sensor (CIS) Process

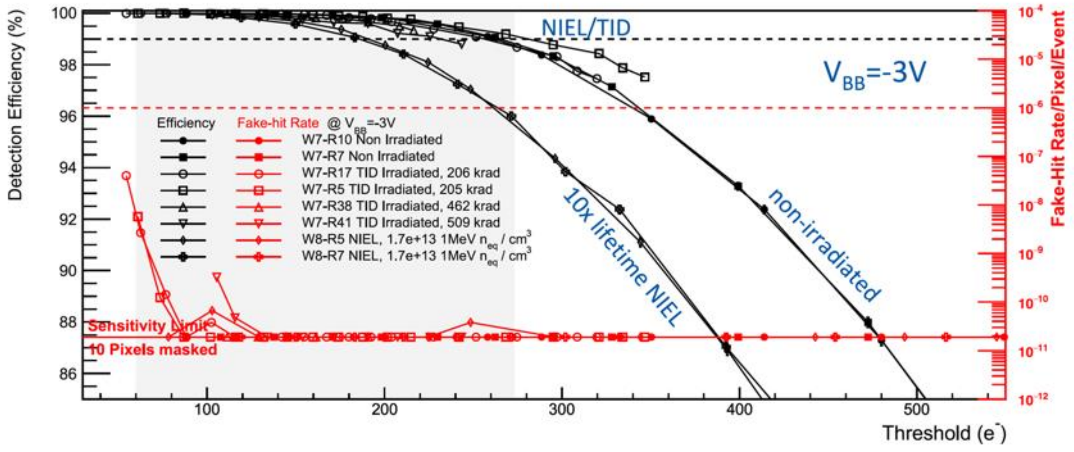
ALPIDE Key Features

- In-pixel: Amplification, Discrimination, multi event buffer
- **In-matrix zero suppression:** priority encoding
- **Ultra-low power < 47mW/cm^2 (< 140mW full chip)**
- **Detection efficiency > 99%**

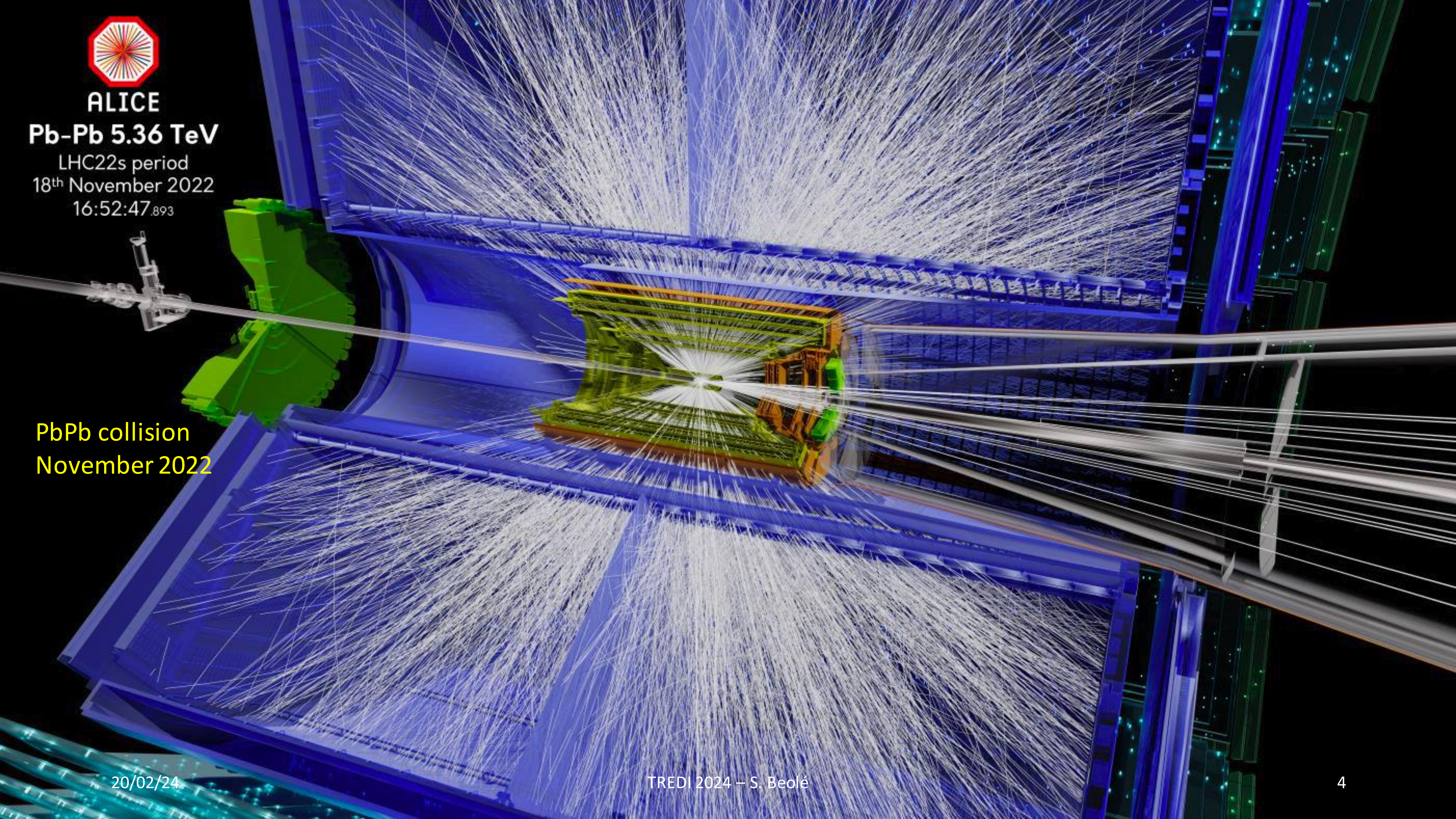
- **Spatial resolution ~5µm**
- Low fake-hit rate: << 10^{-6}/pixel/event (10^{-8}/pixel/event measured in data taking)
- Radiation tolerance: >270 krad (TID), > 1.7 10^{13} 1MeV/n_{eq} (NIEL)

Same chip used in ALICE2 for ITS and Muon Forward Tracker (MFT

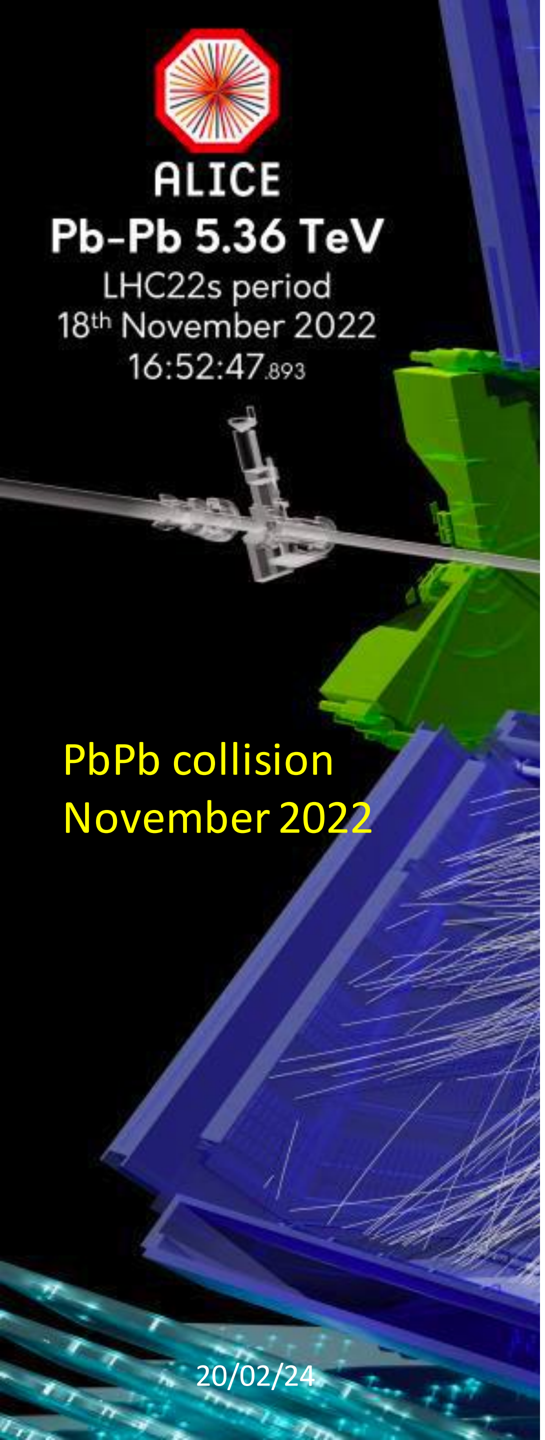




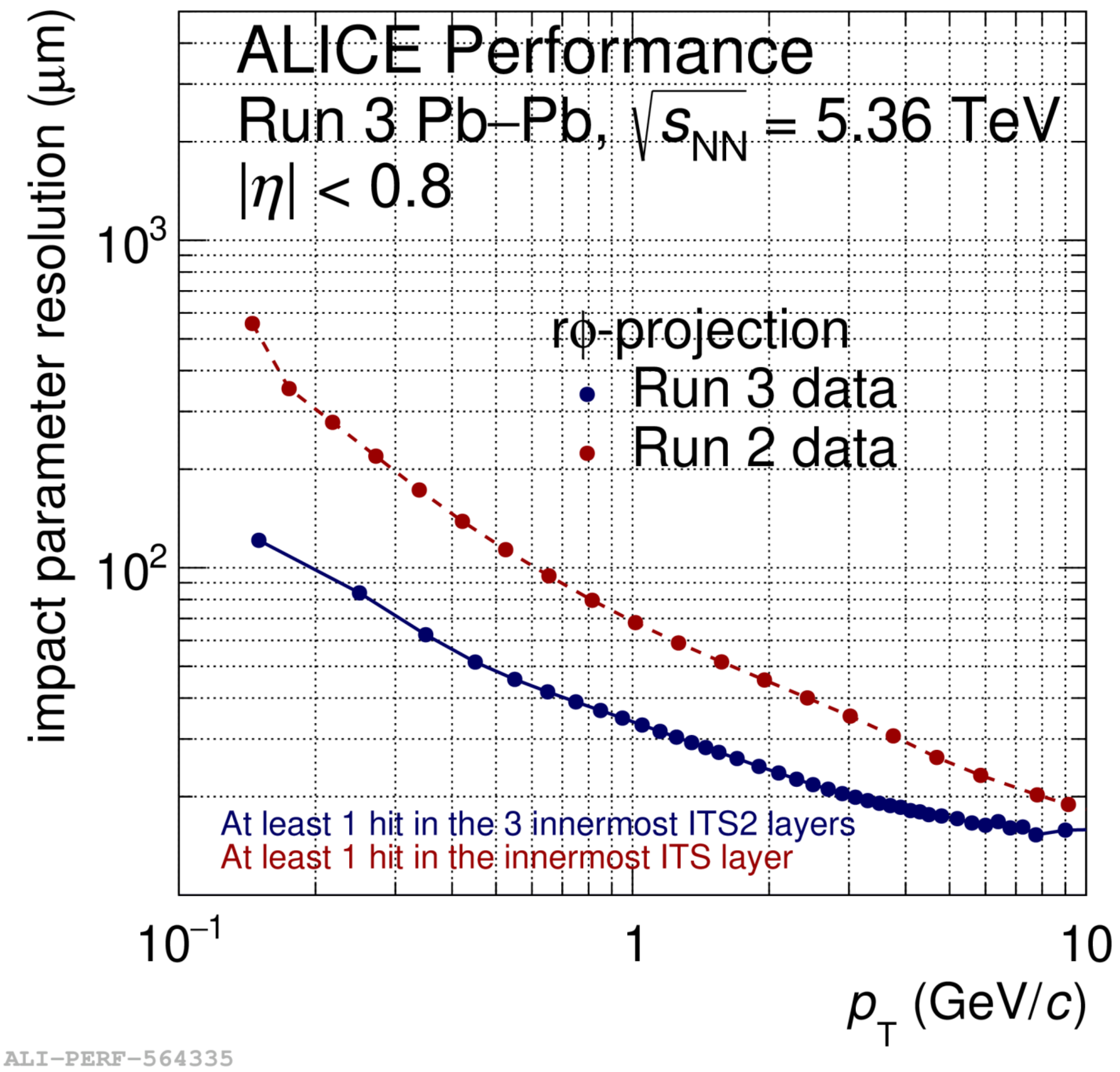
ALPIDE detection efficiency and fake hit rate

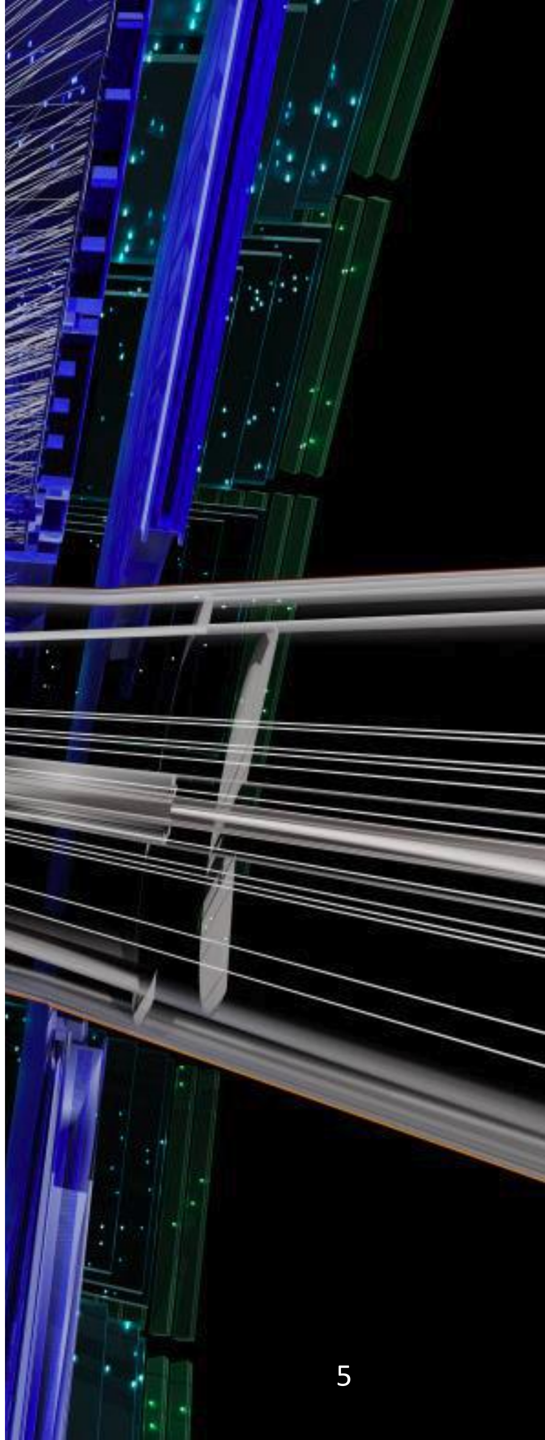


PbPb collision
November 2022



PbPb collision
November 2022

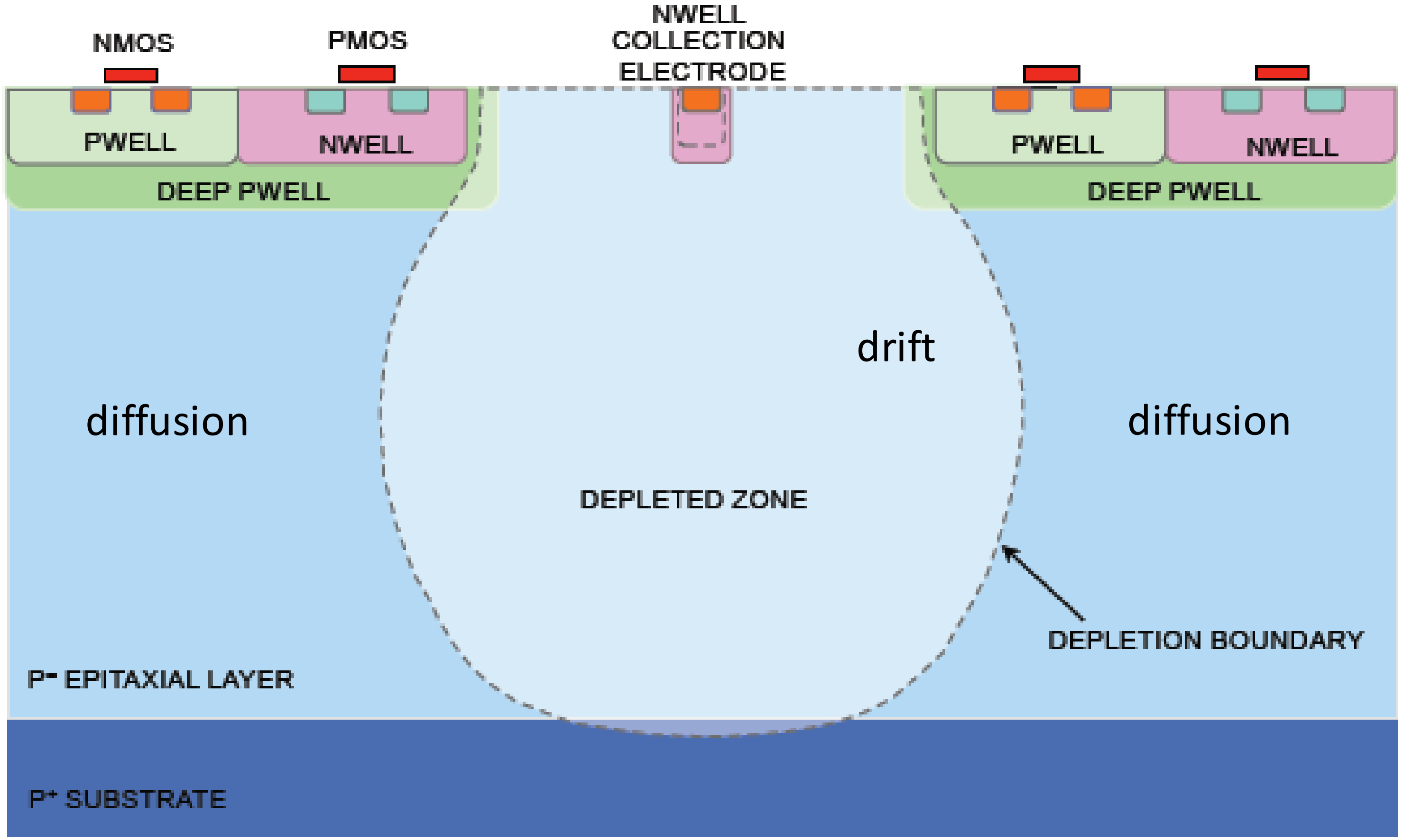




MAPS detectors state of the art

- Pro:
  - good spatial resolution
  - low material budget
  - low power consumption
  - fully efficient
- Limits:
  - Standard process: sensitive epitaxial layer not depleted -> slow response, integration time > 2μs
  - limited radiation hardness

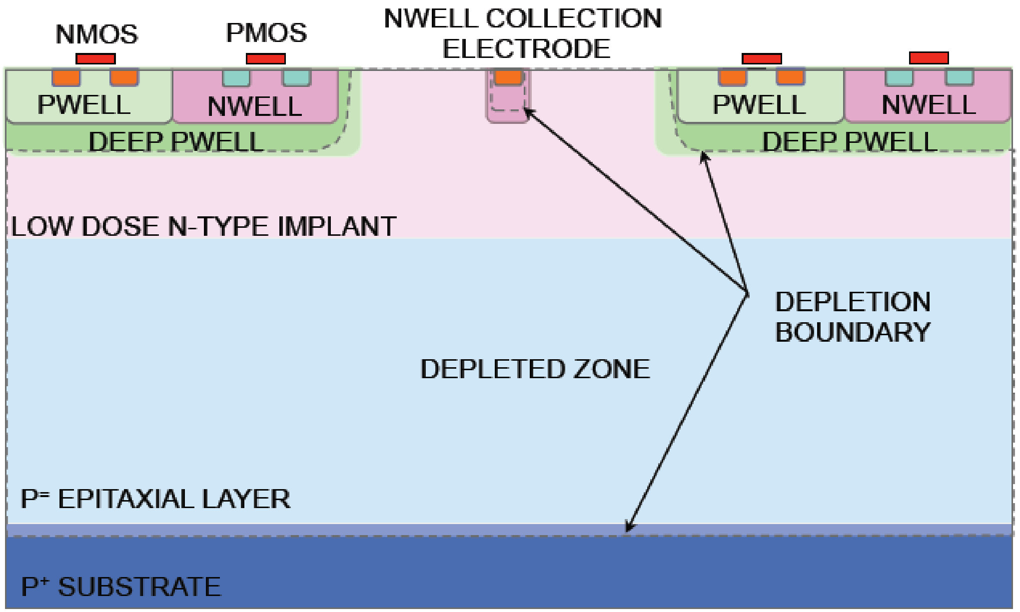
ALPIDE: Standard process: sensitive epitaxial layer not depleted



- Signal charge is collected from the non-depleted layer, diffusion dominated and prone to trapping after irradiation
- Deep well and substrate limit extension of the depletion:
  - to fix this -> pixel design/process modification, see next slide.

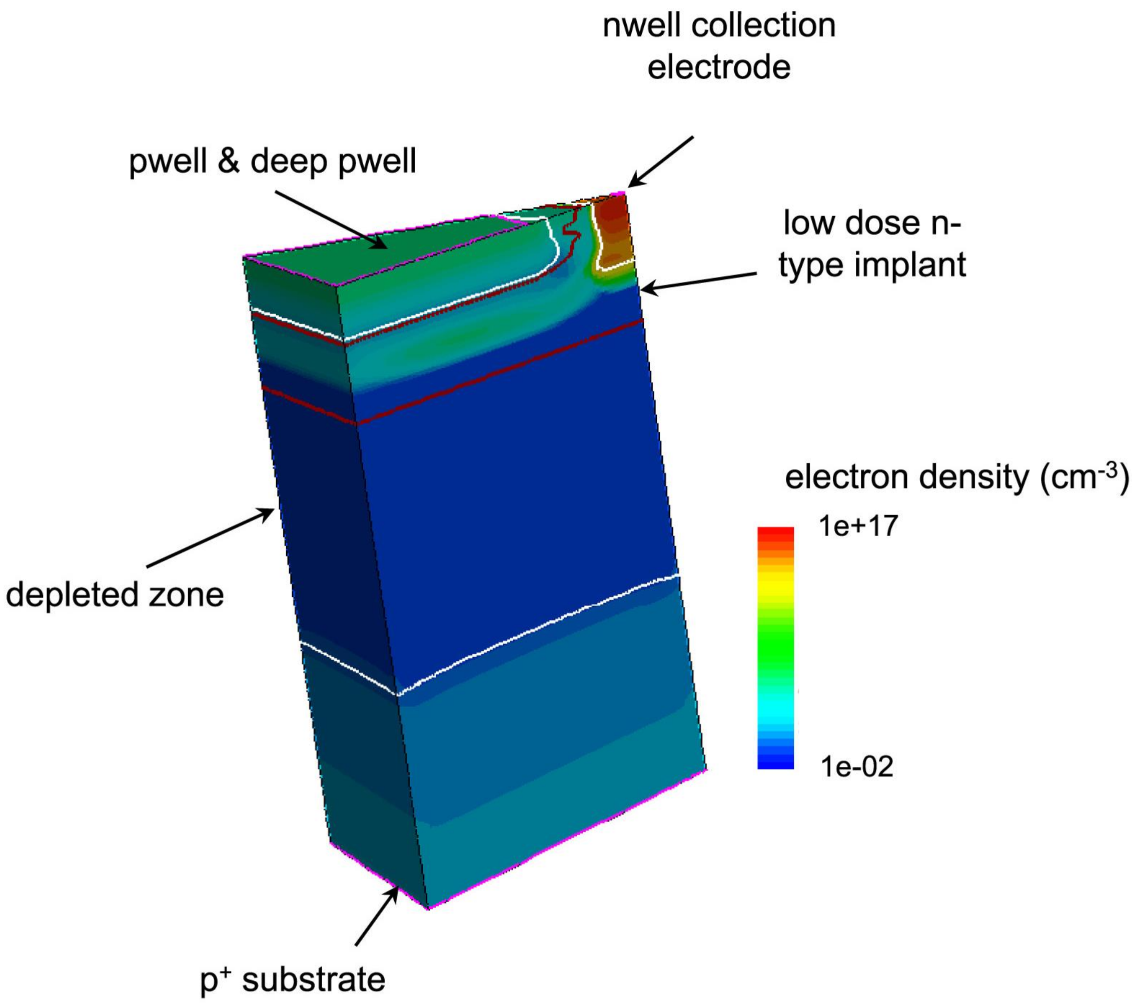
Tower Semiconductor 180nm

Sensor optimization (1): DEPLETED MAPS



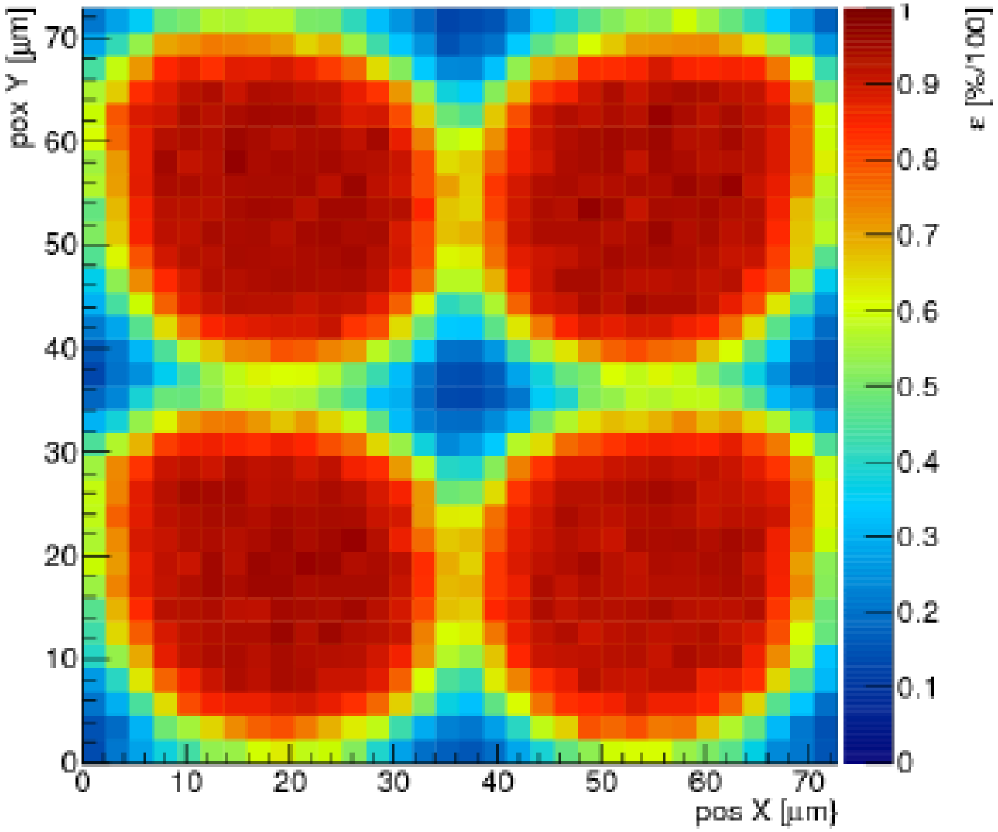
- GOAL: create planar junction using deep **low dose n-type implant** and deplete the epitaxial layer
- initial interest from ATLAS followed by many others: MALTA/TJ MONOPIX development (Bonn, CPPM, IRFU and CERN)

https://doi.org/10.1016/j.nima.2017.07.046 (180nm)



Tower Semiconductor 180nm

Sensor optimization (1): results on detection efficiency



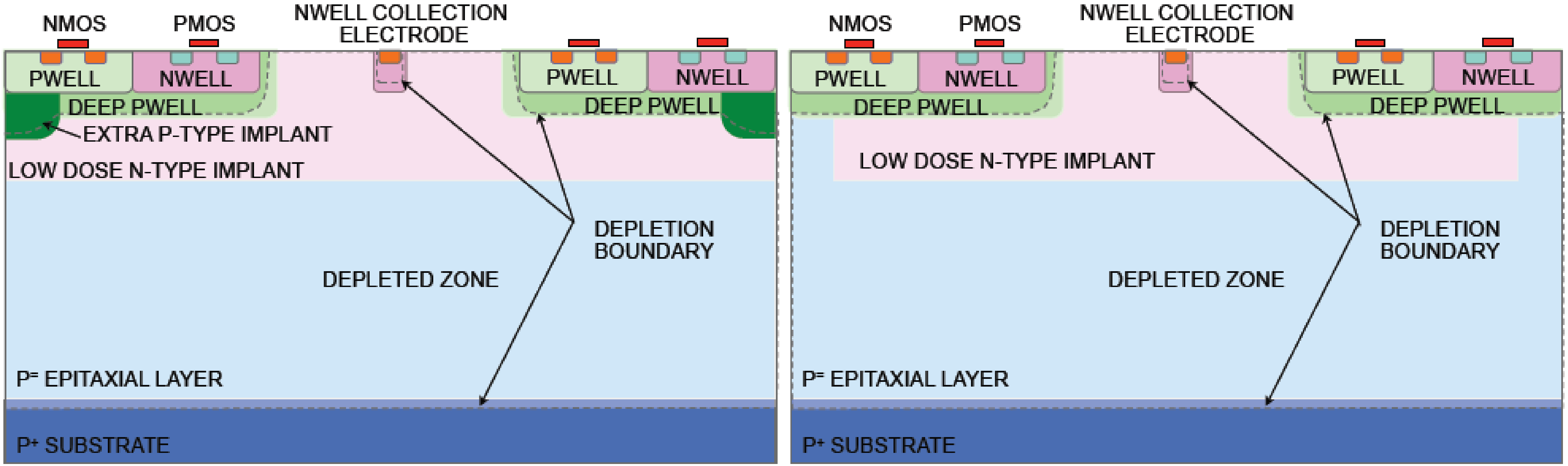
https://doi.org/10.1016/j.nima.2019.162404

However:

- efficiency loss at ~ 10^{15} 1 MeV n_{eq}/cm^2 on the pixel edges and corners due to a too weak lateral field
- Lateral electric field not sufficient to push the deposited charge towards the small central electrode.
- **Efficiency decreases in pixel corners**
- Effect amplified by radiation damage

Tower Semiconductor 180nm

Sensor optimization (2): improvement of the lateral field

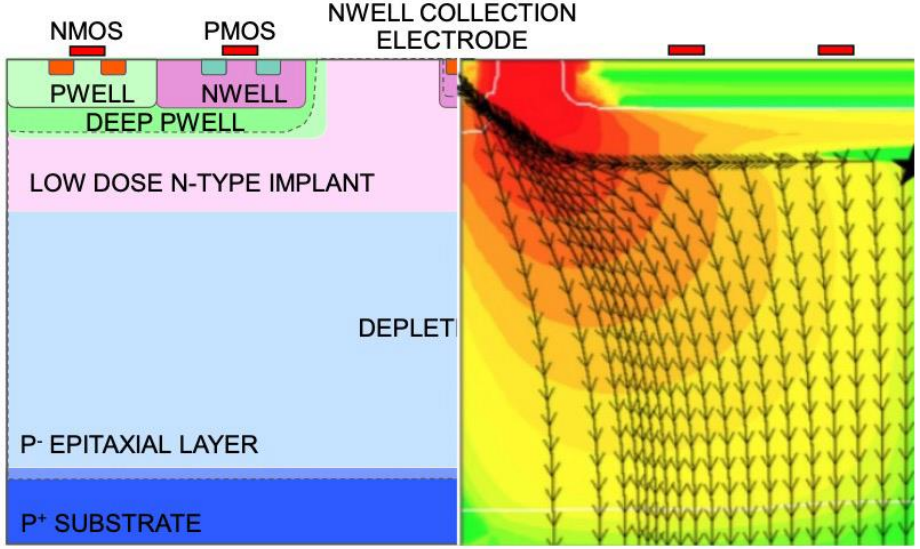


3D TCAD simulation M. Munker et al. PIXEL2018 https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

- Additional deep p-type implant or gap in the low dose n-type implant improves lateral field near the pixel boundary and accelerates the signal charge to the collection electrode.

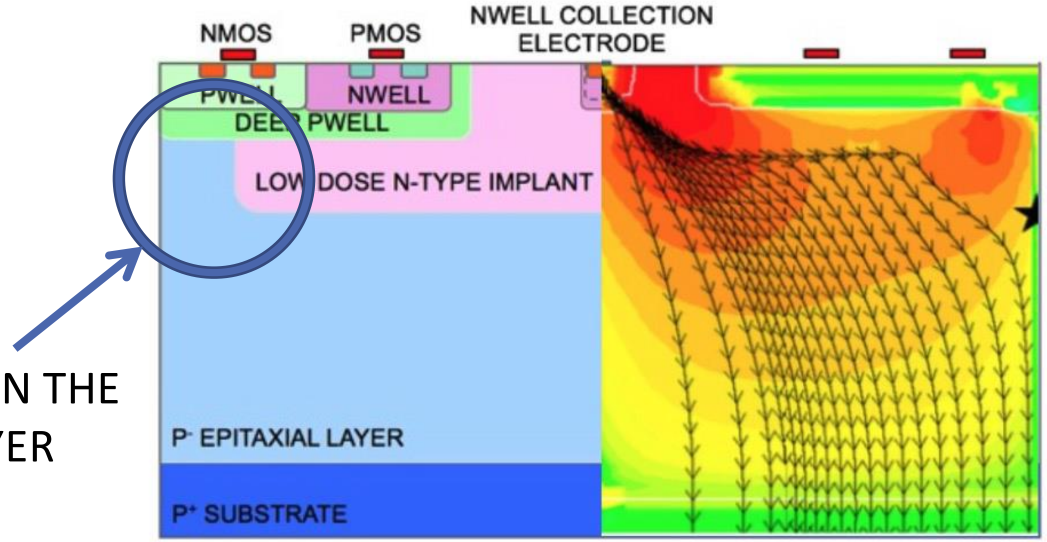
Tower Semiconductor 180nm

Sensor optimization (2): improvement of the lateral field



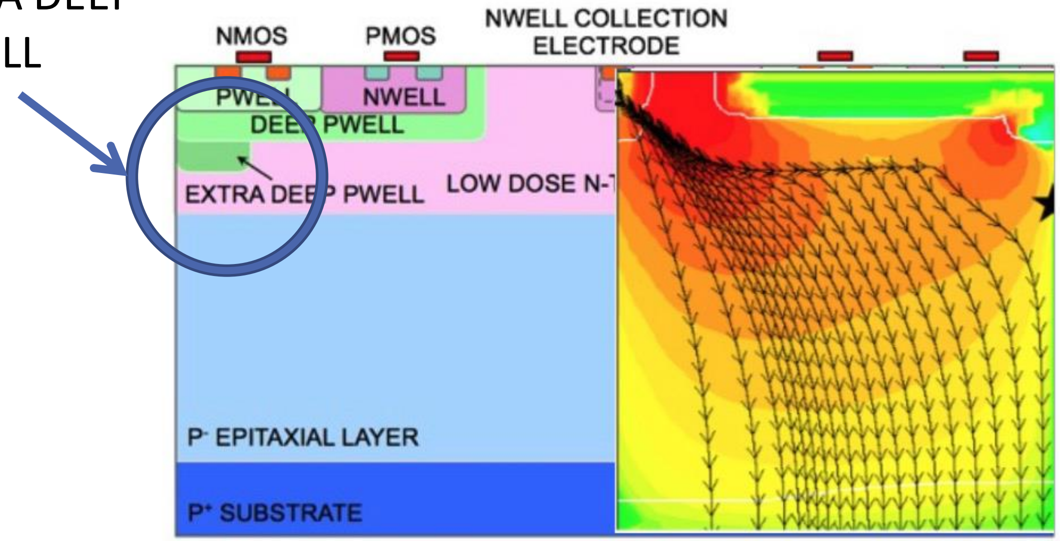
Standard modified process

GAP IN THE N LAYER



Gap in the n- layer (NGAP)

EXTRA DEEP P-WELL



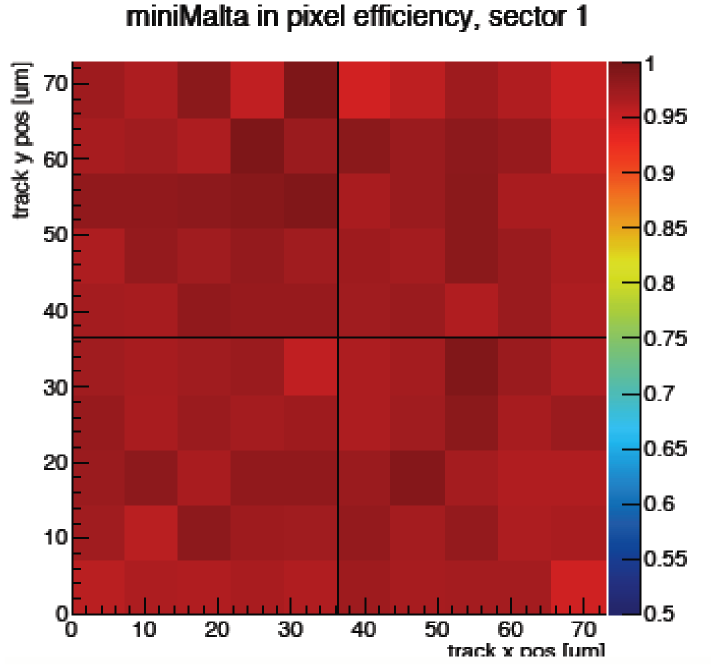
Extra deep p-well (EDPW)

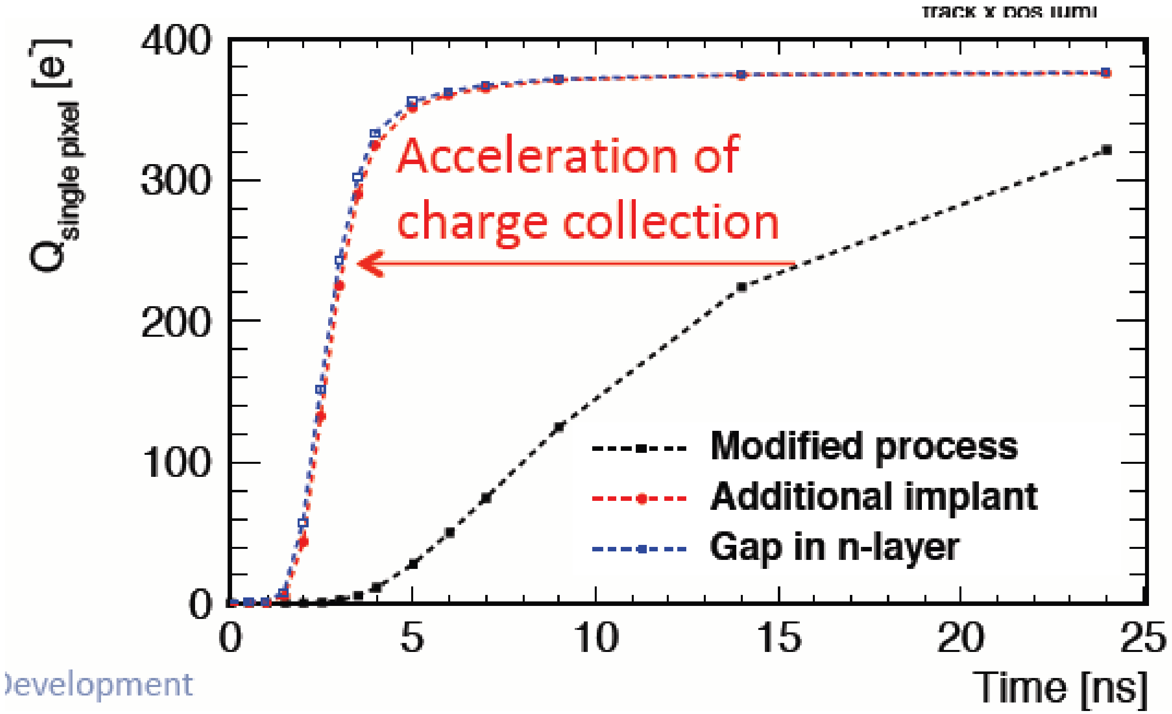
Process modifications to improve charge collection in the pixel edges

3D TCAD simulation M. Munker et al. PIXEL2018 https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

Tower Semiconductor 180nm

Sensor optimization (2): results on detection efficiency





- Full detection efficiency at $10^{15}\ n_{eq}/cm^2$
- better sensor timing

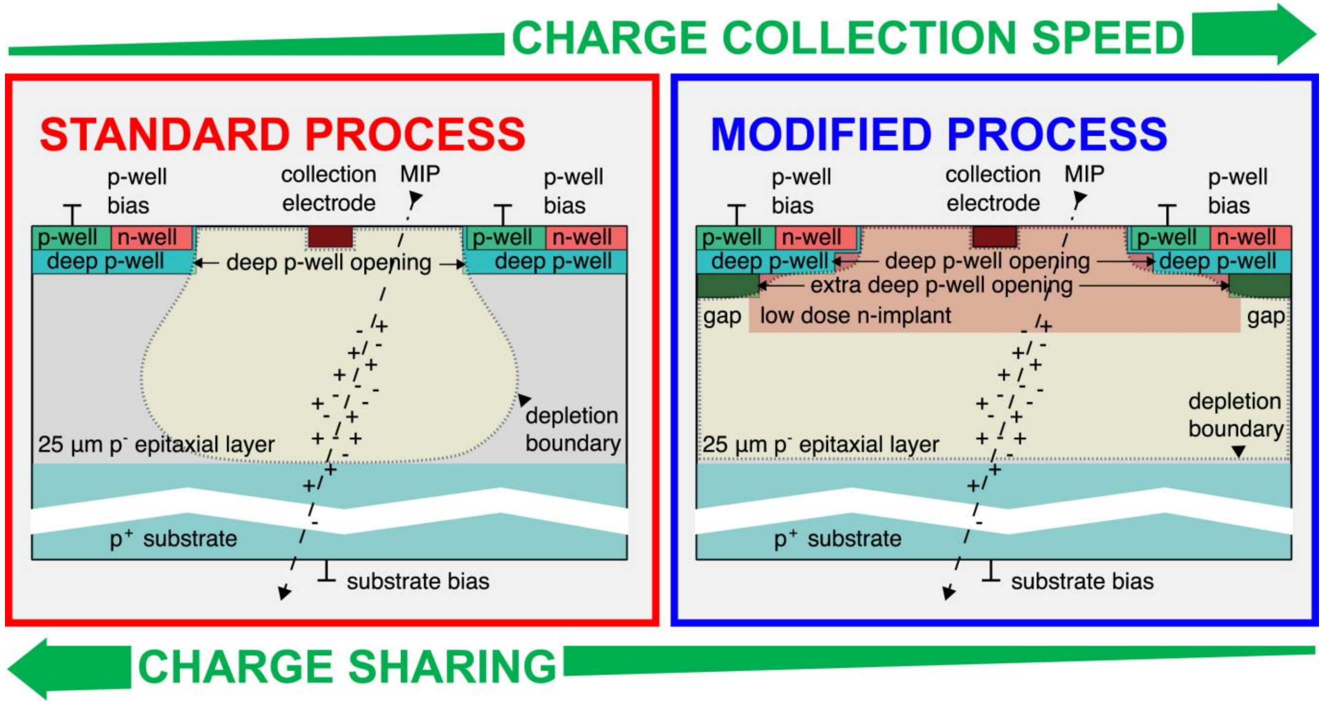
H. Pernegger et al., Hiroshima 2019,
M. Dyndal et al 2020 JINST 15 P0200

3D TCAD simulation M. Munker et al. PIXEL2018
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

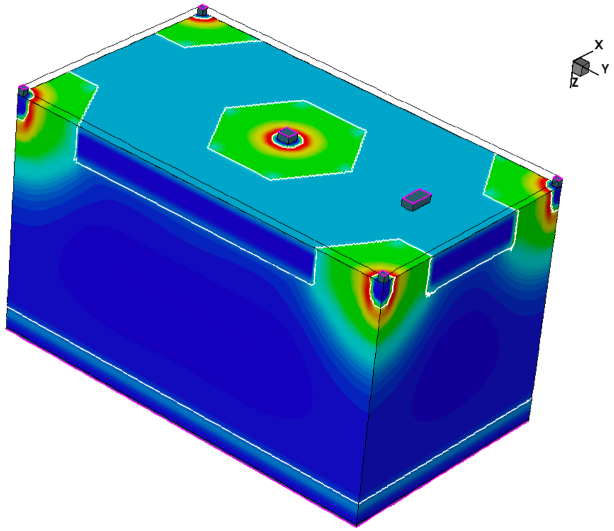
Tower Semiconductor 180nm

FASTPIX

- Hexagonal design
  - reduces the number of neighbors and charge sharing → **higher efficiency**
  - minimizes the edge regions while maintaining area for circuitry → **faster charge collection**
- Optimisations important not only for timing, but also for efficiency and radiation tolerance



Simulated hexagonal unit cell – electrostatic potential:



Tower Semiconductor 180nm

J. Braach et al. Instruments 6 (2022) 13

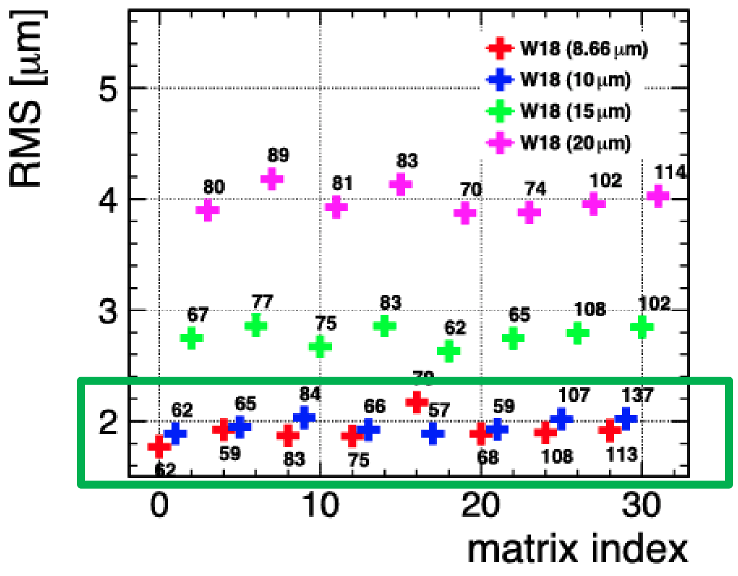
FASTPIX

- **FASTPIX reaches a spatial resolution down to 1μm and O(100ps) timing precision** for the modified process with higher-dose deep n-implant (W18).
- The largest relative improvement was observed for additional triangular corner gaps, followed by improvements from a change in collection electrode and p-well opening size.
- The obtained FASTPIX results with 180nm technology demonstrate the large potential of targeted sensor process and TCAD simulation-based design optimizations for the detector performance.

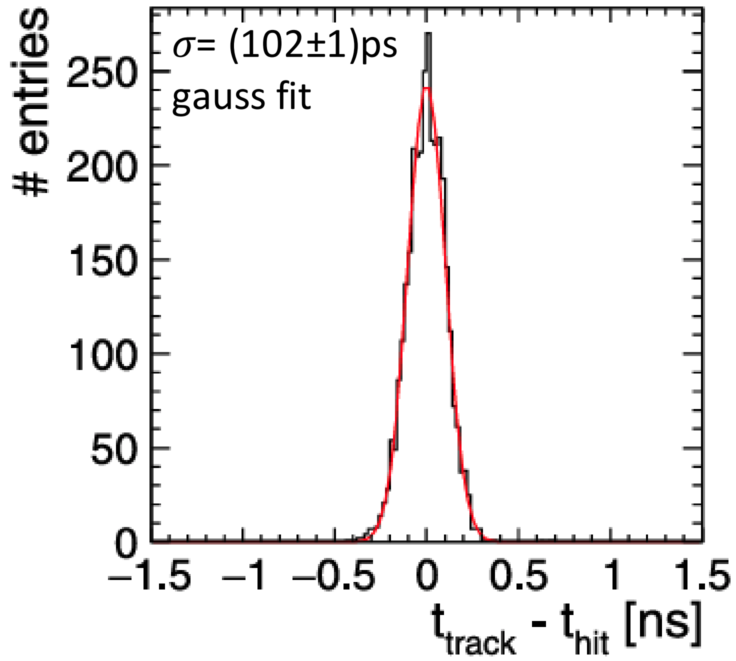
[J. Braach et al. NIMA1056(2023)168641](#)

W18 sample.

Spatial residuals along the x-axis.
The superscript of each data point gives the threshold in electrons for the respective matrix.



Time residual for the 20μm pitch matrix at a threshold of 74e$^-$.
The full distribution yields RMS=(107±2)ps, $RMS_{99.7\%}$=(103.0±0.3)ps and $\sigma_{fit, gaus}$=(102±1)ps.
The errors represent statistical uncertainties.

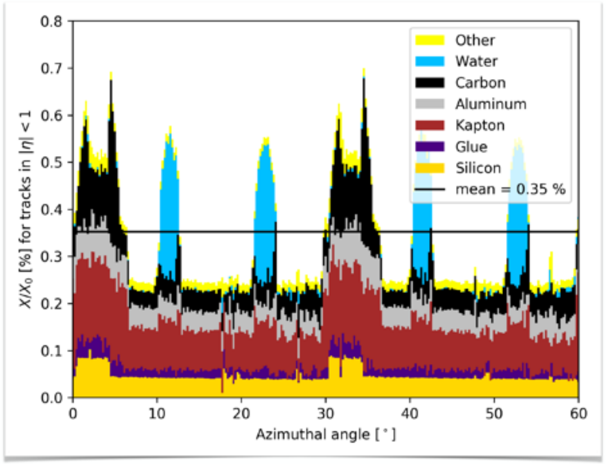


Tower Semiconductor 180nm

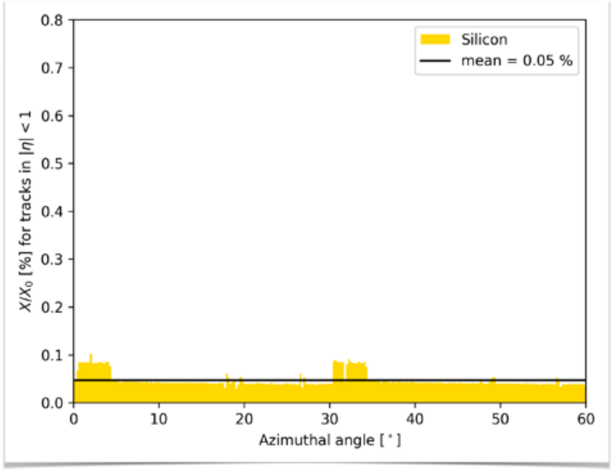
Moving to 65 nm: ALICE ITS3 + EP R&D development

- GOAL for ALICE ITS3:
  - improve determination of primary and secondary vertices at high rate
  - go closer to interaction point
  - reduce material budget X/X_0 0.35%→0.05%
- "SILICON ONLY" TRACKER?
  - exploit stitching → large area sensors
  - thin and bend → sigle sensor half layers
- TECHNOLOGY CHOICE:
  - **65 nm TPSCo (Tower & Partners Semiconductor):** 300mm wafers and stitching available
  - 65 nm → lower power consumption
  - 7 metal layers

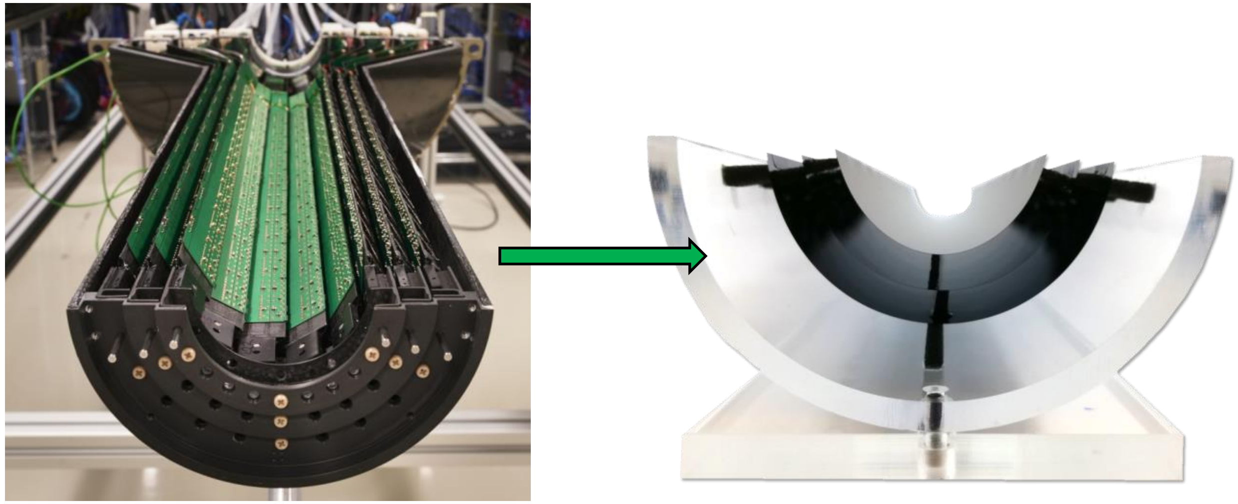
Interesting for EIC, NA60+, FCC ...



ITS2 Inner Barrel



ITS3 mechanical mockup

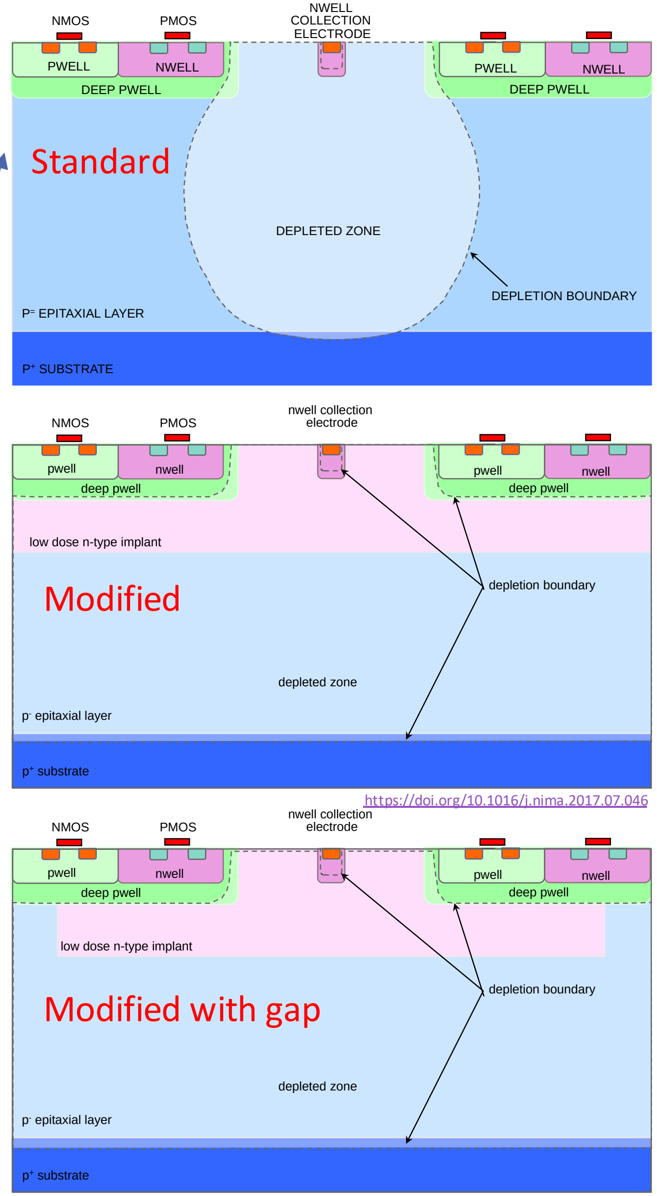


Optimization of the sensor: same approach as 180nm

- Process optimization: more needed/beneficial in 65 nm due to a **thinner epitaxial layer**
  - Add and adjust the low-dose deep n-well implant in the pixel to obtain easier depletion
  - Adjust the deep p-well implant
    - improve the isolation between the circuit and the sensor,
    - prevent punch through between deep n-type implant and circuitry
    - prevent local potential wells retaining the signal charge.

- 4 process splits: moving gradually from default to optimized process

- 3 main pixel designs implemented in all process splits



https://doi.org/10.1016/j.nima.2017.07.046

https://doi.org/10.22323/1.420.0083

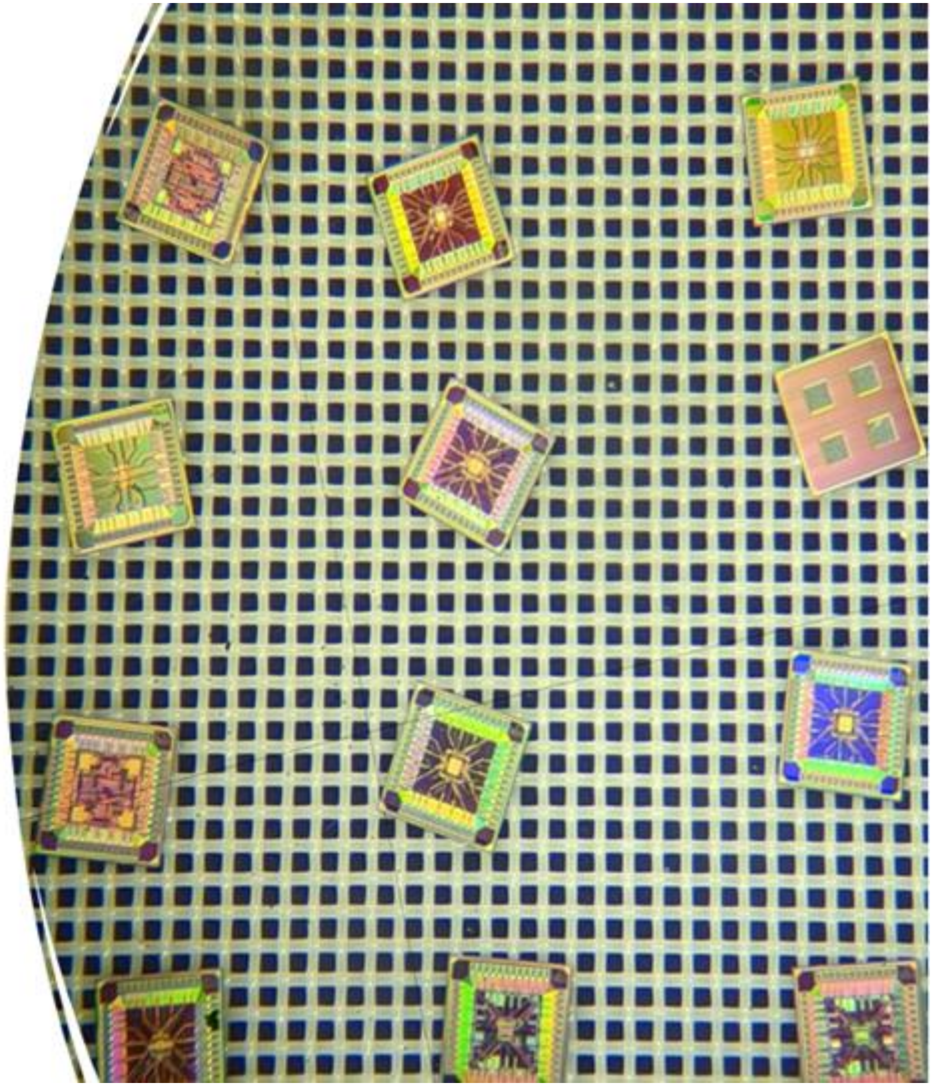
https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

First test submission: MLR1

Follow Rebekka Wittwer talk on Thursday!!

ALICE

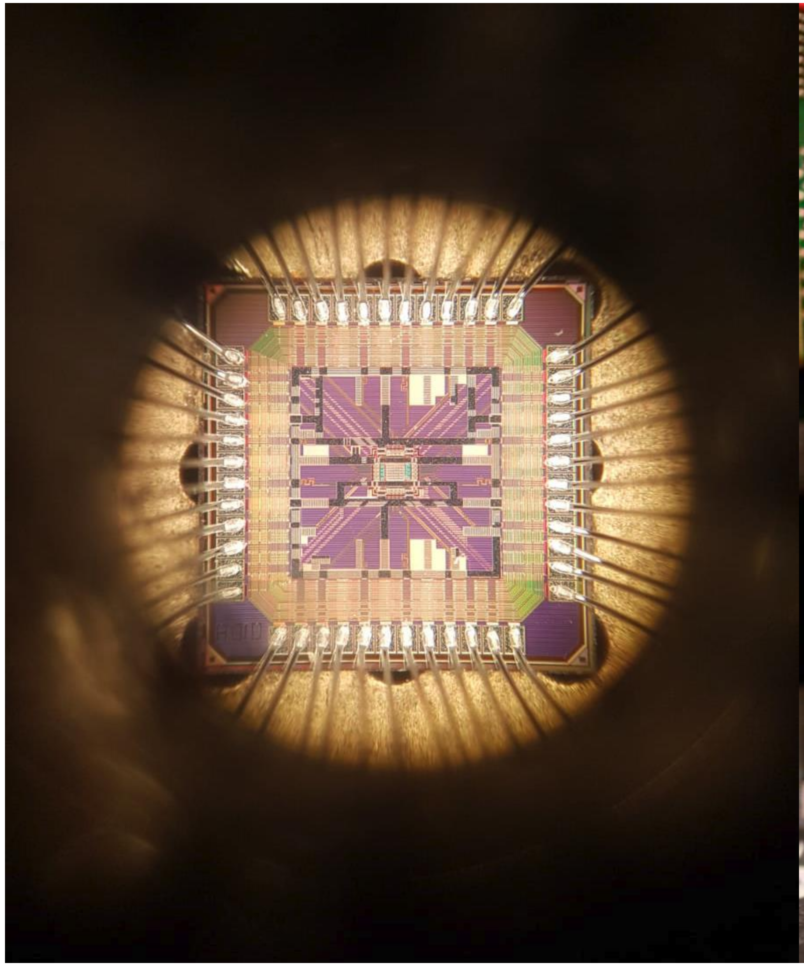
- Submitted in December 2020
- Main goals:
  - Learn technology features
  - Characterize charge collection
  - Validate radiation tolerance
- Each reticle (12×16 mm^2):
  - 10 transistor test structures (3×1.5 mm^2)
  - 60 chips (1.5×1.5 mm^2)
    - Analogue blocks
    - Digital blocks
    - **Pixel prototype chips: APTS, CE65, DPTS**
- Testing since September 2021:
  - huge effort shared among many institutes
  - laboratory tests with ^{55}Fe source
  - beam tests @ PS, SPS, Desy, MAMI, etc...

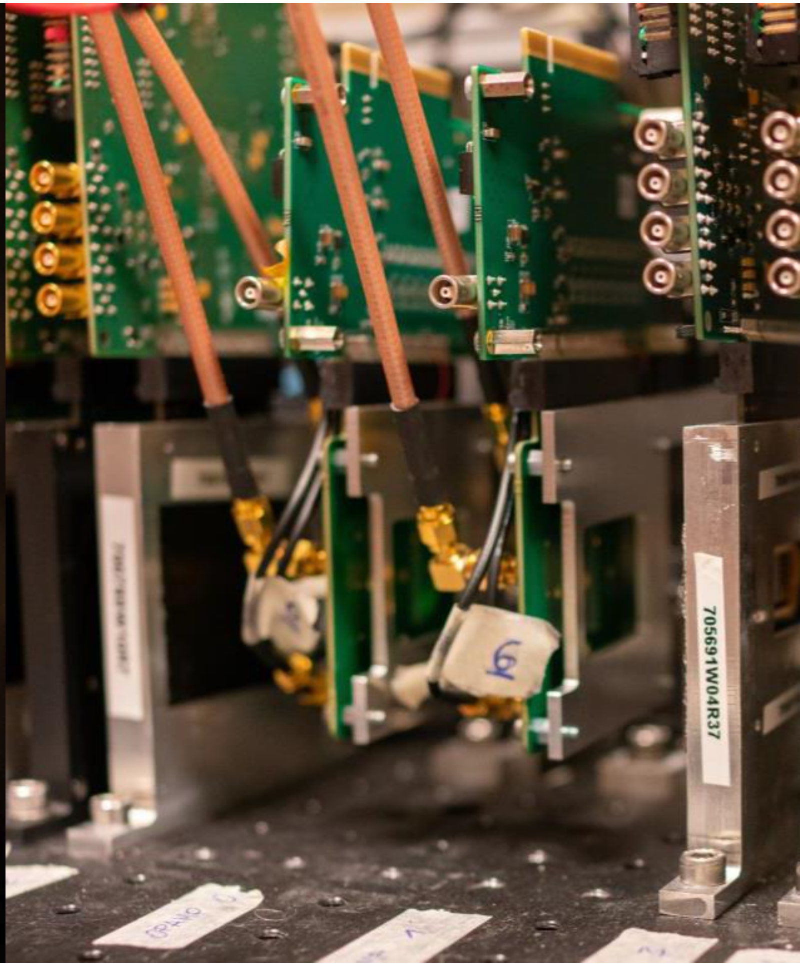


APTS OpAmp

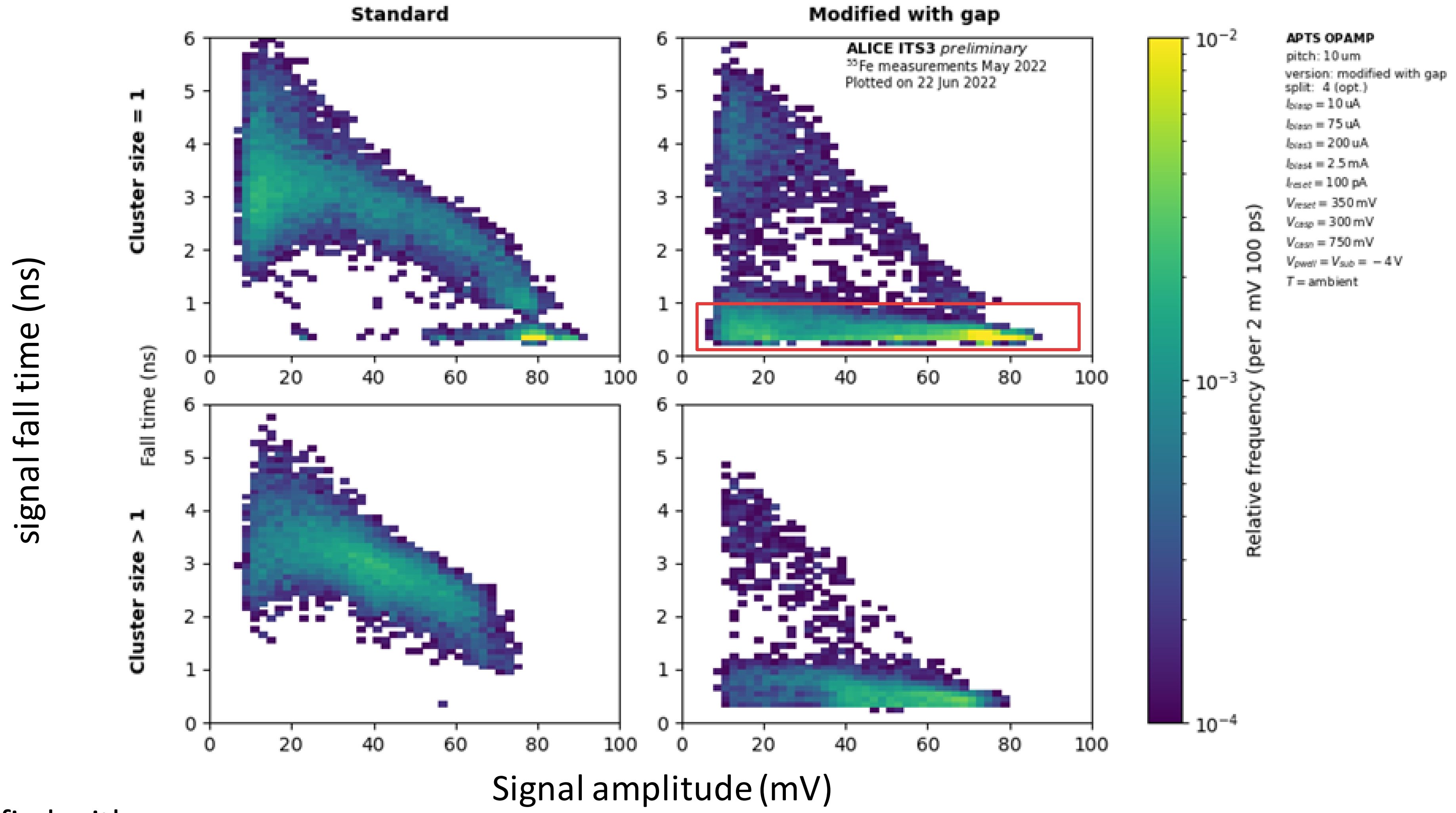
- Test structure with OpAmp Analog output to start verifying the timing performance of the 65nm technology

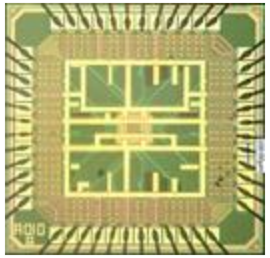
- Results from beam tests in 2022 and 2023 are available:
  - timing performance
  - detection efficiency





APTS OpAmp - Fall time vs amplitude





Modified with gap:
80% of cluster size 1 events lies in the region with fall time lower than 1 ns, compared with 20% of the standard process

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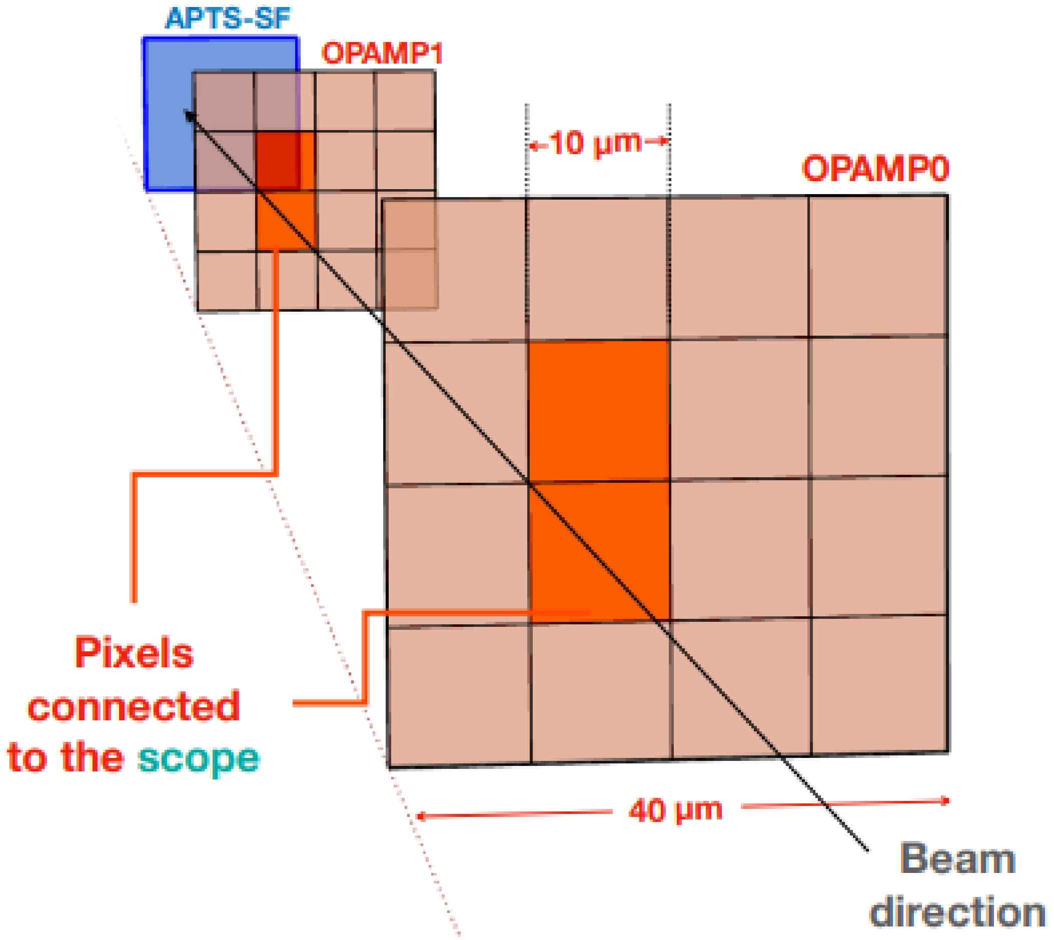
Timing resolution measurement @SpS

Measurement strategy:

- Time residuals Δt distribution of tracks associated to the pixels of both DUT measured with the oscilloscope

DUT alignment

- Challenging alignment of < 5 µm accuracy
- Online analysis of alignment runs and position adjusted with moving stages



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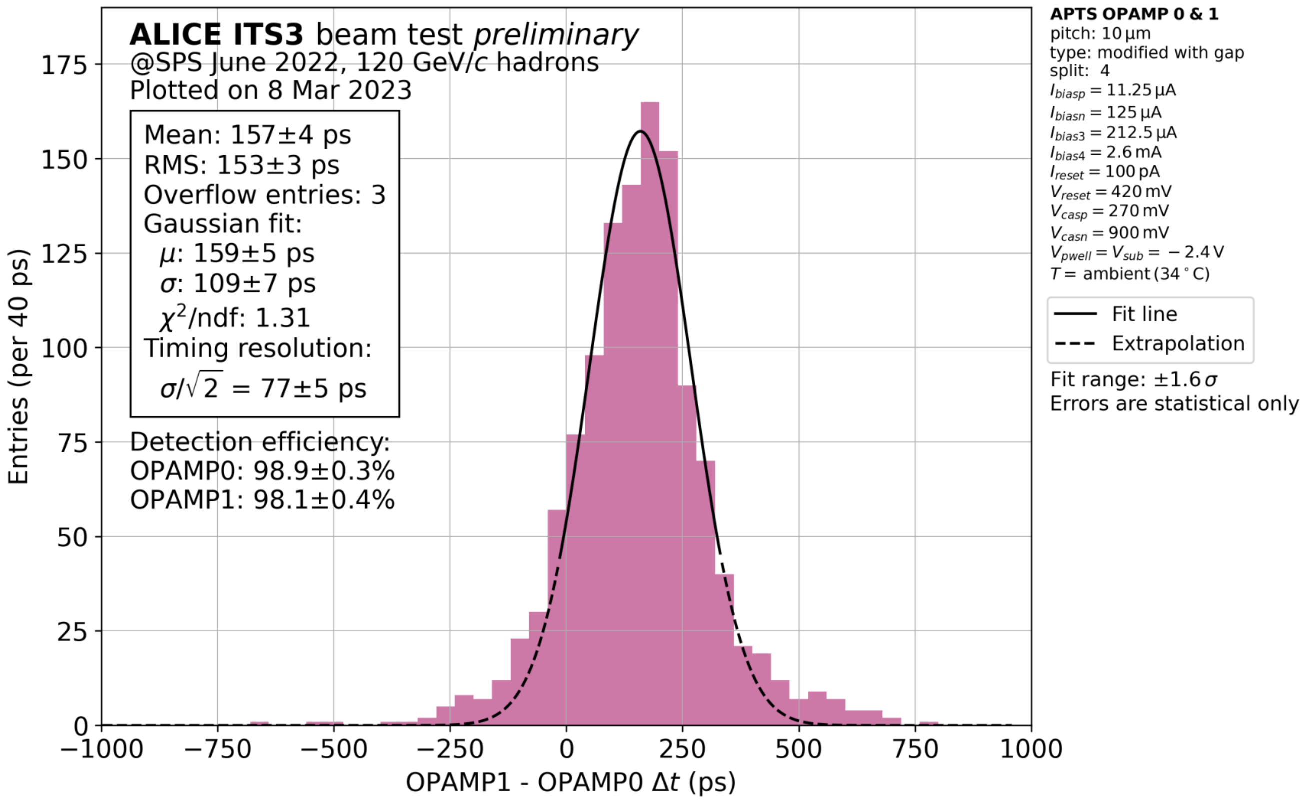
Results from 2022

Time residuals distribution at 10% of signal amplitude fraction $\Delta t = t^{1}_{10\%CFD} - t^{0}_{10\%CFD}$

- DUTs operated at reverse bias= – 2.4 V
- Efficiency of both DUTs of the order of 99%
- Time residuals distribution fitted with a gaussian function within ± 1.6 σ range (solid line)

- Timing resolution of 77 ± 5 ps without jitter/time walk correction



new results available, will be presented soon!!!

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Large area 65nm chip development roadmap

ALICE

PAST

- **MLR1: first MAPS in TPSCo 65nm** (2021) - successfully qualified the 65nm process for particle detectors

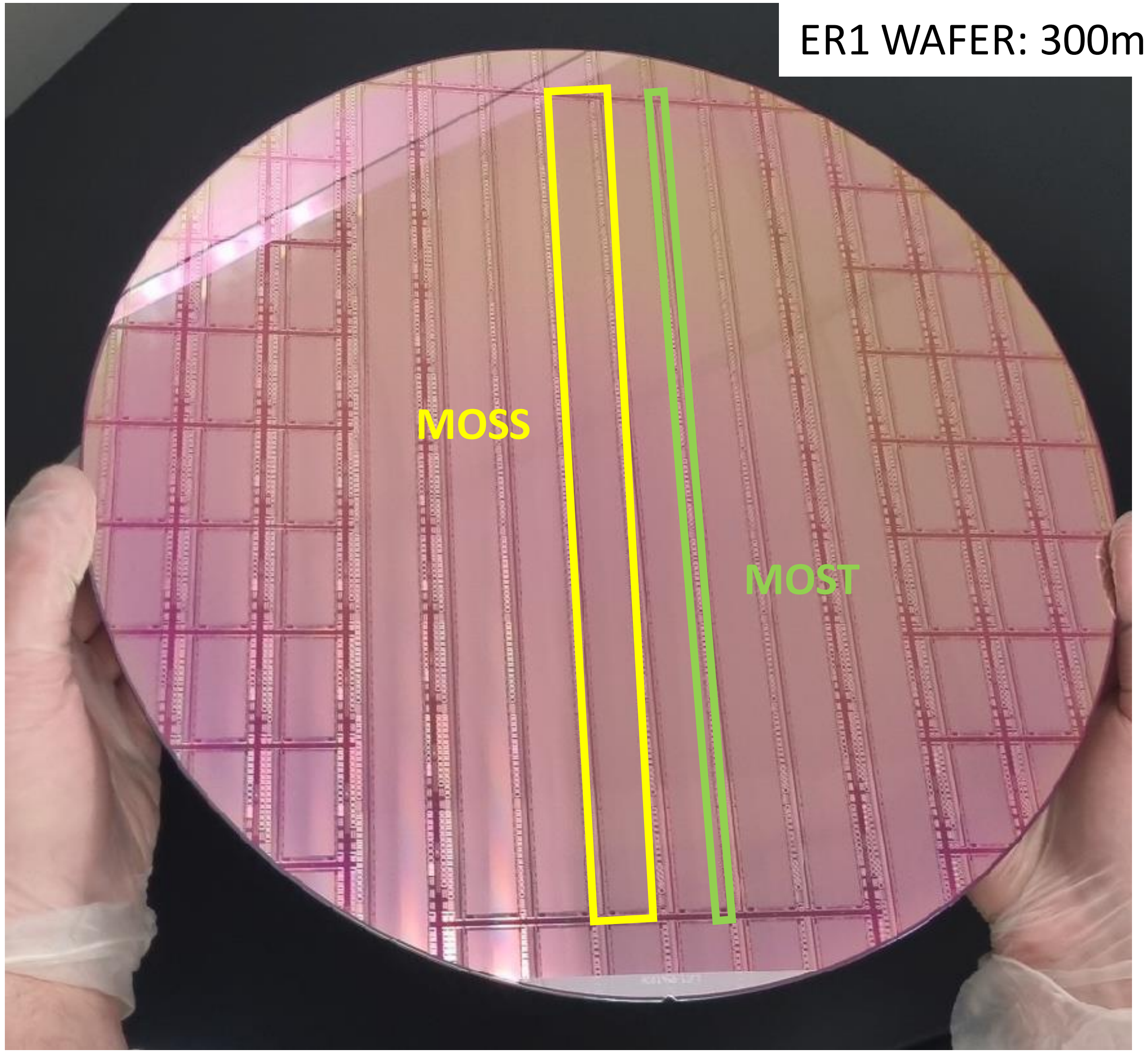
PRESENT

- **ER1: first stitched MAPS** (2023)
  - large design "exercise"
  - "**MOSS**": 14 x 259 mm, 6.72 MPixel (22.5 x 22.5 and 18 x 18 µm2): conservative design, different pitches
  - "**MOST**": 2.5 x 259 mm, 0.9 MPixel (18 x 18 µm2): more dense design

FUTURE

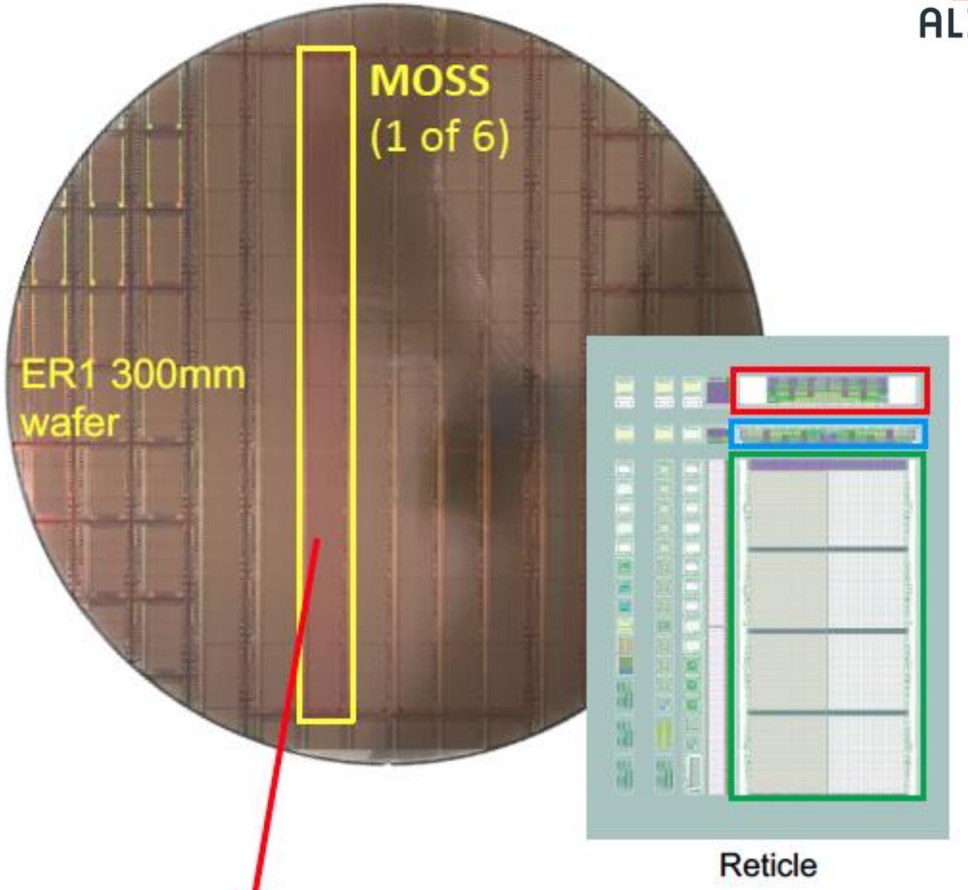
- **ER2: first ITS3 sensor prototype** (2024)
- **ER3: ITS3 sensor production** (2025)

ER1 WAFER: 300mm



ER1 submission: MOSS

Primary Objectives
Learn design with stitching to build wafer scale particle detectors
Distribute power and signals on wafer scale chip
Study manufacturing yield and constraints
Study power, leakage, noise, spread

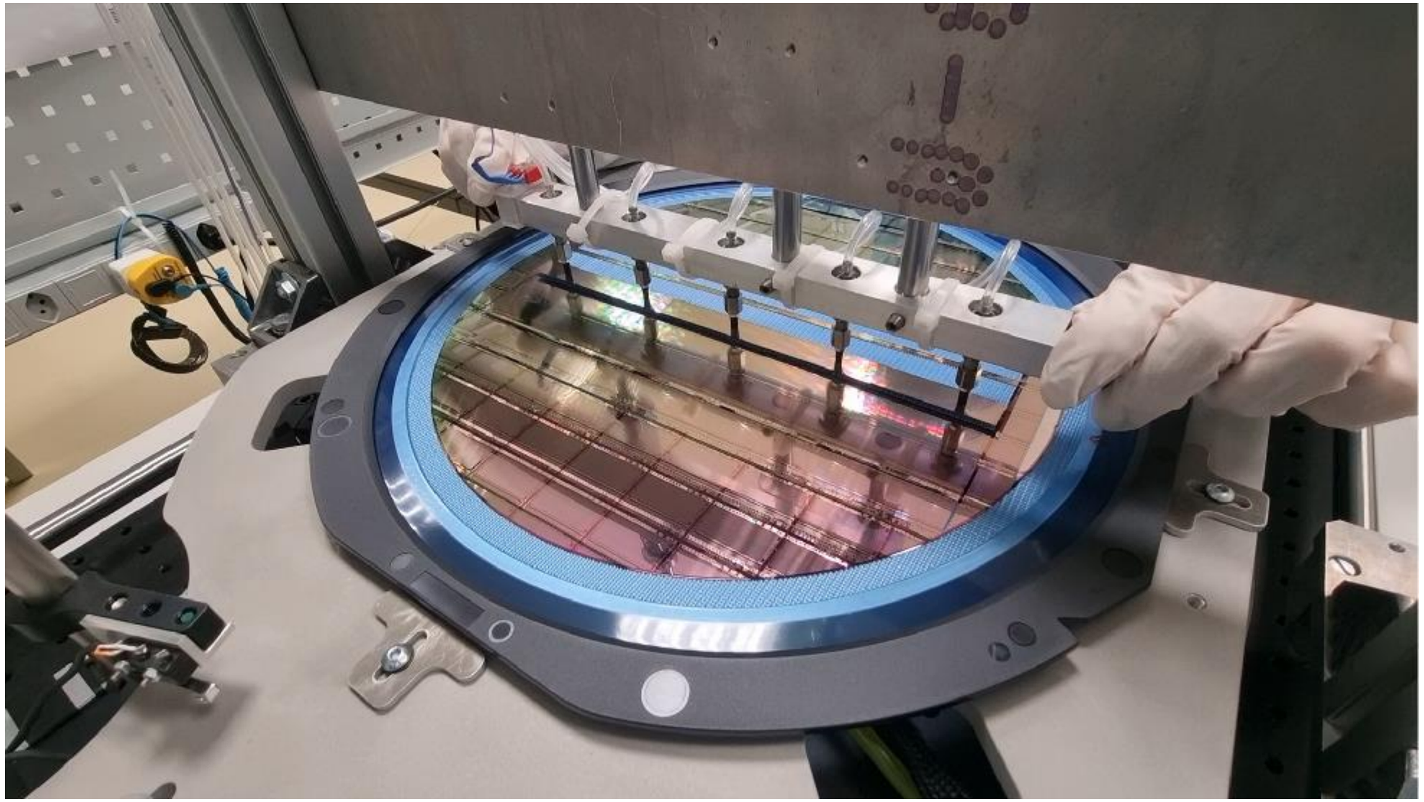


Repeated units abutting on short edges

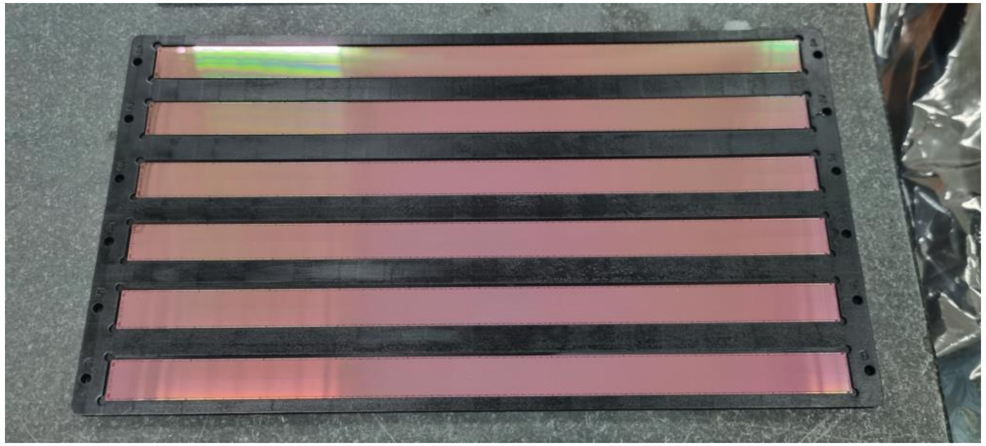
- Repeated Sensor Unit, Endcap Left, Endcap Right
- Functionally independent designs
- Metal traces cross stitching boundaries for power distribution and long range on-chip control and data transfer
- Module integration on wafer scale die for the first time

Large area prototypes: handling

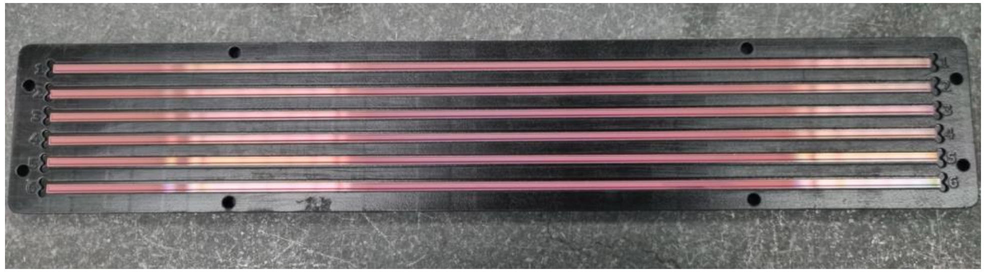
- ER1 wafers are thinned down to 50 µm
- Tools to pick, handle and ship chips have been developed



MOSS

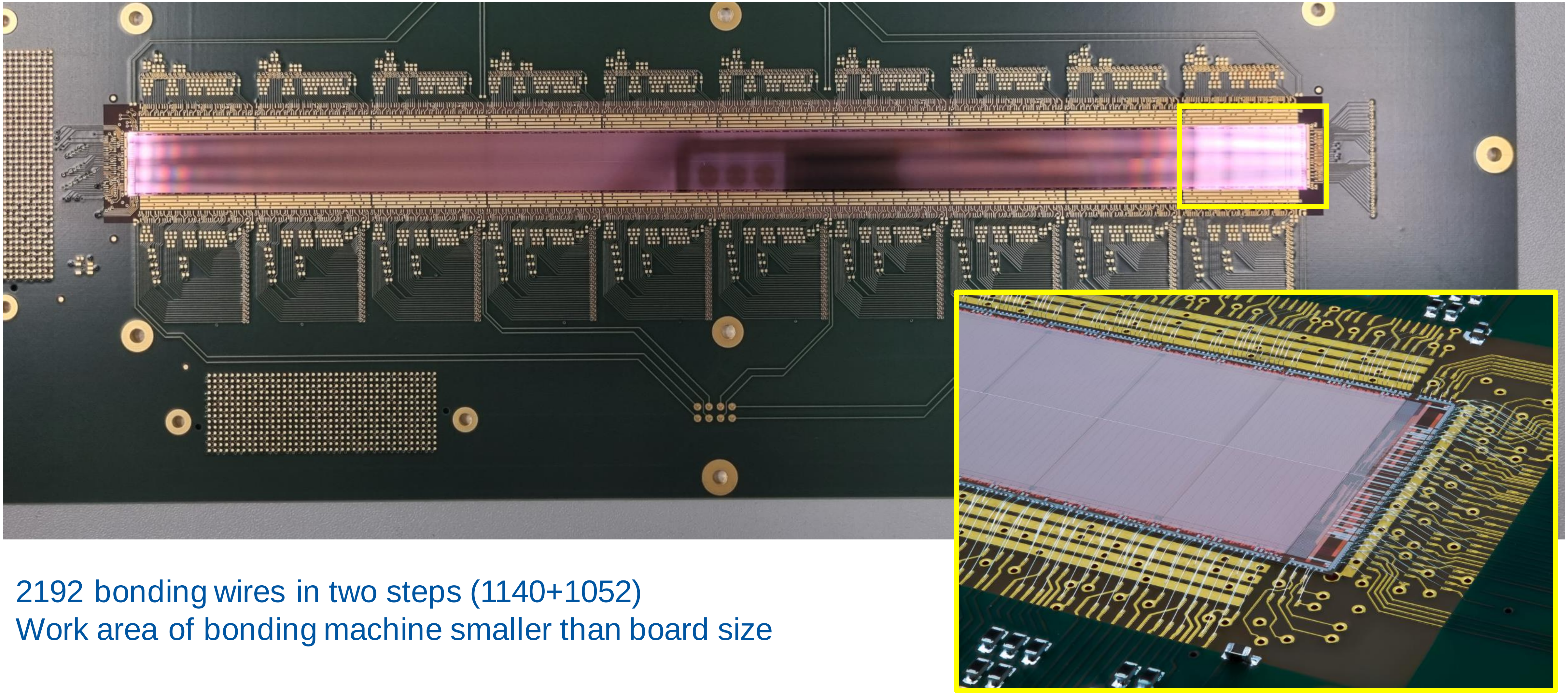


MOST



A set of dedicated tools have been developed — handling is under control

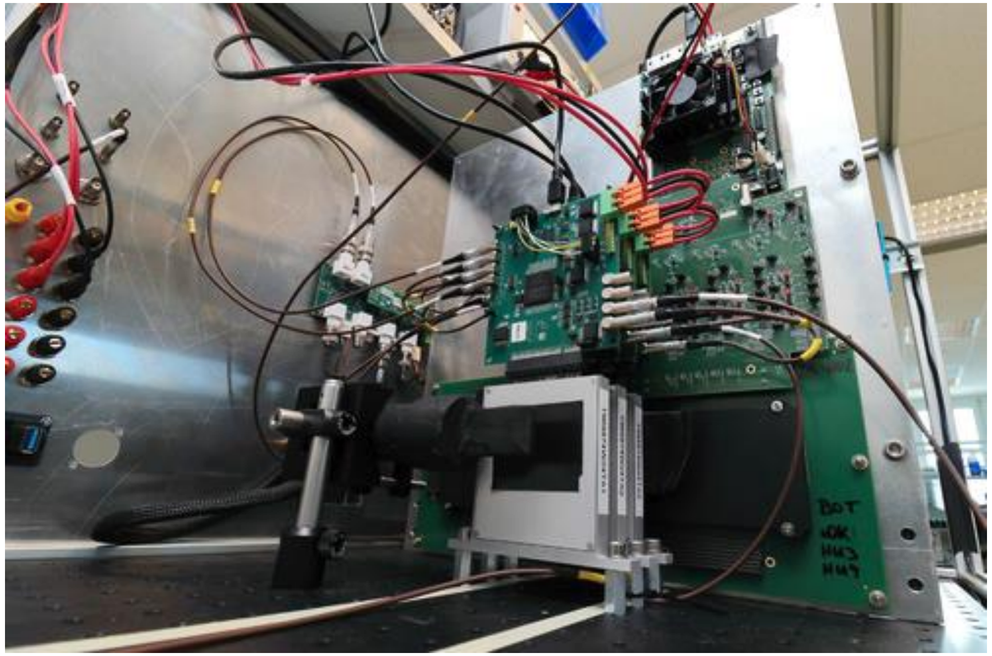
Assembly on carrier boards for characterization

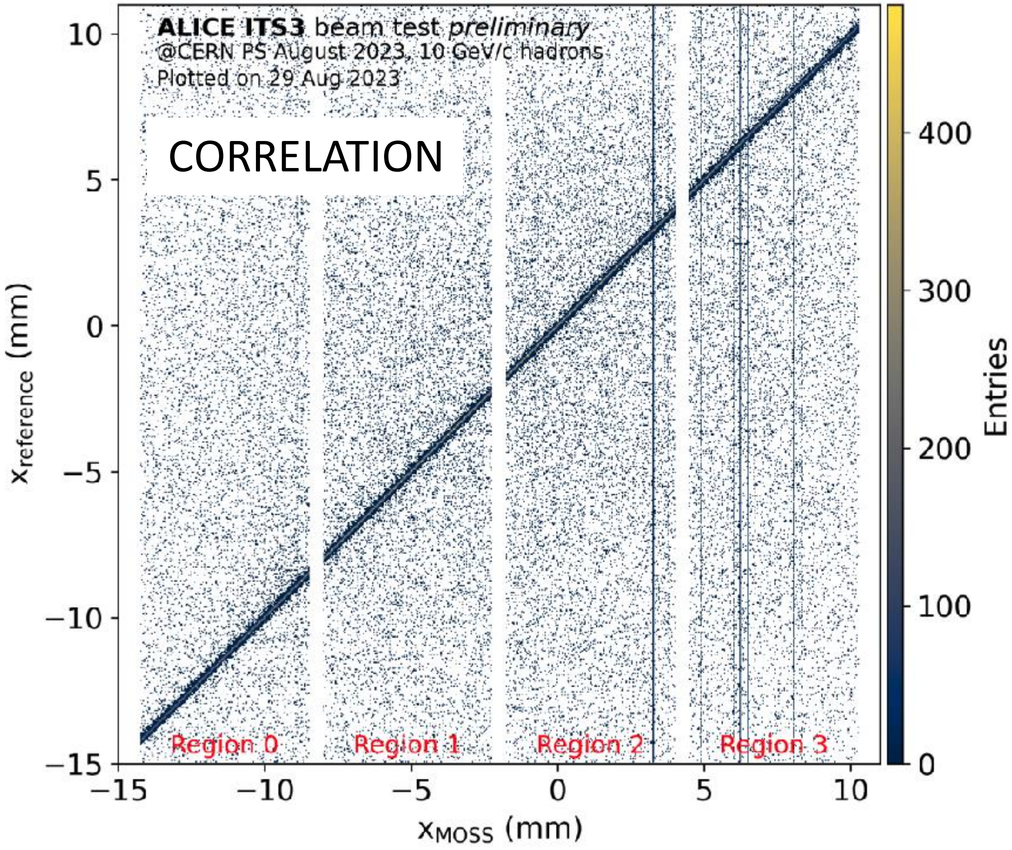


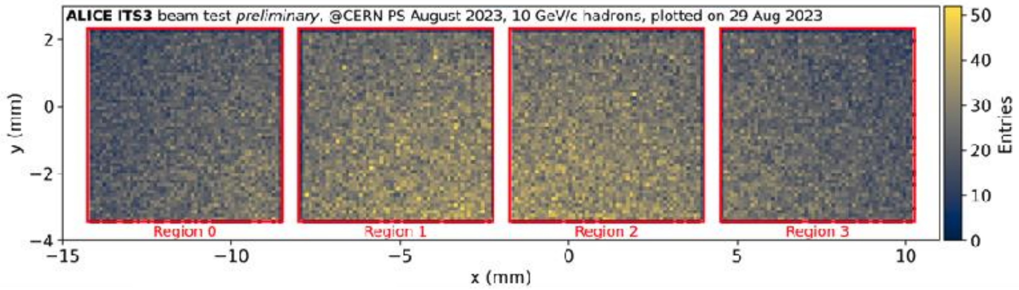
2192 bonding wires in two steps (1140+1052)
Work area of bonding machine smaller than board size

MOSS test beams

- Several campaigns in 2023
- Works out of the box
- Parameters still to be optimised and data to be analysed in more detail
- But very encouraging result!



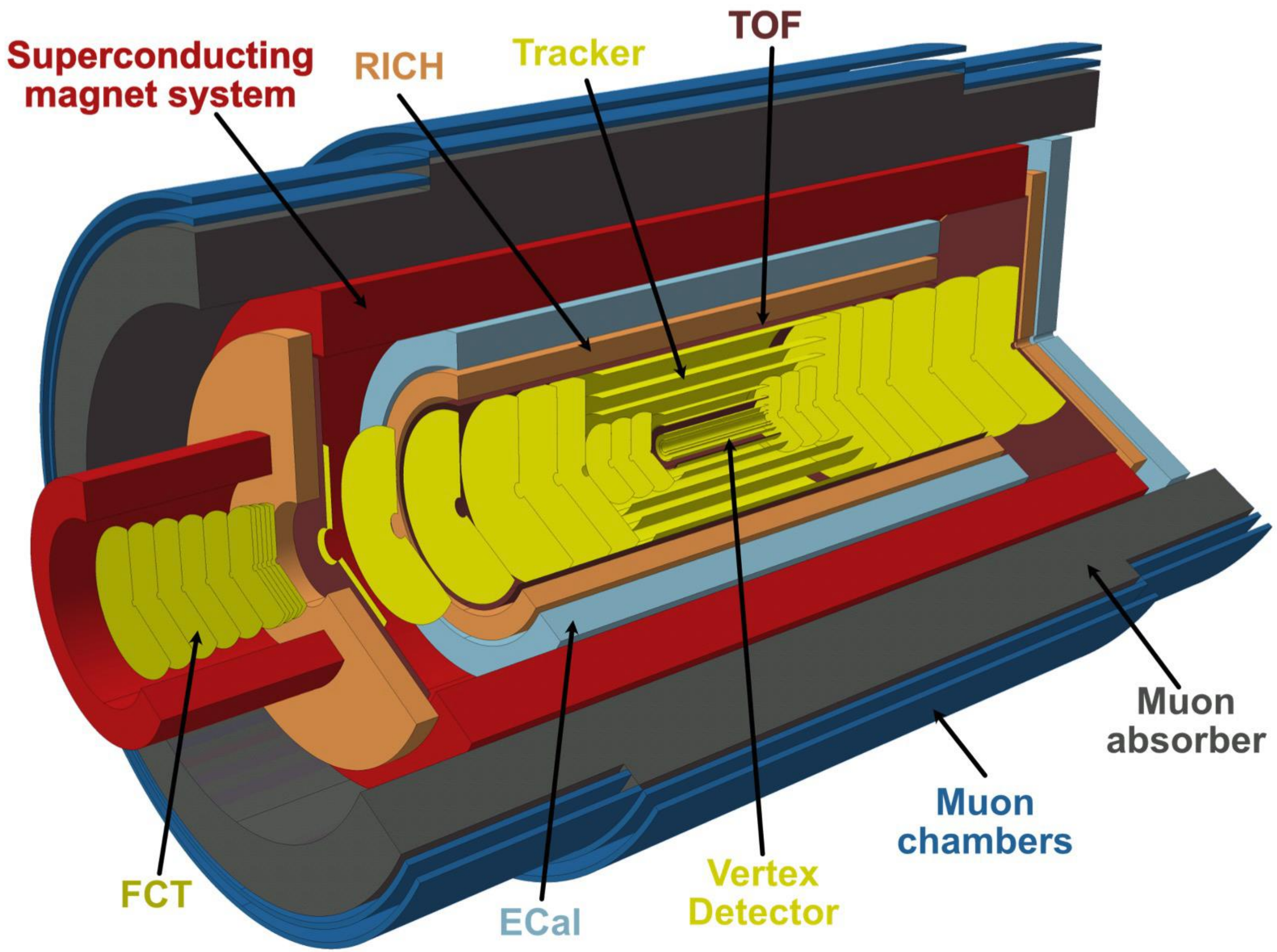




HITMAPS

Large future silicon based experimental set-ups

LHC timeline after RUN 4:



ALICE3

Ambition to design a new experiment to continue with a rich heavy-ion programme at the HL-LHC" mentioned in the Update of the European strategy for particle physics

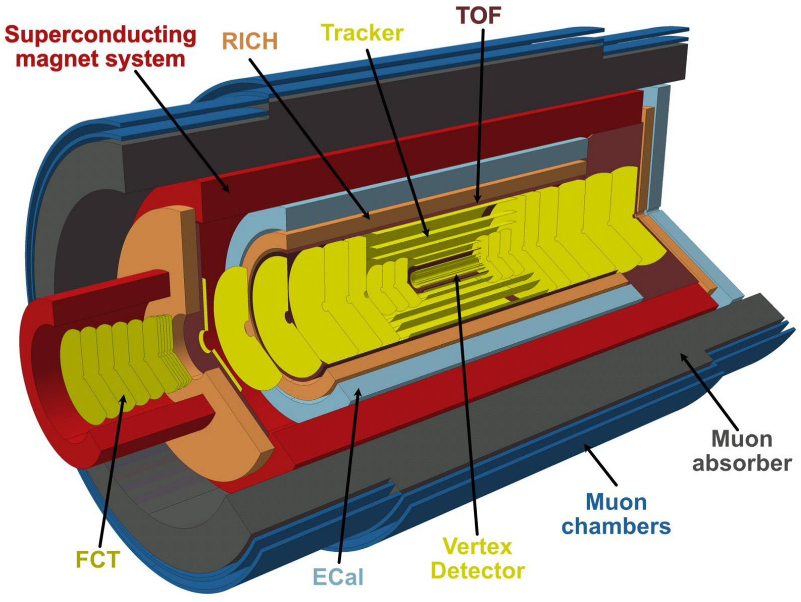
arXiv:2211.02491

LoI positively reviewed by LHCC last year

ALICE3 Time of Flight

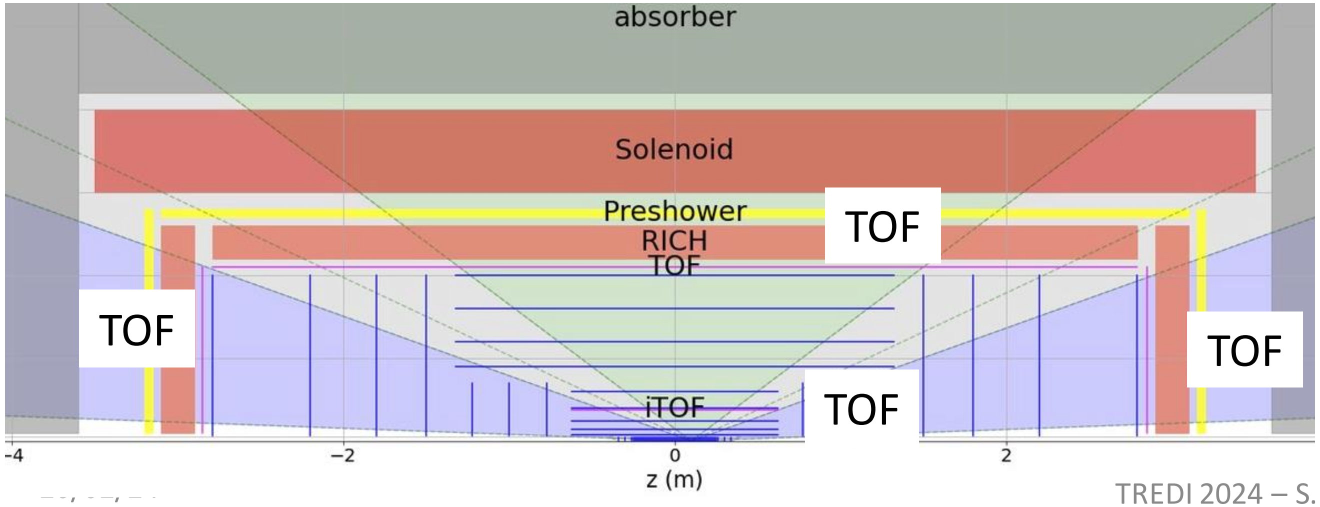
Innovative detector concept

- ❑ Compact and lightweight all-silicon tracker
- ❑ Retractable vertex detector
- ❑ Extensive particle identification
- ❑ Large acceptance
- ❑ Superconducting magnet system
- ❑ Continuous read-out and online processing



TOF

- outer TOF at R ≈ 85 cm
- inner TOF at R ≈ 19 cm
- forward TOF at z ≈ 405 cm



Separation power ∝ L/σ_{TOF}

- distance and time resolution crucial
- larger radius results in lower p_T bound

2 barrel + 1 forward TOF layers 45 m^2 in total

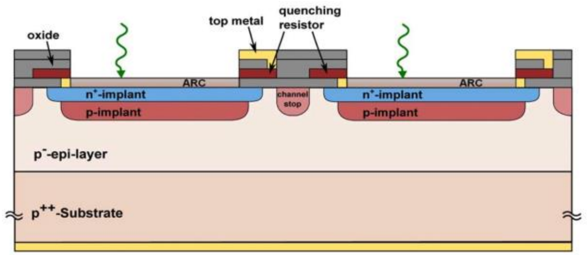
Silicon timing sensors ($\sigma_{TOF} \approx 20$ ps)

Material budget: 1-3% X/X0

Power consumption: <50mW/cm^2

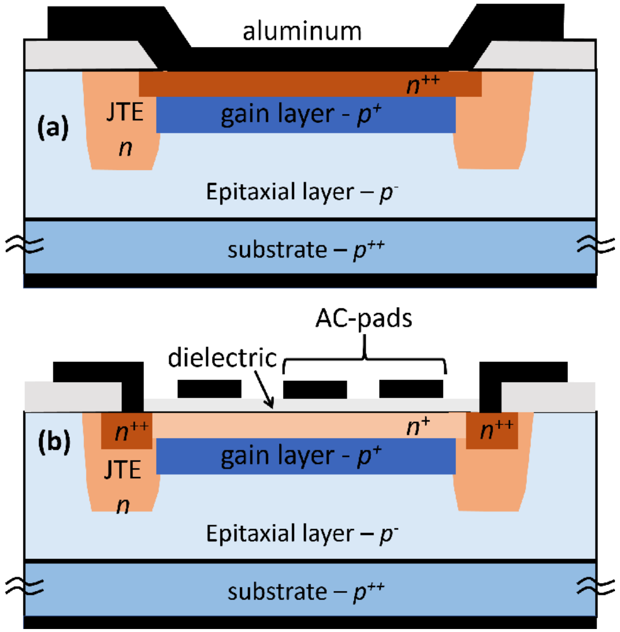
Choice of technology for TOF

SIPM



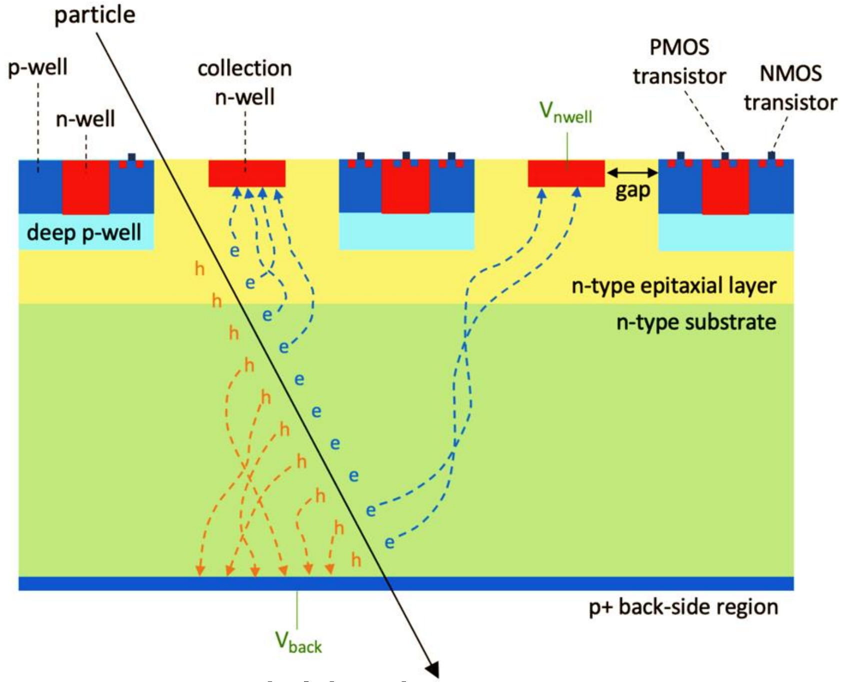
- Timing resolution of ~ 20 ps only for photons detection so far
- Feasibility to be demonstrated with charged particles

L-GAD



- Timing resolution of ~ 20-30 ps demonstrated with 50 µm up to (1-2)10^{15} 1-MeV-n_{eq}/cm^2
- thinner LGADs produced by different manufacturers

HV DEPLETED MAPS

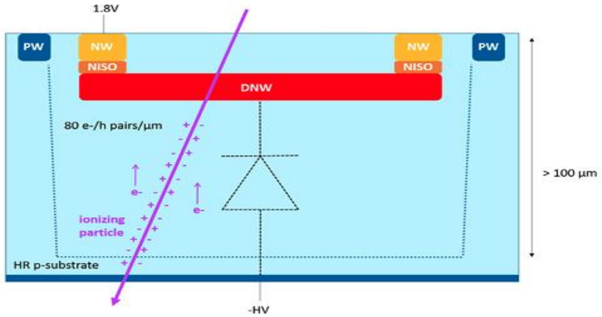


Low material budget
- High SNR
- Low power
- Investigation on innovative design to proof timing performance

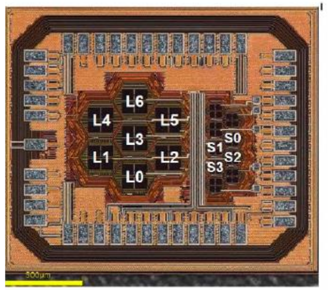
some examples in the next slides

TIMING WITH MONOLITHIC SENSORS: OPPORTUNITIES AND CHALLENGES

- Advantages:
  - Potentially 100% efficiency
  - Excellent radiation hardness demonstrated for several processes
  - Cost-effectiveness–on chip digitization, time-tagging and data pre-processing

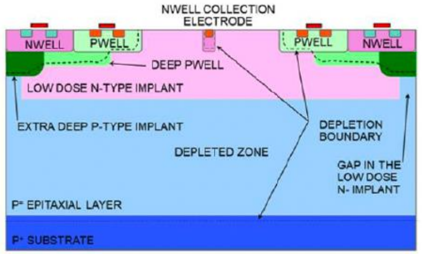


Degerli et al. NIM A Volume 1039, 2022, 167022



G. Iacobucci et al., 2019
JINST 14 P11008

M. Milanesio et al 2024
JINST 19 P01014



T. Kugathasan et al., Nucl. Inst. Meth. A
Vol. 979, Nov. 2020

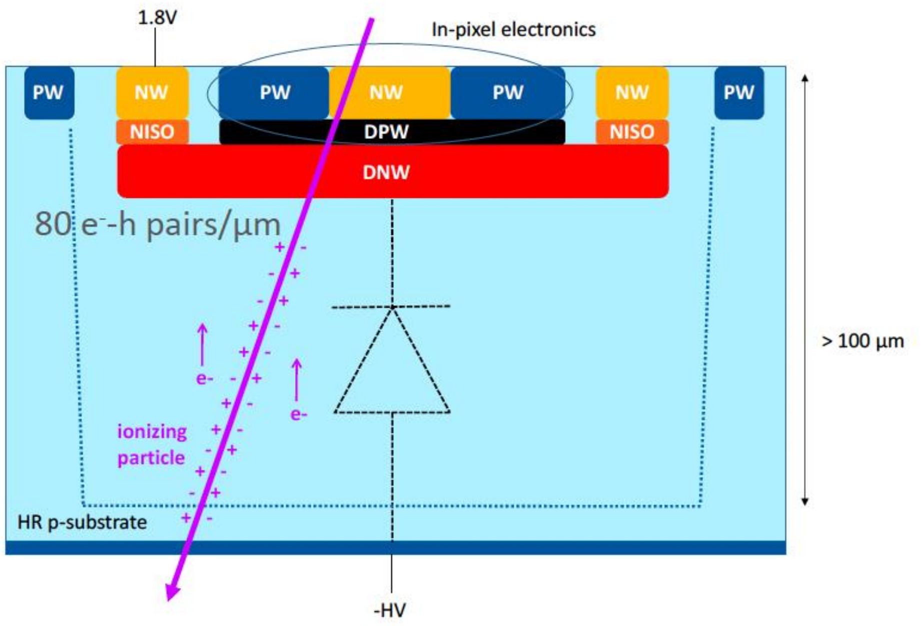
Several monolithic projects targeting enhanced timing resolution

- Challenges
  - Fast collection (100s of ps) and low capacitance at the same time
  - Low power consumption
  - **20 ps resolution obtained experimentally recently by Monolith project** (see talk by G. Iacobucci on Thursday), not yet in reach for the other developments…

TIMING WITH HV-CMOS/DMAPS

- Development of a monolithic timing sensor in a commercial HV-CMOS process (150-110 nm)
- LFoundry 150 nm HV-CMOS is one of the CMOS processes studied extensively for the CMOS option of the ATLAS Inner Tracker Upgrade
- Several large size demonstrators already designed and tested for tracking applications (LF-CPIX, LF-MONOPIX1, LF-MONOPIX2) in this process with proven radiation hardness (Bonn, IRFU and CPPM coll.)
- Wafers can be thinned and backside processed (for backside polarization and good charge collection uniformity)

HV-CMOS Sensor Pixel



DNW/HR p-substrate charge collection diode

- HV (≥ 300 V) applied on the substrate (from top or back)
- Large depletion depth (≥ 300 μm)
- **Charge collection by drift (fast)**
- **No internal amplification**
- **Electronics can be integrated inside charge collection diode**

HVCMOS/DMAPS 150nm: CACTUS* and MiniCactus

CACTUS demonstrator for timing in LFoundry 150 nm process designed in 2019

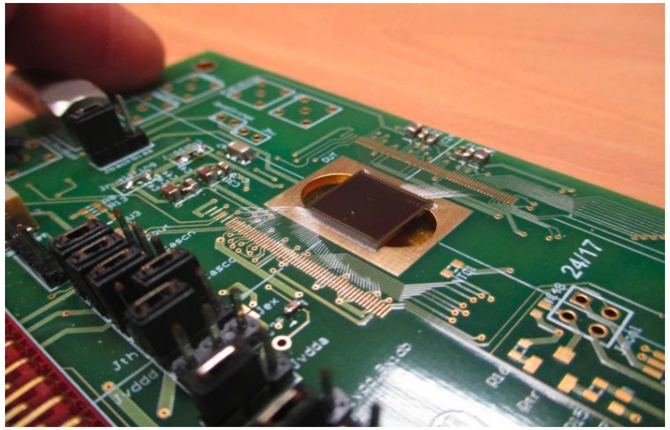
- Expected timing resolution from Cadence & TCAD simulations: **50-100 ps**

- Promising results obtained with the CACTUS detector:
  - high breakdown voltage, homogenous charge collection, deep depletion depth
  - good yield
- but:
  - very low S/N observed
  - Very long & large power rails needed to distribute power into pixels increased significantly detector capacitance in CACTUS
  - Timing possible only with high thresholds (leading to very low efficiency)

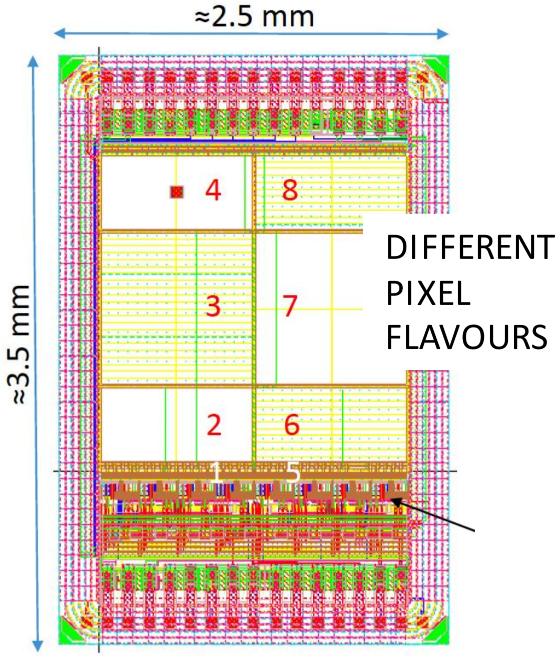
Y. Degerli et al. JINST 15, 2020

MiniCACTUS is a smaller detector prototype designed in order to address the *low S/N issue* of CACTUS

- Main change in MiniCACTUS: FE integrated at column level, pixels mostly passive



The CACTUS demonstrator on PCB
(chip size : 1 cm x 1 cm)

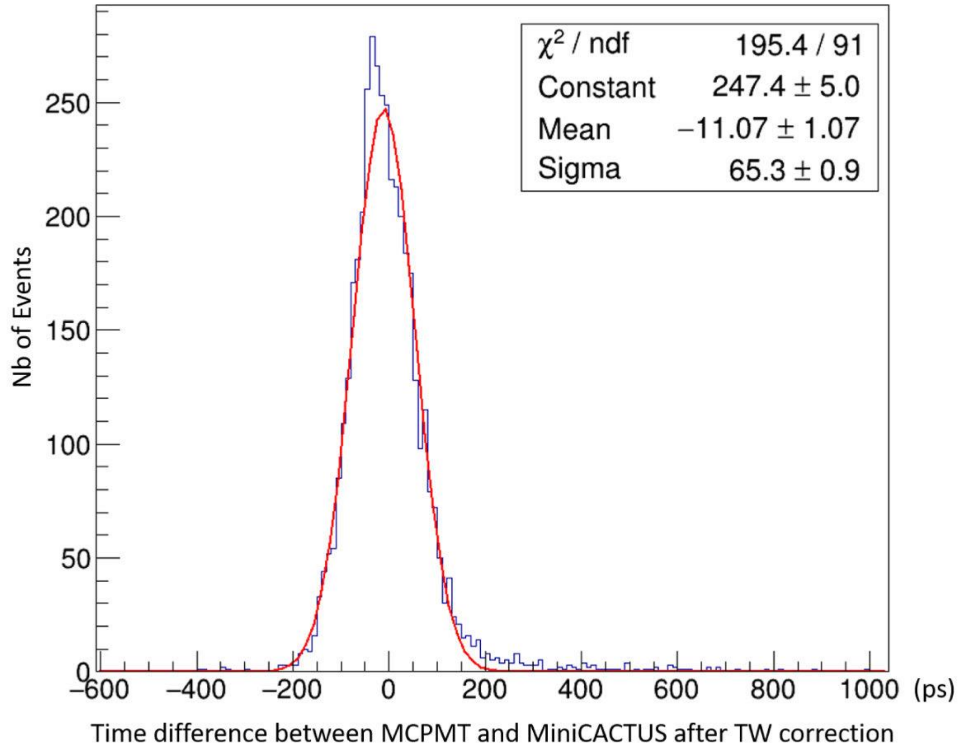


Layout of MiniCACTUS chip

*CMOS **AC**tive**T**iming **µS**ensor

Mini-CACTUS performance in test beam with MIPs at CERN SPS

- A **time resolution of 65.3 ps** has been measured with 0.5 x 1.0 mm pixels biased at −500 V with muons. The measurement includes already the on-chip FE and discriminator.
- This time resolution has been measured consistently **over several test beam campaigns and with several sensors**.
- The **power consumption is 300mW/cm²**, which is compatible with the requirements of large high-energy physics collider experiments.
- This prototype is an important step toward a fully monolithic large size sensor.



185 µm-thick sensor (active part thicknesses)

Y. Degerli et al. IEEE Transactions on Nuclear Science, vol. 70, no. 11, pp. 2471-2478, Nov. 2023, doi: 10.1109/TNS.2023.3325947.

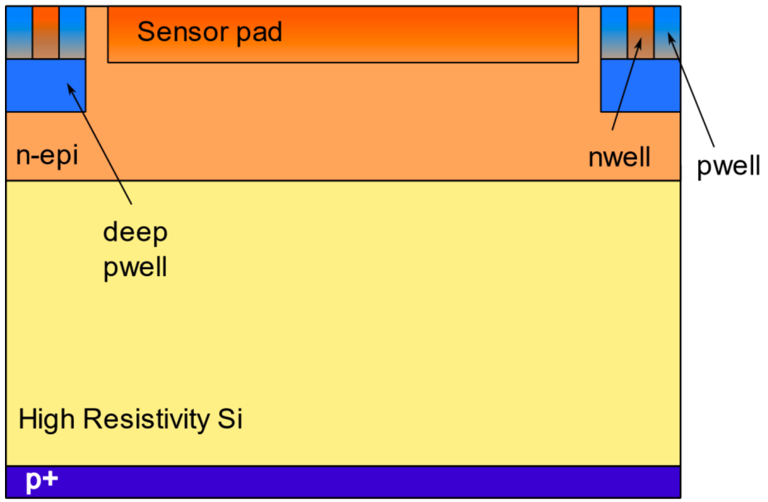
LFoundry 150 nm CMOS process

DEPLETED MAPS 110nm: ARCADIA

110 nm Technology, 6 metal layers developed between INFN and LFoundry

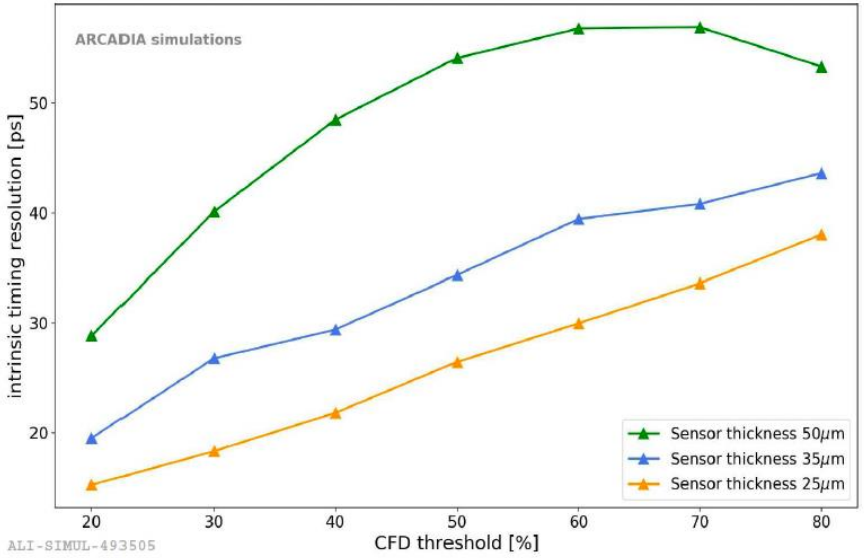
- 3D simulations necessary to quantify accurately the effect of weighting field non-uniformity at the borders
- Electric Field and Weighting Potential evaluated with TCAD simulations
- Intrinsic timing resolution with MIPs evaluated with AllPix2 on a 3x3 pixel domain

ARCADIA pad sensor



L. Pancheri 2022

50 μm pitch, Vnwell=3.3 V, Vback = Vpw @ 10 mW/cm^2
Epitaxial layer thickness 8 μm



Intrinsic timing resolution: $\sigma_{\text{distortion}}$ and $\sigma_{\text{Landau noise}}$

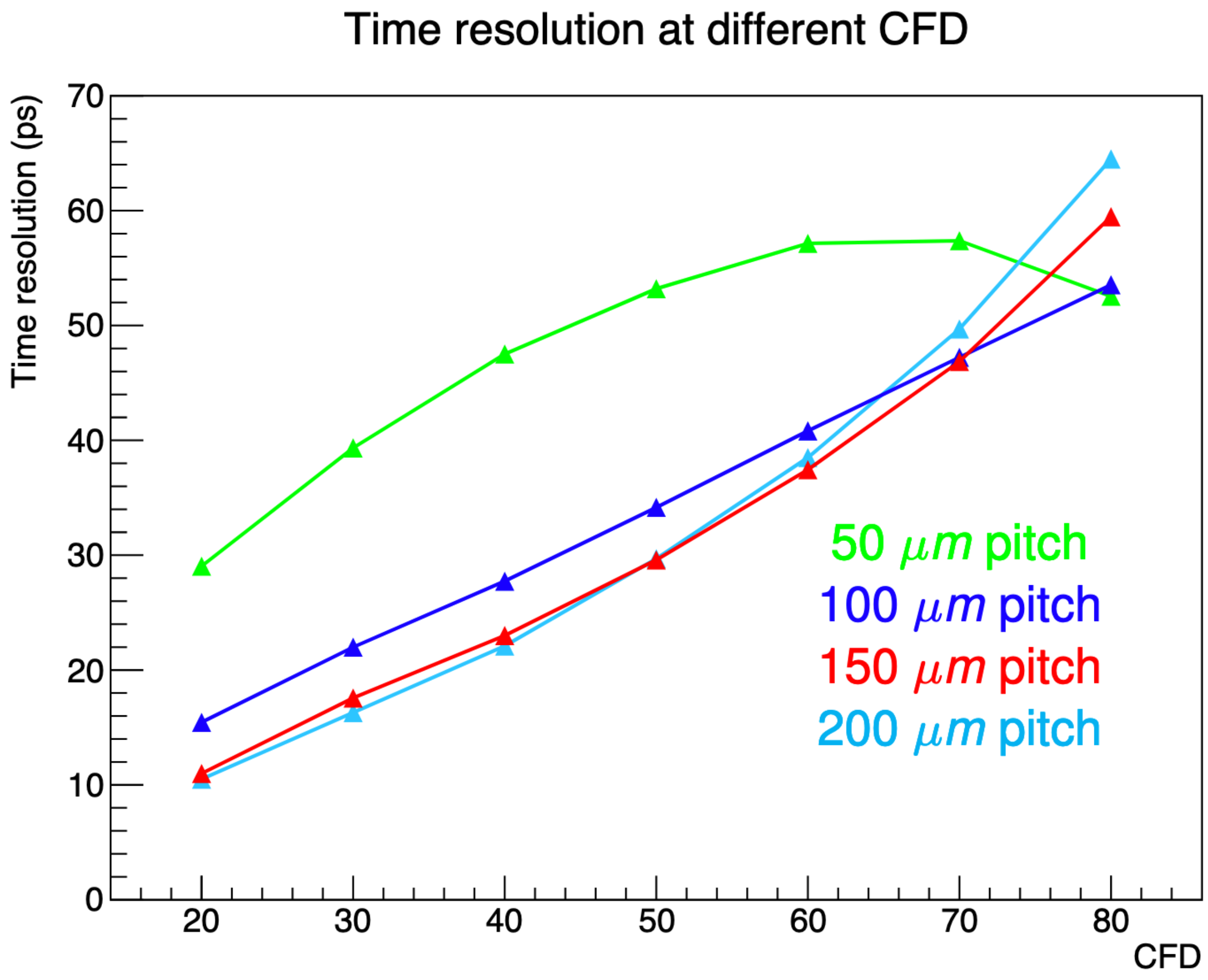
→ Resolution is **20÷30 ps** for the **50 μm pitch**

↳ **Larger PAD sizes** allow for a better field uniformity
And better area Efficiency!

→ **Thinner sensors** have a better time resolution
Still, less charge is generated
→ **Increase in the electronics jitter**

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 67, NO. 6, JUNE 2020

DEPLETED MAPS 110nm: ARCADIA



Thickness: 50μm

Increasing the pixel pitch for a better time resolution

- 150 μm and 200 μm pixel pitches show very close time resolution values

• Add a gain layer to reach 20ps?

follow Umberto Follo's talk on Thursday!!

Conclusions

- Many encouraging results for different developments on MAPS:
  - excellent detection efficiency
  - high spacial and timing resolution

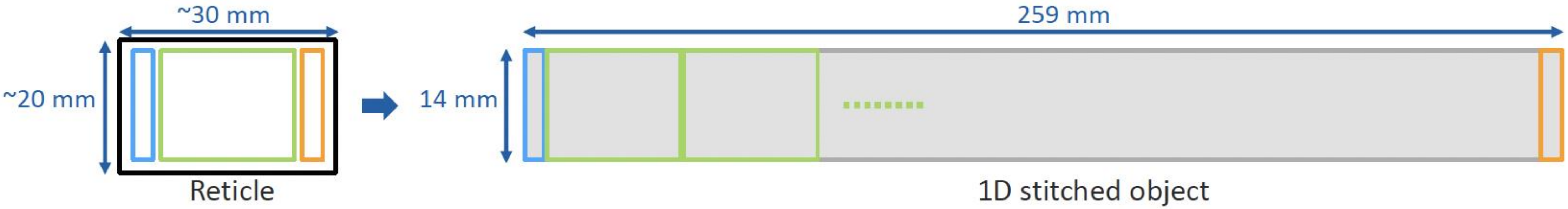
- MAPS represent a very attractive solution for very large area 4D tracking or Time of Flight detector systems

- we have a very exciting though challenging path ahead of us!!!

Back up

Wafer scale stitched sensors

- 1D stitching



- 2D stitching