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Tests and Characterization of ASTRA-64 ASIC for Silicon Micro-Strip Detectors Read-Out

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ASTRA-64 (Adaptable Silicon sTrip Read-out ASIC) is a 64-channel mixed-signal custom IC designed for micro-strip silicon sensors read-out. Manufactured in a 110-nm technology node, it comprises two identical mirrored subcircuits, each accommodating 32 channels.

Recursively, each channel integrates two main blocks: a charge-sensitive amplifier and a shaper. The former features two programmable gain settings suitable for positive and negative input polarities, whereas the latter provides four adjustable peaking time. The overall gain is calibrated to provide linear charge measurements of up to 160 fC and 80 fC –depending on the amplifier settings –optimizing the noise performance based on the detector capacitance.

ASTRA-64 offers two distinct read-out modes. In the analog one, sampled voltages are sent off-chip via an analog multiplexer linked with a differential output buffer. Conversely, the digital read-out mode employs a Wilkinson ADC for each channel to digitize voltage and a shared serializer to transmit data via an SLVS driver. Additionally, ASTRA-64 embeds a fast shaper and a leading-edge hysteresis discriminator per channel to produce rapid trigger signals. A FAST-OR logic merges these signals to provide a single off-chip trigger.

The IC first application is the Silicon Charge Detector of the HERD experiment –slated for installation aboard the Chinese space station in 2027 –to implement tracking and supplementary charge measurements. The space application adds the necessity to comply to its stringent requirements, primarily with a power-dissipation limit of 600 μ W per channel.

In this work we will present the tests, characterization, and performance of ASTRA-64, mainly focusing on its charge linear input range and resolution.

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