INFN Perugia

Tests and Characterization of ASTRA-64 ASIC for Silicon Micro-Strip Detectors Read-Out

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Silicon Micro-Strip Detectors @ PG

- We extensively use μStrip detectors
  - Charge measurements
  - Position measurements

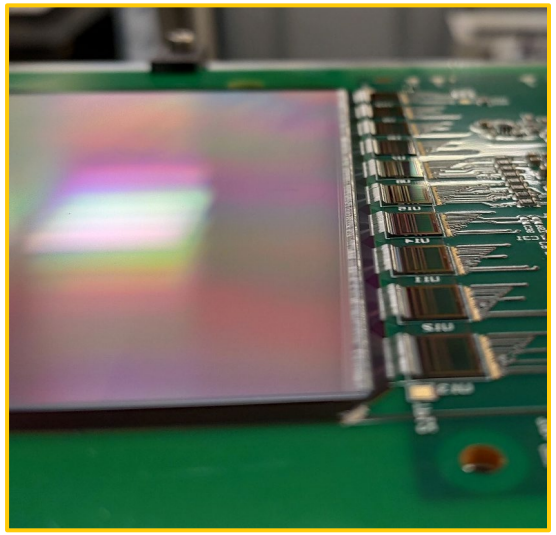
- Mainly because they
  - Cover large areas with relatively low power consumption
    - *e.g.,* AMS: 6.5 m^2, 155 W
  - Add few material in the particles path
    - *e.g.,* FOOT: 150 μm per layer

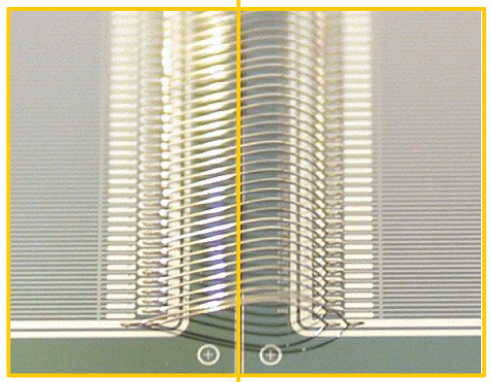
- PLUS: Already tested and used in space and radioactive environments

Silicon μStrip Detectors @ PG

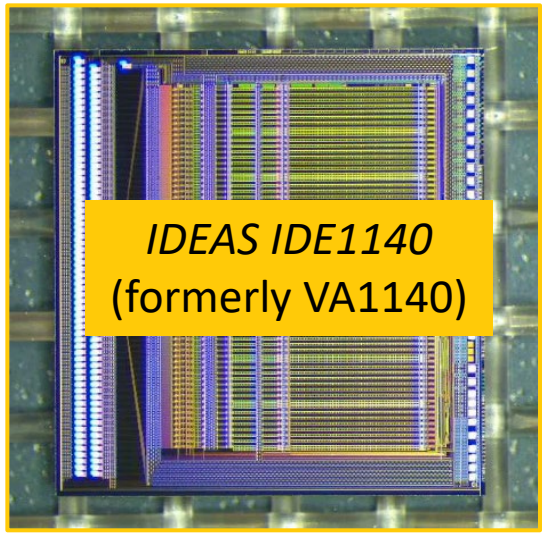
Three main components

Silicon sensors

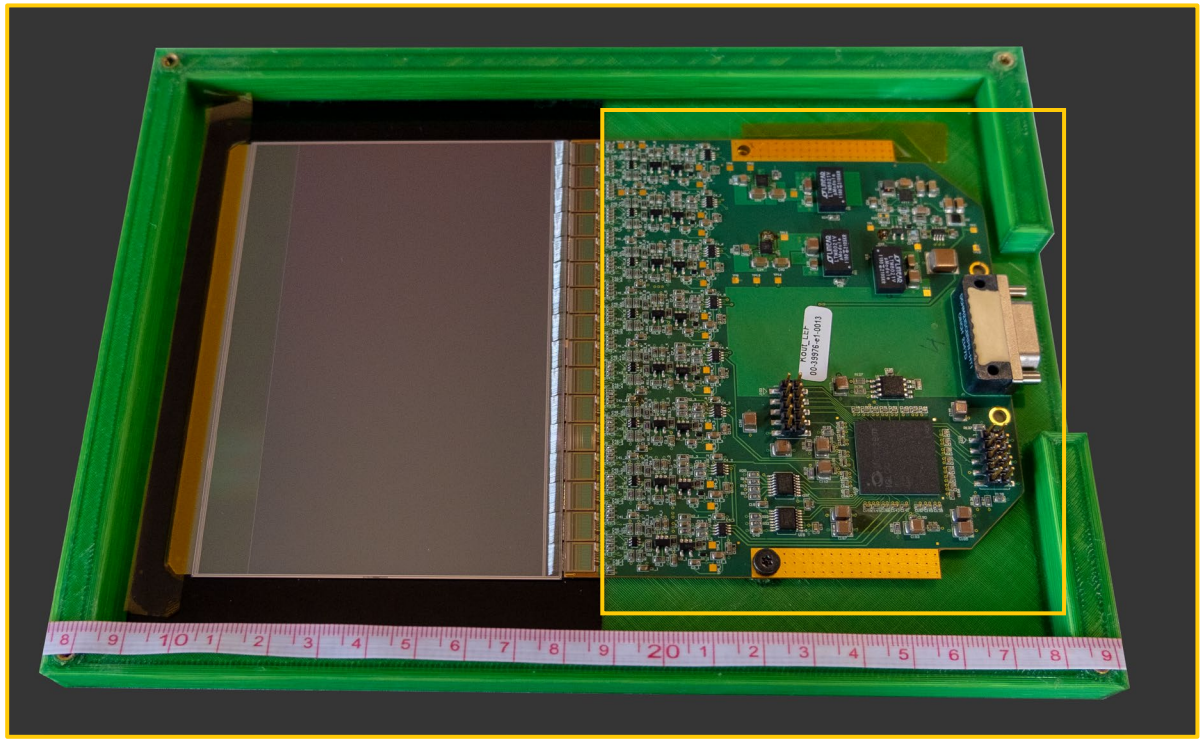


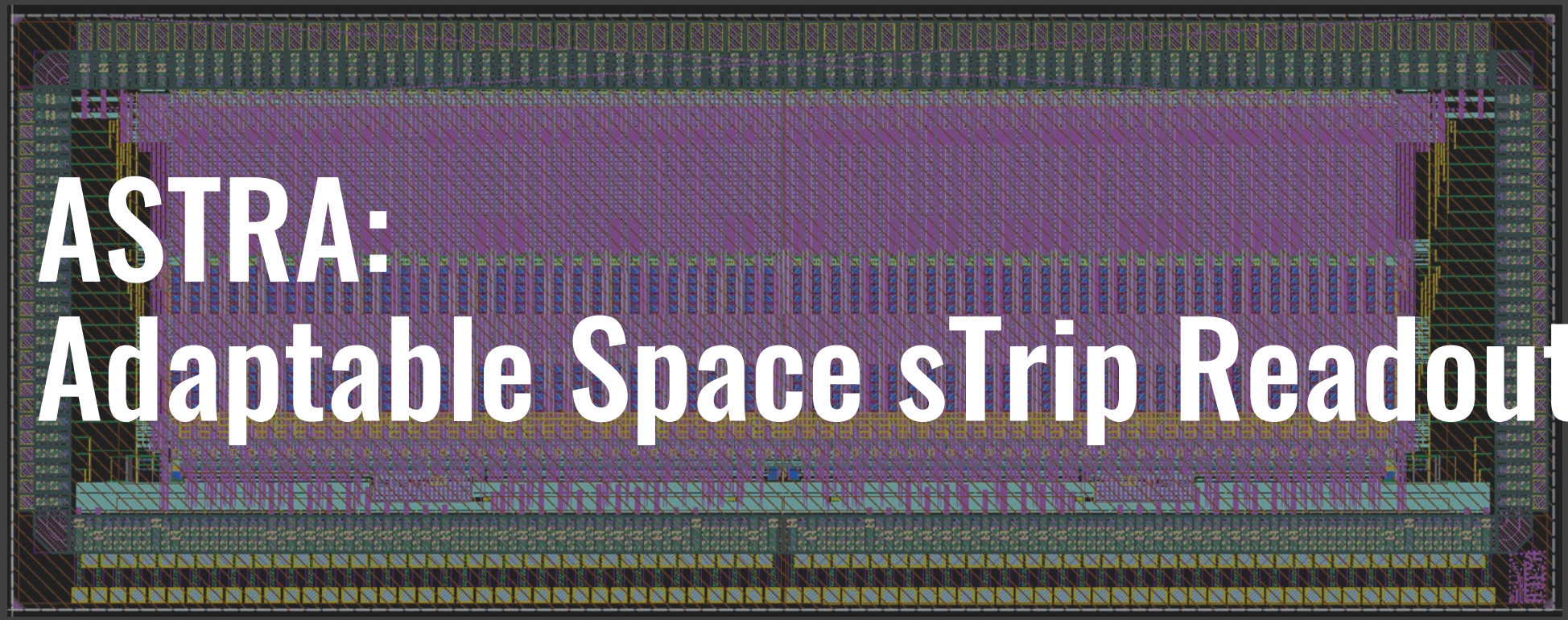


Readout ASICs



ADCs and DAQ system





ASTRA: Adaptable Space sTrip Readout ASIC

Designed by INFN Torino

- Electronics for the read-out 110-μm-pitch silicon μStrip Detectors
- Electronics + Sensor Monolithic ASIC

ASTRA Requirements

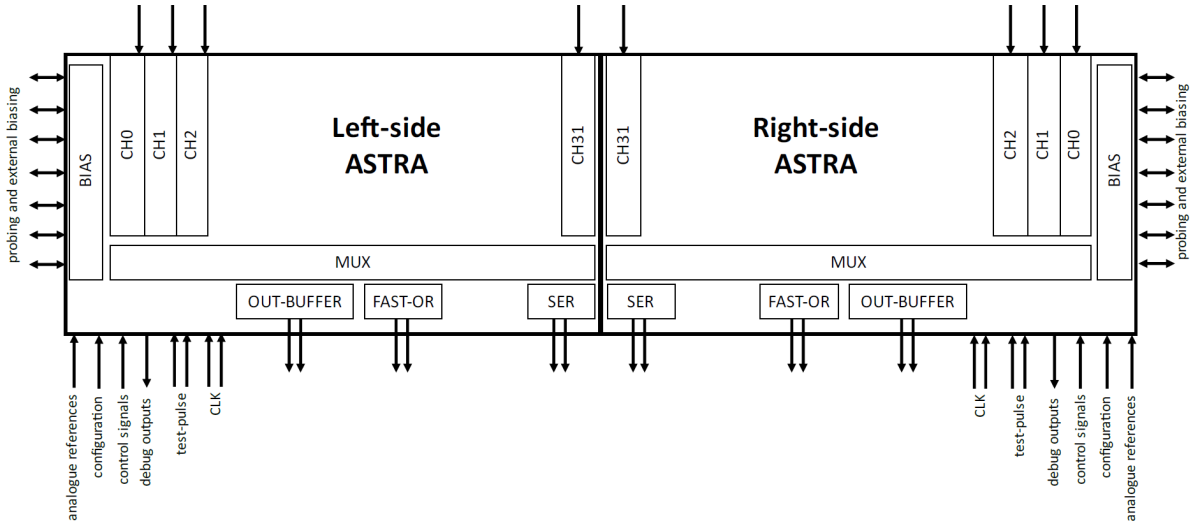
	ASTRA Requirements
Channels	64
Dynamic Range	± 160 fC
Linearity Region	± 160 fC
Shaping Time	Adjustable in 1÷10 μs
ENC	< 1000 e^- @ C_{in} 100 pF
Output	Multiplexed pulse height Digitized pulse height Channels FastOR
Power supply	Positive (only) supply
Channel power consumption	< 1 mW per channel
Production Process	110 nm CMOS
Size	6x6 mm^2

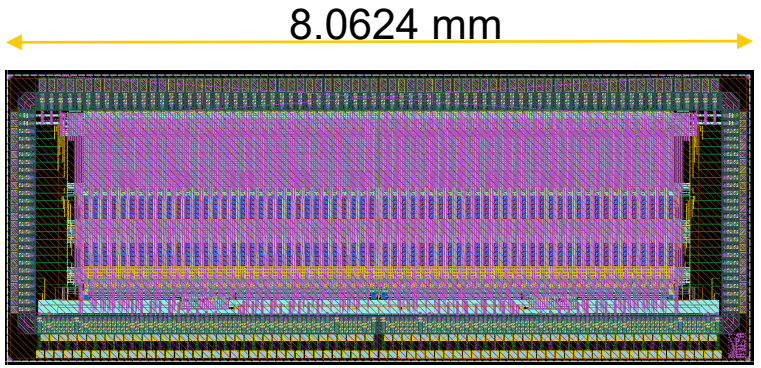
- Requirements tailored to HERD Silicon Charge Detector (SCD)
- Produced at LFoundry
  - Only HVT transistors (1.2 V) available

ASTRA: Adaptable Space sTrip Readout ASIC

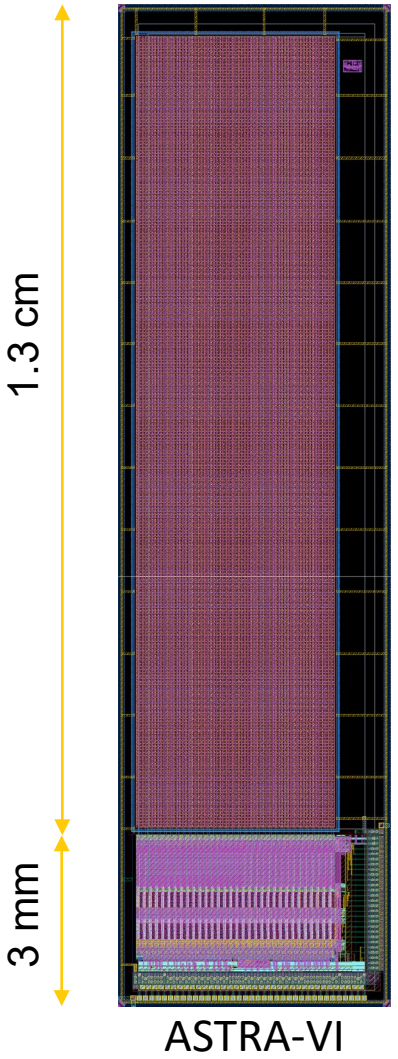
- First prototype in the framework of the INFN project ARCADIA
  - 64 channel read-out: ASTRA64
  - 32-strips fully-depleted monolithic active CMOS microstrip sensor: ASTRA-VI

- The two versions share the same electronics
  - configurable Gain
  - configurable Peaking Time
  - configurable Readout mode (analog or digital)





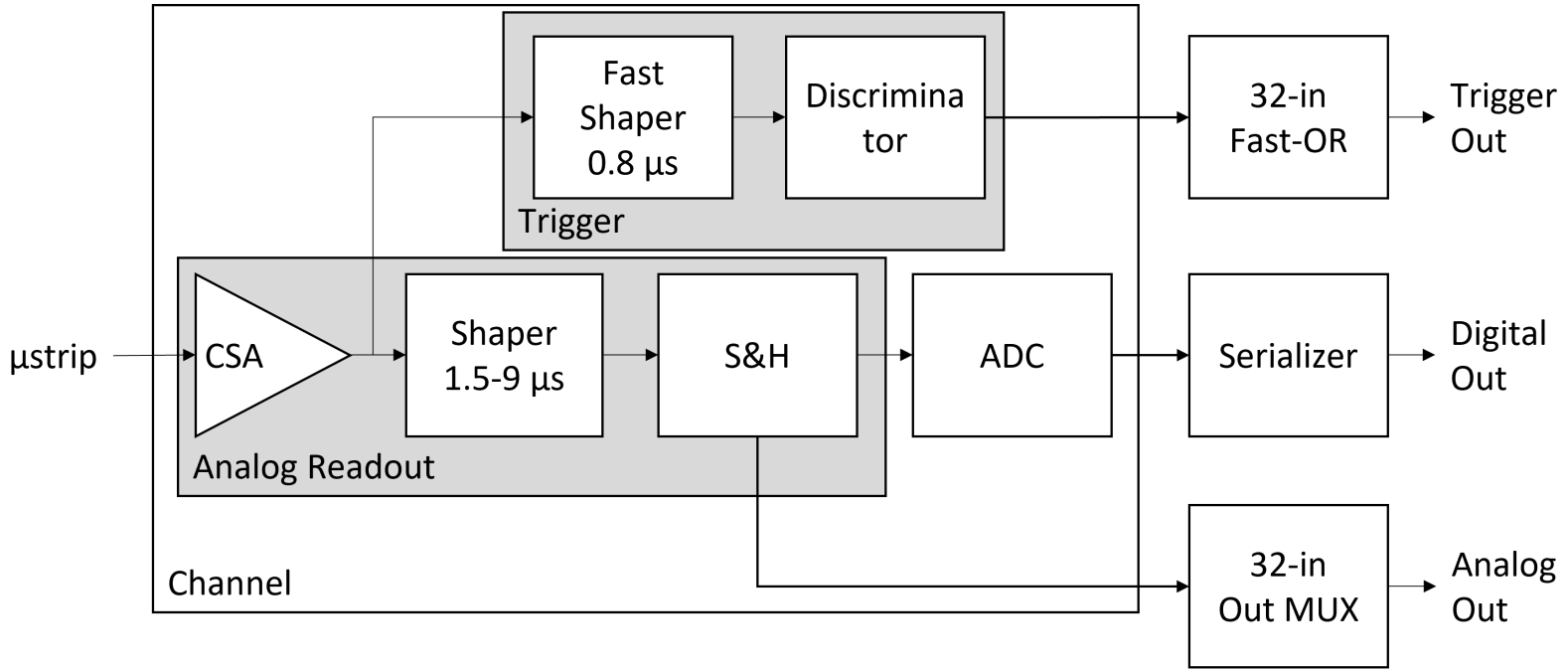
ASTRA64



ASTRA-VI

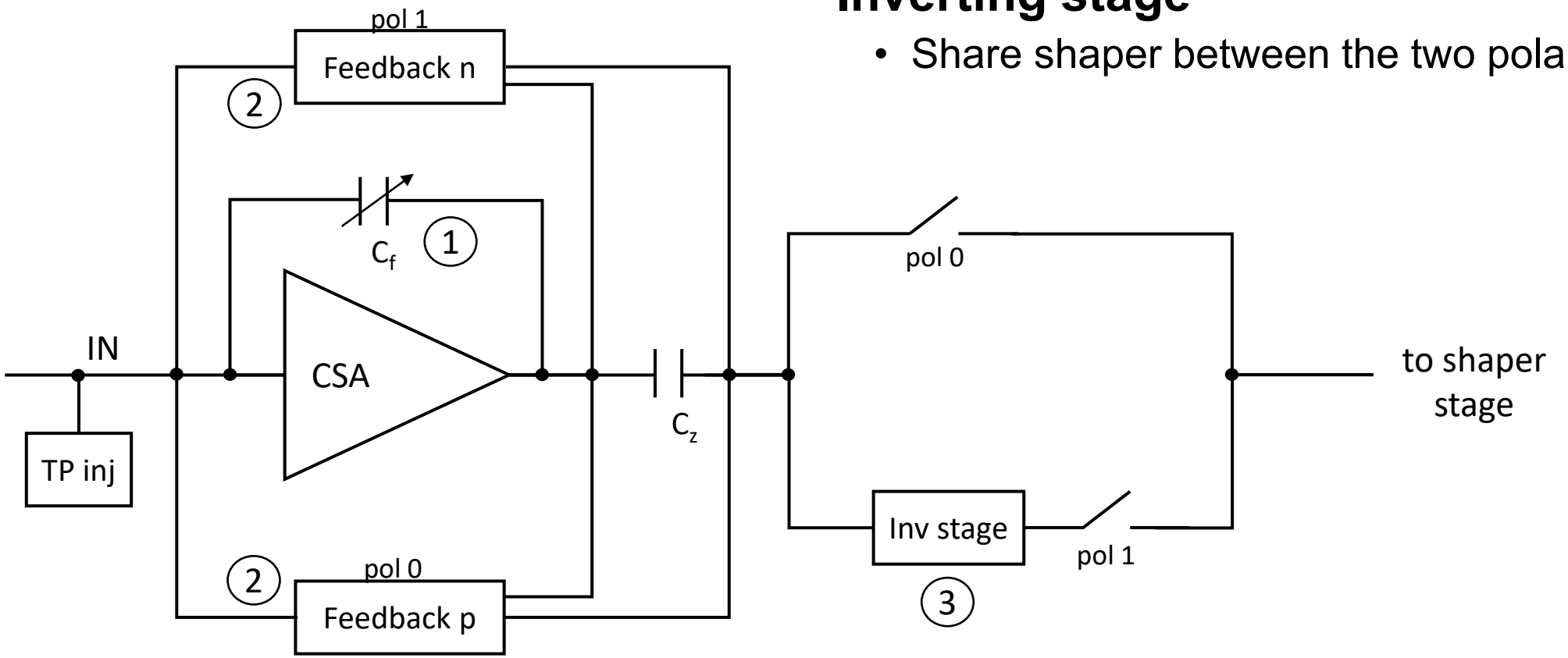
ASTRA Architecture

- **PreAmp**
  - Charge Sensitive Amplifier
  - Test-pulse injection circuit
- **Slow Shaper**
  - Charge measurement
  - Externally-controlled S&H circuitry
- **Analogue readout**
  - MUX-differential output buffer
- **Digital readout**
  - Wilkinson ADC and serializer
- **Fast Shaper**
  - Trigger output
  - Fast-OR output

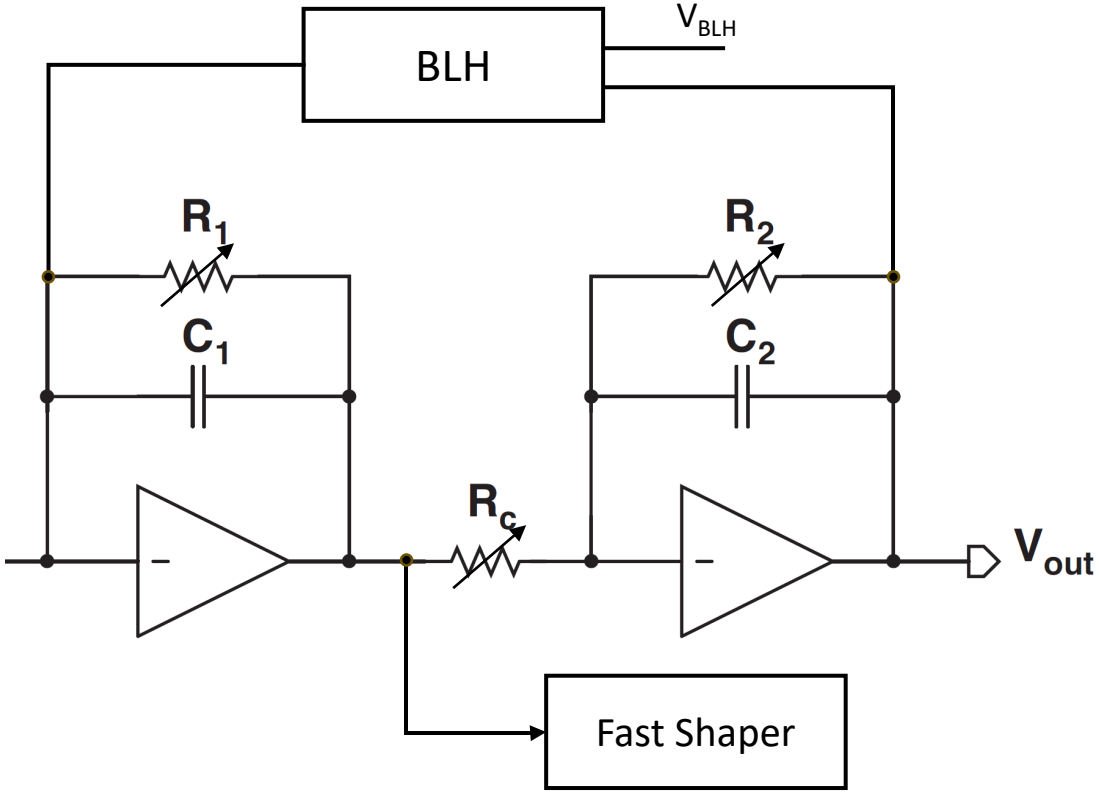


Preamplifier Stage

- **CSA**
  - Both input polarities
  - Two programmable gain configurations
    - 4.2 mV/fC, 7.6 mV/fC
- **Gm feedback** implemented with current mirrors
  - Output charge amplification with pole-zero cancellation
- **Inverting stage**
  - Share shaper between the two polarities



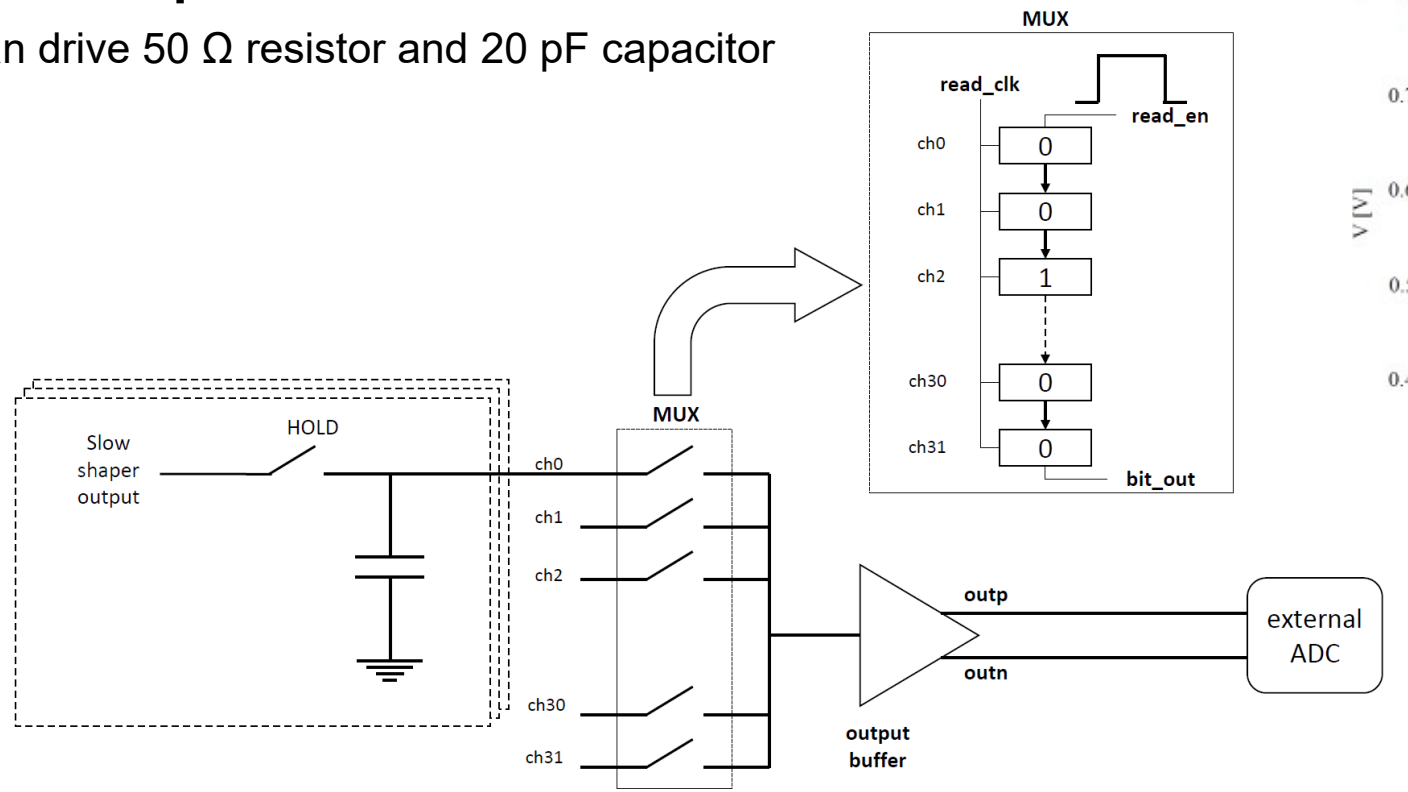
Shaper Stage

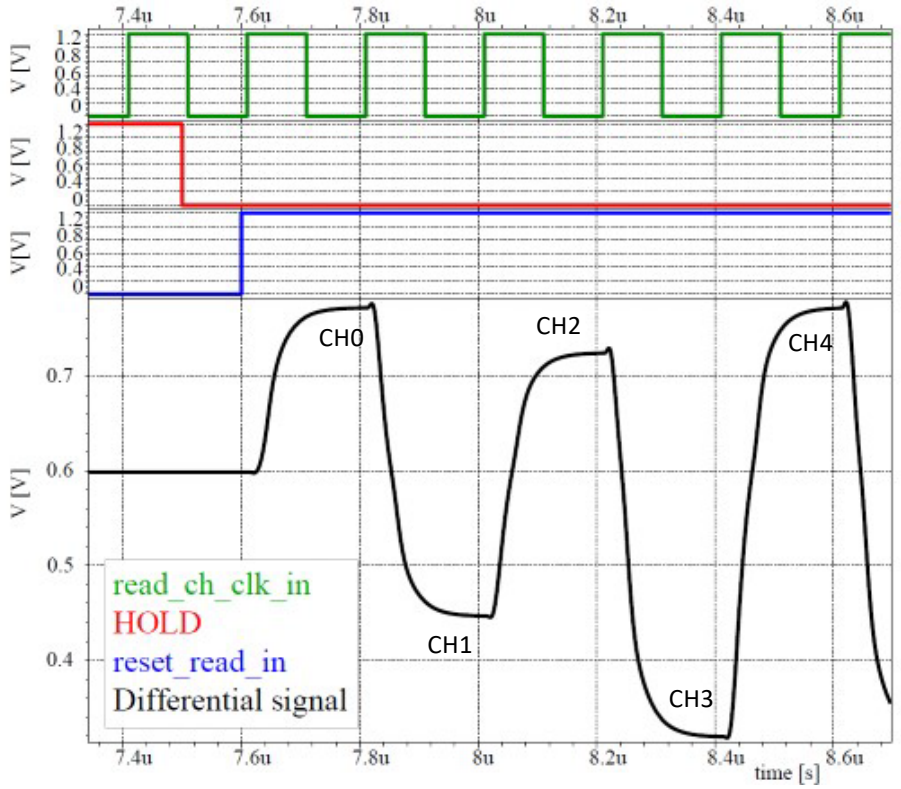


- CR-RC Shaper
- **Four** programmable **peaking time**
  - 1.5 µs, 3.5 µs, 6.5 µs, and 9 µs
- Shaper core amplifiers share CSA architecture
  - Down-scaled bias current and transistors size
- **Baseline holder** (BLH) circuit
  - Control Shaper DC output voltage
    - Nominal V_{BLH} = 870 mV

Analog Readout

- **External HOLD** signal
  - Store shaper output peak voltage for each channel
- **MUX** to send off-chip the sampled signals
  - Max. 5 MHz read-out clock
- Unity-gain single-ended to differential cascode amplifier
- Class-AB **output buffer**
  - Can drive 50 Ω resistor and 20 pF capacitor





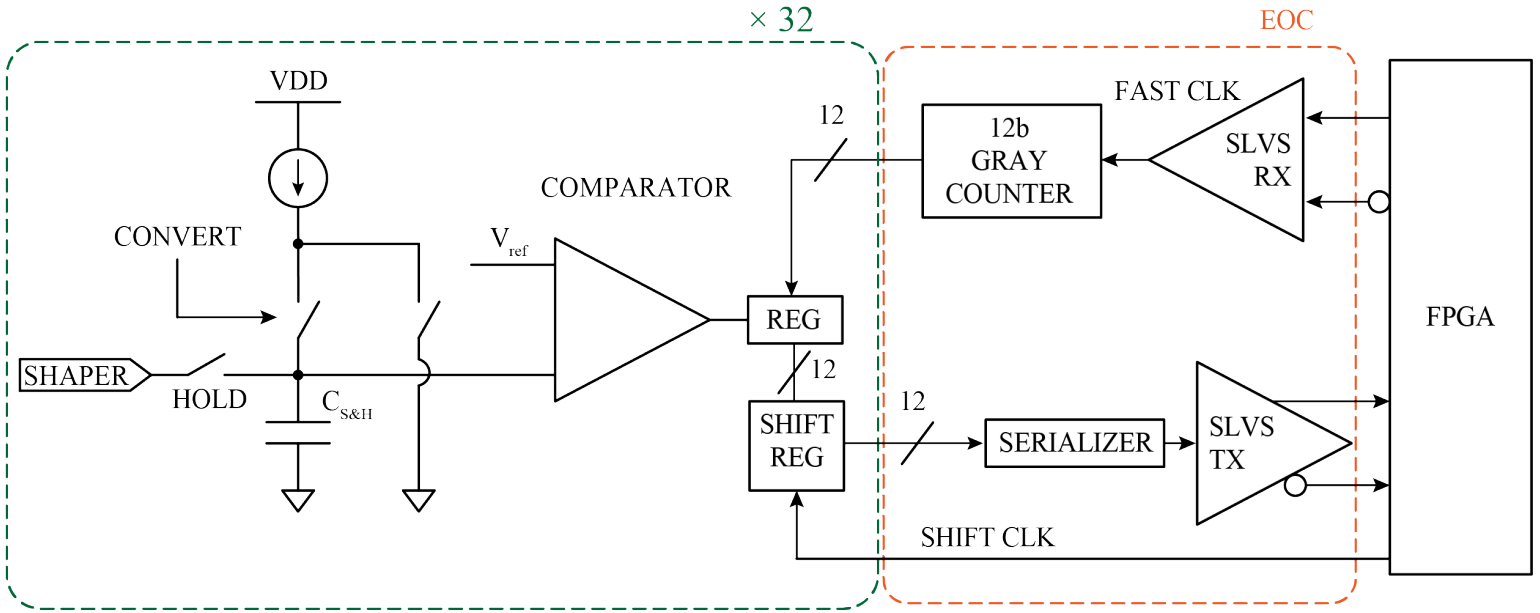
Digital Readout

- S&H signal digitized by on-channel **Wilkinson ADC**
  - Programmable recharge current
  - Output: **12-bit Gray counter** of the recharge time

- Single **Serializer** + SLVS TX link
  - Data output at Double-Data-Rate
    - t_s= 80 ns -> t_{ro}= 2.56 µs

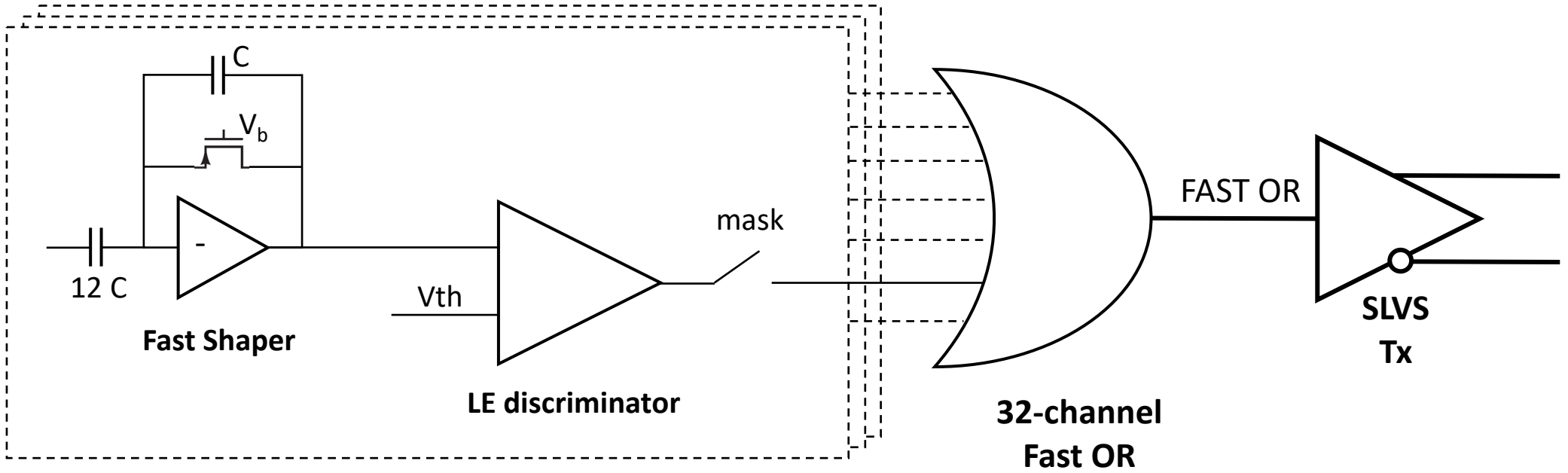
} 100 MHz clock

I_{ADC} [nA]	MAX recharge time [µs]	# BITs
70	2.7	8
35	5.4	9
17	11.1	10
9	20.9	11
4.5	41.9	12

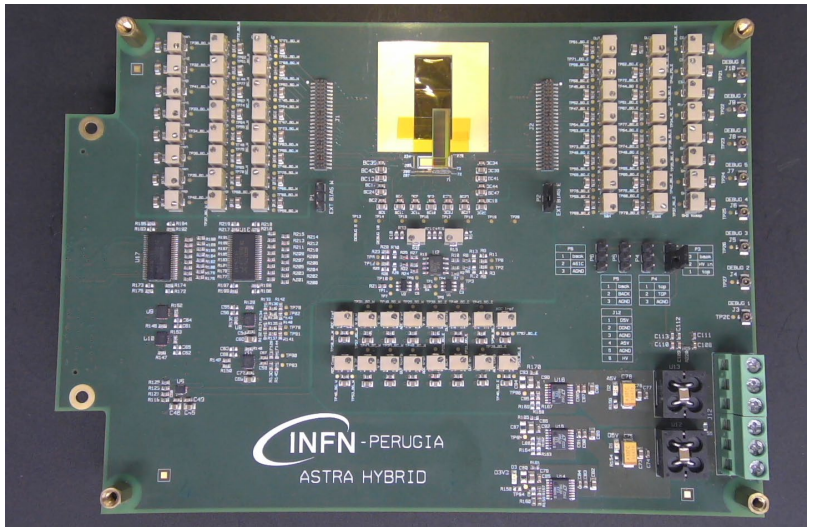


Fast Branch – Trigger Output

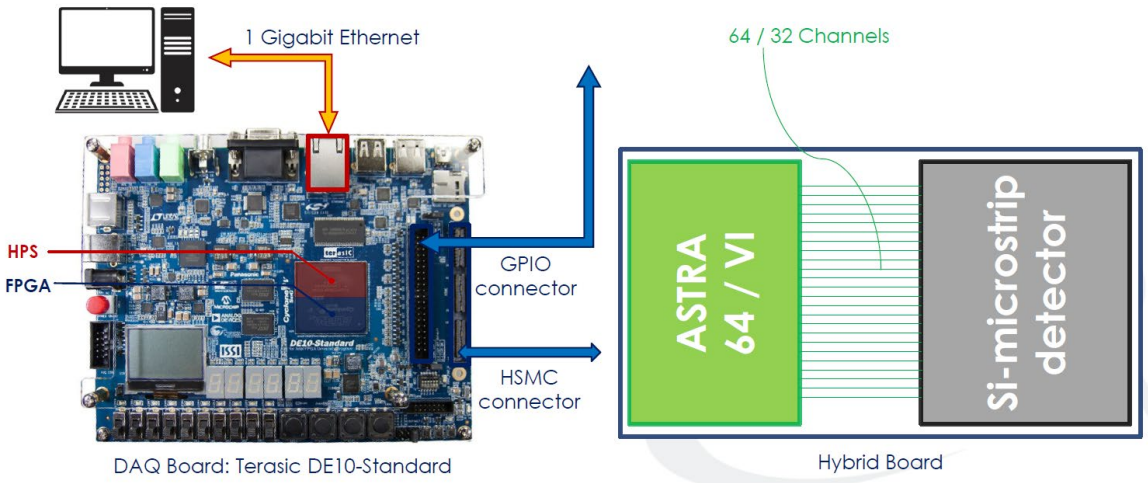
- **Fast shaper**
  - 800 ns peaking time, 25 mV/fC
- **LE discriminator** with hysteresis
  - V_{th} generated off-chip and common to all 32 channels
- **Fast OR** logic to generate trigger output
  - Each channel can be masked to remove noisy channels



ASTRA Test Board and DAQ



- ADCs for analog output digitization
- Analog/Digital Power Supplies
- Level shifters and SLVS converters
- Can accommodate both ASTRA-VI and ASTRA-64
- Trimmer resistors for external bias
- Sensor HV bias

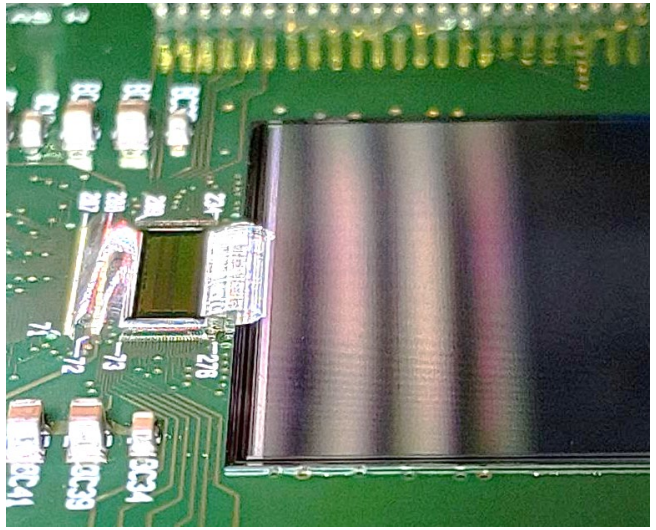


DAQ

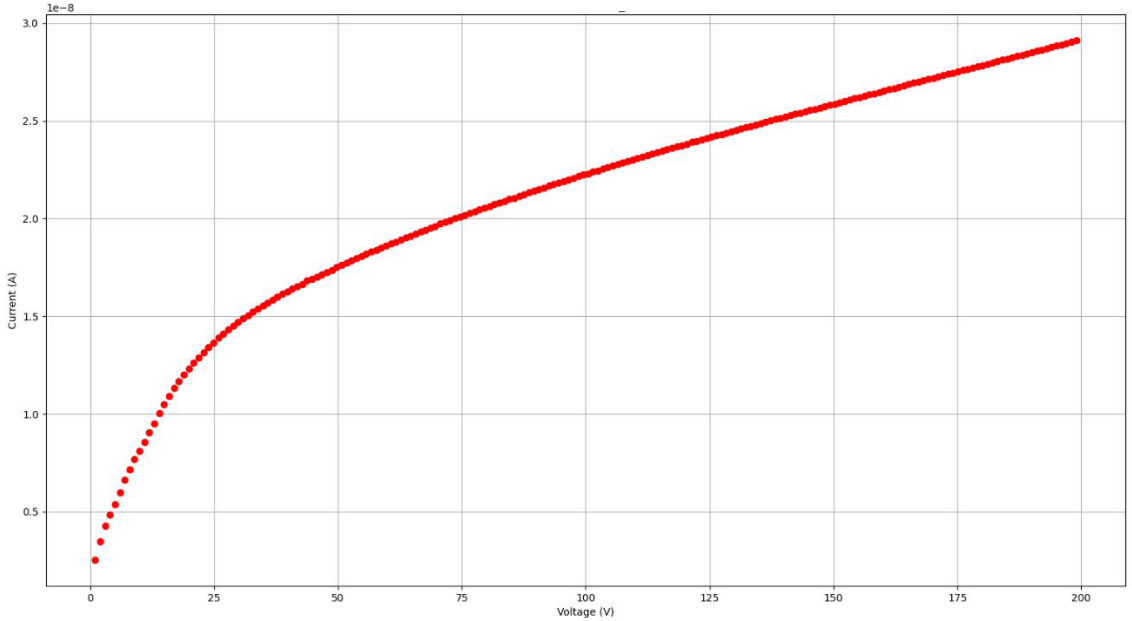
- ASTRA configuration, readout operations, and data acquisition
  - *Terasic DE10-Standard*
    - *Intel Cyclone V* FPGA

ASTRA Characterization

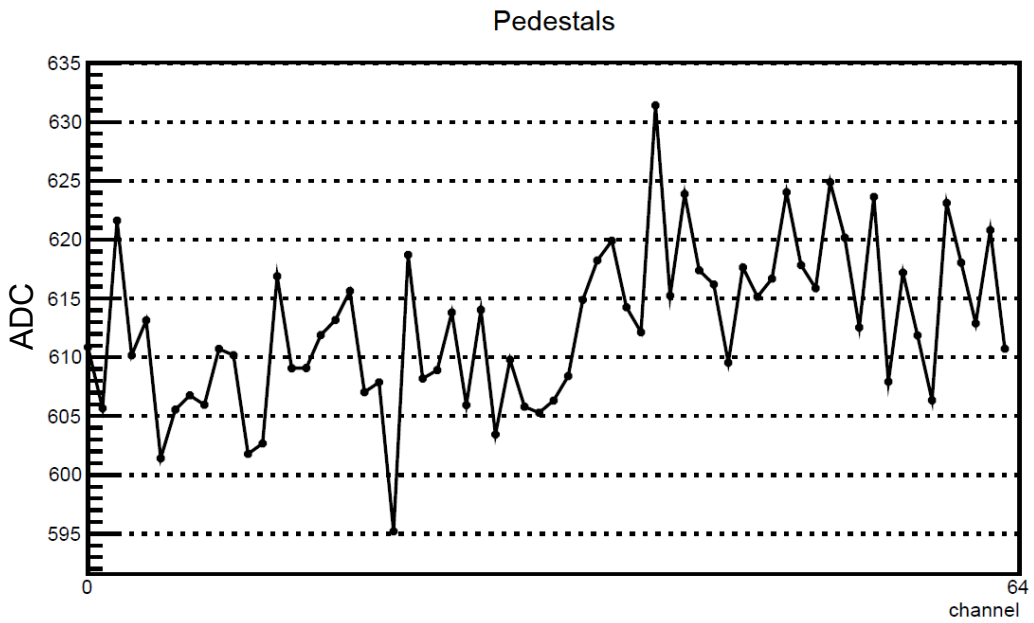
- Used the test board to characterize ASTRA-64
  - For the moment, we only verify the analog read-out

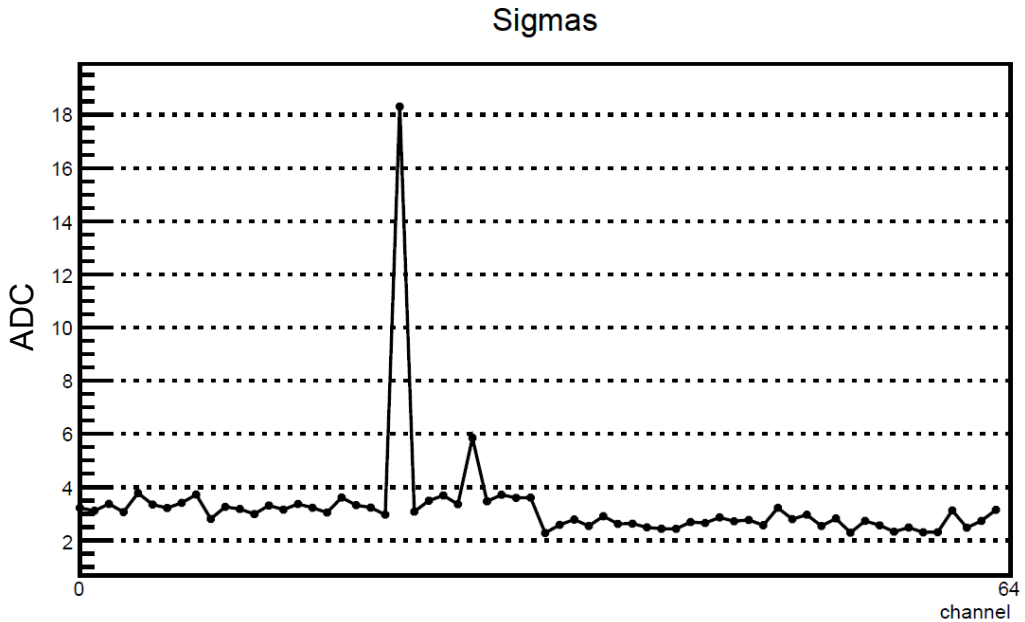


- Verification campaign to test all the functionalities
  - FOOT sensors
    - 3x3 mm^2
    - 50 μm implantation pitch
    - 150 μ m readout pitch
  - Integrated test-pulse injection
  - 1058-nm laser



ASTRA Characterization: External ADC Calibration

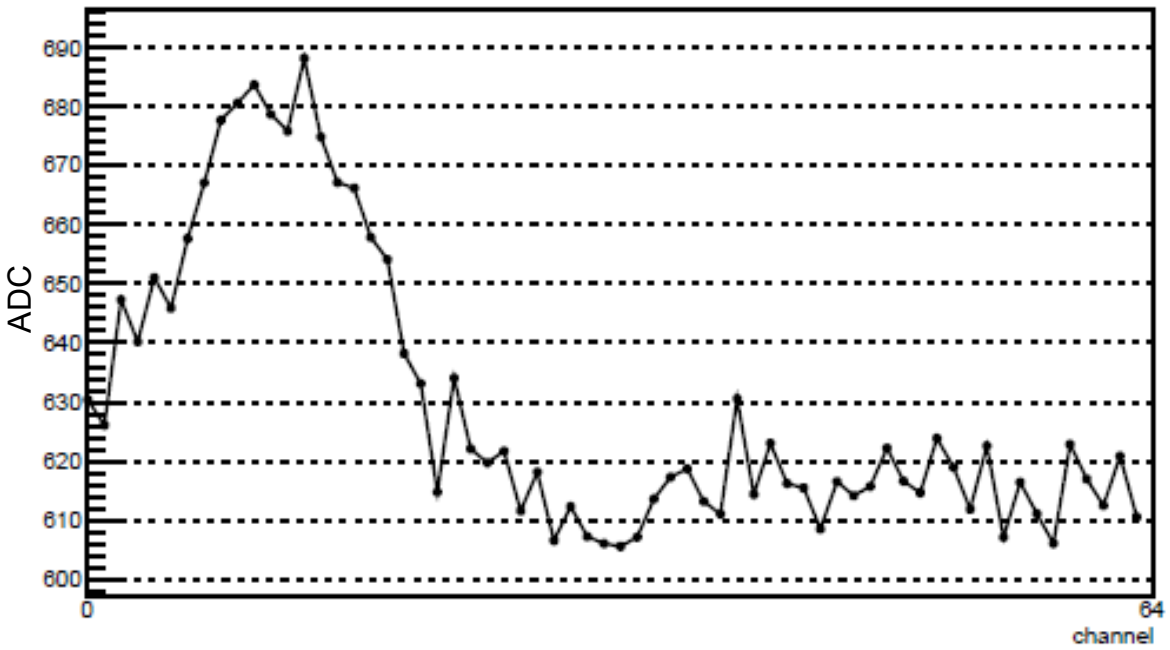


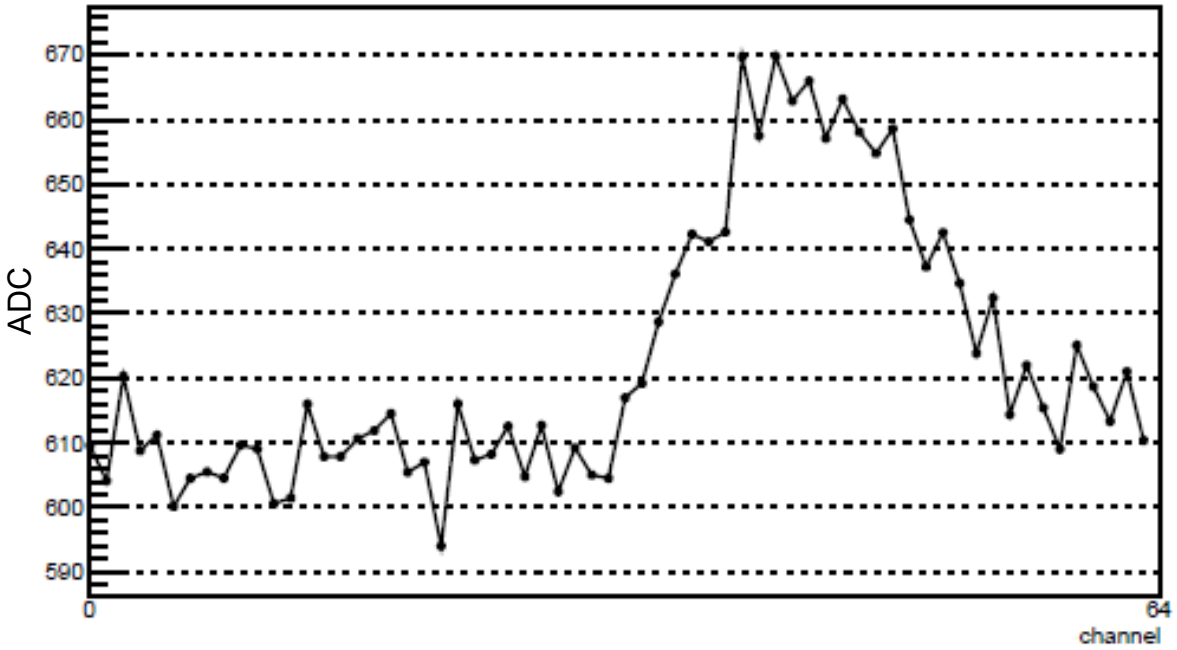


- Tested ASTRA analog output
  - Pedestal: base-line of the strips without crossing particles (average value)

- Same noise figures as in FOOT / POX / HERD hybrid boards

ASTRA Characterization: External ADC Laser



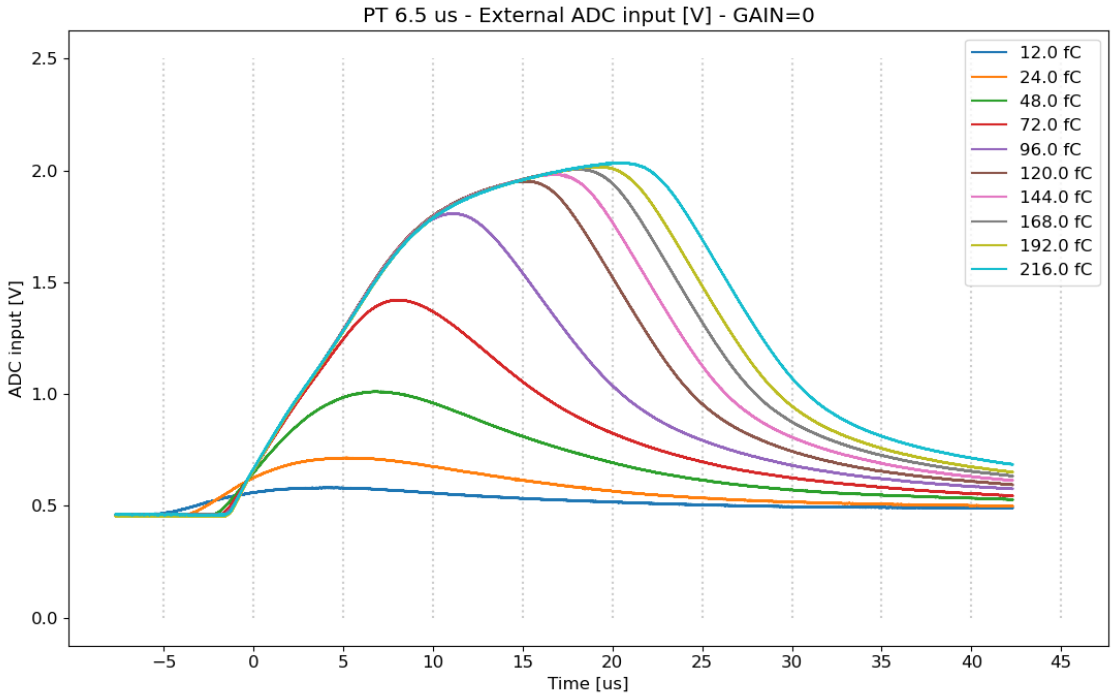


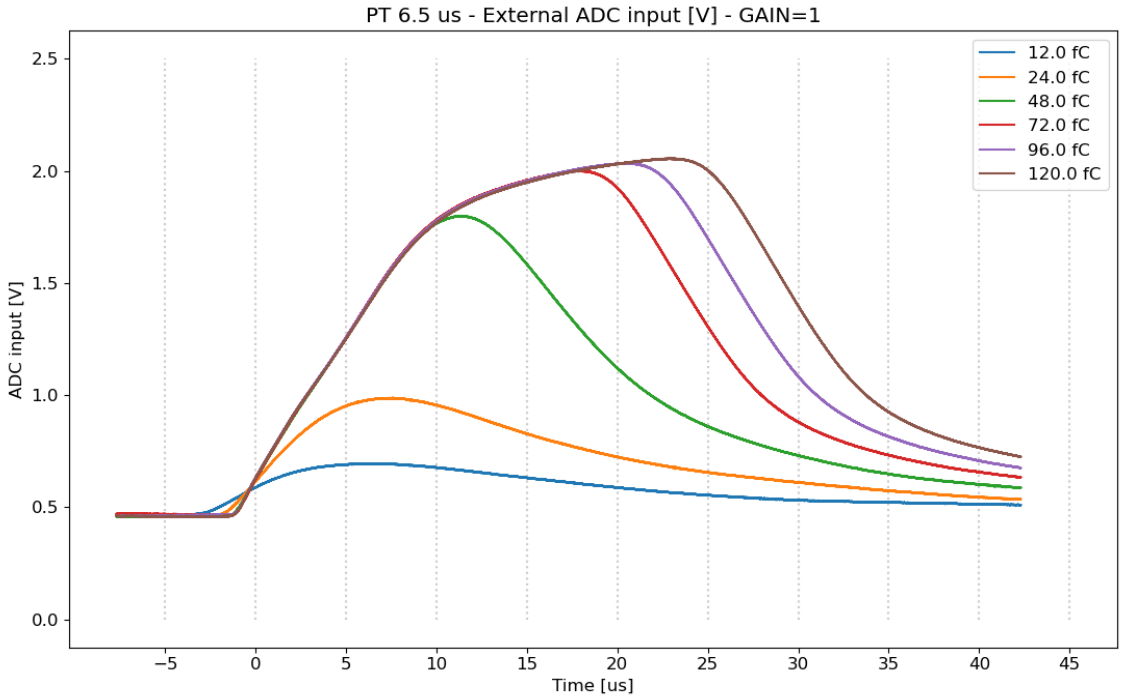
- Illuminated the sensor with 1058-nm laser
- Verified that both ASTRA-64 halves were receptive
  - Laser can only induce big signals onto the detector

ASTRA Characterization: Front-End Response

- Freeze one channel in output and send *integrated* test pulses
  - Shaping time 6.5 µs
  - Conversion from V_{tp} to Q_{inj}
    - C_{inj} = 240 fF

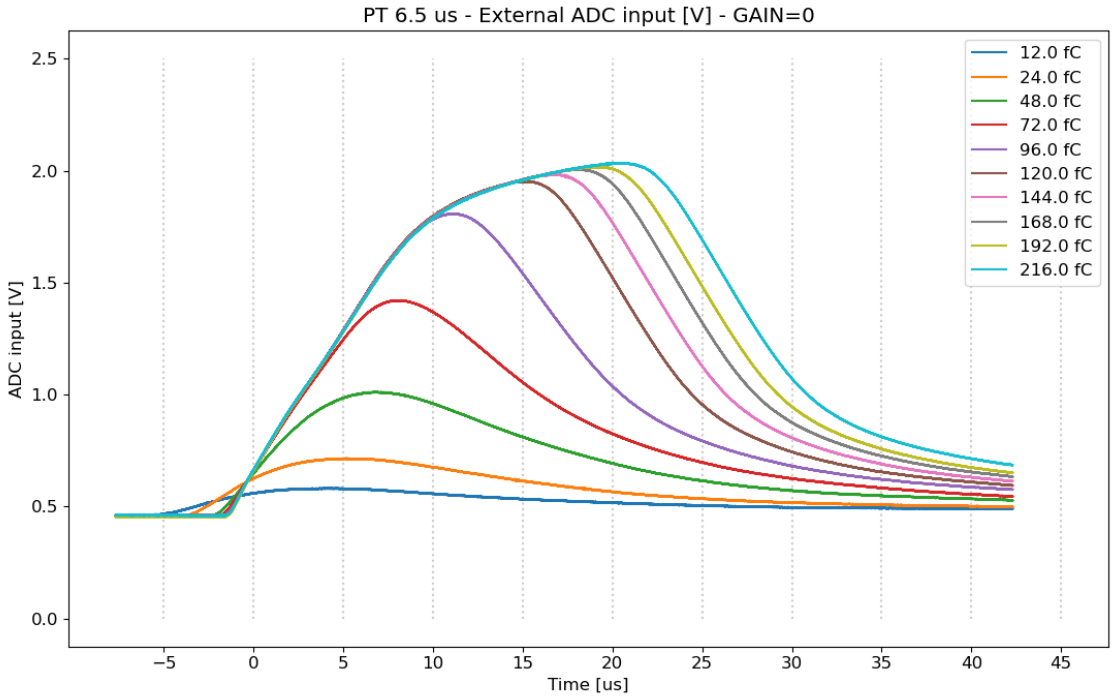
- Measure and validate
  - Pedestals
  - Max/min value
  - Noise
  - Gain
  - …

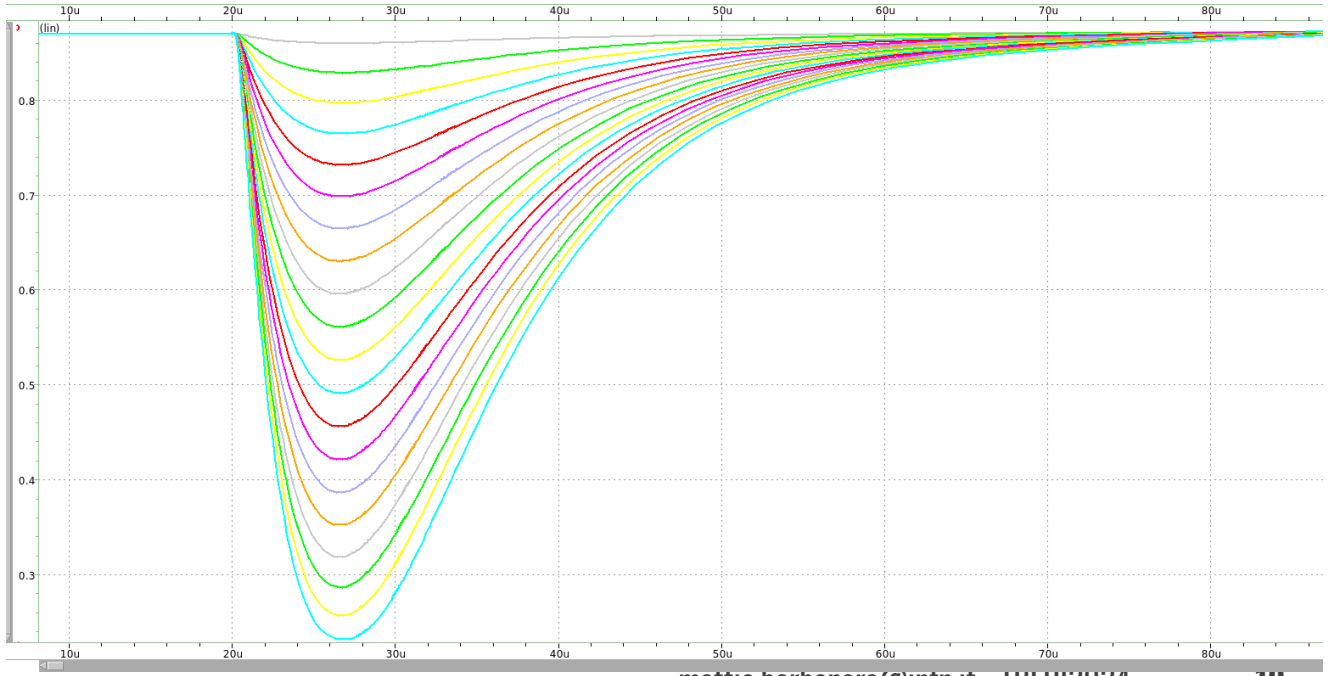




ASTRA Characterization: Test-Pulse Injection

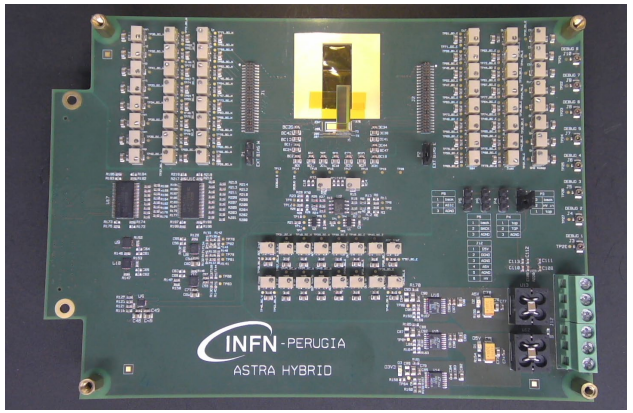
- Full chain shows two main issues regarding the external ADC input:
  - Does not cover its full input dynamic range (0 – 3.3 V)
  - Saturation of the signal
    - Resulting in a double slope of the gain
- To separate the response of the CSA+Shaper from the output buffer
  - Observe the debug output
  - Direct output of the shaper for some of the channels

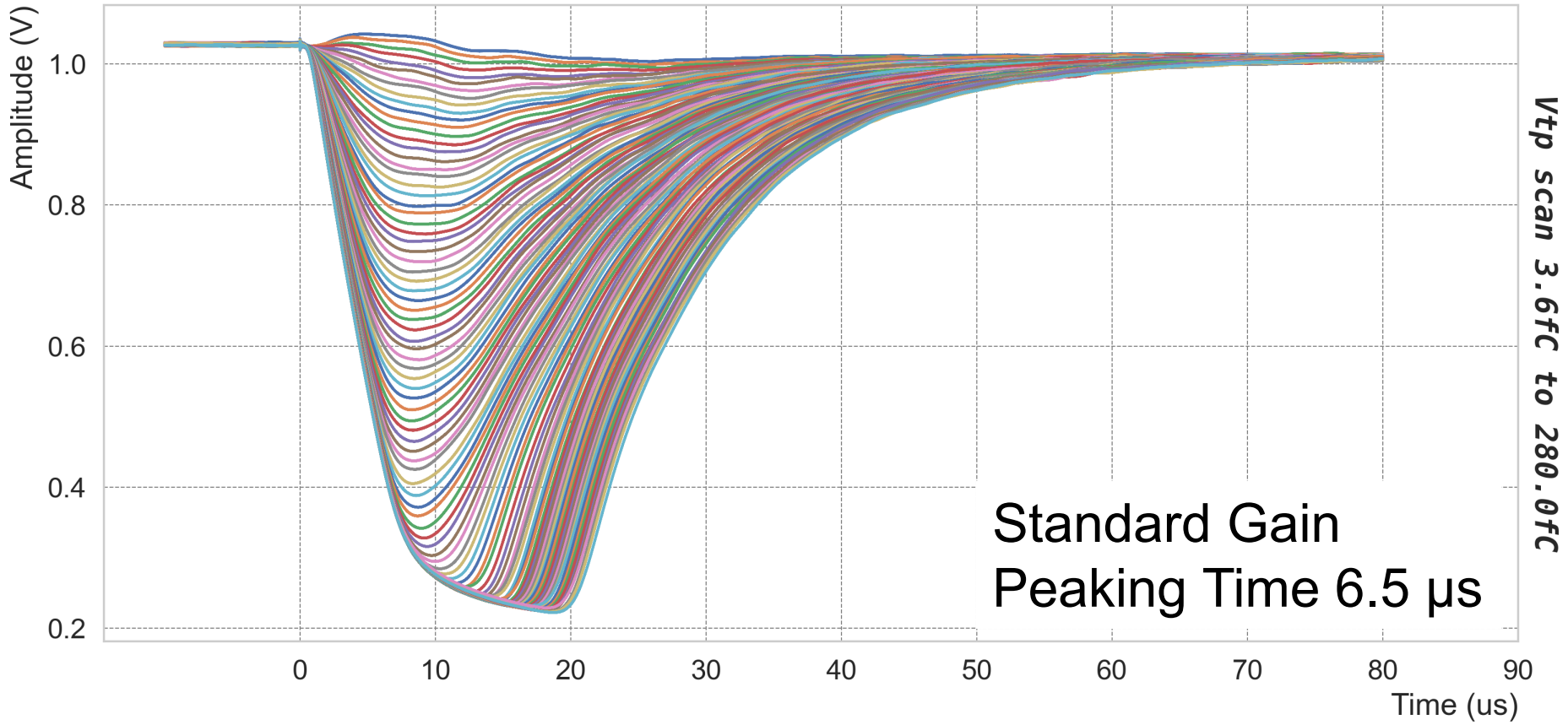




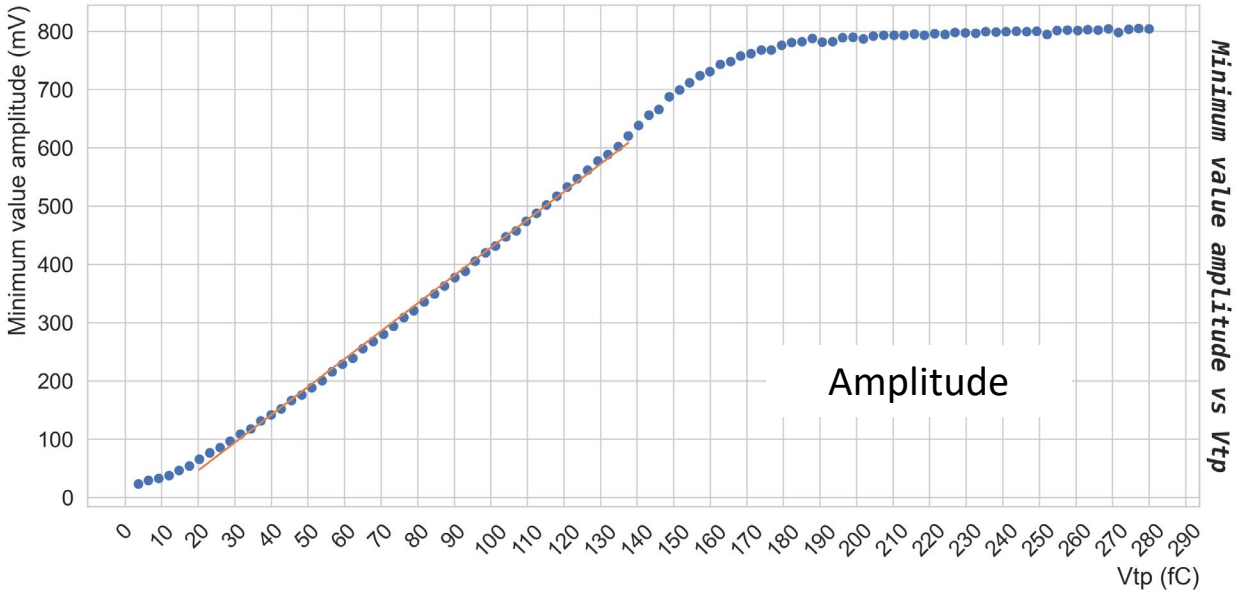
Measures: CSA + Shaper Output

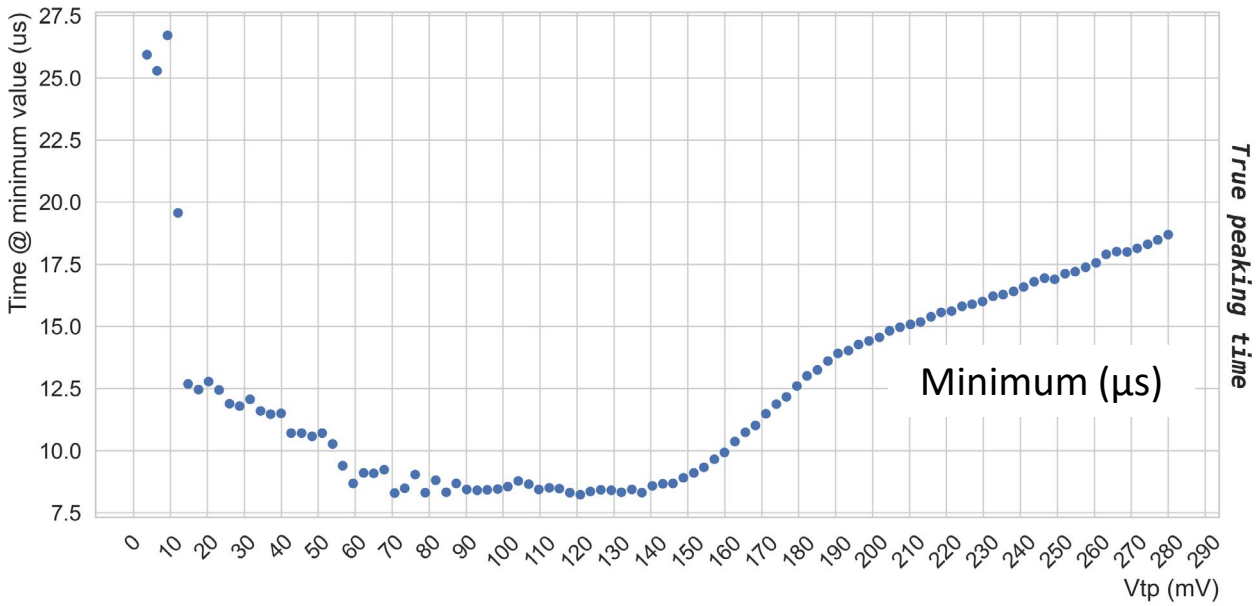
- V_{tp} scan by varying combinations of the parameters
  - Gain: Standard / High
  - Peaking Time: 3.5 µs, 6.5 µs, 9 µs
- V_{BLH} set to the maximum possible value (~1.1 V)
  - Saturation occurring at higher input charges

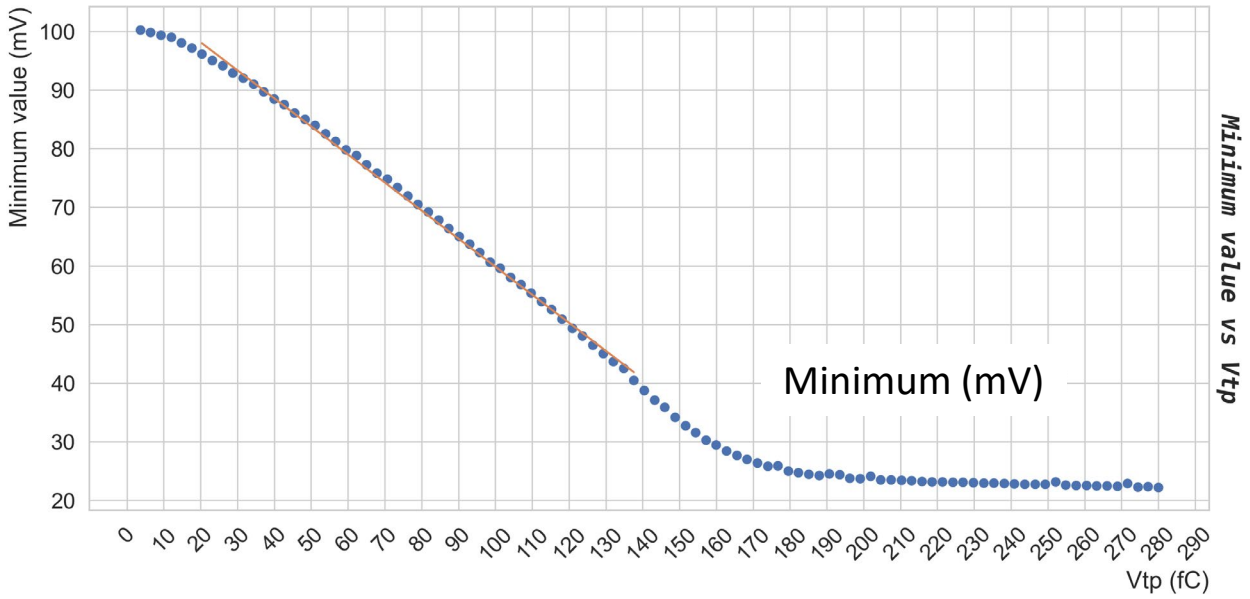




CSA + Shaper Output: Measured Parameters



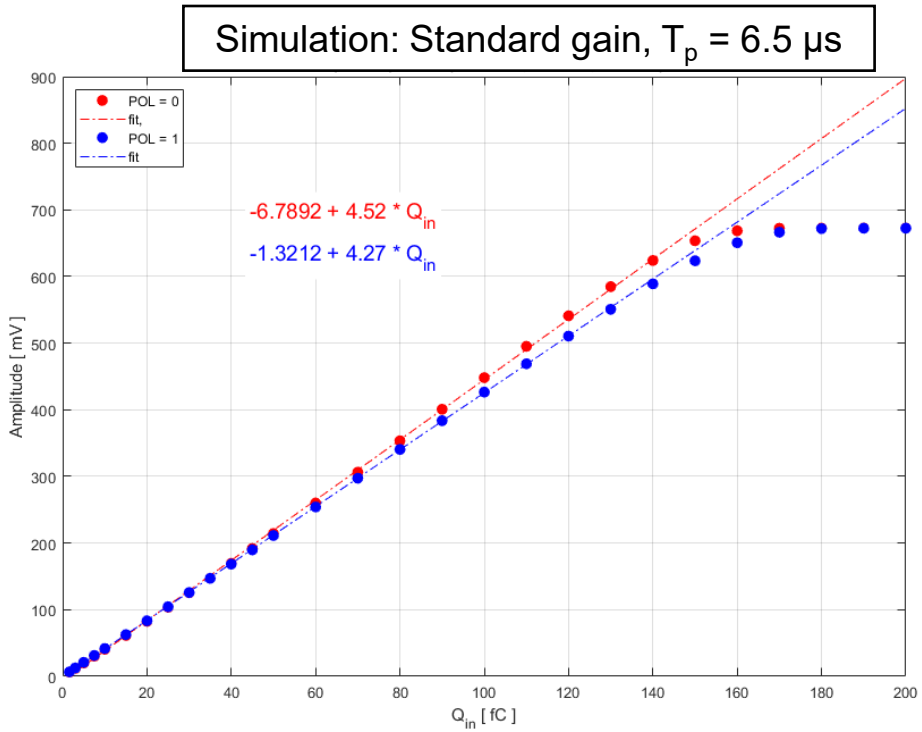




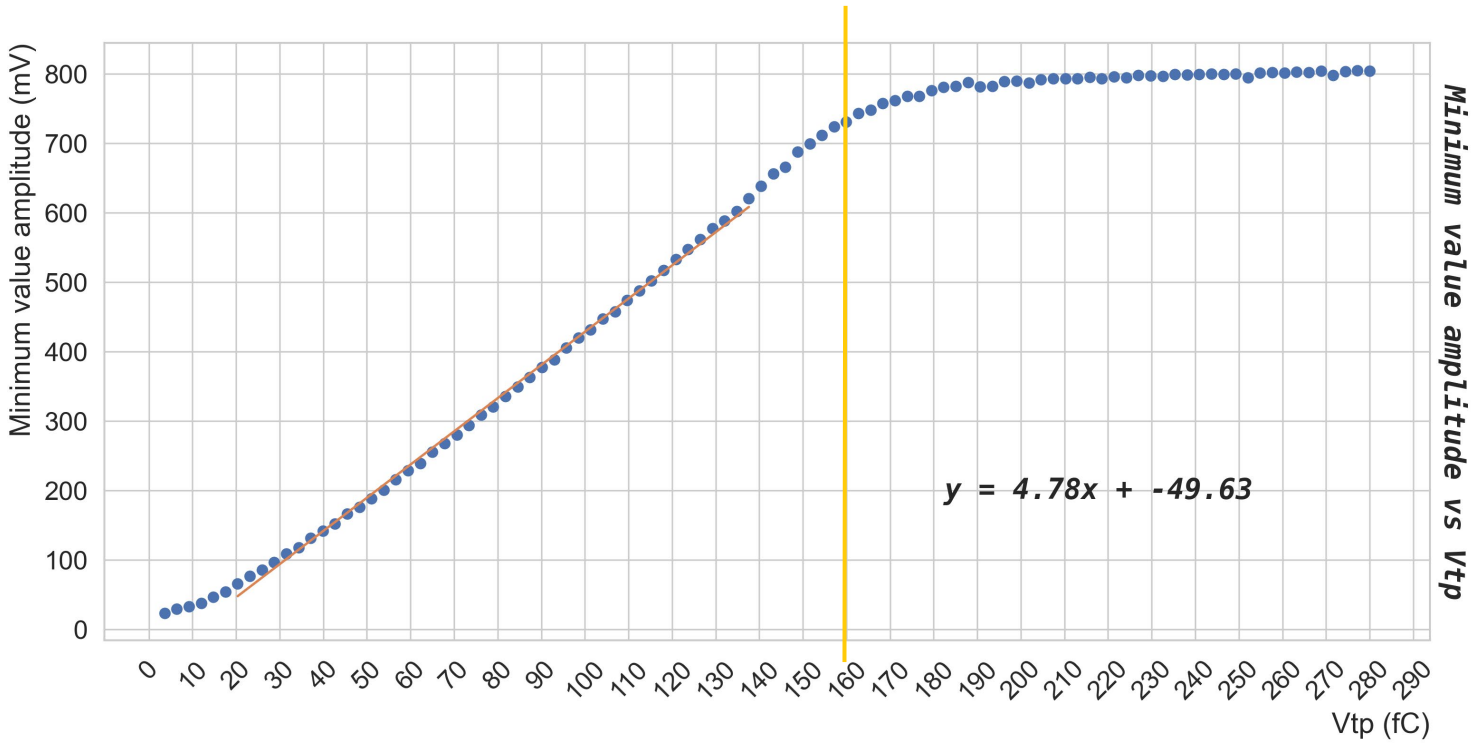
Standard Gain
Peaking time: 6.5 µs
Charge pulses: 3.6-280 fC

ASTRA Characterization: Front-End Linearity

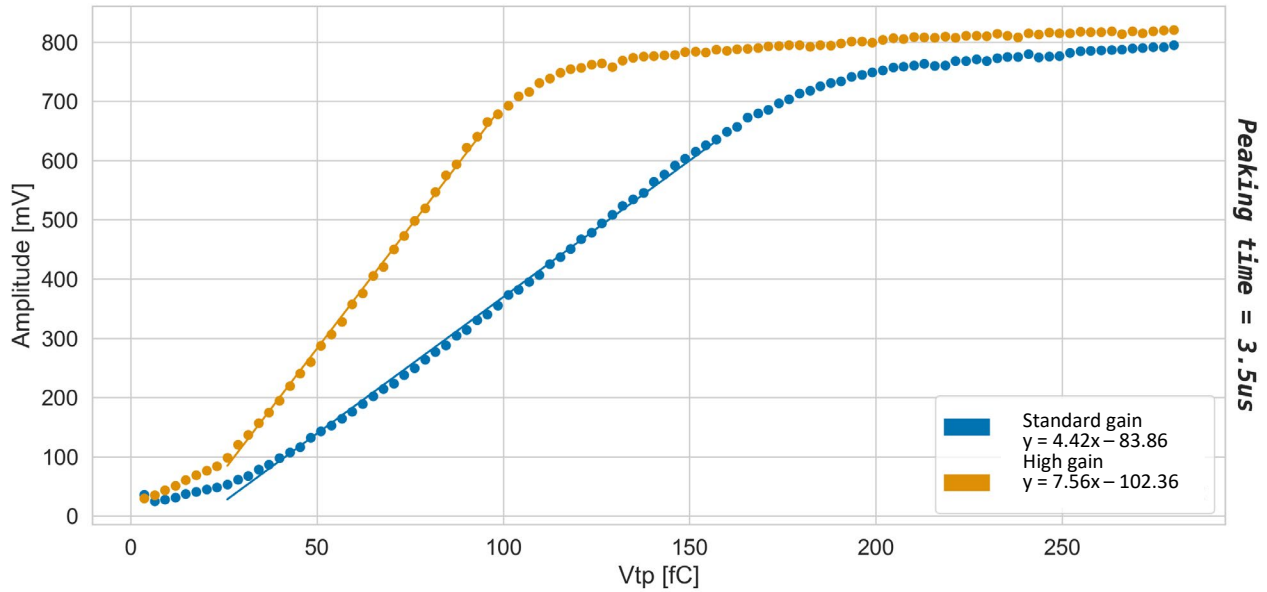
- Shaping time: 6.5 µs
- Slightly higher gain compared to simulations
  - 4.78 mV/fC VS 4.3 mV/fC
  - 8.72 mV/fC VS 8.1 mV/fC

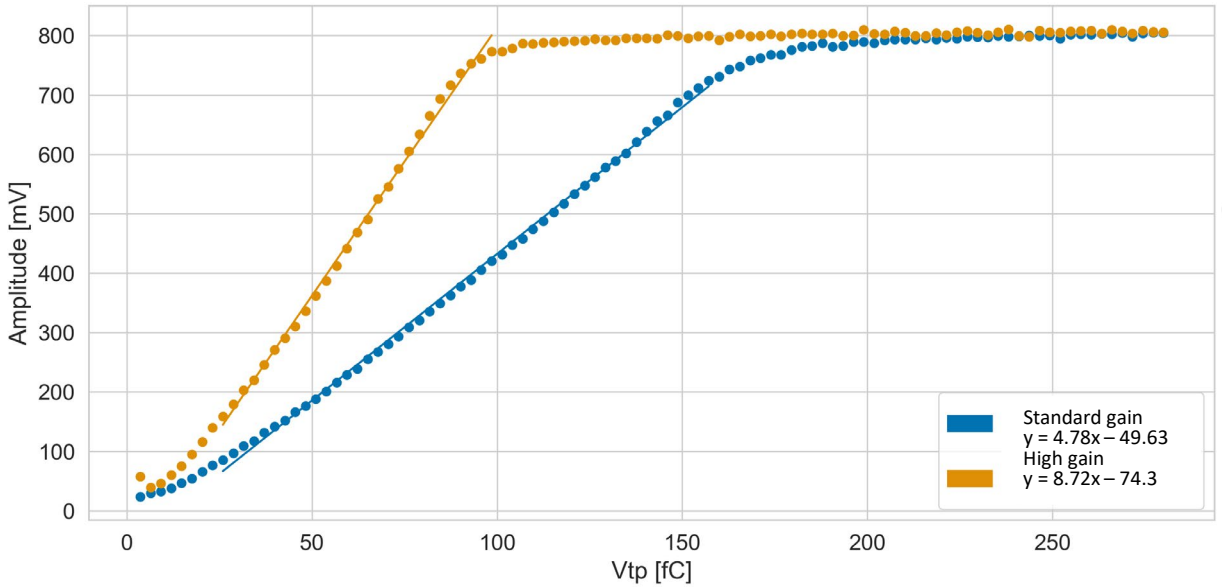


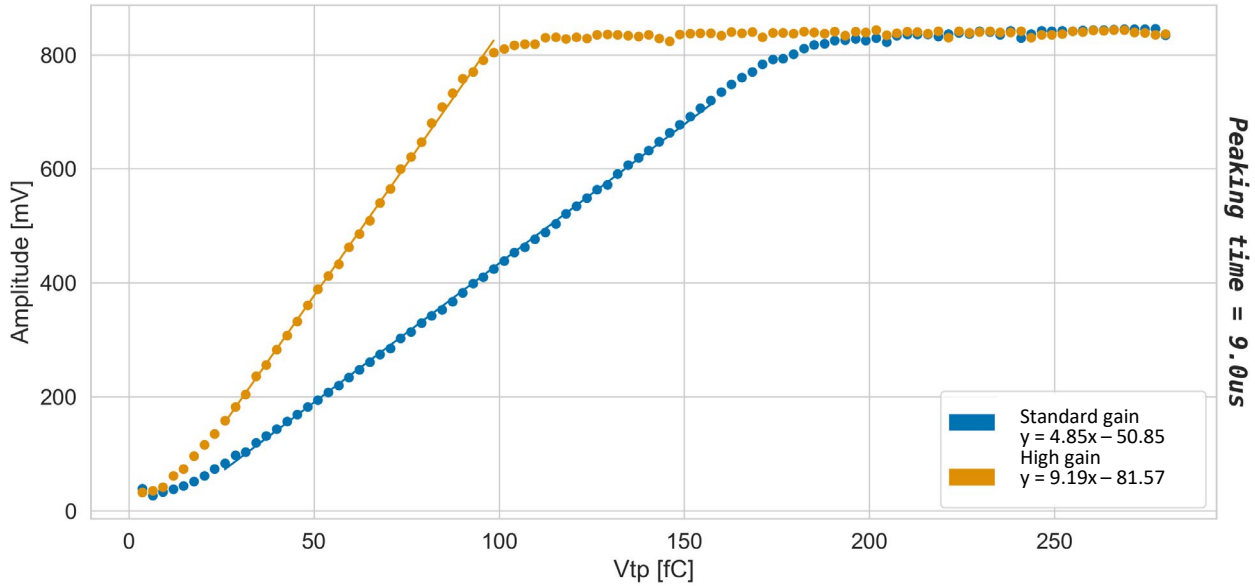
Linear up to 160 fC



ASTRA Characterization: Actual Gain







Gain (mV/fC)	V_{tp} 3.5 µs	V_{tp} 6.5 µs	V_{tp} 9 µs
Standard	4.42	4.78	4.85
High	7.56	8.72	9.19

ASTRA Requirements and Specs

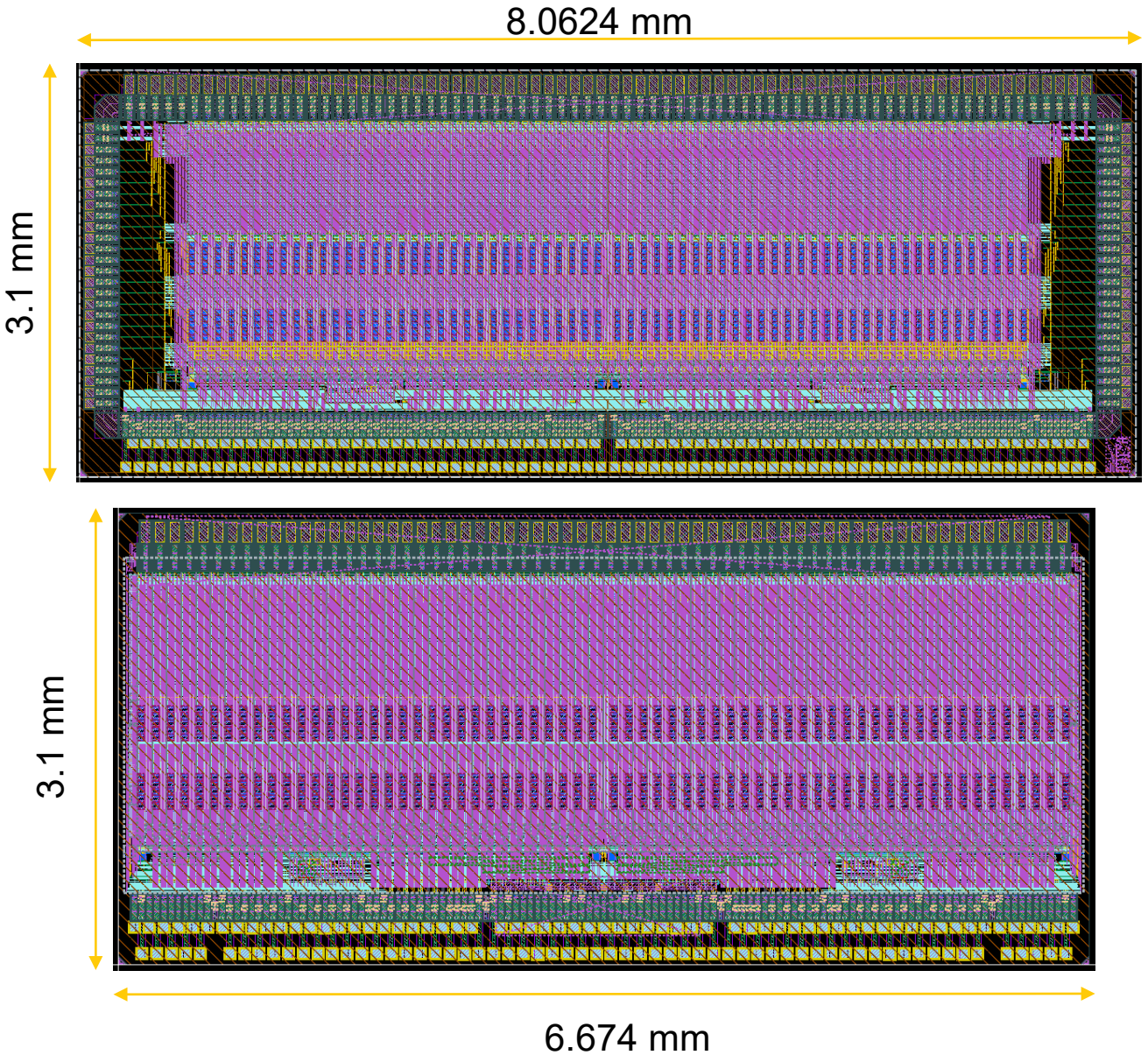
	Requirements	Specs (v1)
Channels	64	64
Dynamic Range	± 160 fC; ± 80 fC	160 fC; 90 fC
Linearity Region	± 160 fC; ± 80 fC	160 fC; 90 fC
Shaping Time	Adjustable in 1÷10 μs	1.5 μs, 3.5 μs, 6.5 μs, 9 μs
ENC	< 1000 e^- @ C_{in} 100 pF	< 1000 e^-
Gain	4.3; 8.1 mV/fC [peaking time 6.5 μs]	4.78; 8.72 mV/fC [peaking time 6.5 μs]
Output	Multiplexed pulse height Digitized pulse height Channels FastOR	Multiplexed pulse height, Digitized pulse height, Channels FastOR
Power supply	Positive (only) supply	1.2 V
Overall power consumption	-	Test board: 1.4 W
Channel power consumption	< 1 mW	<1 mW
Production Process	110 nm CMOS	110 nm CMOS
Size	6x6 mm^2	8.06x3.1 mm^2

Still missing the other polarization

Stage	Power/ch [μW]
Preamplifier	300
Inverting stage*	24
Shaper	66
Fast Shaper	32
Discriminator	18
S&H	108
ADC	36
Single-to-Diff. Amp.	8
Output Buffers (2)	37
Counter + Serializer	0.12
SLVS RX (3)	9
SLVS TX (2)***	190

630 μW/channel for analog readout
830 μW/channel for digital readout

ASTRA-64 v1 vs v2



- Removed side pads to be 2-side abuttable
- Already available from ARCADIA RUN2
- Design of PCB hosting ~4 ASTRA-64 v2 ASICs starting soon

Conclusions

- ASTRA: 64-channel ASIC readout electronics for Si µStrips
  - in house design of versatile chip
  - possible application in different space and ground experiments

- Each ASTRA channel performs signal amplification and charge measurement
  - Positive and negative input signal polarities readout capability
  - 2 gain settings providing input dynamic range up to 80 or 160 fC
  - 4 peaking time configurations: 1.5 µs, 3.5 µs, 6.5 µs, 9 µs
  - Dual-readout mode: analog and digital
  - FastOR trigger output

- ASTRA characterization still in progress
  - Exploit all the functionalities
  - Optimize behavior with external biases
  - Use it in actual beam tests