Contribution ID: **25** Type: **not specified**

Characterisation of the Analogue Pixel Test Structures produced in the 65 nm TPSCo process

Thursday, 22 February 2024 11:35 (20 minutes)

The ITS3 project foresees the use of ultra-light monolithic active pixel sensors (MAPS) for the vertex detector in the ALICE experiment at the LHC to drastically improve the performance of the ALICE tracking and vertexing system. The MAPS are produced in a 65 nm CMOS process in large, 12-inch wafers. Stitching allows the fabrication of wafer-scale sensors that can be thinned to around 50 µm and bent to form half-cylindrical detection layers.
This contribution discusses the analogue pixel test structure (APTS) produced in 65 nm. The APTS is used to understand the analogue properties of the TPSCo 65 nm technology and to compare the charge collection performance in different processes and pitches. Recent results from lab and test beam characterisation are presented, showing that a hit efficiency of more than 99% is achieved for all collection electrode geometries before and after irradiation up to 1e14 1 MeV n_eq. In-pixel studies show the dependence of the efficiency on the position inside the pixel cell. The achievable spatial resolution of less than 3 µm for pixel pitches of 10 µm. Finally, the applicability of 65 nm MAPS for FCC-ee vertex detectors that feature similar requirements as ALICE ITS3 will be discussed shortly.

Primary author: WITTWER, Rebekka

Presenter: WITTWER, Rebekka

Session Classification: MAPS 2