The ASIC FAST3, a front-end integrated circuit optimized to read out 50 µm LGAD sensors

M. Ferrero, R. Arcidiacono, N. Cartiglia, F. Fausti, C. Hanna, L. Lanteri, J. Olave, M. Rolo, A. M. Rojas, L. Menzio, R. Mulargia, F. Siviero, V. Sola, R. S. White

In collaboration with the Microelectronic group and electronic Laboratory of INFN Turin

19th TREDI Workshop on Advanced Silicon Radiation Detectors

Outline

- The ASICs FAST3

- Laboratory characterization of FAST3:
  - Signal shape
  - Gain
  - Temporal Jitter
  - Uniformity

- Comparison between measurements and simulations

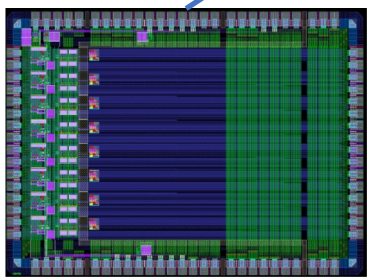
- Study of the performance of FAST3 coupled with LGAD sensors using β-source.
  - Temporal resolution
  - Gain
  - Electronic Cross-talk

Readout electronic for timing: the family of FAST ASICs

FAST is a family of ASICs designed in CMOS 110 nm technology

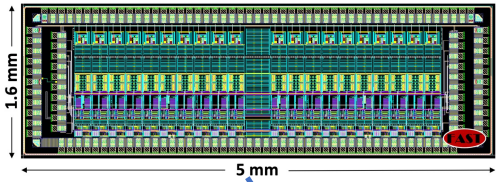
TOFFEE

The first chip (8-ch) designed for LGADs readout.
Jitter of ~40 ps.



F. Cenna et al., TOFFEE: a full custom amplifier-comparator chip for timing applications with silicon detectors, JINST 12 (2017) C03031

Development of front-end readout electronics for high time resolution measurements with UFSD, J. Olave et al., *2018 IEEE Nuclear Science Symposium, Medical Imaging Conference (NSS/MIC)*, 2018, 10.1109/NSSMIC.2018.8824333



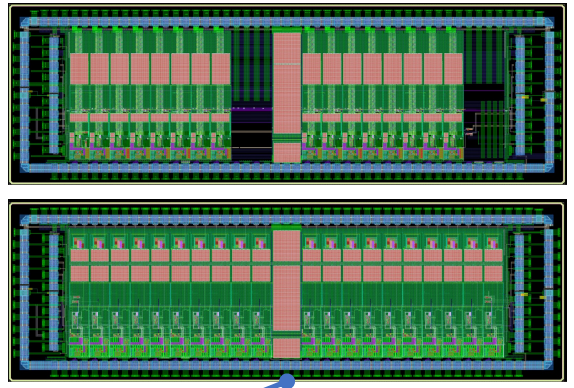
FAST1

20-channel ASIC with a resistive feedback preamplifier and a discriminator stage.
Jitter < 30 ps.

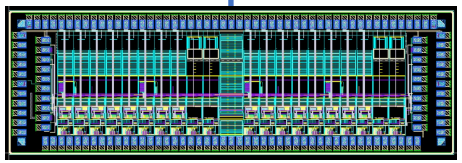
FAST2

Two version od ASICs
- Preamplifier-only (2 designs)
- Discriminator stage

Jitter < 30 ps.



2016/2017	2018/2019	2020/2021	2022/2023



FAST3

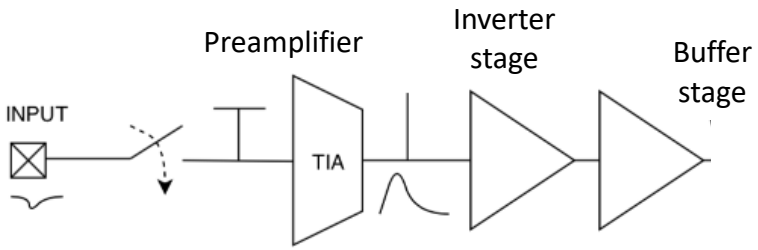
Two version od ASICs
- Preamplifier-only
- Discriminator stage

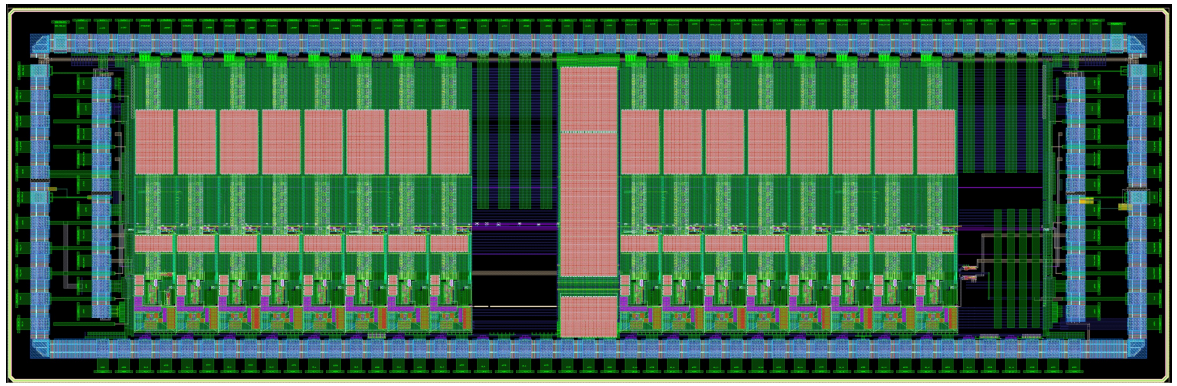
Jitter <20 ps.

The ASIC FAST3 family

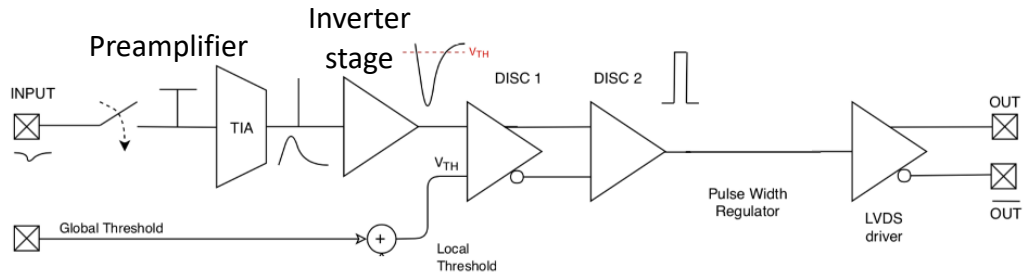
FAST3 family includes two different ASIC designed in UMC 110 nm CMOS technology

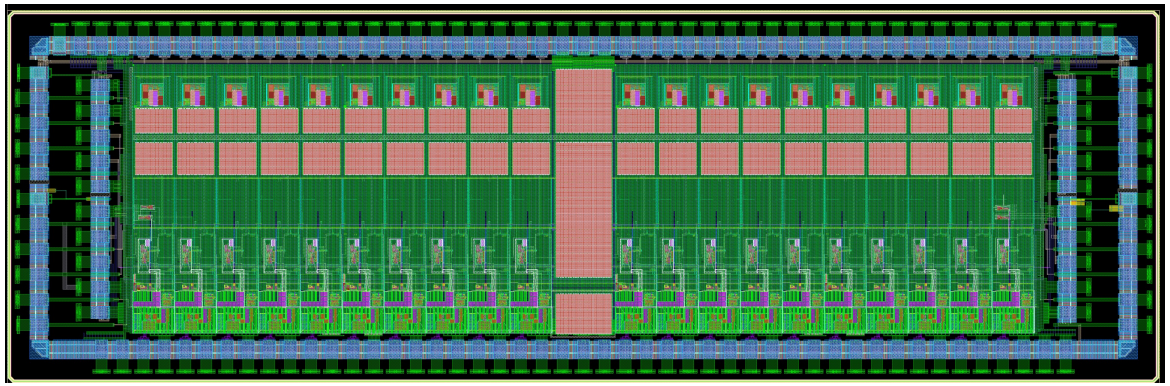
Amplifier-only architecture (FAST3-Analog)
- 16 channels





Amplifier-comparator architecture (FAST3-Digital)
- 20 channels

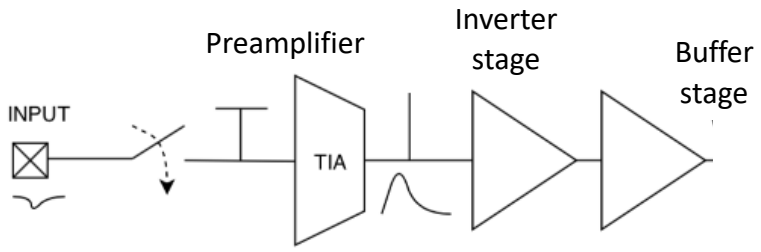




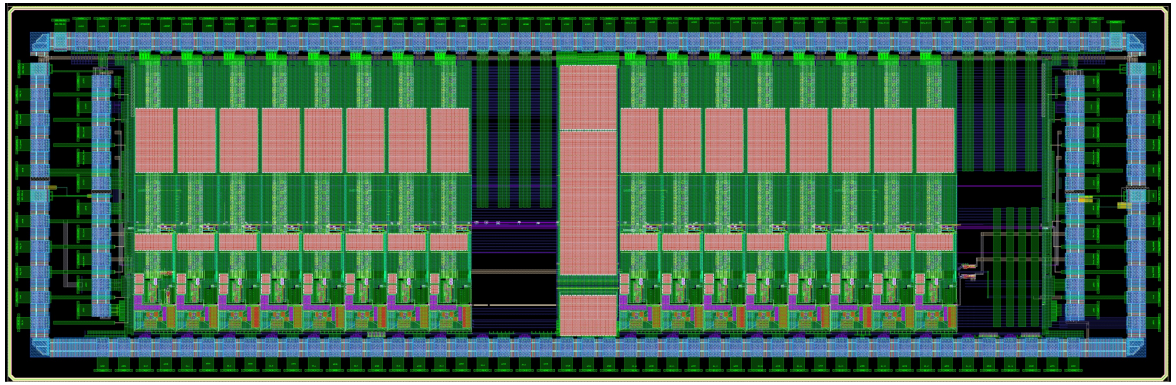
FAST3: Front-End Electronics to Read Out Thin Ultra-Fast Silicon Detectors for ps Resolution, AM. Rojas, et al., *J. 2022 IEEE Latin American Electron Devices Conference (LAEDC)*, 2022, 10.1109/LAEDC54796.2022.9908192

FAST3 Analog

Amplifier-only architecture (FAST3-Analog)



Output

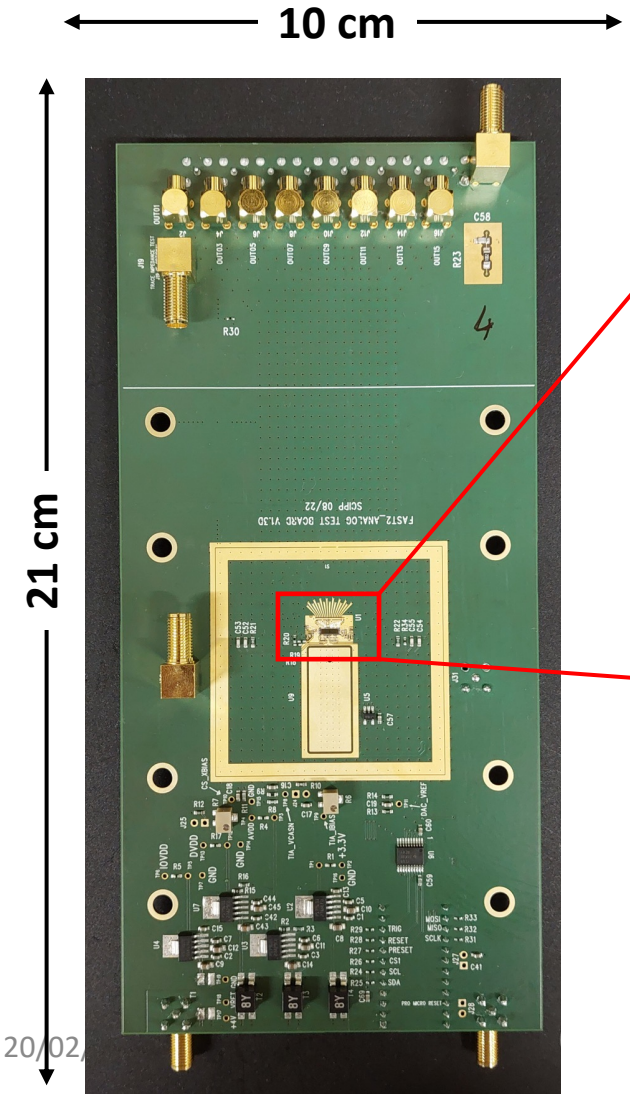


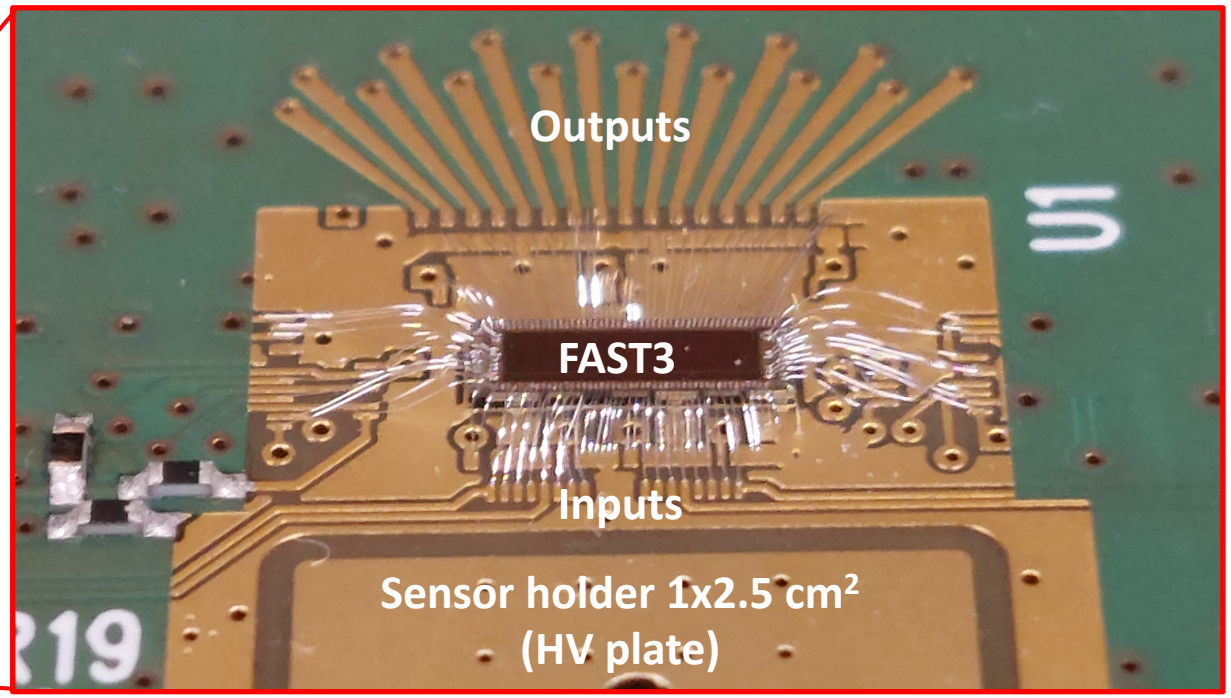
Input

UMC 110 nm CMOS technology	
Transimpedance amplifier	
8 programmable gains	
Dimension	1 x 5 mm^2
Power rail	1.2 V
Power consumption	~ 2.5 mW/ch
Input dynamic range	3-40 fC
Voltage output range	~ 700 mV
Input impedance	50 Ω
Bandwidth	~ 1 GHz
Temporal Jitter	20 ps (@ 8fC)
Number of channels	16

Readout Board

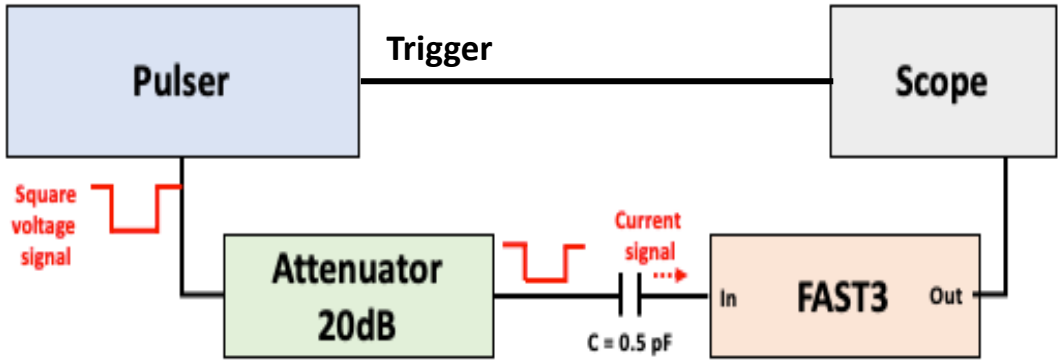
The read-out board has been developed by the University of Santa Cruz for FAST2 ASICs and optimized in Turin for FAST3





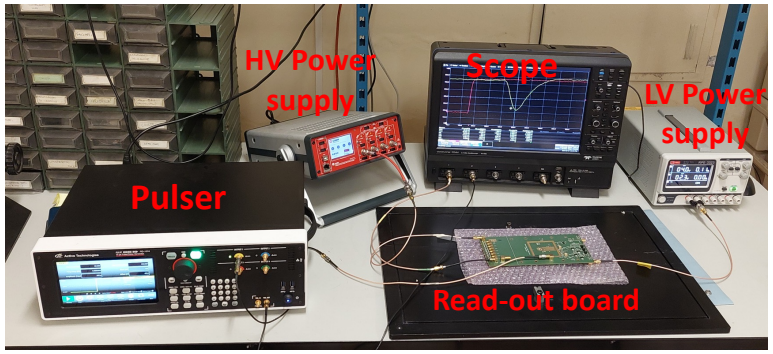
Channels 1, 5, 12 and 16 have input traces instrumented with capacitances of **0.5pF** to allow charge injection through an external pulser.

Measurement setup - pulser

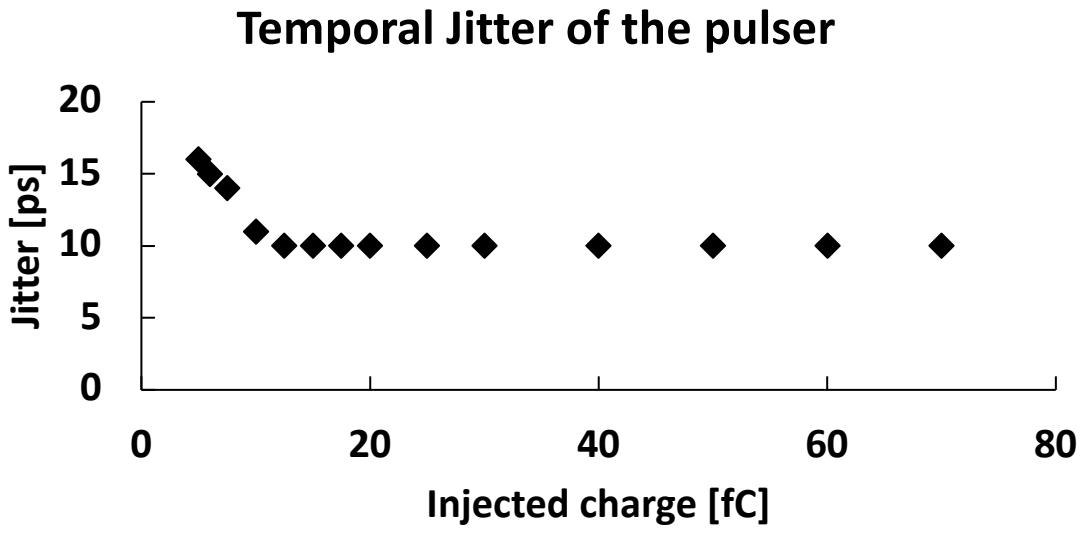


The setup is used to study:

- **Signal shape**
- **Gain**
- **Jitter**

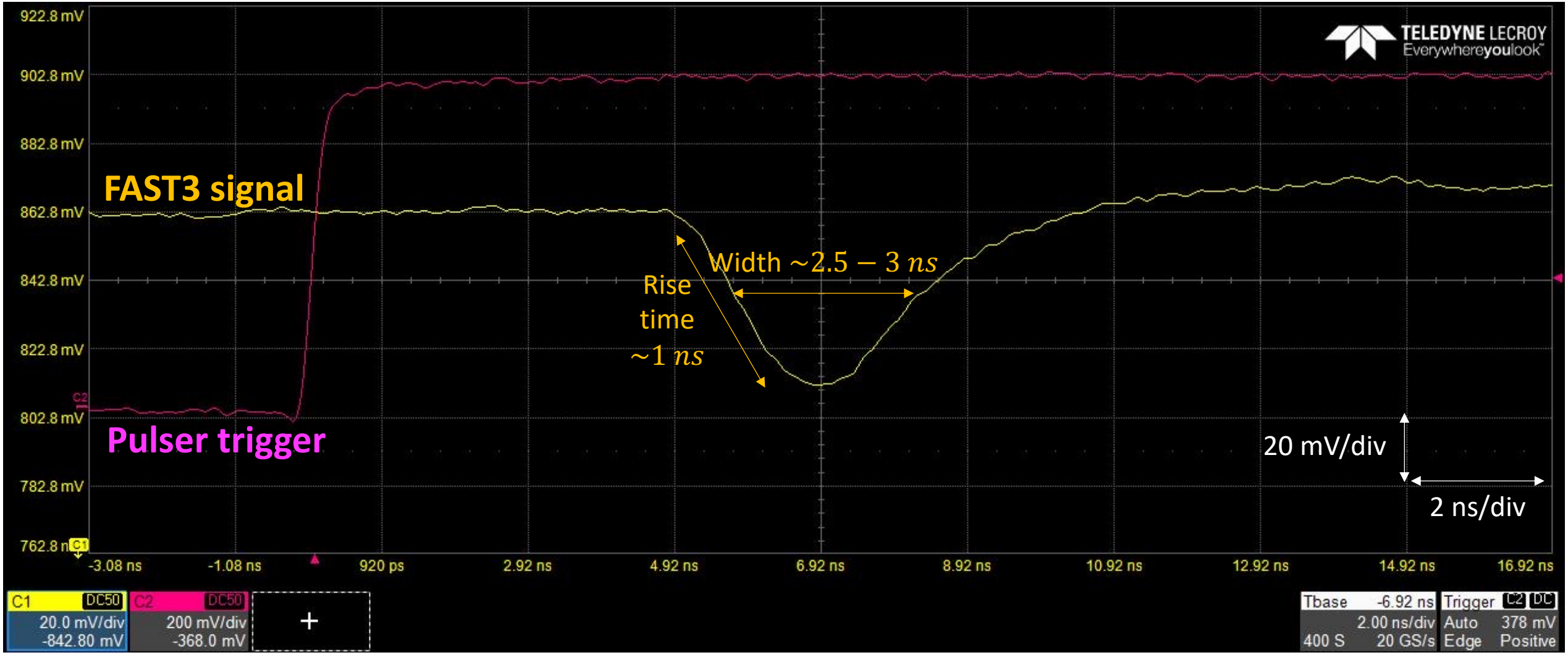


- **Pulser:** Active Technology PG-1074
- **Oscilloscope:** Lecroy-WaveRunner 9254M (2.5GHz – 40Gs/s)



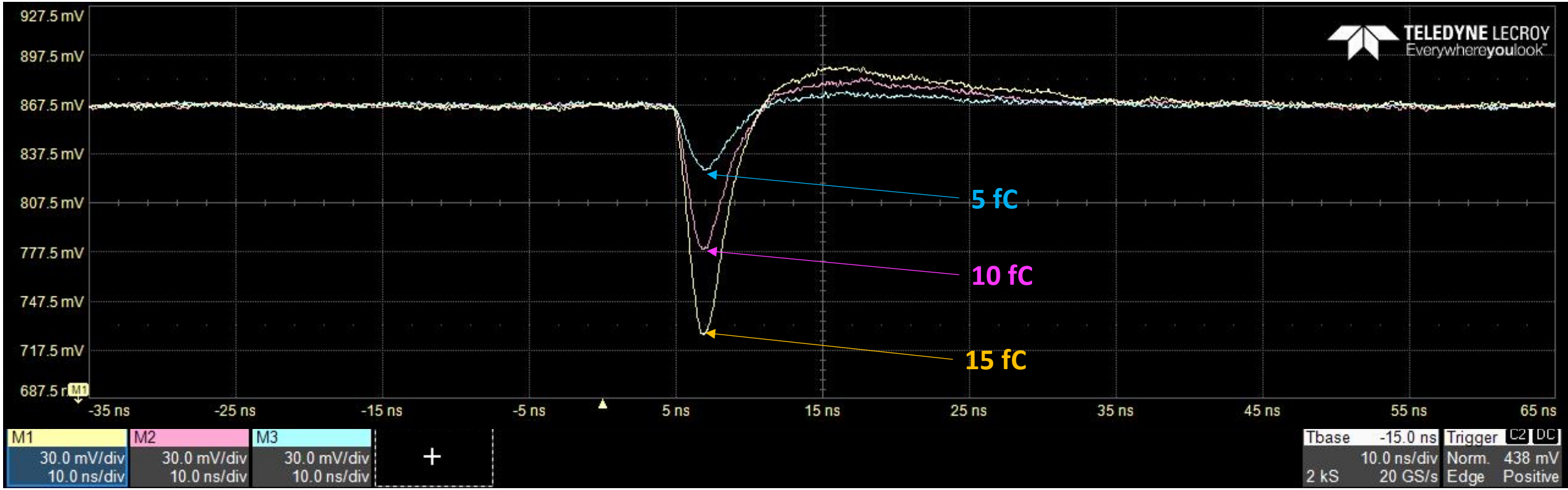
The typical output signal of FAST3

Signal generated by 6fC of charge injection



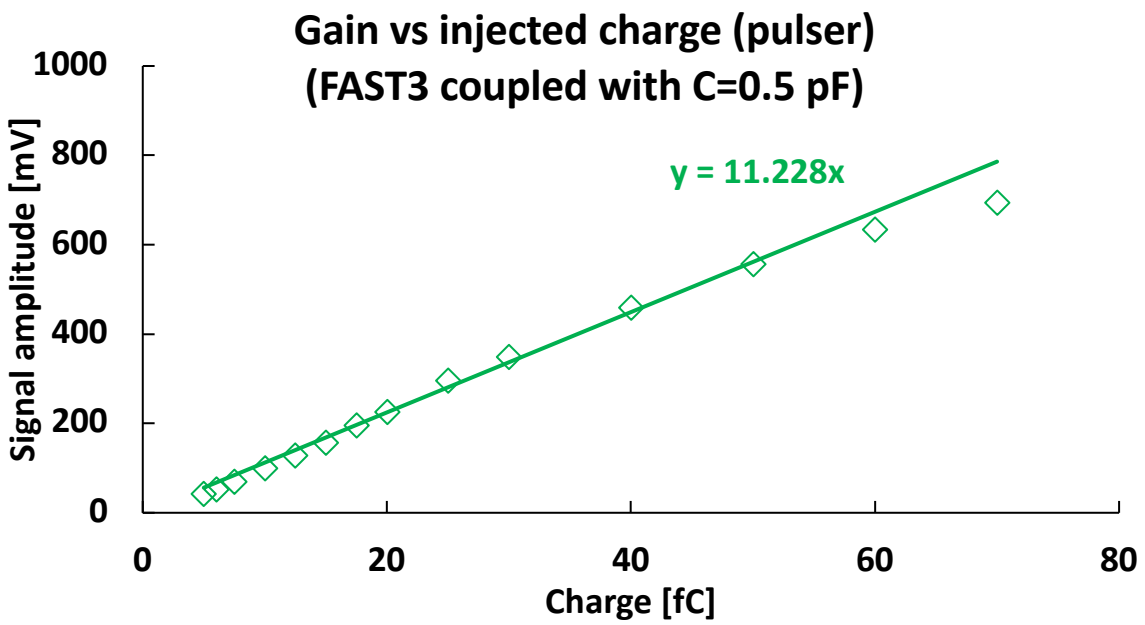
The typical output signal of FAST3

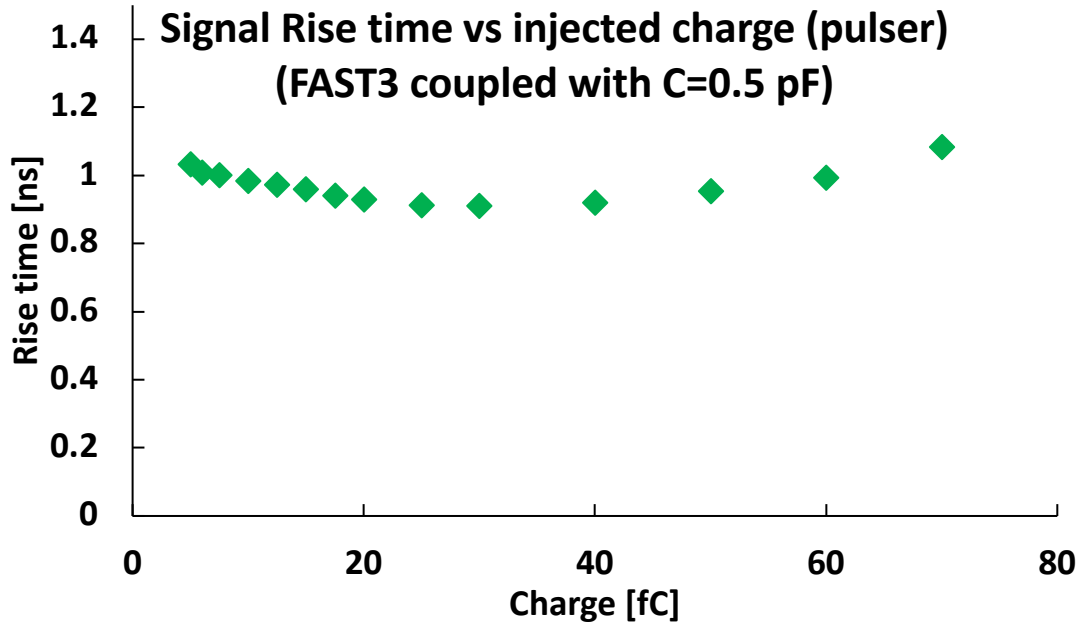
Signals generated by charge injection of 5/10/ 15fC



Linear scaling of the amplitude as a function of the injected charge

Signal Features - Amplitude and Risetime



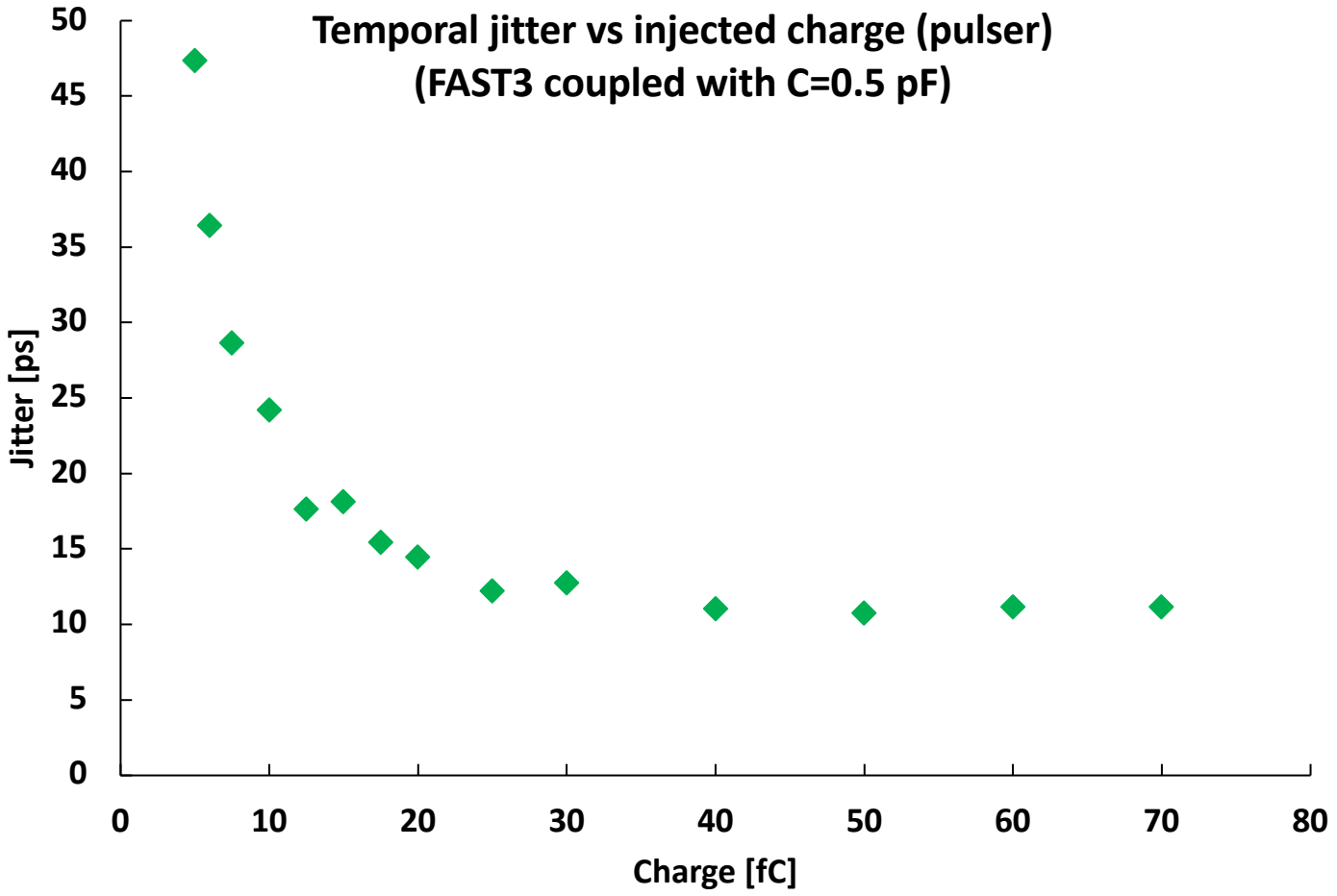


- Good linearity of the signal amplitude as a function of the injected charge
- Gain ~ 11 mV/fC
- Linear gain up to signal amplitude 600 mV (Q ~ 50 fC)

- Risetime between 0.9 and 1.1 ns

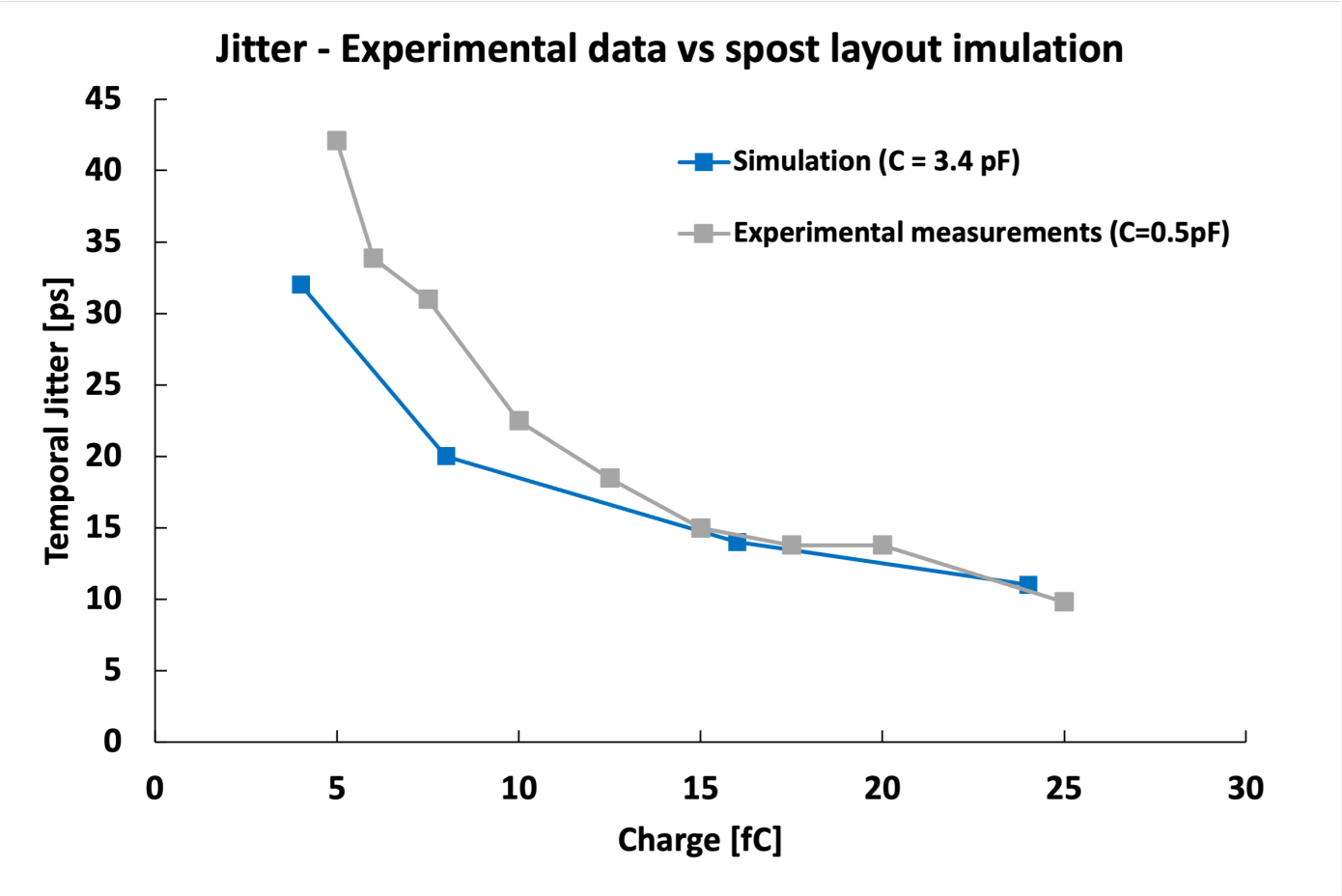
The output range, gain and rise time are in agreement with post layout simulation

Jitter



- Jitter below 25 ps at 10 fC
- Jitter plateau at 10 ps

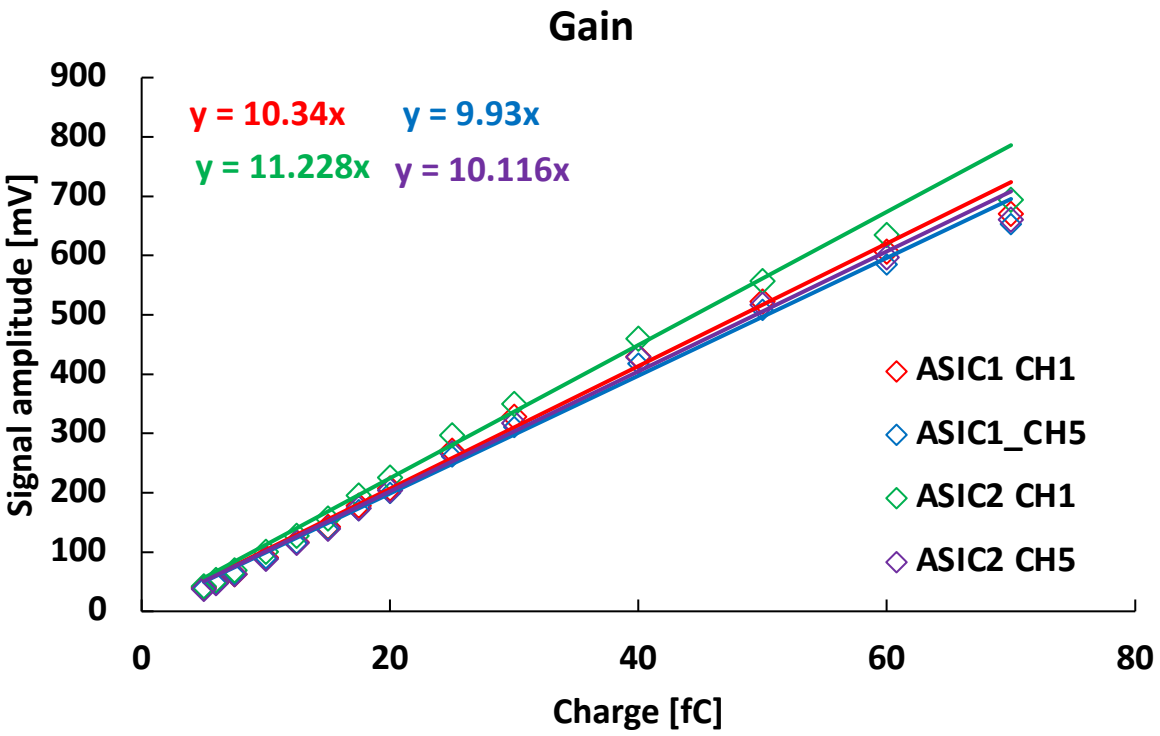
Jitter - Simulation vs measurement

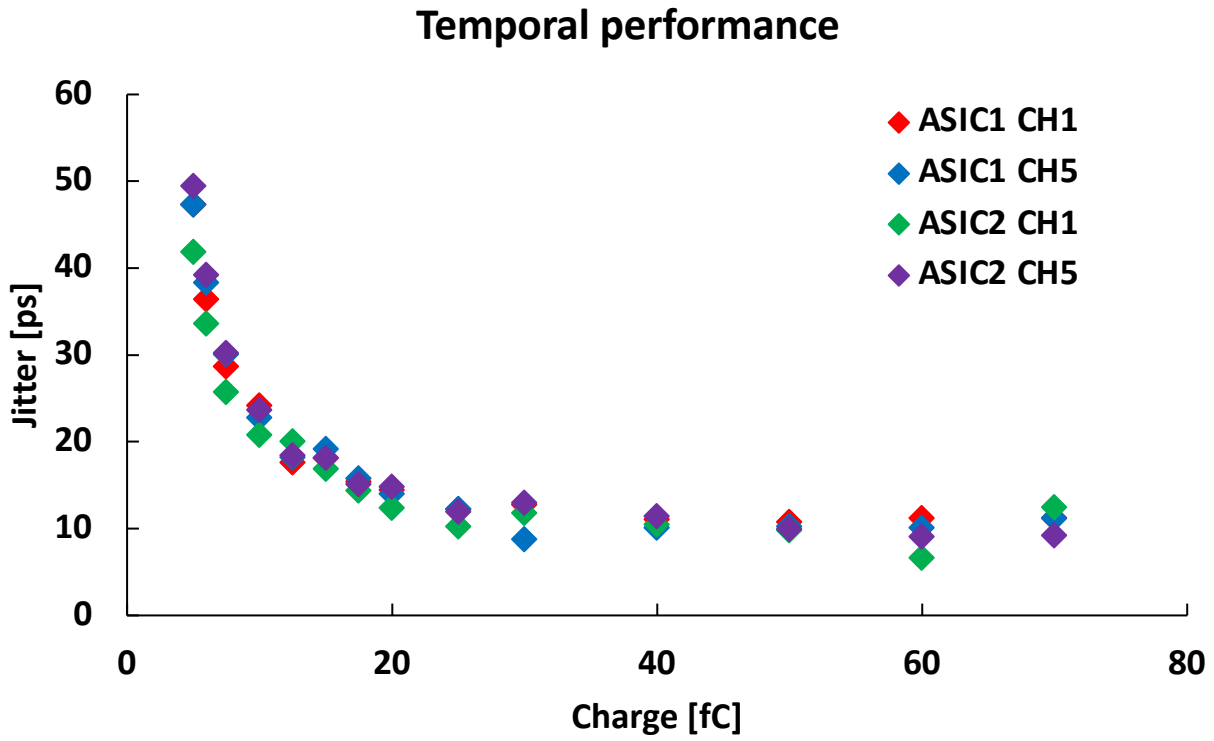


- Excellent agreement between Experimental data and post layout simulation for charges above 12 fC
- The difference at low charges is due to an high frequency noise not observed in simulation

Gain and Jitter uniformity

The studies for gain and jitter uniformity have been performed on 2 ASICs and two channel for each ASIC

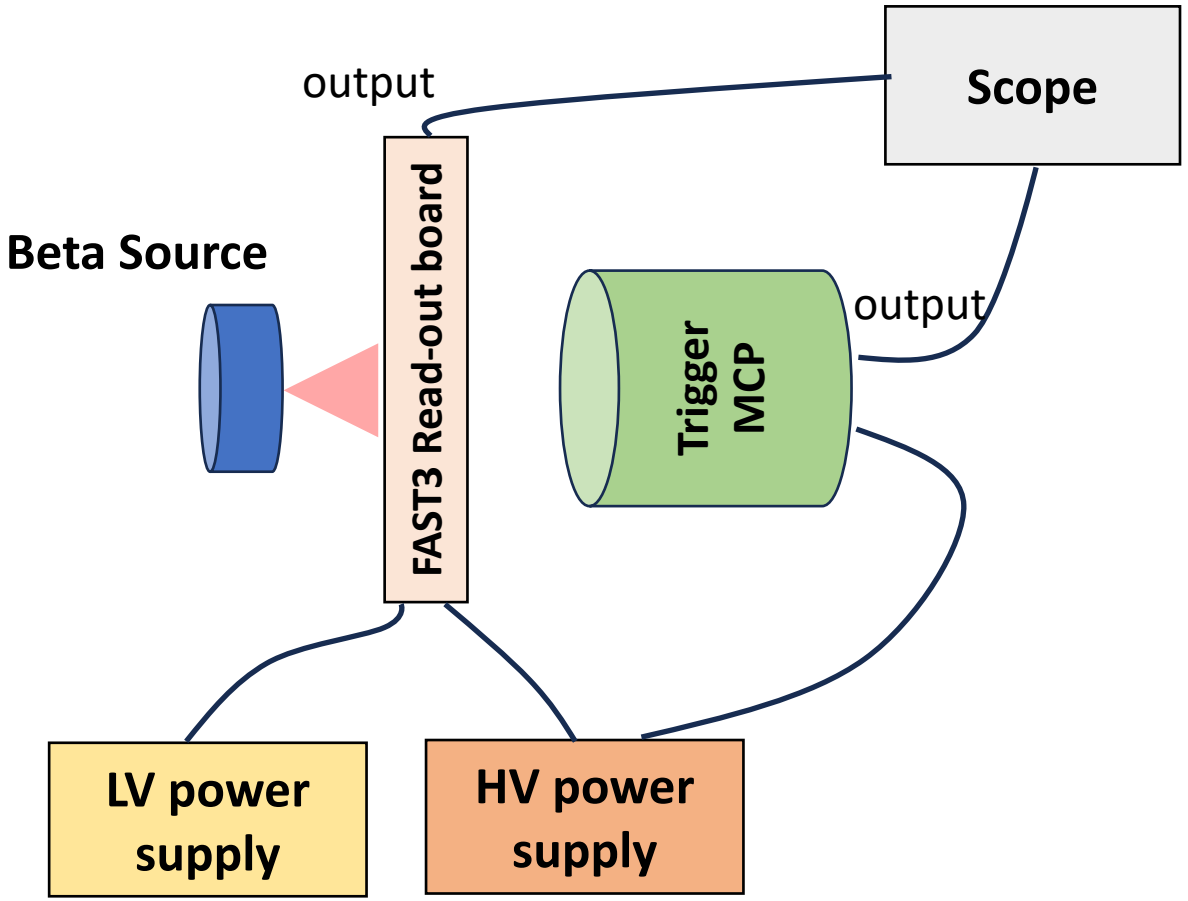




Excellent uniformity between different ASICs and FAST3-channels

Beta telescope

Evaluation of the temporal performance of FAST3 coupled with LGAD sensor

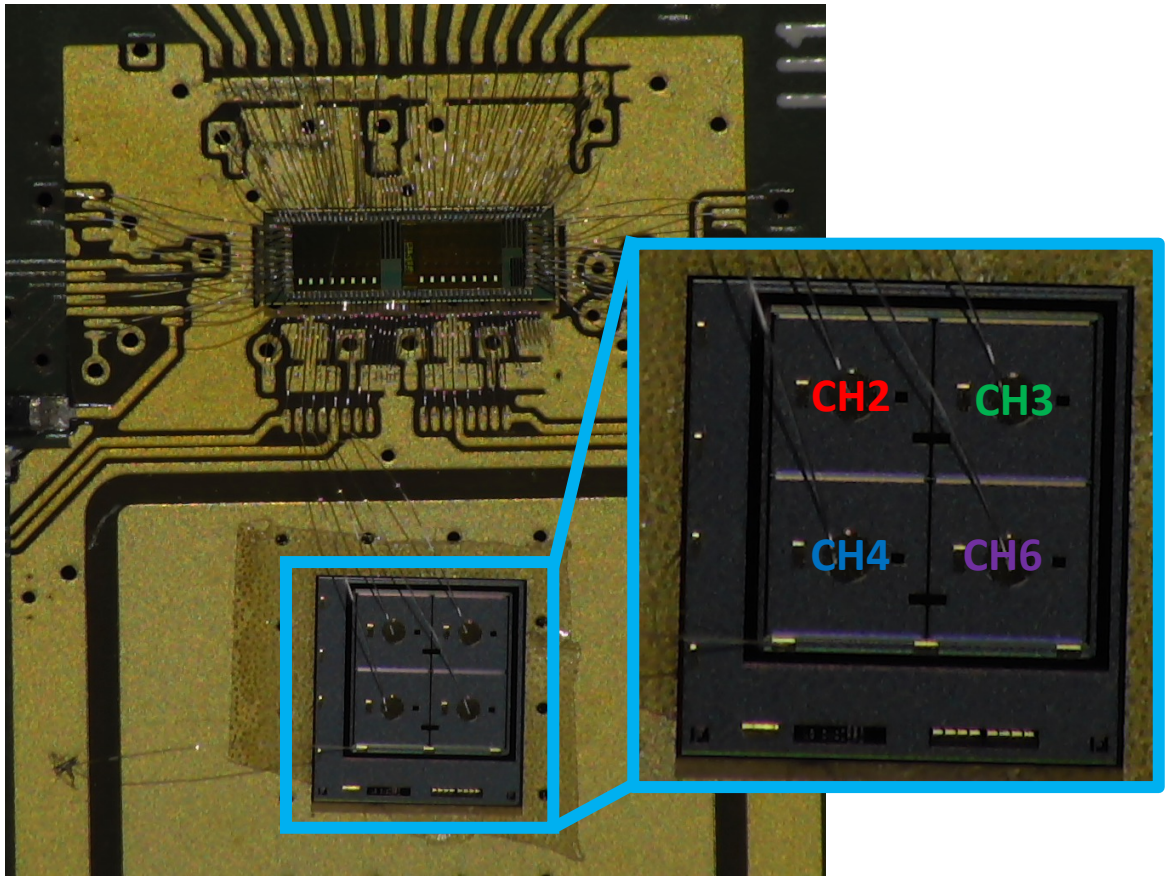


- **Oscilloscope:** Lecroy-WaveRunner 9254M (2.5GHz – 40Gs/s)
- **HV Power supply**: CAEN DT1471ET
- **Time reference**: MCP Photonics (time resolution of 15-20 ps)
- **Beta source**: Sr^{90} (activity ~ 37 kBq)

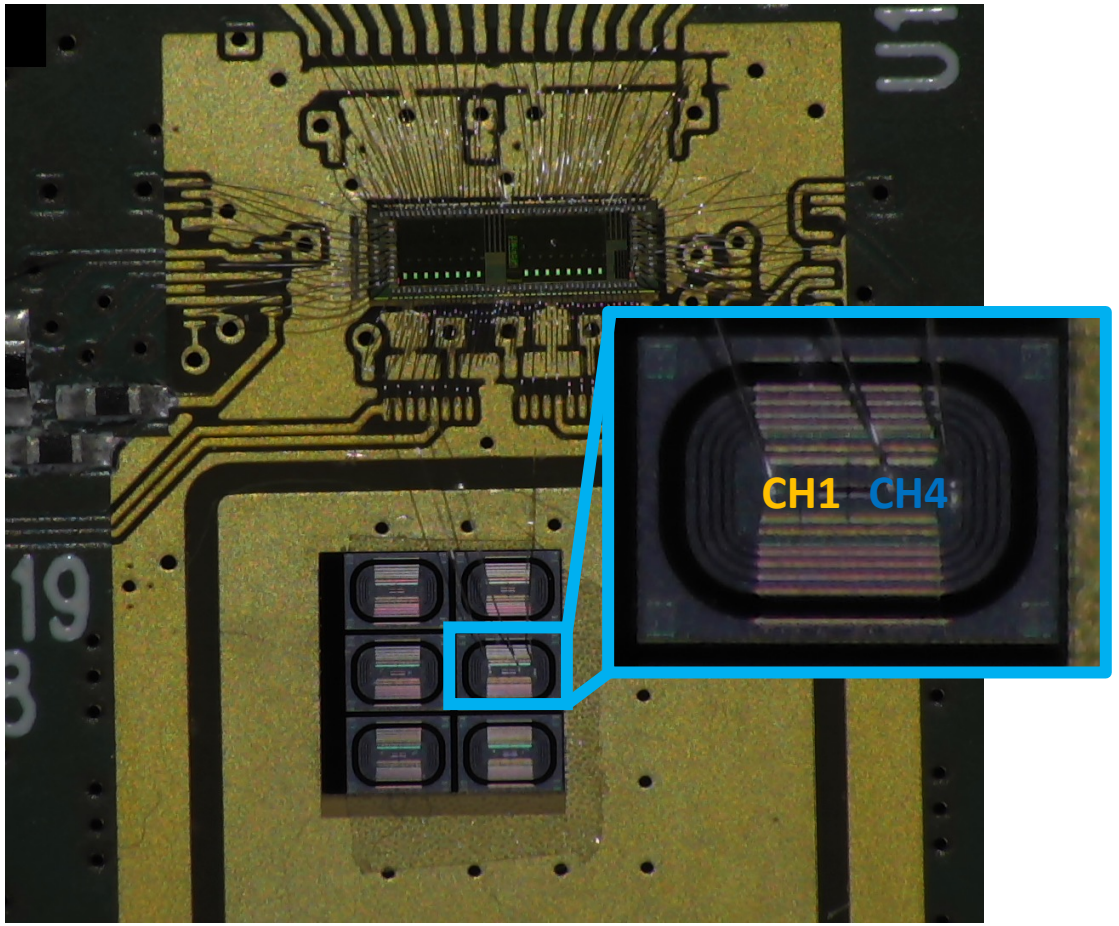
Beta runs

Beta acquisitions have been performed with two different FAST3-LGAD pairs

ASIC1 + HPK2-Split4 2x2 array (45µm-thick)
Sensors pixel size ~ 1.3 x 1.3 mm^2 (C = 3.8 pF)

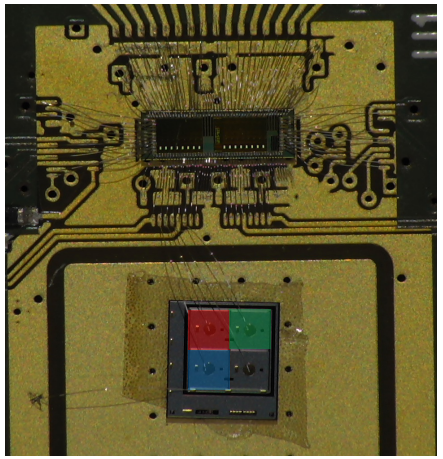


ASIC2 + FBK-TI-LGAD1 2x1 array (45µm-thick)
Sensor pixel size: 250 x 375 µm^2 (C = 0.2 pF)

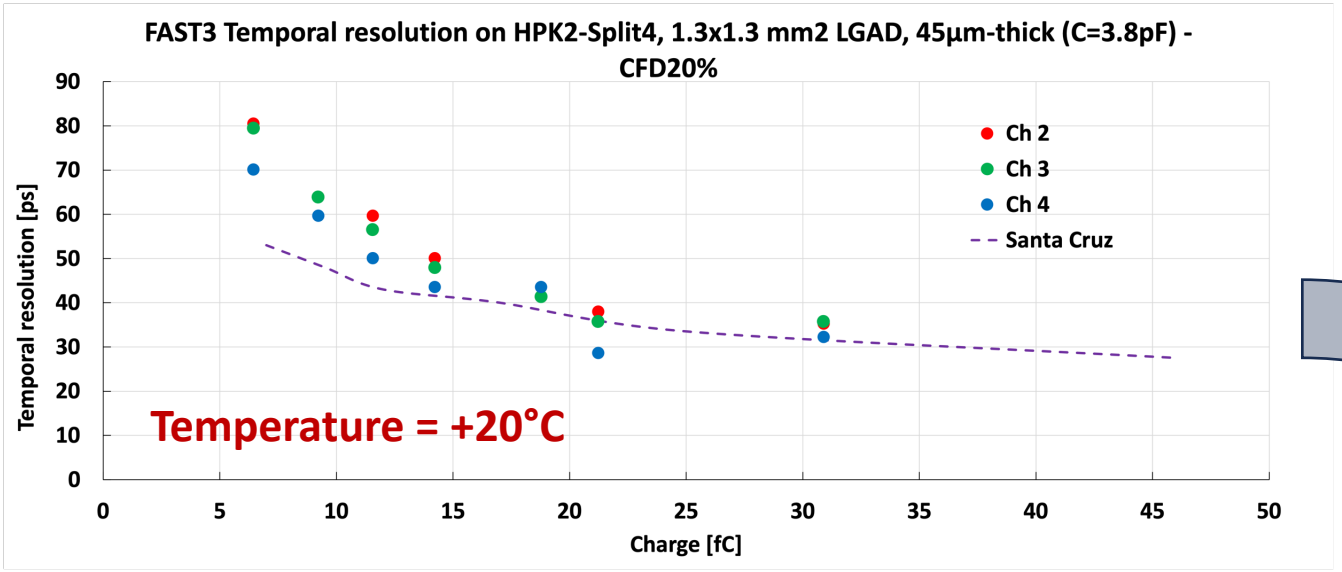


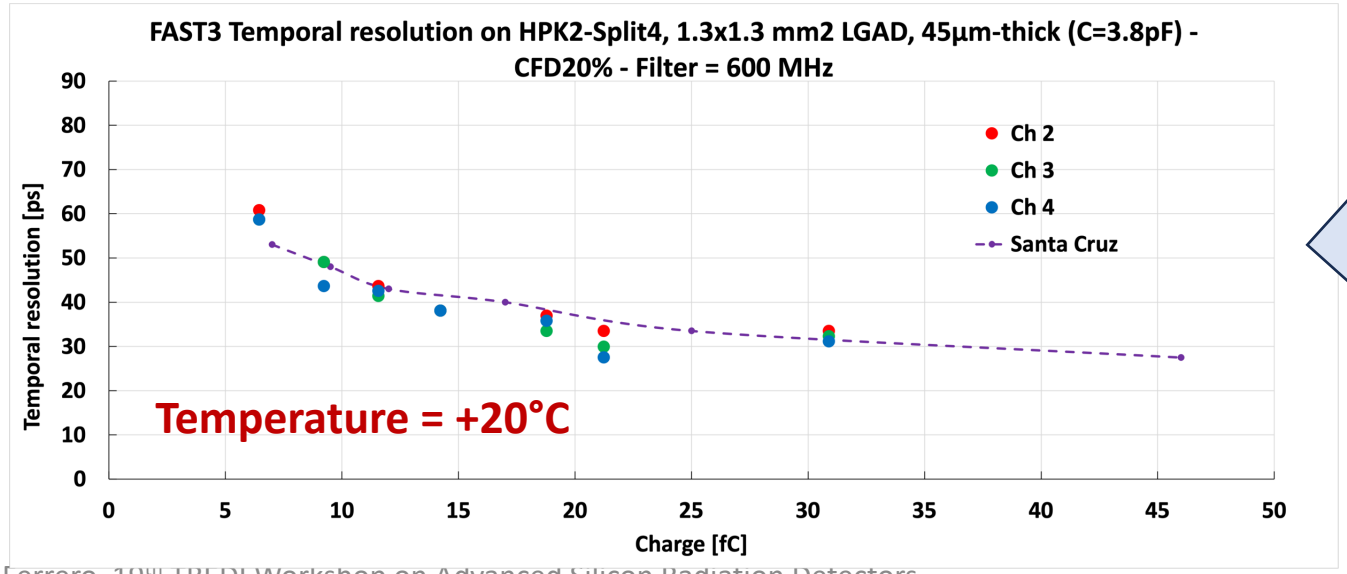
Temporal resolution

ASIC1 + HPK2-Split4 2x2 array (45µm-thick)
Sensors pixel size ~ 1.3 x 1.3 mm^2 (C = 3.8 pf)



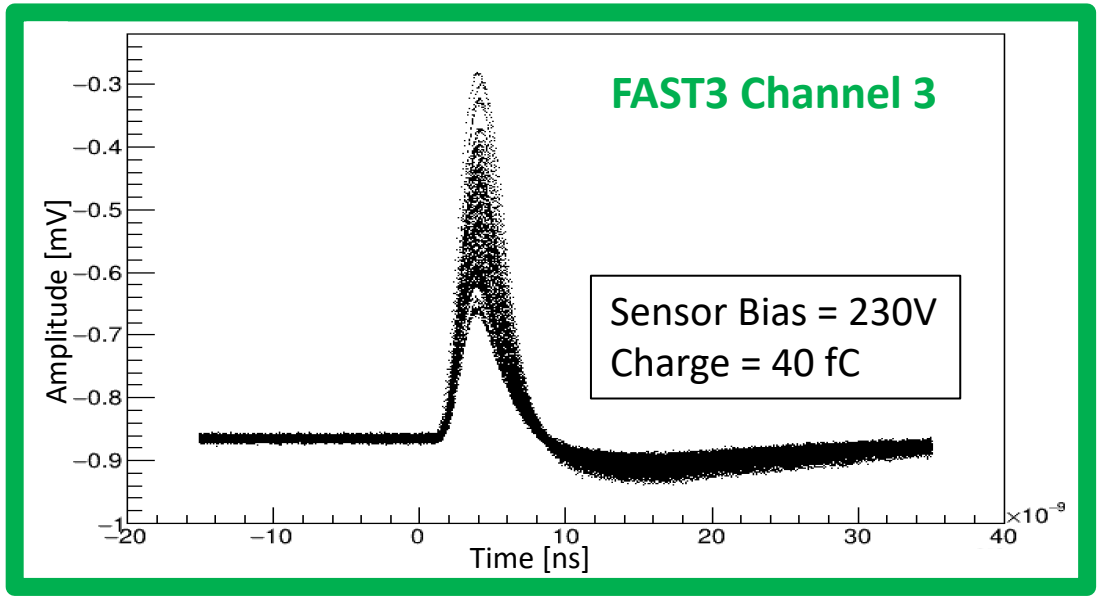
- The temporal performance of FAST3 are in excellent agreement with performance obtained with single channel Santa Cruz board
- Excellent uniformity between different channels

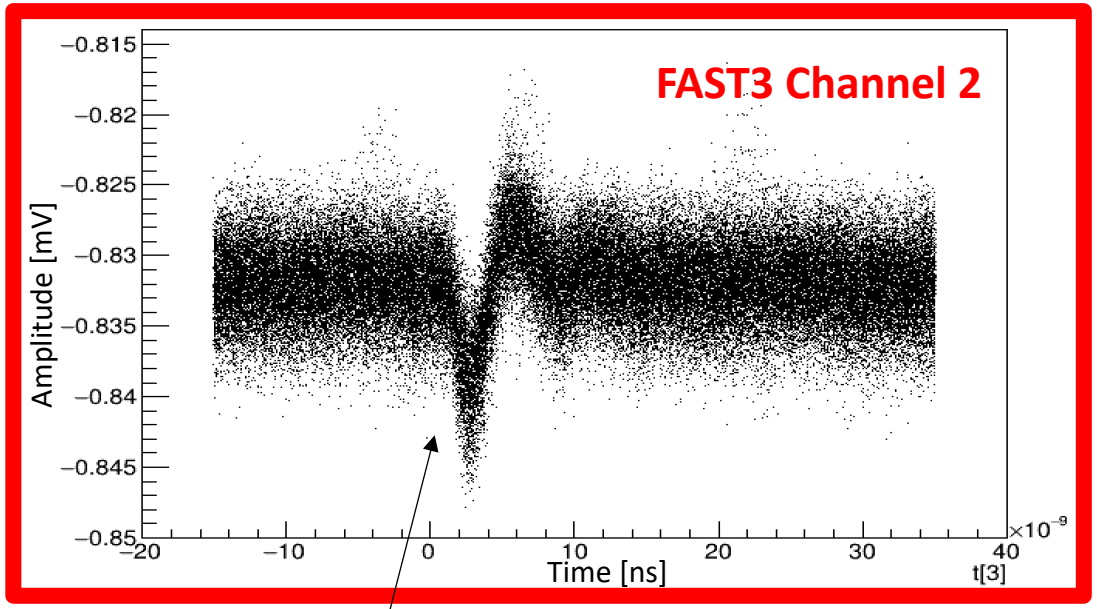


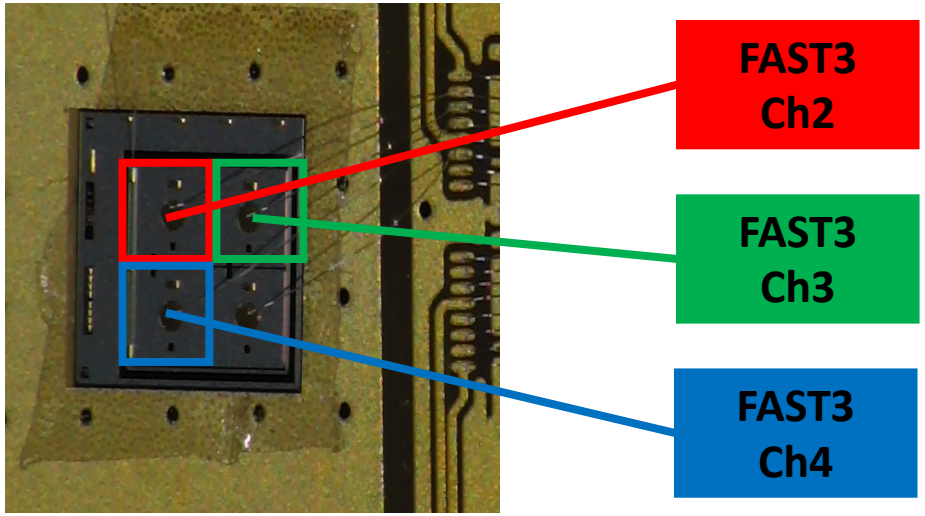


600 MHz filter was applied in offline analysis

Electronic Cross-talk



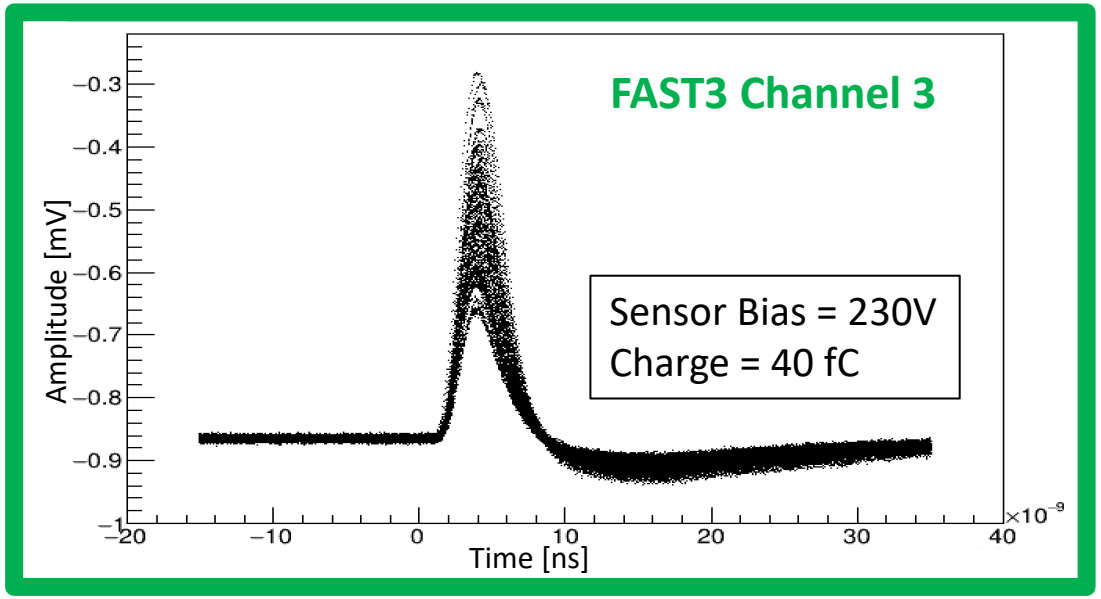


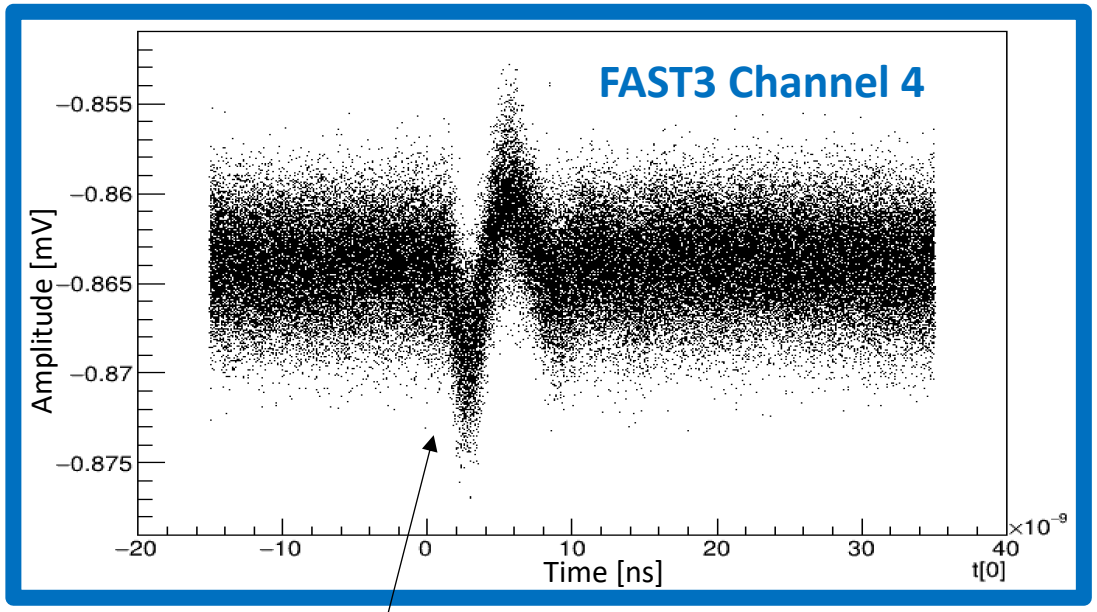


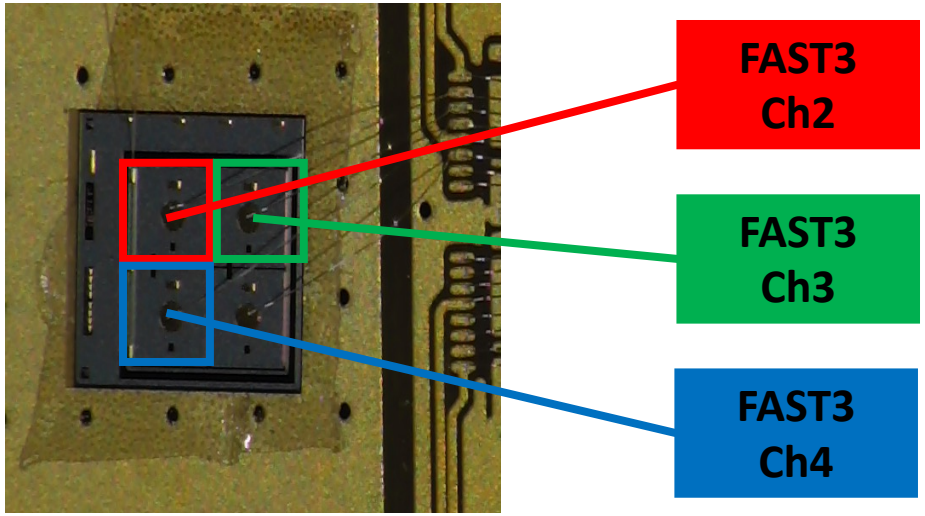
Bipolar signal induced by current signal on adjacent channel

No electronic Cross-talk was observed

Electronic Cross-talk



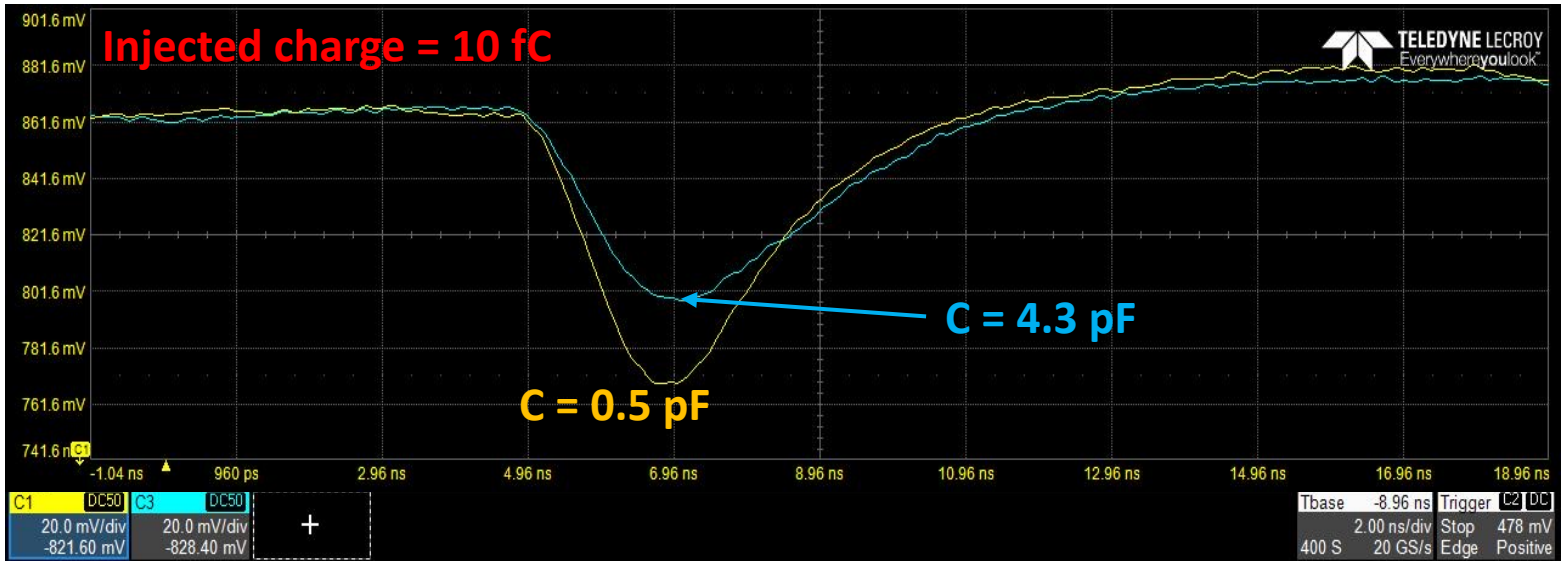


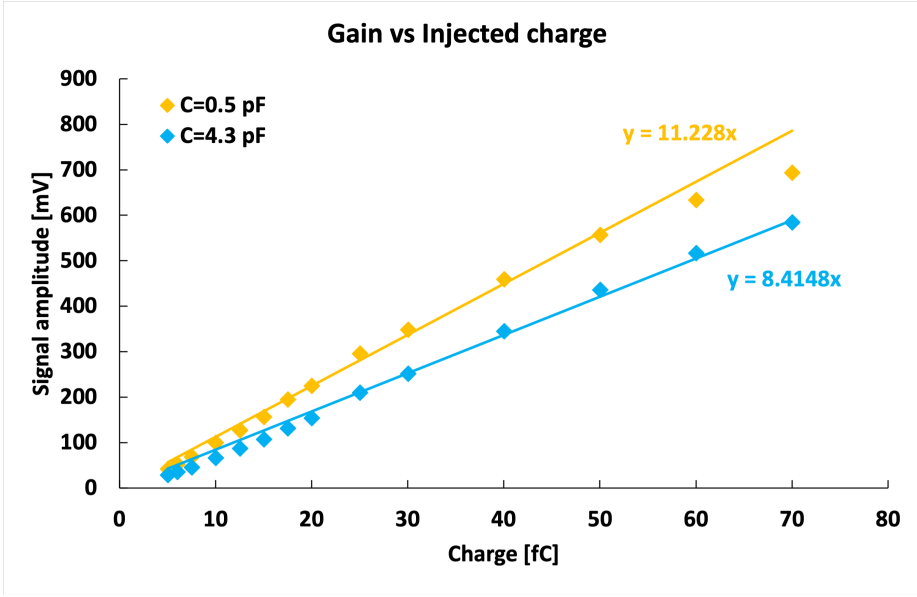


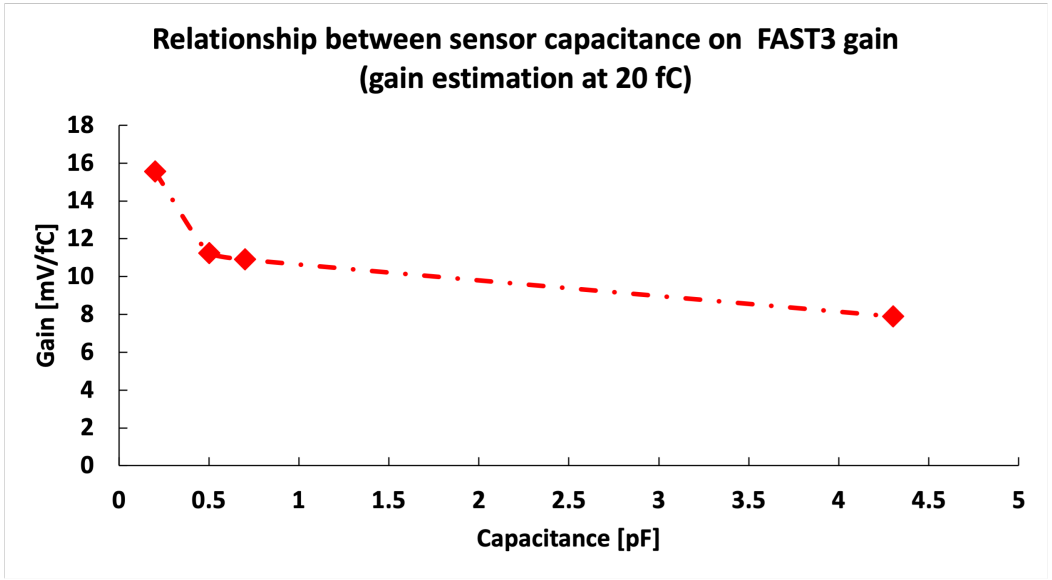
Bipolar signal induced by current signal on adjacent channel

No Electronic Cross-talk was observed

The effect of the sensor capacitance upon FAST3-gain



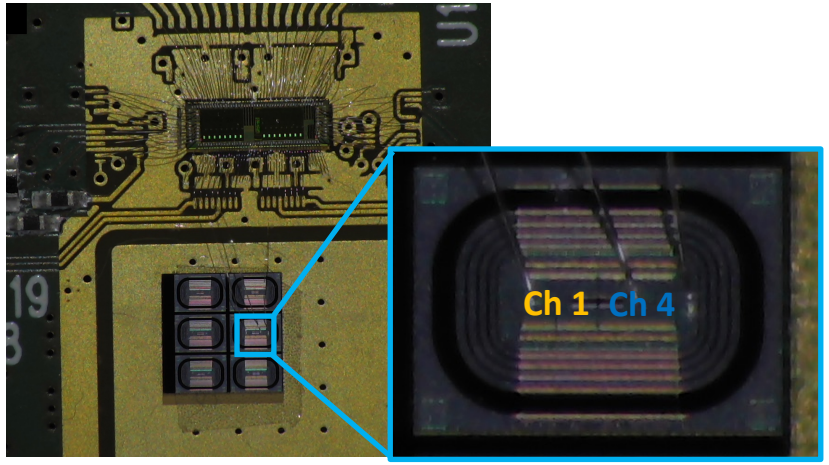




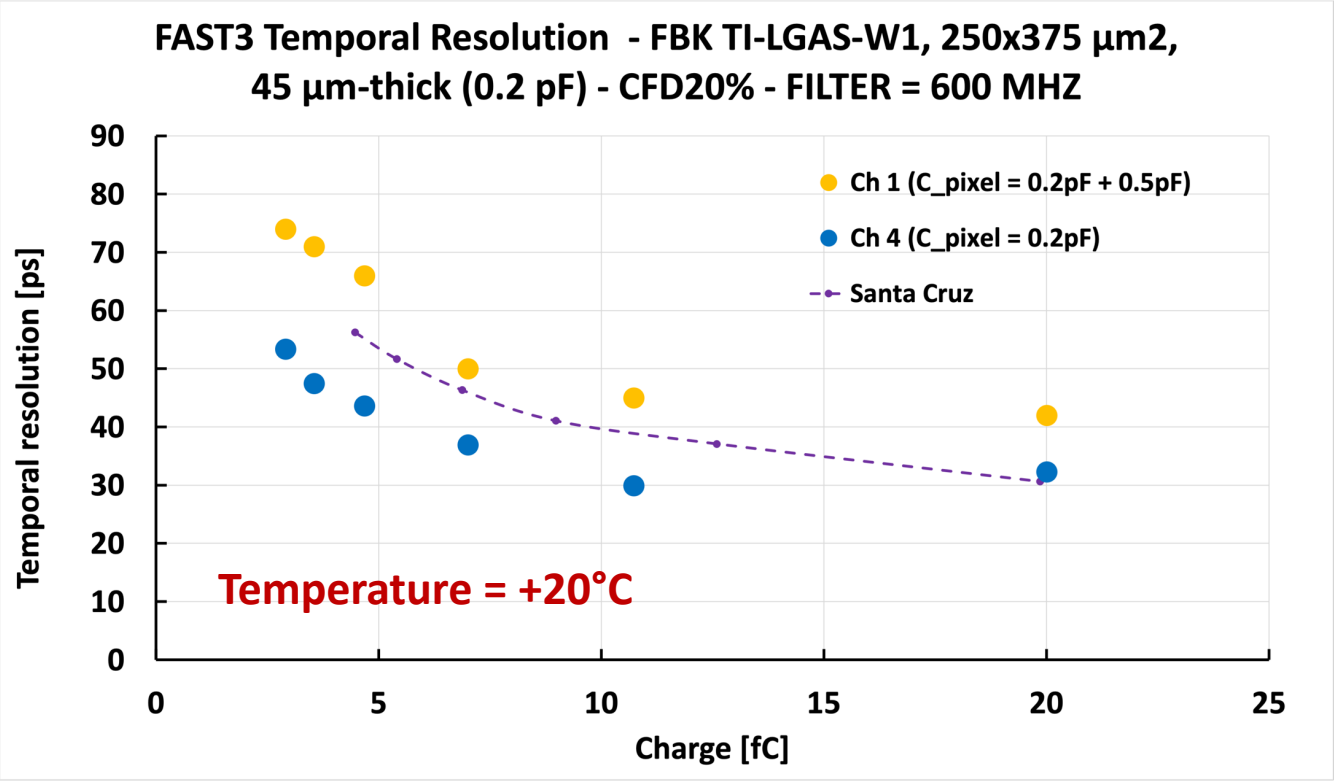
- The capacitance of the sensor affects the gain of FAST3
- The gain of FAST3 decreases with increasing sensor capacitance

The effect of the sensor capacitance on FAST3-performance

ASIC2 + FBK-TI-LGAD1 2x1 array (45µm-thick)
Sensor pixel size: 250 x 375 µm^2 (C_{pixel} = 0.2 pf)



- Ch 1 → C = 0.5pF + 0.2pF (C_{pixel})
- Ch 4 → C = 0.2pF (C_{pixel})



- The difference in performance between Ch1 and Ch4 is solely due to the different capacitance in input to FAST3-channels
- FAST3 performance are for smaller pixels (C_{pixel} < 0.5pF)

Conclusions

- FAST3-ASIC has been successfully produced at the end of 2023
- Preliminary characterization with pulser showed:
  - Good linearity of the gain as a function of the injected charge
  - Gain of ~ 10-11 mV/fC
  - Excellent temporal jitter, below 25 ps at 10 fC of charge
  - Good uniformity of gain and temporal jitter between different channels and ASICs+
  - Good agreement between measured and simulated jitter

- Preliminary tests of FAST3 coupled with LGADs have been performed with β-source
  - The couple FAST3-LGADs achieves temporal resolution of 30-35 ps, comparable with the state-of-art electronic for LGAD read-out
  - The FAST3-channels isolation is excellent, no cross-talk between adjacent channel was observed
  - A relationship between sensor capacitance and FAST3-gain and –jitter was observed

FAST3 is an excellent multichannel amplifier suitable to readout LGAD sensors

RD50-DRD3 project

16-channel amplifier for thin Low Gain Avalanche Diodes based on the FAST3 ASIC – FAST3-Amplifier

Project activities and deliverables:

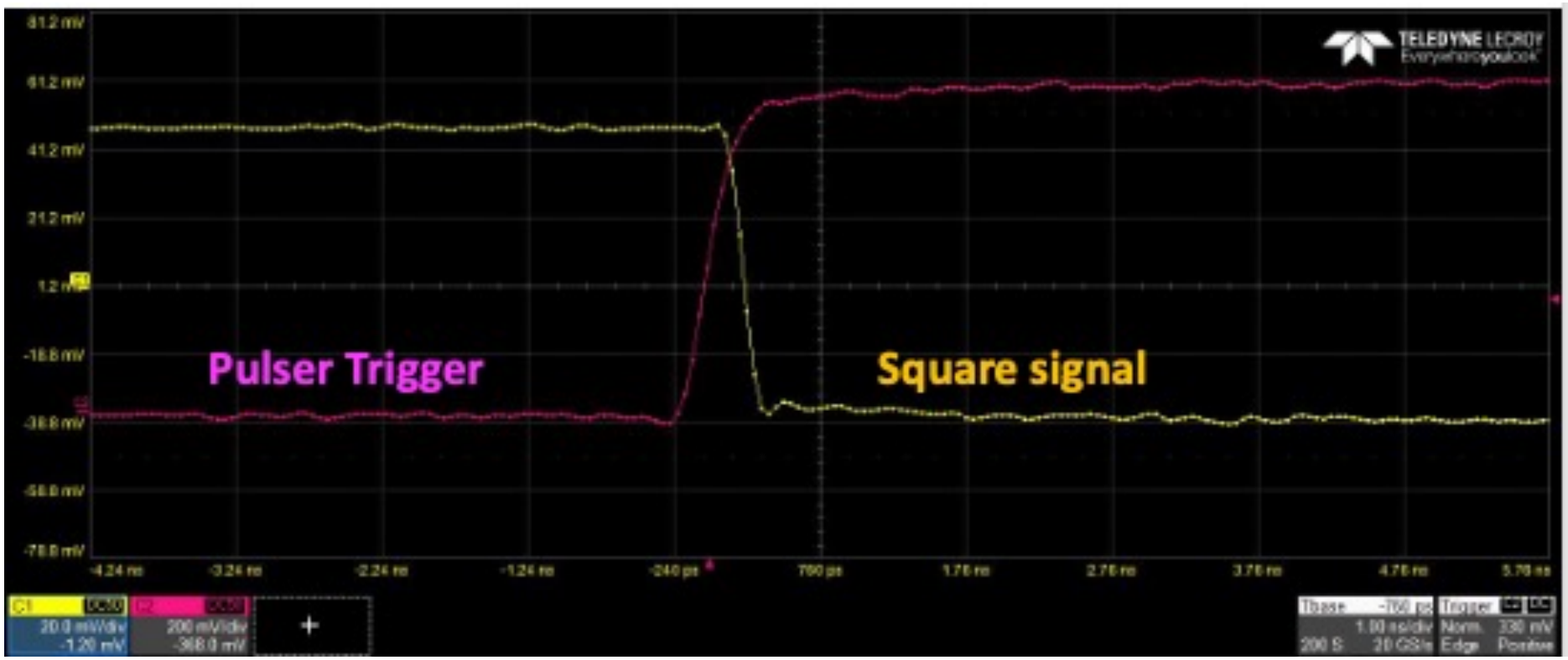
- Development of a packaging technology for FAST3
- the design, production, and assembly of a dedicated read-out board
- Distribution of the product to the involved groups.

Involved institutes:

- INFN Torino
- UC Santa Cruz
- CERN
- Jozef Stefan Institute
- HEPHY
- TU Dortmund
- KIT

Backup

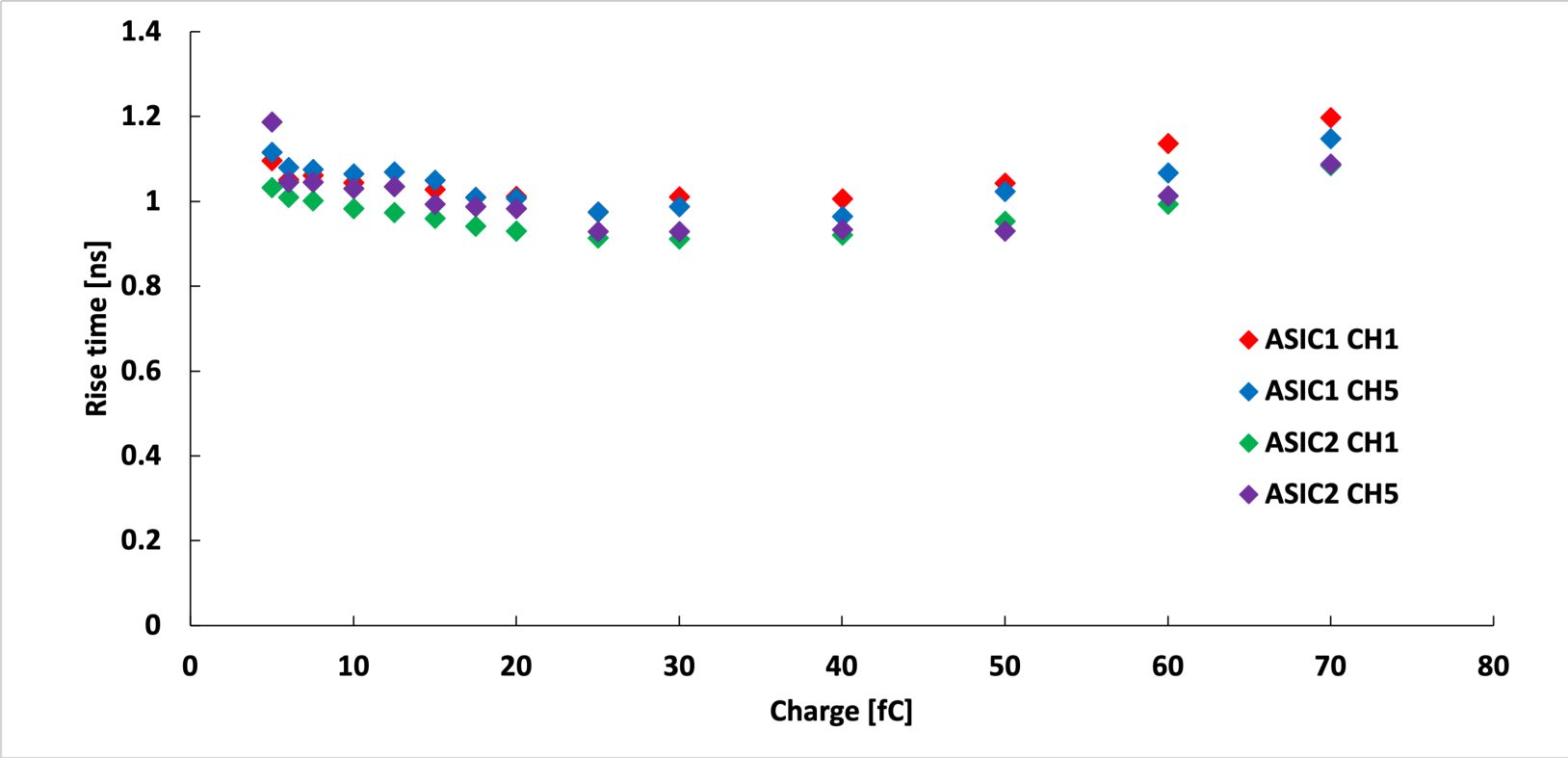
Pulser Jitter



The temporal jitter of the pulser has been measured as the standard deviation of the temporal distance between the trigger signal and the square signal generated by the Pulser

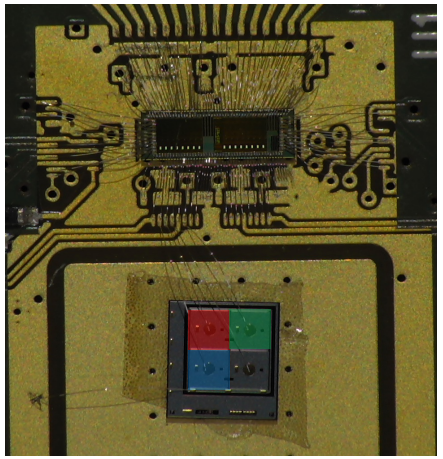
Rise time uniformity

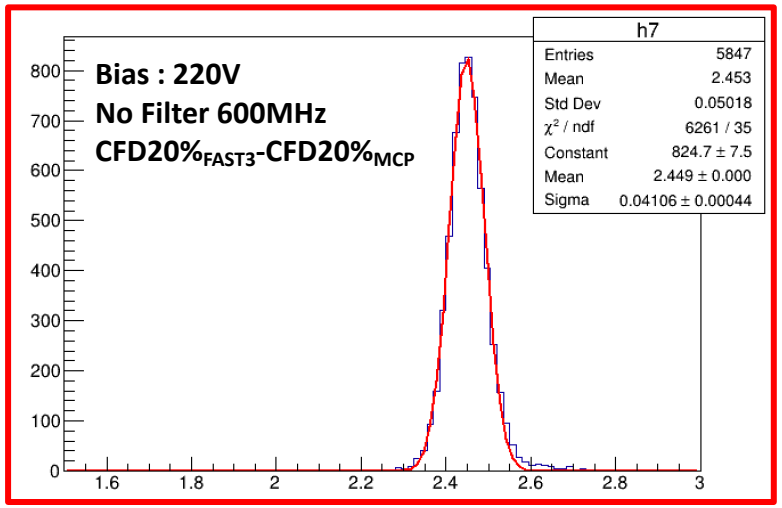
The studies for gain and jitter uniformity have been performed on 2 ASICs and two channel for each ASIC

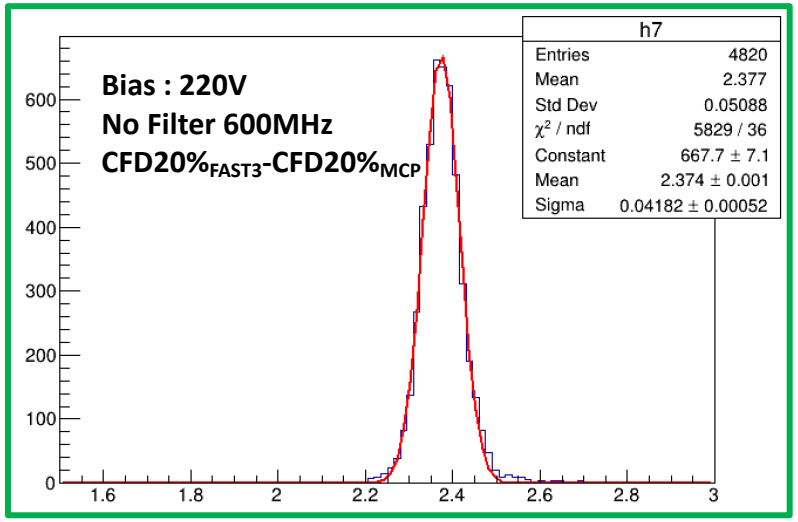


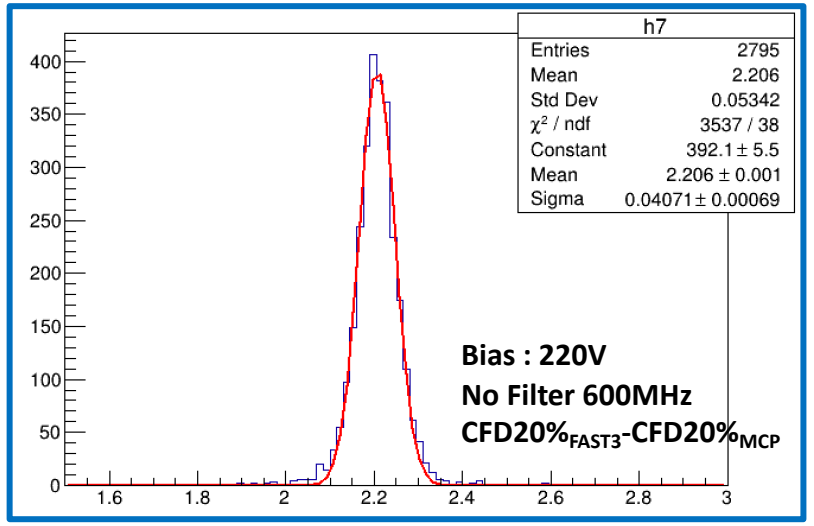
Temporal resolution distribution

ASIC1 + HPK2-Split4 2x2 array (45µm-thick)
Sensors pixel size ~ 1.3 x 1.3 mm^2 (C = 3.8 pf)



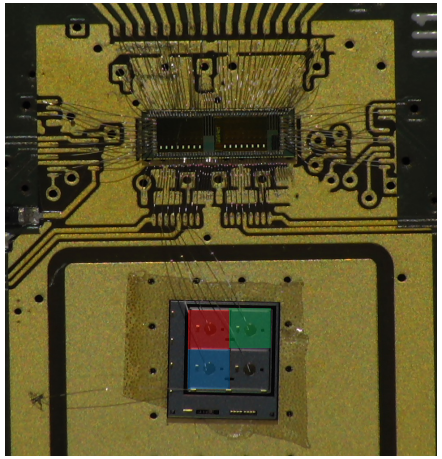


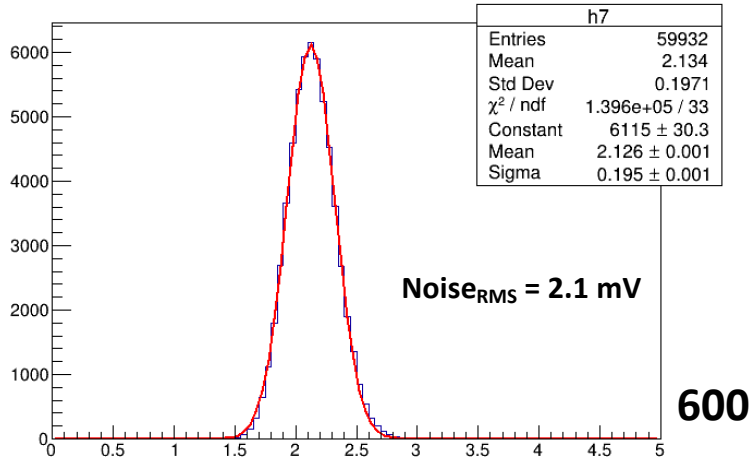




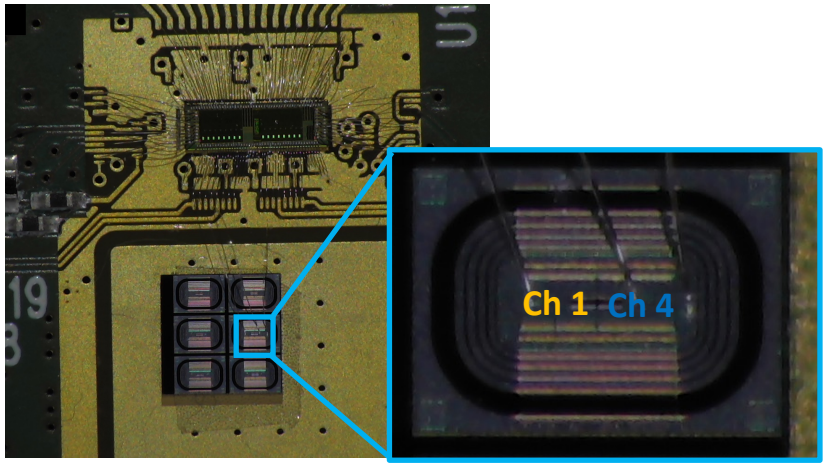
RMS Noise

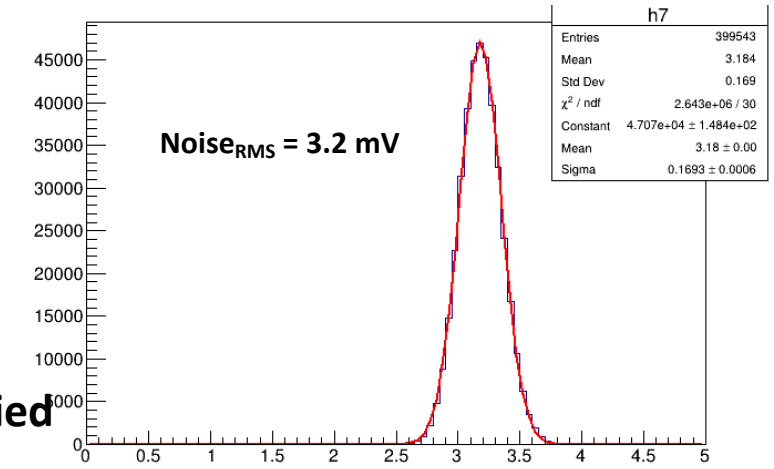
ASIC1 + HPK2-Split4 2x2 array (45µm-thick)
Sensors pixel size ~ 1.3 x 1.3 mm^2 (C = 3.8 pf)





ASIC2 + FBK-TI-LGAD1 2x1 array (45µm-thick)
Sensor pixel size: 250 x 375 µm^2 (C_{pixel} = 0.2 pf)

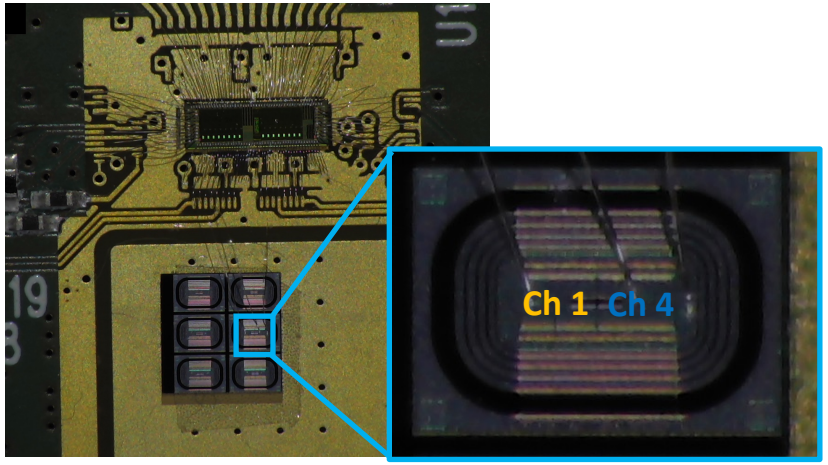




600 MHz filter not applied

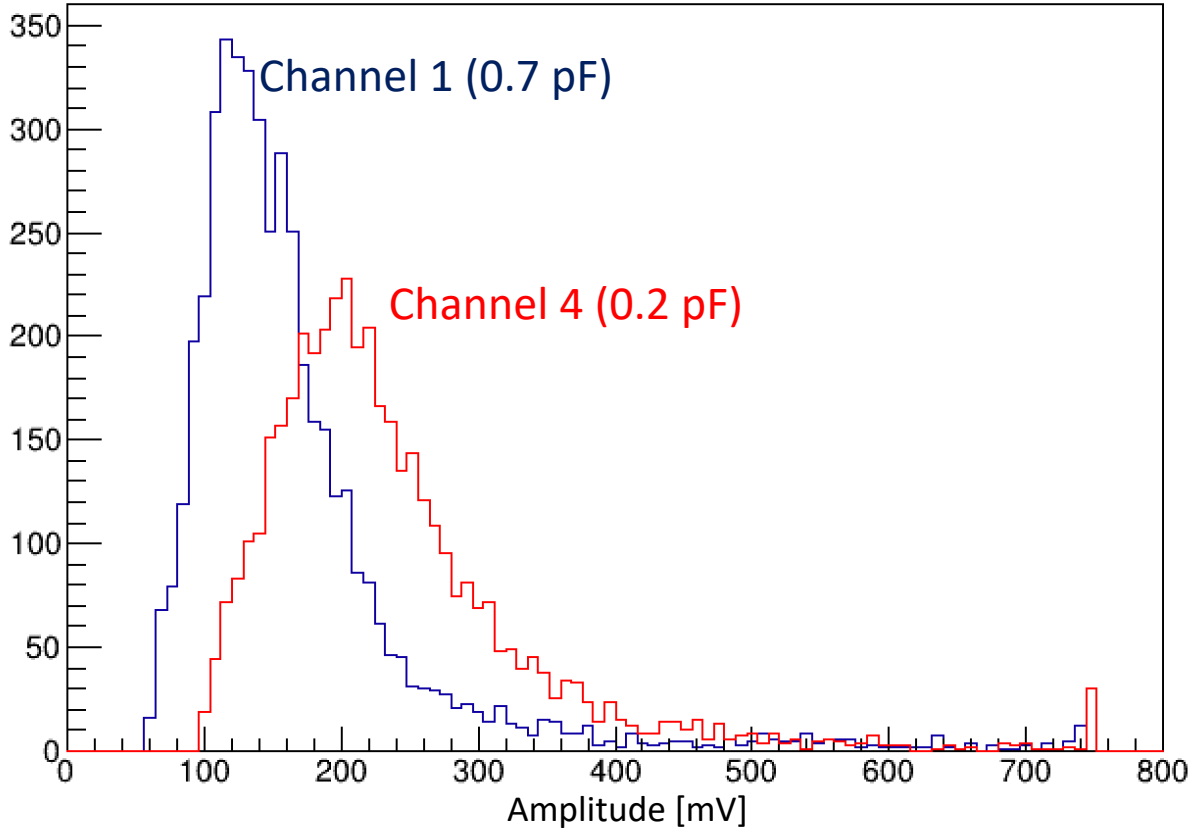
The effect to the capacitance on the signal amplitude

ASIC2 + FBK-TI-LGAD1 2x1 array (45µm-thick)
Sensor pixel size: 250 x 375 µm^2 (C_{pixel} = 0.2 pf)



- Ch 1 → C = 0.5pF + 0.2pF (C_{pixel})
- Ch 4 → C = 0.2pF (C_{pixel})

Signal amplitude distribution
Bias = 290V – temperature = +20°C



Channel