Silicon Pixel Detector development for a Bent Crystal Channeling Efficiency Measurement at the LHC

SARA CESARE – ON BEHALF OF THE TWOCRYST COLLABORATION

19° TREDI WORKSHOP ON ADVANCED SILICON RADIATION DETECTORS – 20/02/2024

Outline

- Introduction
- Fixed-target experiment with bent crystal
- Detector for proof-of-principle (PoP) test
- Silicon pixel sensors
- Detector integration in a Roman Pot
- Summary

Electromagnetic dipole moments

For particles with spin = $\frac{1}{2}$ we can define

$$\boldsymbol{\delta} = \frac{1}{2} d \mu_B \mathbf{P} \quad \text{EDM}$$

$$\boldsymbol{\mu} = \frac{1}{2} g \mu_B \mathbf{P} \quad \text{MDM}$$

Where P is the polarization vector

$$\mathbf{P} = 2 < \mathbf{S} > / \hbar$$

Hamiltonian of the system

$$H = -\mu \cdot B - \delta \cdot E$$

$$\downarrow \text{T,P}$$

$$H = -\mu \cdot B + \delta \cdot E$$

The EDM violates T and P, therefore it violates CP through CPT theorem.

- **EDMs** are source of possible physics Beyond the Standard Model.

  (not measured yet for charm and beauty baryons and tau leptons)

- **MDMs** provide important anchor points for QCD calculations.

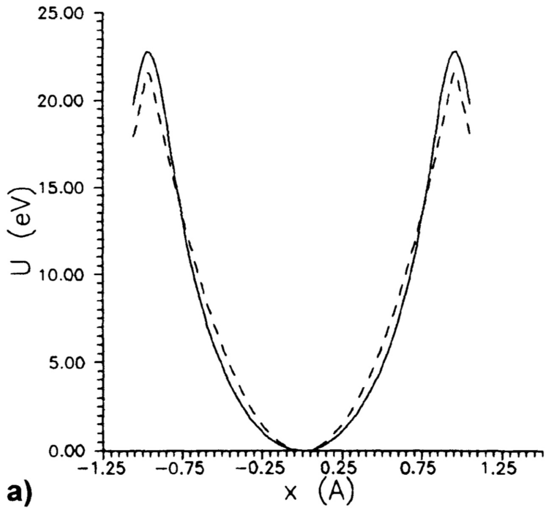
Phys. Lett. B291 (1992) 293

To measure EDM and MDM of short-lifetime particles (~5cm) strong EM field are needed.

In bent crystal we obtain:

- Electric field E ≈ 1 GV/m

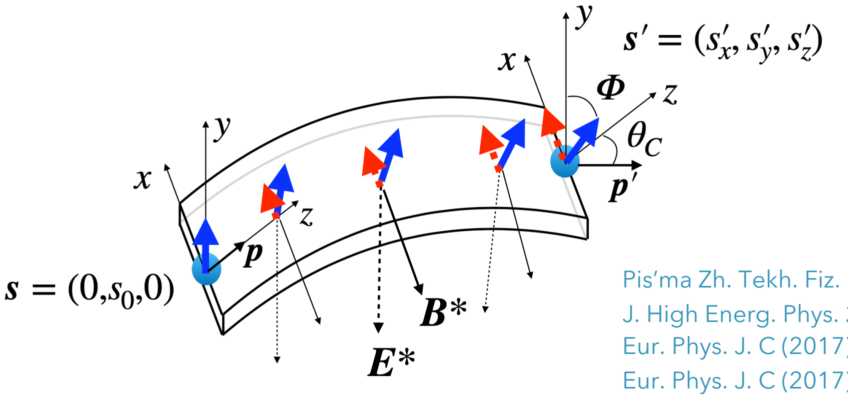
- Effective magnetic field B ≈ 500 T



Positively charged particles are **channeled** between the atomic planes if their impact angle is small enough.

- Steer the particle trajectories of a given angle.
- Induce a **spin precession** of the particles in a short distance

$$\Phi \approx \frac{g-2}{2}\gamma\theta_C \qquad s_x \approx s_0 \frac{d}{g-2}(\cos\Phi - 1)$$

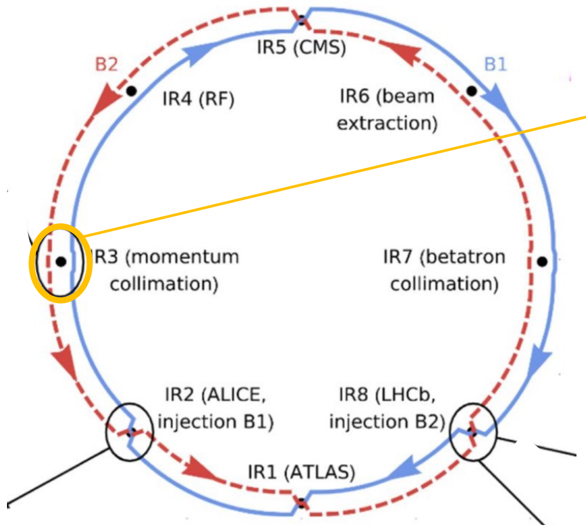


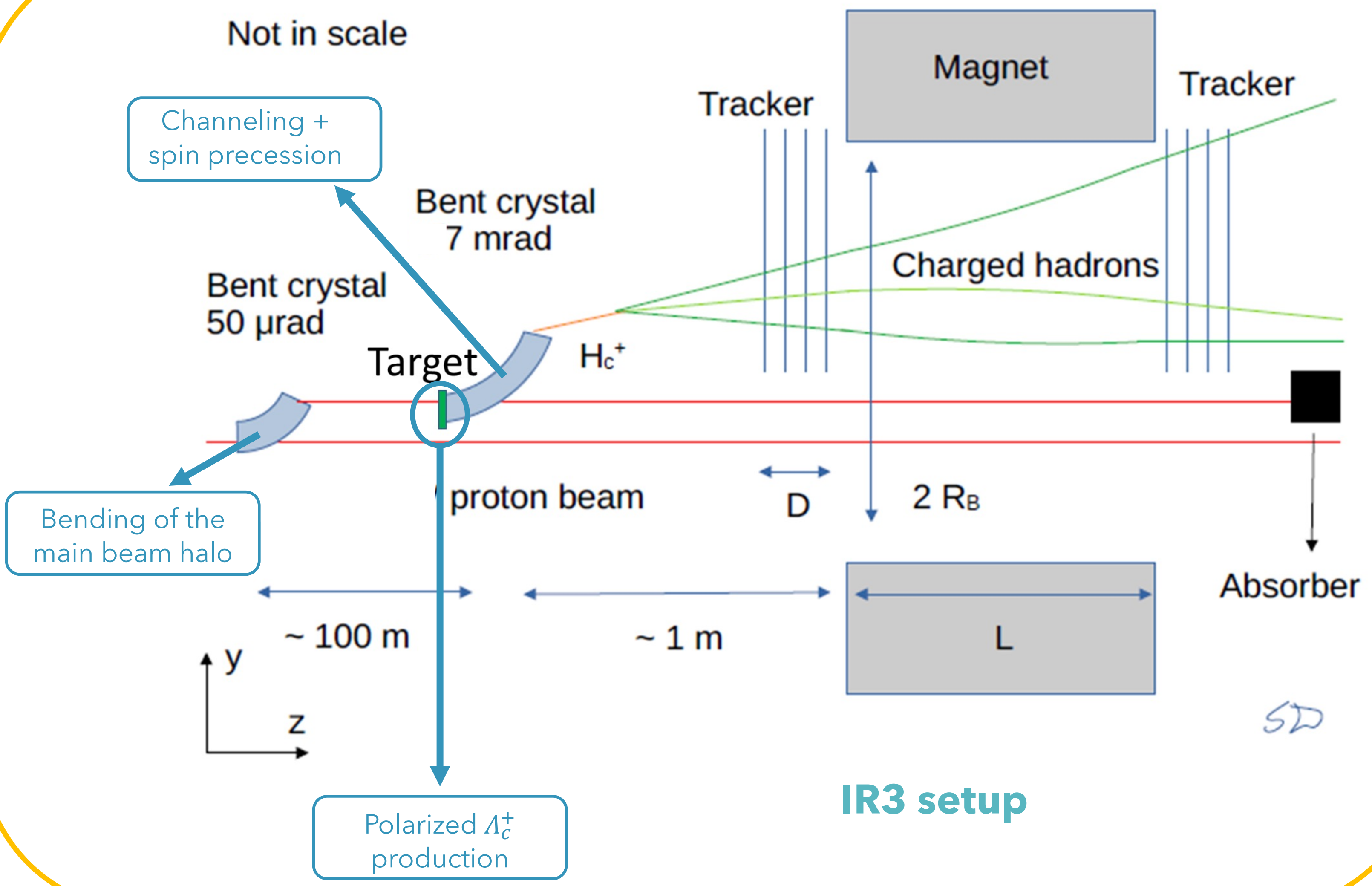
D. Chen et al. [E761 collaboration], Phys. Rev. Lett. 69, 3286 (1992).

Pis'ma Zh. Tekh. Fiz. 5 (1979) 182
J. High Energ. Phys. 2017 (2017) 120
Eur. Phys. J. C (2017) 77:181
Eur. Phys. J. C (2017) 77:828

Two alternative scenarios:

1. Target placed in front of the LHCb detector.
2. New independent experiment at IR3 (LHC).





Proof-of-principle test (PoP)

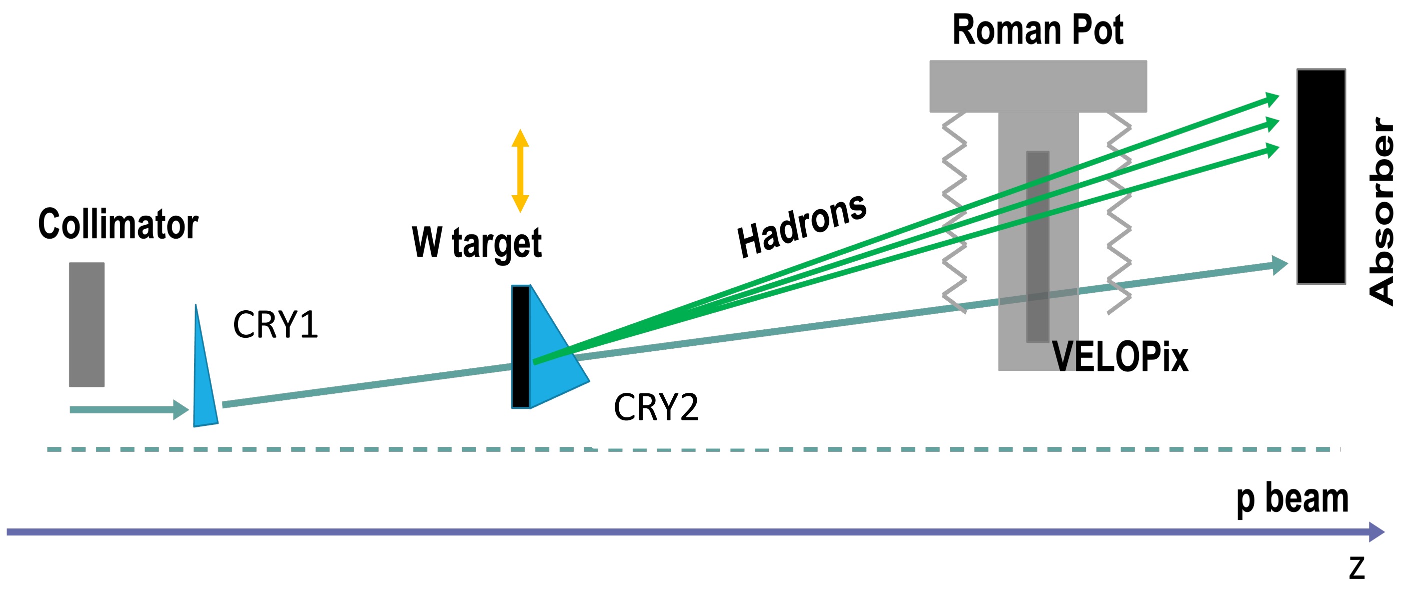
The PoP test is called TWOCRYST and was approved by the LMC (LHC Machine Committee) to take data in 2025.

Goals of the test

1. Demonstrate the operational feasibility of the double crystal and tracking detector setup at the LHC
2. Confirm the estimated achievable rates of proton on target
3. Measure channeling efficiency of long crystals at TeV energies
4. Background studies

Experimental set-up

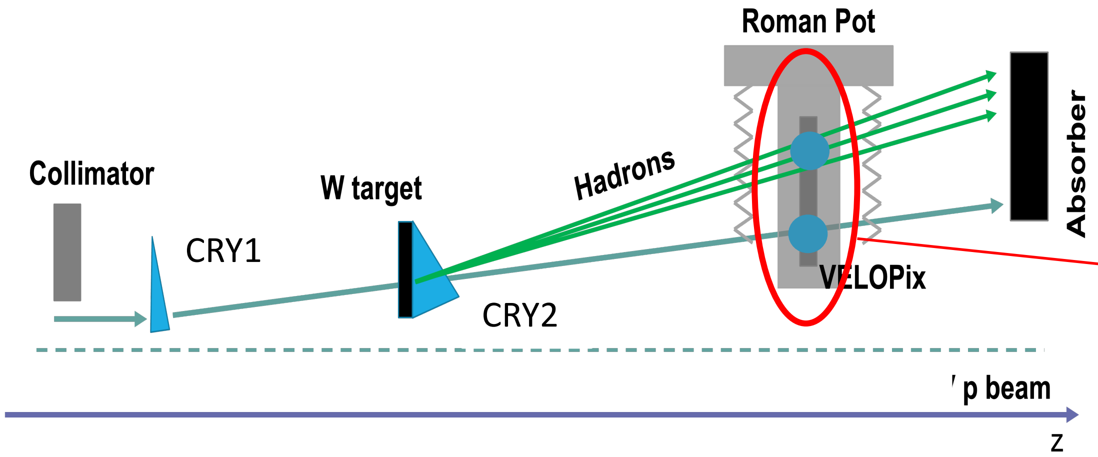
- Short crystal for beam-halo deflection
- W target
- Long crystal for Λ_c^+ channeling
- One tracking station in a Roman Pot
- Absorber

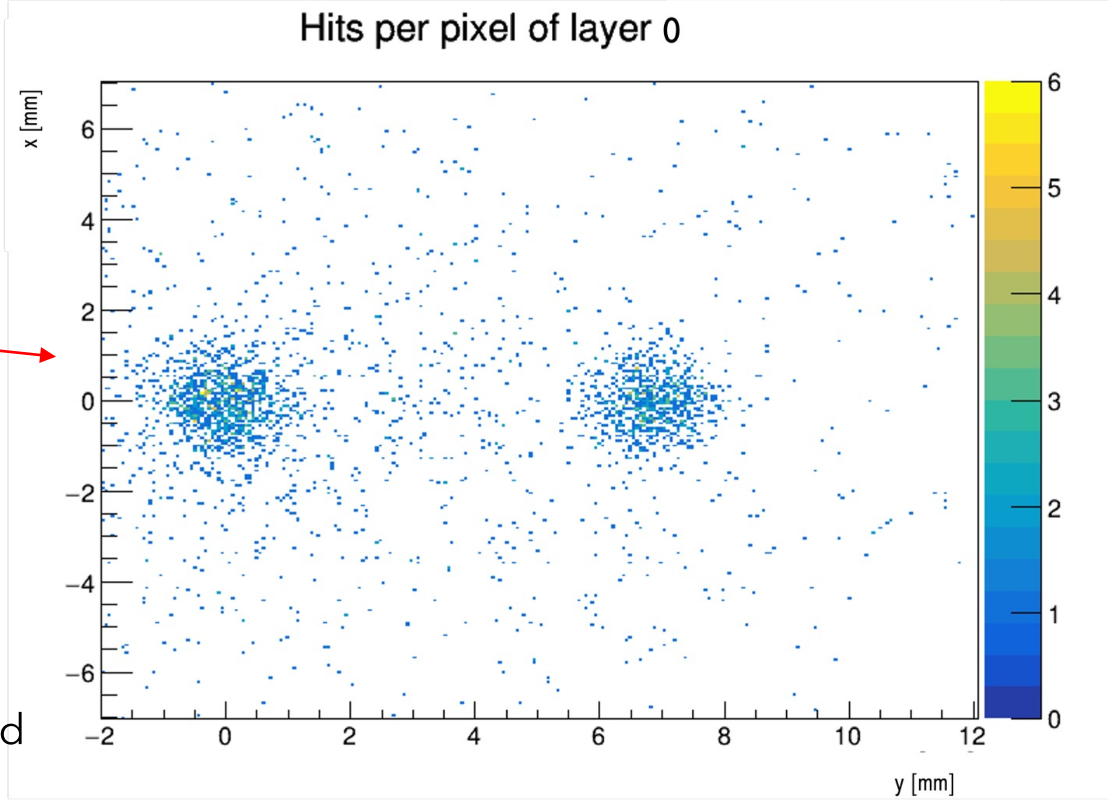


Proof-of-principle test

Measurement of the channeling efficiency

- Simulation studies of 1 TeV protons channeled with the double crystal setup
- Second crystal – tracker layer distance **d=1m**
- Need to measure both the channelled and unchanneled protons from the second crystal.





Background studies

- High granularity is needed to resolve between tracks in pW and pSi collisions (with target in place) in the future experiment

Detector specifications – Proof-of-Principle

Detector requirements

- Minimum 1 layer for background studies and channelling efficiency

- Detect both channelled and unchanneled particles

↓

Active area $\geq 1\times1$ cm^2

- Distance between main circulating beam and centre of the target is < 1 cm

↓

tracking detector must inside the beam pipe

Solution: Roman Pot

- Expected fluences of $\sim 10^{12}$ 1 MeV n eq/cm^2 → detector can operate at room temperature

Technology	Silicon pixel sensors
N layers	≥ 1
Distance target-first layer	70 ± 5 cm
Transverse distance from the LHC beam	0.5-1 cm
Active area	$\geq 1\times1$ cm^2
Granularity	< 100 μm
Radiation hardness	$\sim 10^{12}$ 1 MeV n eq/cm^2
Operational temperature	$< 20°$ C

Detector specifications – Final experiment

Detector requirements

- Distance target-first layer is optimised for the reconstruction of the invariant mass of $\boldsymbol{\Lambda_c}$

- Resolve between background tracks at first layer

↓

Detector granularity < 100 μm

Silicon pixel sensors

- Expected fluences of $\sim 10^{15}$ 1 MeV n eq/cm^2

↓

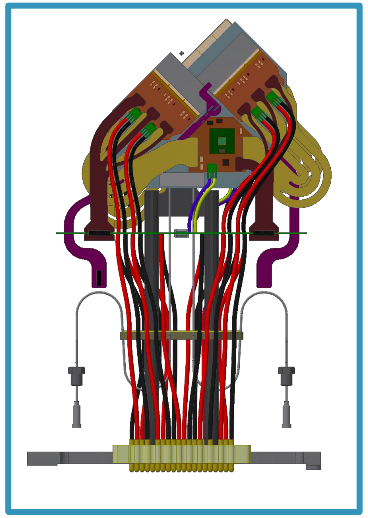
detector must operate at lower temperature

Technology	Silicon pixel sensors
N layers	≥ 1
Distance target-first layer	$70 \pm 5\ cm$
Transverse distance from the LHC beam	0.5-1 cm
Active area	$\geq$ 1×1 cm^2
Granularity	$< 100\ \mu m$
Radiation hardness	$\sim 10^{12}\ 1\ MeV\ n\ eq/cm^2$
Operational temperature	$<\ 20°\ C$

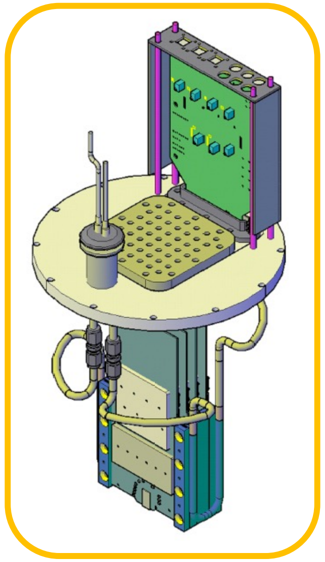
2D Pixel detector proposal

Modular tracking detector based on:

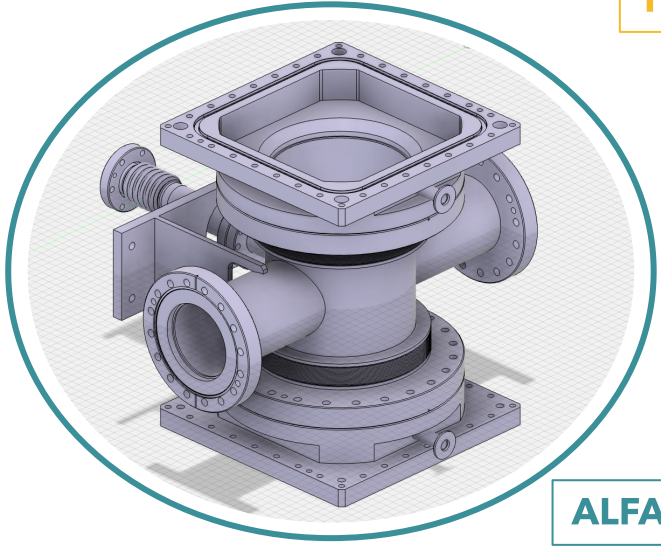
- LHCb Vertex Locator (VELO) silicon pixel sensors + ASIC and readout chain
- CMS TOTEM experiment mechanical support and cooling
- ATLAS ALFA experiment Roman Pot



VELO module



TOTEM support

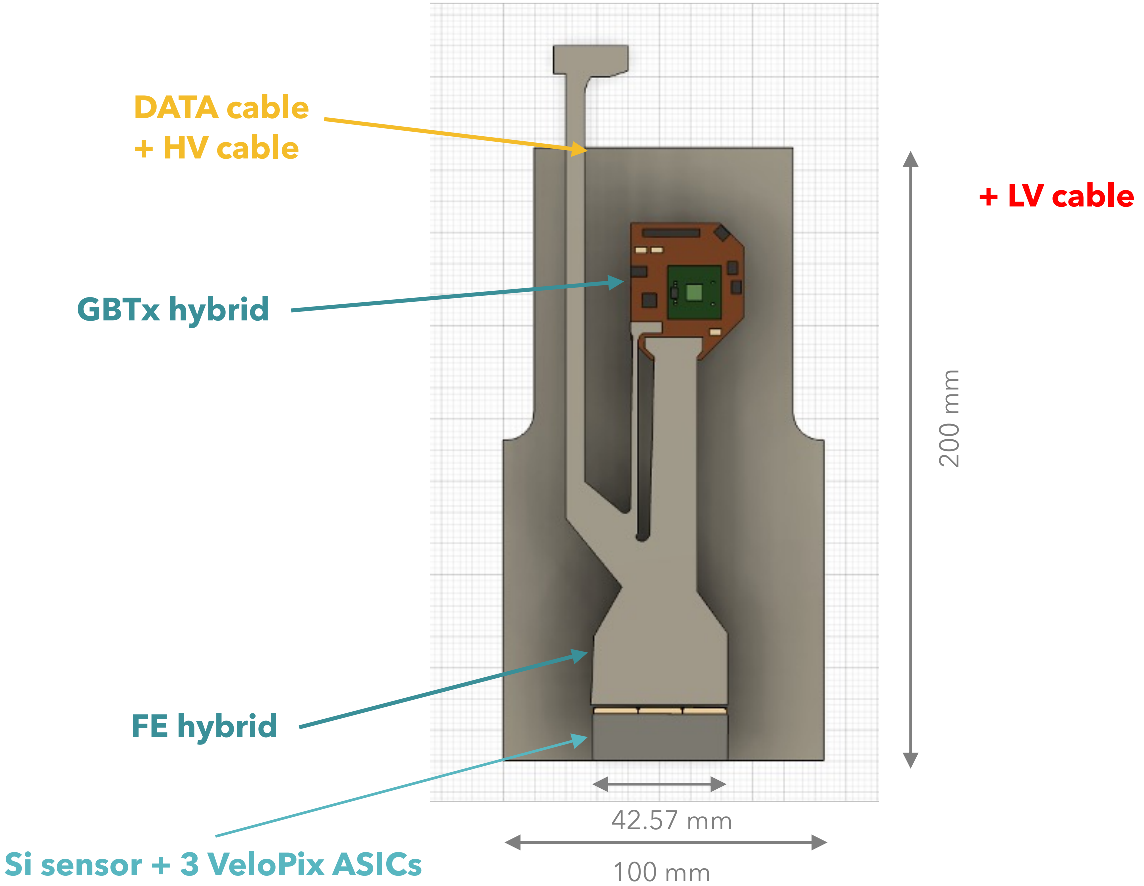


ALFA Roman Pot

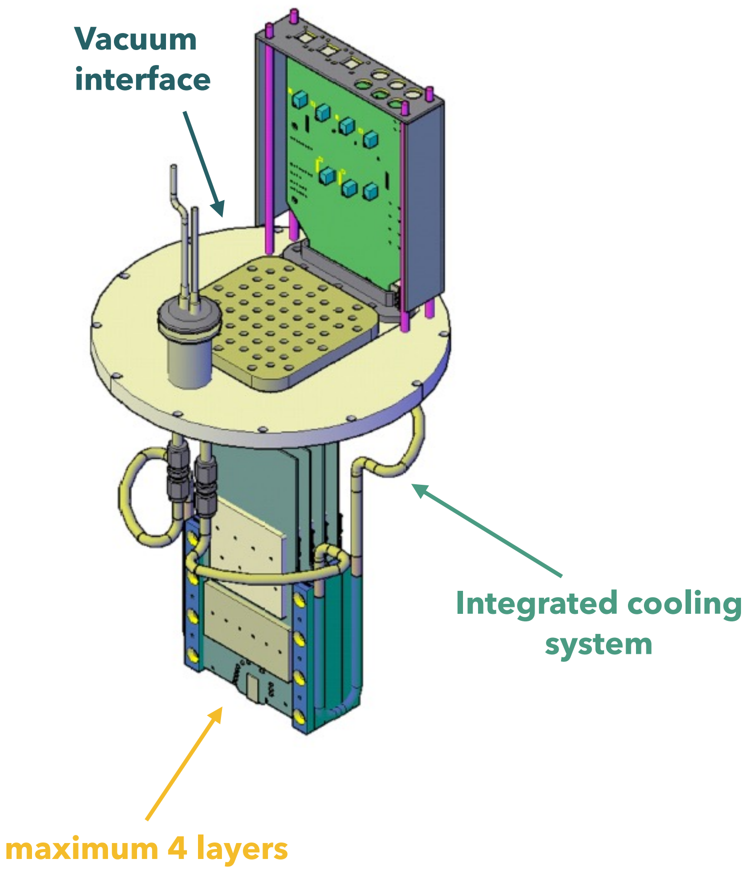
https://cds.cern.ch/record/1624070/files/LHCB-TDR-013.pdf
https://cds.cern.ch/record/2017378/files/ATLAS-TDR-024.pdf
https://iopscience.iop.org/article/10.1088/1748-0221/3/08/S08007/pdf

Tracking module

Tracking module

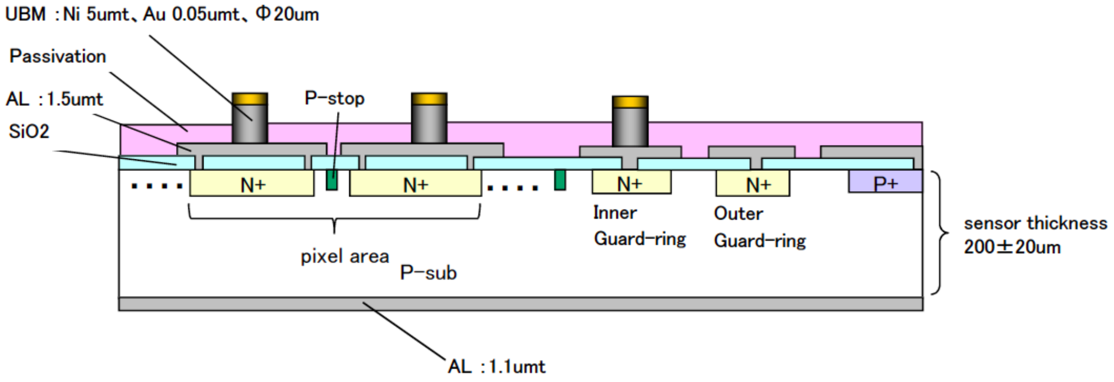


TOTEM mechanical suport



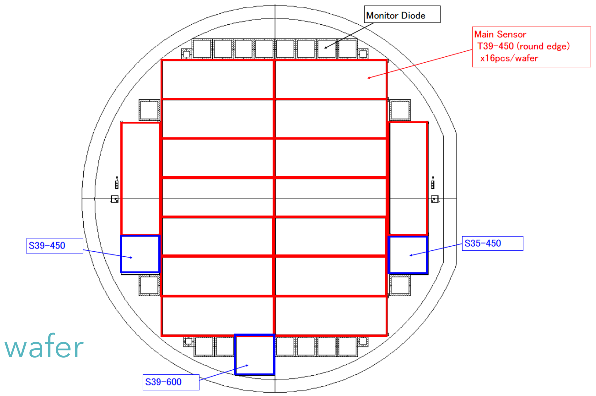
HAMAMATSU silicon sensors – same as LHCb VELO detector

- High resistivity p-type float-on silicon wafers
- Thickness – 200 μm
- Active area – 42.57 x 14.08 mm^2
- In the regions between ASICs the pixels are elongated by a factor 2.5 to allow a gap between the ASICs
- The pixels are metallised with Ni/Au UBM pads



Bulk material thickness	200 μm n-on-p silicon
Most probable unirradiated signal charge	16 000 e^-
Minimum end-of-life signal charge	6 000 e^-
Maximum operational voltage	800 V
Required charge collection efficiency	> 99%

Sensors wafers have been purchased from HAMAMATSU and have been delivered at CERN in November 2023



Sensor wafer

https://edms.cern.ch/ui/#!master/navigator/document?P:1340134179:100310887:subDocs

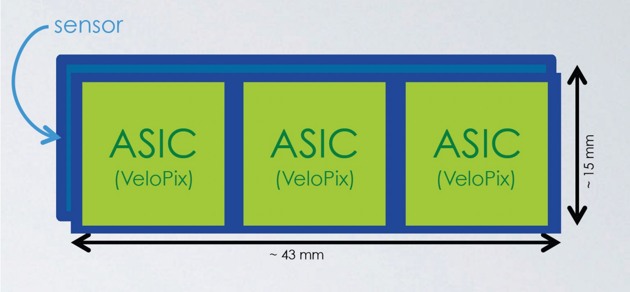
VeloPix ASICs

- Commercial 130 nm CMOS
- 256 x 256 pixel with 55 μm pitch
- Chip size 14.14 x 16.60 mm^2
- Radiation hardness up to 8×10^{15} 1 MeV n eq/cm^2
- Super-pixel readout logic
  - Fast return to baseline - 300 ns
  - 2 event deep buffer
  - Column bus data transfer rate 13.3 M packet/s

VeloPix received from the VELO group and bump bonded to the sensors by ADVAFAB company

Bonded finished and tiles received in January 2024

3 ASICs = 1 tile



Technology	TSMC 130 nm CMOS
Radiation hardness	> 4 MGy, SEU tolerant
Pixel size (analogue part)	$55\,\mu m \times 55\,\mu m$ ($55\,\mu m \times 14.5\,\mu m$)
Peak rate per ASIC (per pixel)	9×10^8 hits/s (5×10^4 hits/s)
Maximum of charge distribution	16 000 e^-
Minimum threshold	500 e^-
Timing resolution (range)	25 ns (9 bits)
Super-pixel data size	30 bits
Maximum data rate per ASIC	20.48 Gbit/s
Power consumption per ASIC	$\sim$ 1.2 W (spec. 3 W)

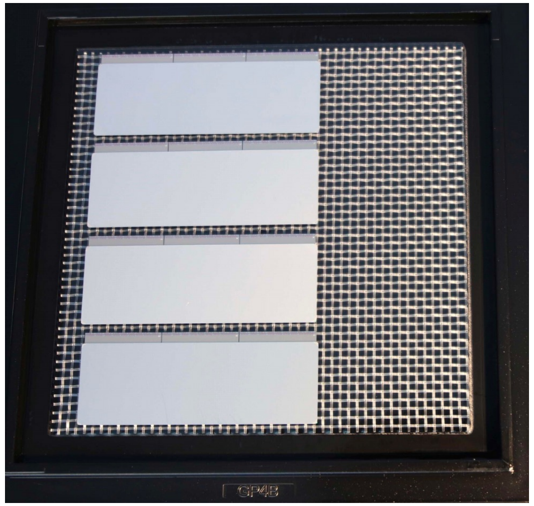
https://cds.cern.ch/record/2692574/files/MCWG_LHC_TID_Run2_report_ostein_kbilko_08102019.pdf
https://dx.doi.org/10.1088/1748-0221/9/01/C01007

Tiles Quality Assurance

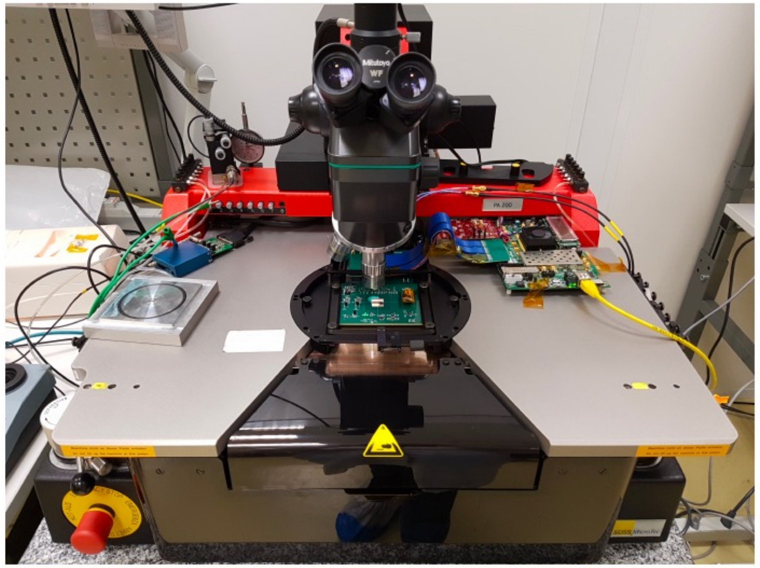
BUMP-BONDING QA (ADVAFAB)

- Visual inspection of the wafer ASIC and bump quality
- IV measurements
- Delivered in gel-packs

Tiles



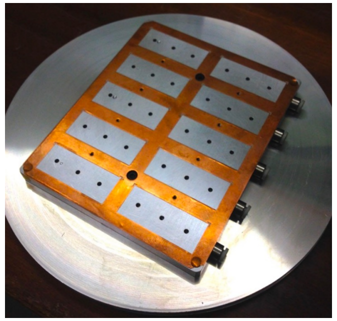
Probe station



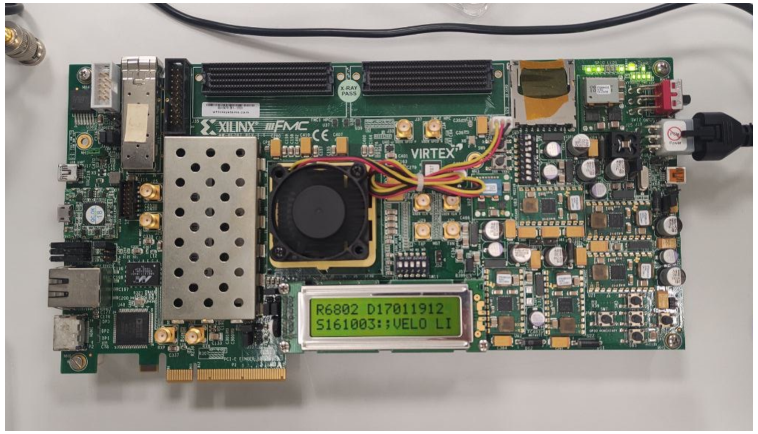
TILES QA (VELO PROCEDURE)

Setup for functional test

- Designed dedicated holder
- Karl Suss PA200 semiautomatic probe- station (PS).
- SPIDR readout board
- Bias the sensors with HV needle



Tiles holder



SPIDR board

Test setup at CERN DSF clean room

Special thanks to Victor Coco from the VELO group

Tiles Quality Assurance

Functionality test of the ASIC

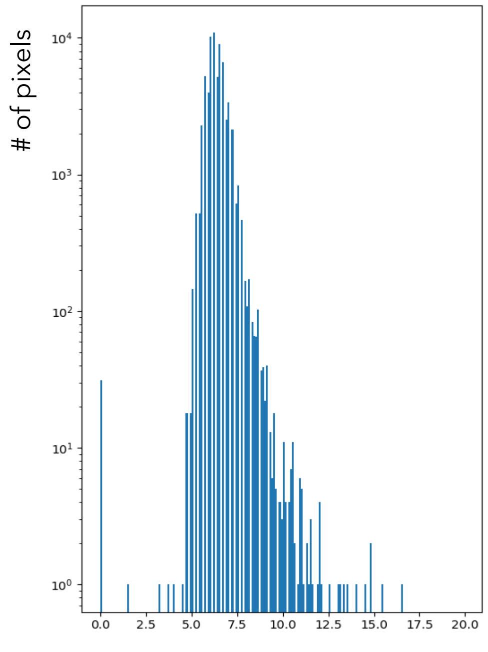
- power-up test
- register test
- ECS matrix test
- DAC scan
- Responses to TFC commands
- Fast equalisation and noise scan.

Scan each ASIC for:

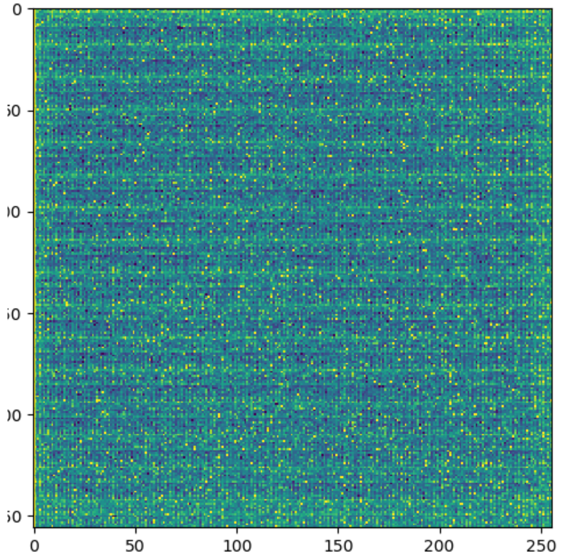
- Masked pixel (non-equalisable)
- Shorted pixel
- Missing pixel

$V_{bias} = -30\ \mathrm{V}$

$I_{bias} = -0.03\ \mu A$



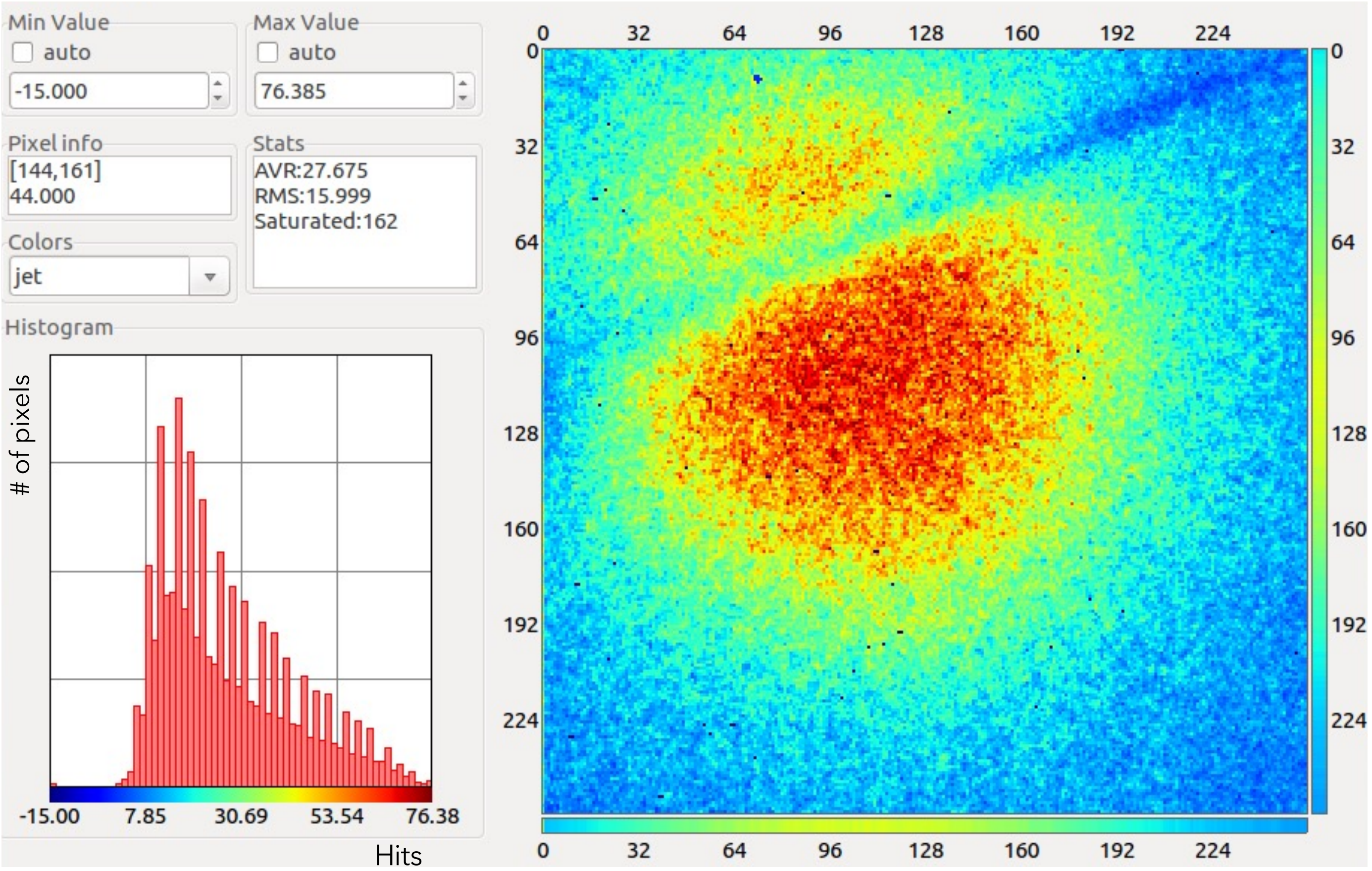
Noise scan



Uniformity check of the noise in all the pixels of one chip of the tile.

Source test with Sr90

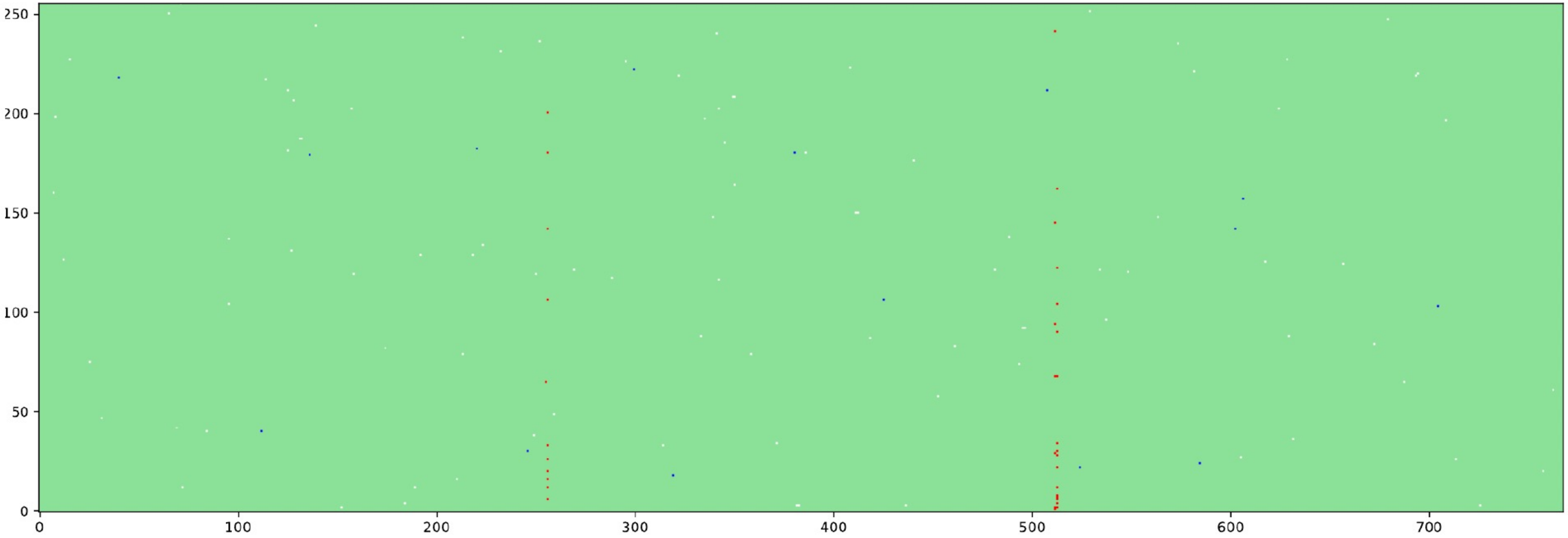
Hit distribution on the chip after being irradiated, the blue area in the middle is due to the presence of the HV needle.



Example of one perfect tile – reference from previous VELO testing campaign

Good pixels: 196465 | 0.0000 %
Masked pixels (white): 95 | 0.0000 %
High Noise pixels (>3*mean): 15 | 0.0000 %
Missing TP: 33 | 0.0000 , Fake TP on neighbourg: 0 | 0.0000 ,Fake TP on neighbourg and Missing TP: 0 | 0.0000 %
Missing Bump: 0 | 0.0000 %

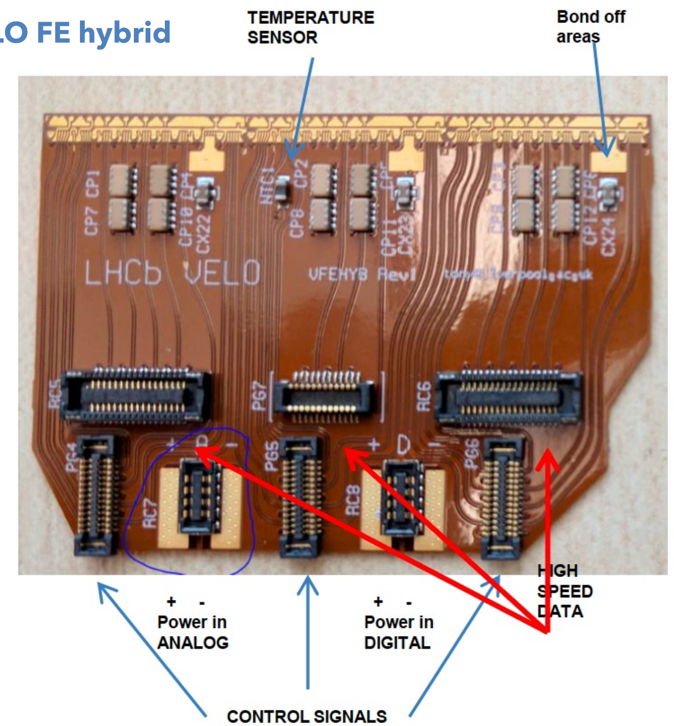
Pixel grading of one VELO tile (three chips)

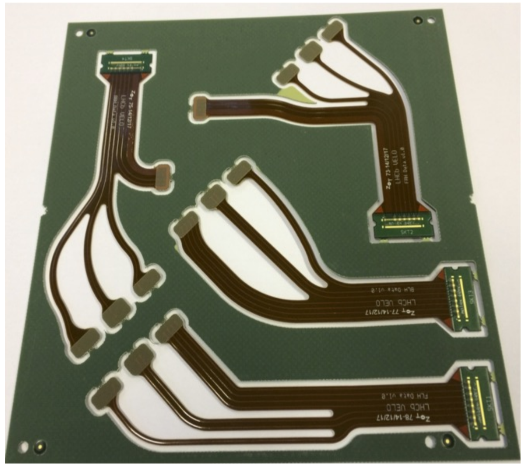


FE hybrid and data cable integration

- Due to the Roman Pot geometry the curved cables have to be redesigned in a straight version
- Integration of the VELO Front-End hybrid and data cables + HV in one single flex cable
- First semi-rigid part to help the wire bonding process
- Flex part routing fast signals and HV to the feed-though and control signals from the GBTx
- Advantage: reduction of the number of connectors

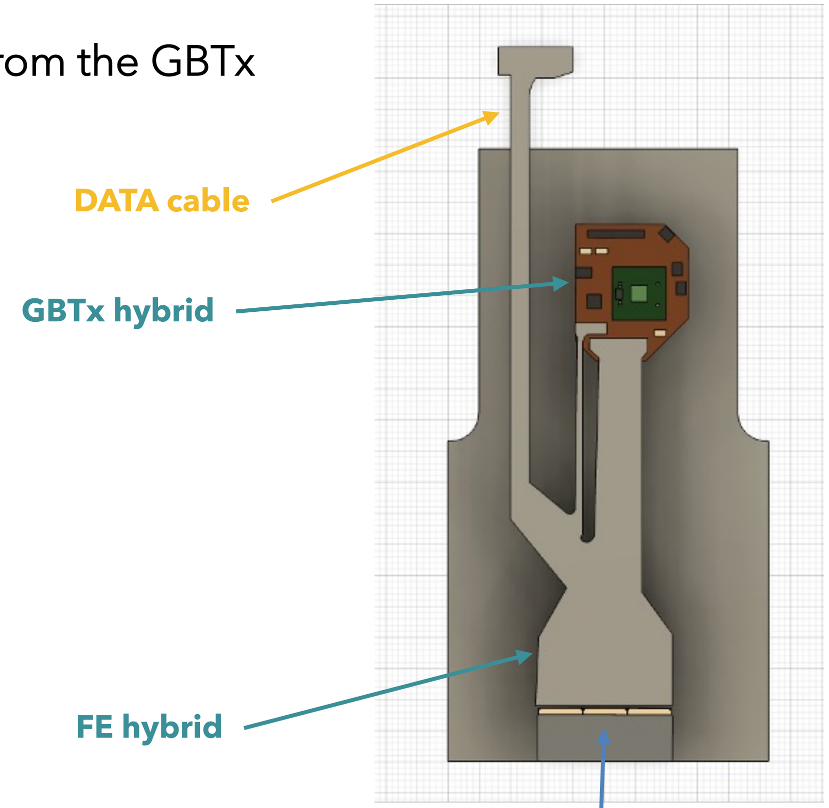
VELO FE hybrid





VELO DATA cables

Tracking module



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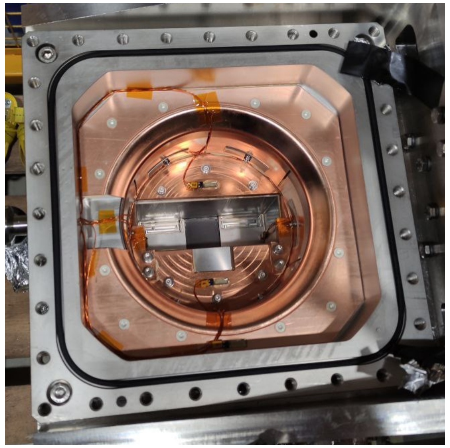
Roman pot box and cooling system

Roman Pot



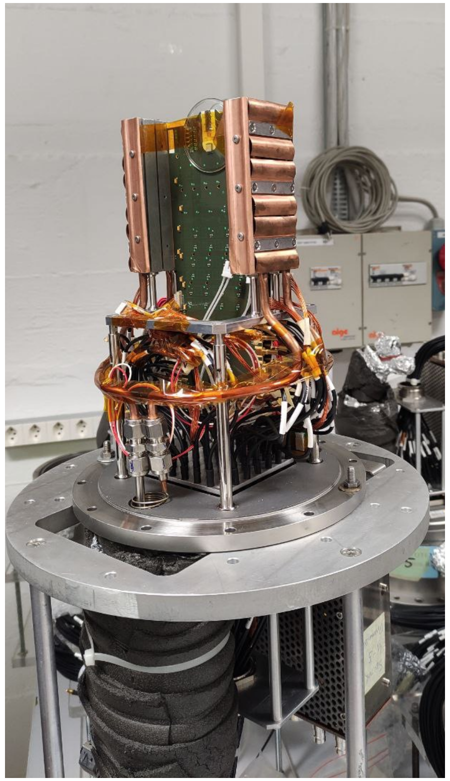
Roman Pot station

ALFA roman pot

- Two ATLAS ALFA Roman Pot stations have already been extracted from the LHC tunnel
- Control system for vertical movement
- Possibility to use both ATLAS ALFA and CMS TOTEM detector package and cooling system
- Diameter of the outer cylinder of the pot ~ 15 cm

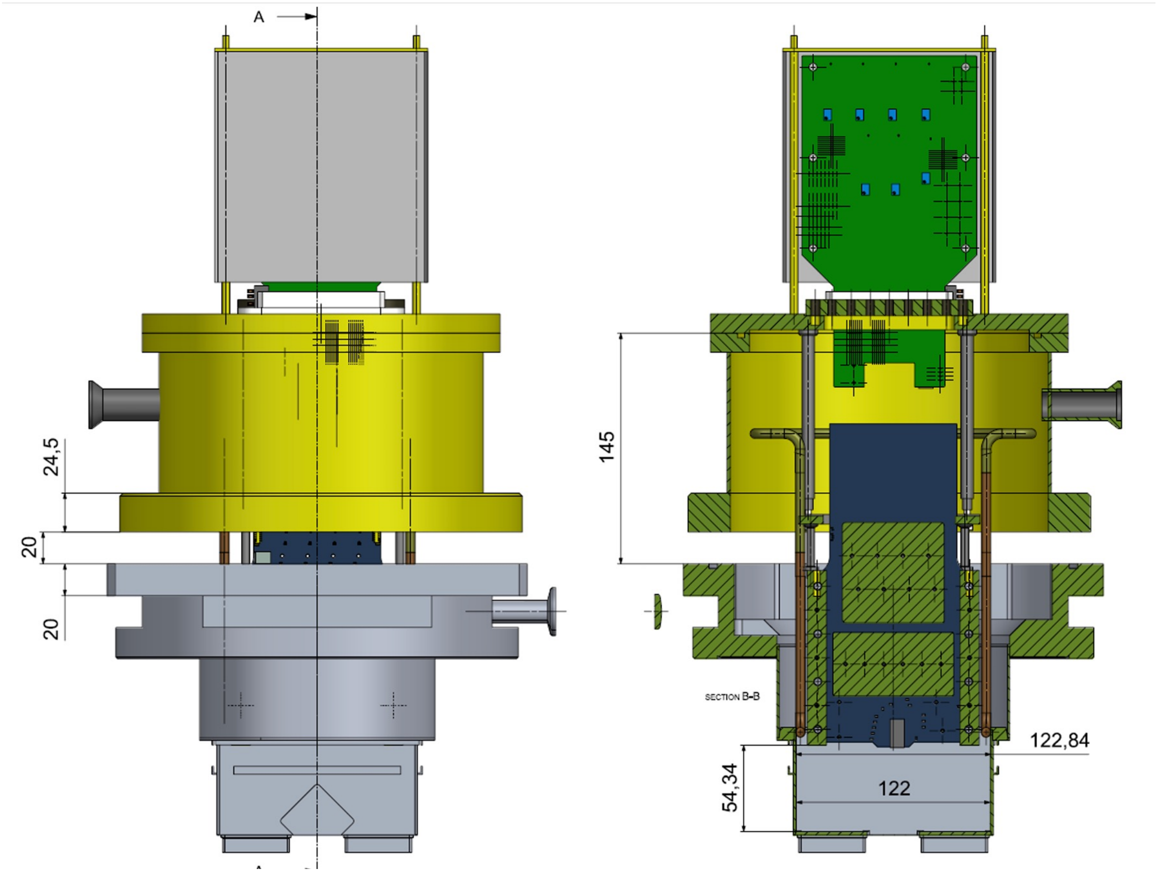
Cooling system

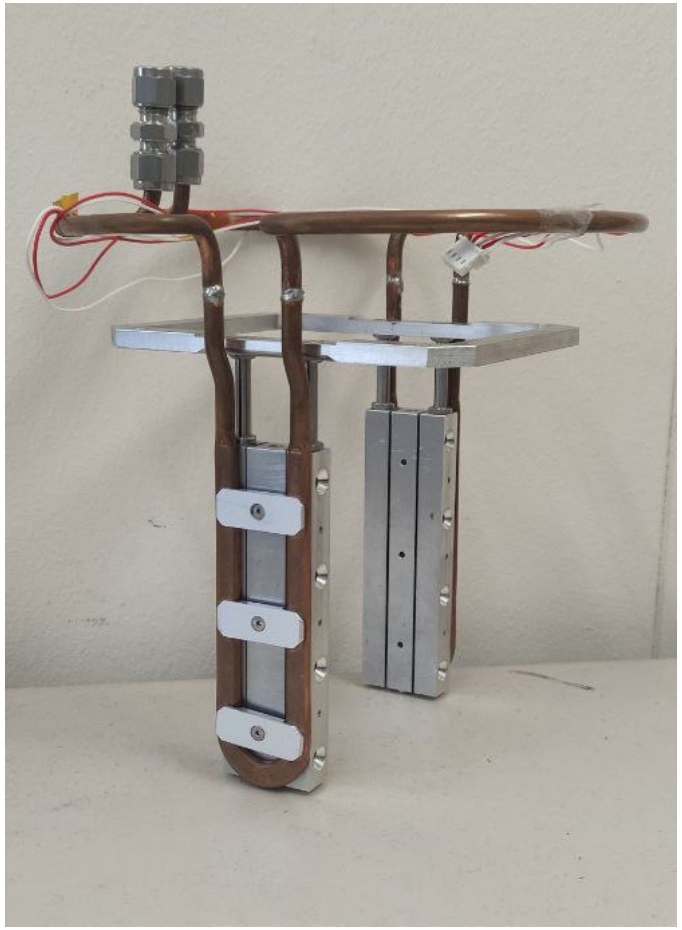
- Each VeloPix generate up to 3W
- Each ASIC additional 5 W
- Maximum 4 module/rp ~ 30 W
- Proof of principle operational temperature ~ 20 ° C
- Water cooling system + thermally conductive support board
- External chiller with local water circuit
- Interlock system



Mechanical integration

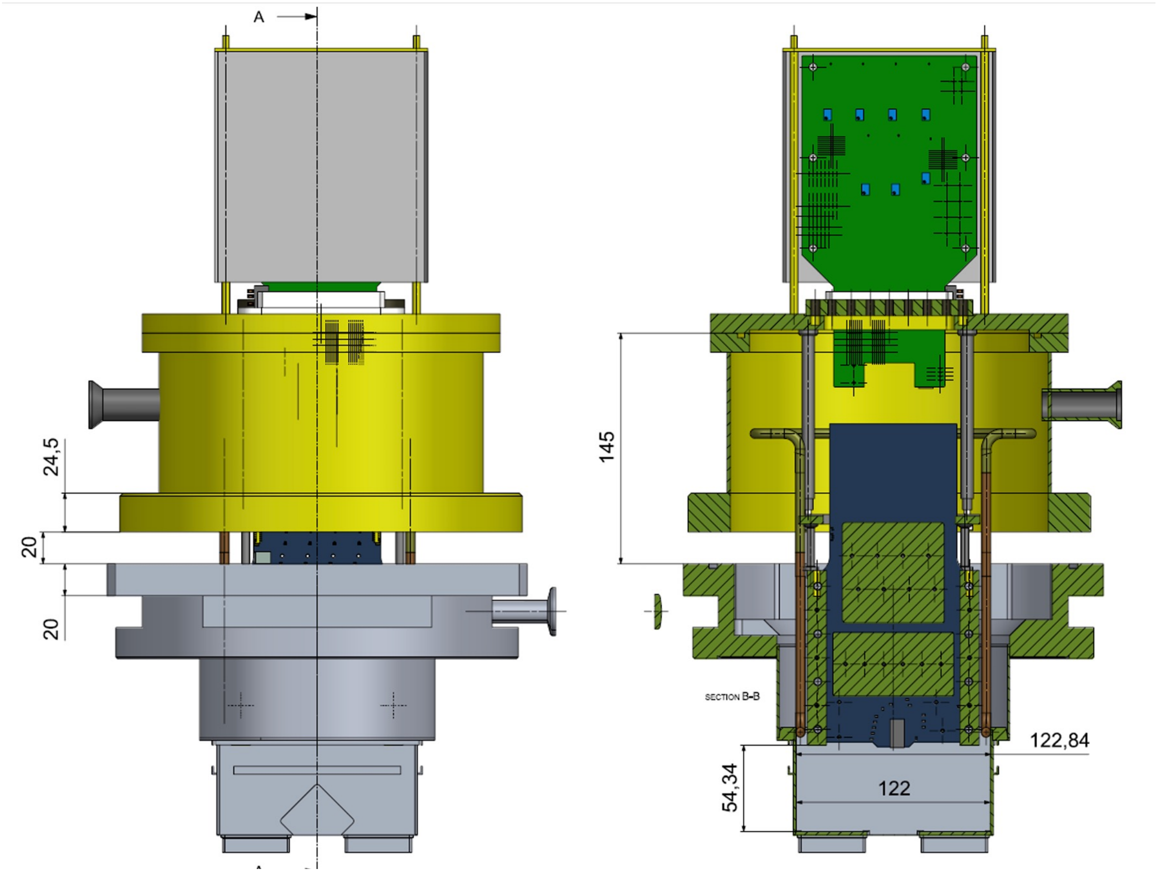
- Module support has been modified to hold 2 modules, not 4, to adapt to the roman pot box dimensions

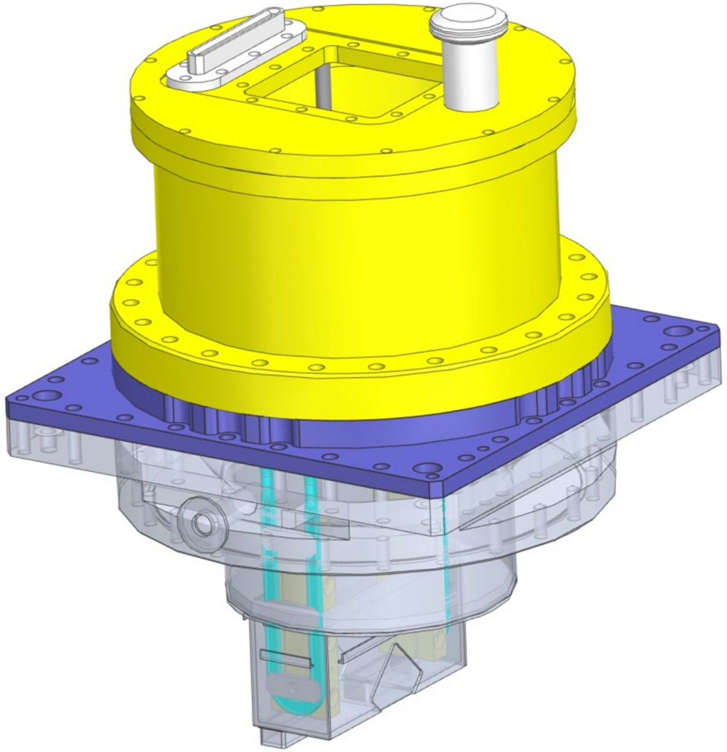




Mechanical integration

- Module support has been modified to hold two modules, not four, to adapt to the roman pot box dimensions
- An additional flange is being designed to match the two parts



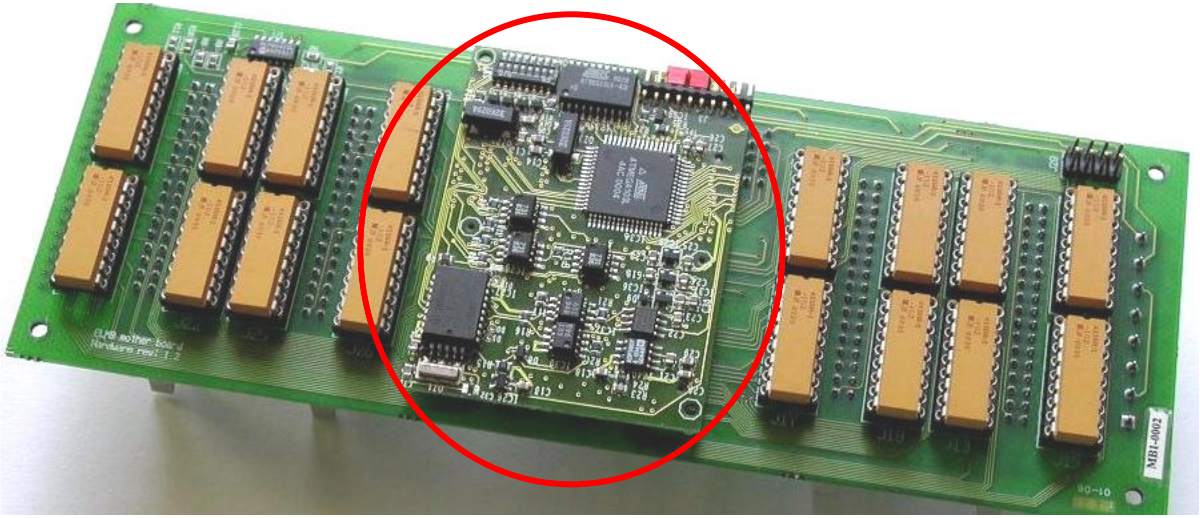


Monitoring system – in progress

- Study are ongoing for the development of the temperature and humidity monitoring system and Interlocks

- Possible solution – ELMB board as used by several subdetector in LHCb
  - PT100 sensors for module and roman pot temperature measurements
  - Humidity sensors

ELMB



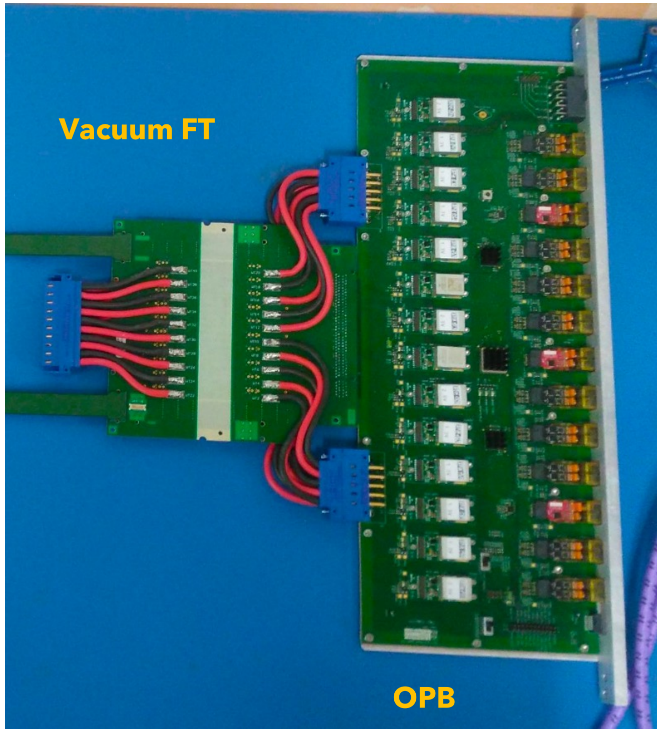
https://cds.cern.ch/record/690030/files/p331.pdf

Off detector electronics

https://edms.cern.ch/ui/#!master/navigator/document?P:1340134179:100310887:subDocs

Vacuum feed-through

- Allow to pass from the secondary vacuum inside the roman pot to the outside area
- The VELO feed-through is being customised to fit the TOTEM exit flange



Opto and Power Board

- Located immediately outside the roman pot .
- They provide the following functionality:

  Electrical to optical conversion for the data sent from the detector module;

  Electrical to optical conversion of the timing, trigger and fast control signals;

  Electrical to optical conversion of the control signals for the components of the OPB;

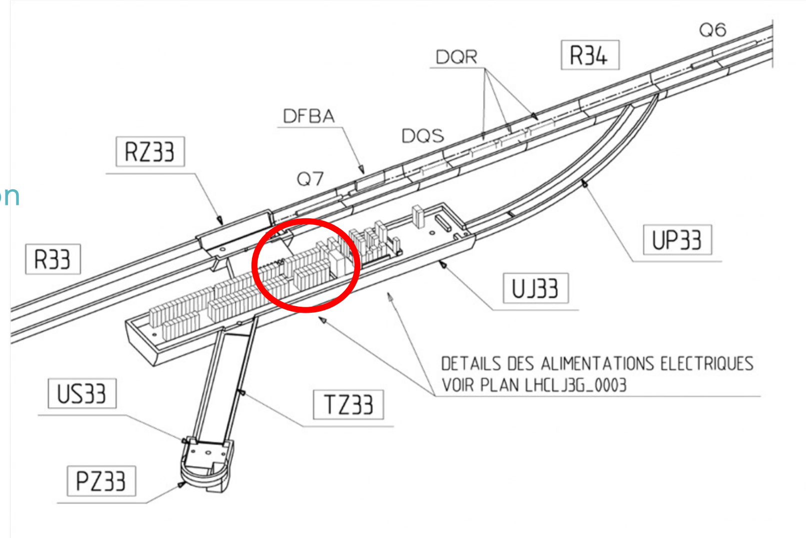
  DC/DC conversion of the supply voltages for the hybrids and OPB itself;

Each OPB can serve 2 GBTx hybrids – with the current design idea 1 OPB is needed for each roman pot

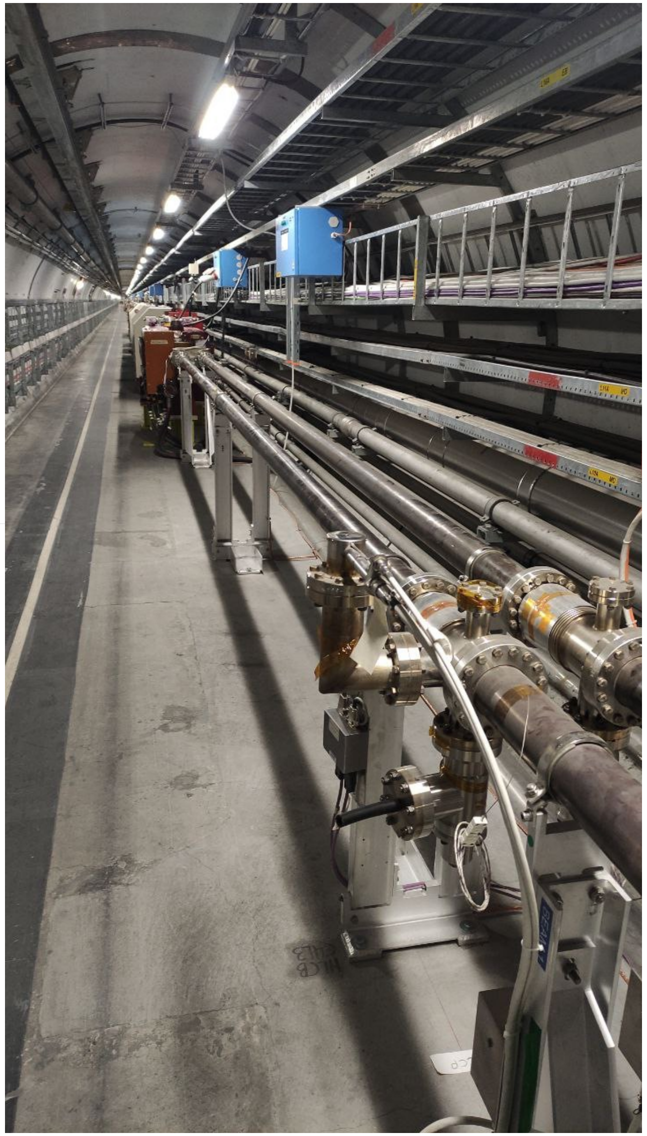
New production will be launched soon

Long cables

- Power distribution has three segments before reaching the Roman Pot/OPB.
- This three segments are separated by patch panels that use terminal blocks to connect/disconnect each line.
    - First segment: is fully enclosed in the racks where the power supplies are installed and (initially) only affect LV power lines.
    - Second segment: is the longest one ~250m running through the tunnel
    - The final segment: between OPB and electronics and includes vacuum region.



Service area of Interaction Region 3 of LHC



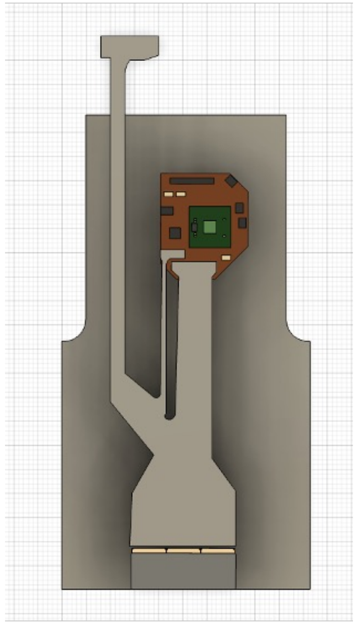
Section of LHC where the tracker will be placed

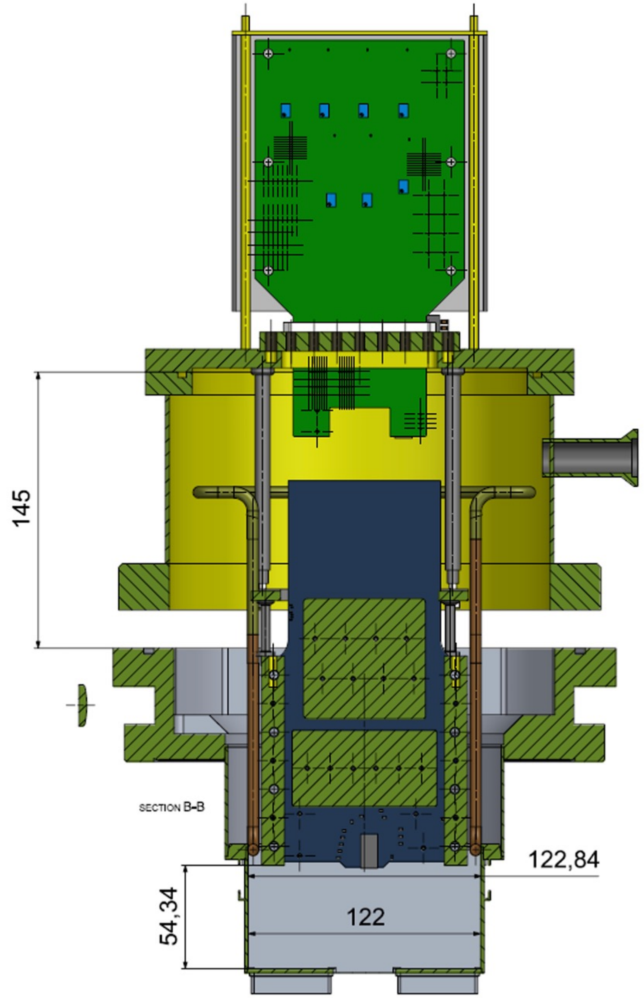
Summary

Pixel detector design

- A tracking detector is being designed for the proof-of-principle test at the IR3
- Selected technology: Silicon pixel detector placed inside a roman pot
- Sensors and ASICs from the VELO detector of LHCb
- Roman pot from the ATLAS ALFA experiment and mechanical support and cooling from the CMS TOTEM experiment

- Installation foreseen during the Year End Technical Stop 2024/2025
- Good progresses:
  - Sensors and ASICs bonded and tested successfully
  - New flex cable design in progress
  - Mechanical integration in the roman pot in progress





Thank you for your attention!

Backups

Acknowledgments

- **LHCb contributors**: S. Aiola, S. Barsuk, N. Conti, F. De Benedetti, J. Fu, J. Grabowski, L. Henry, Y. Hou, S. Jaimes, C. Lin, D. Marangotto, F. Martinez Vidal, J. Mazorra, A. Merli, N. Neri, S. Neubert, E. Niel, A. Oyanguren, M. Rebollo, P. Robbe, J. Ruiz Vidal, I. Sanderswood, E. Spadaro Norella, A. Stocchi, G.Tonani, Z. Wang, M. Benettoni, G. Simi

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- Interesting **discussions/suggestions**: V. Baryshevsky, V. M. Biryukov

- Special acknowledgment to the **LHCb VELO group** for providing the pixel detector and the technical support

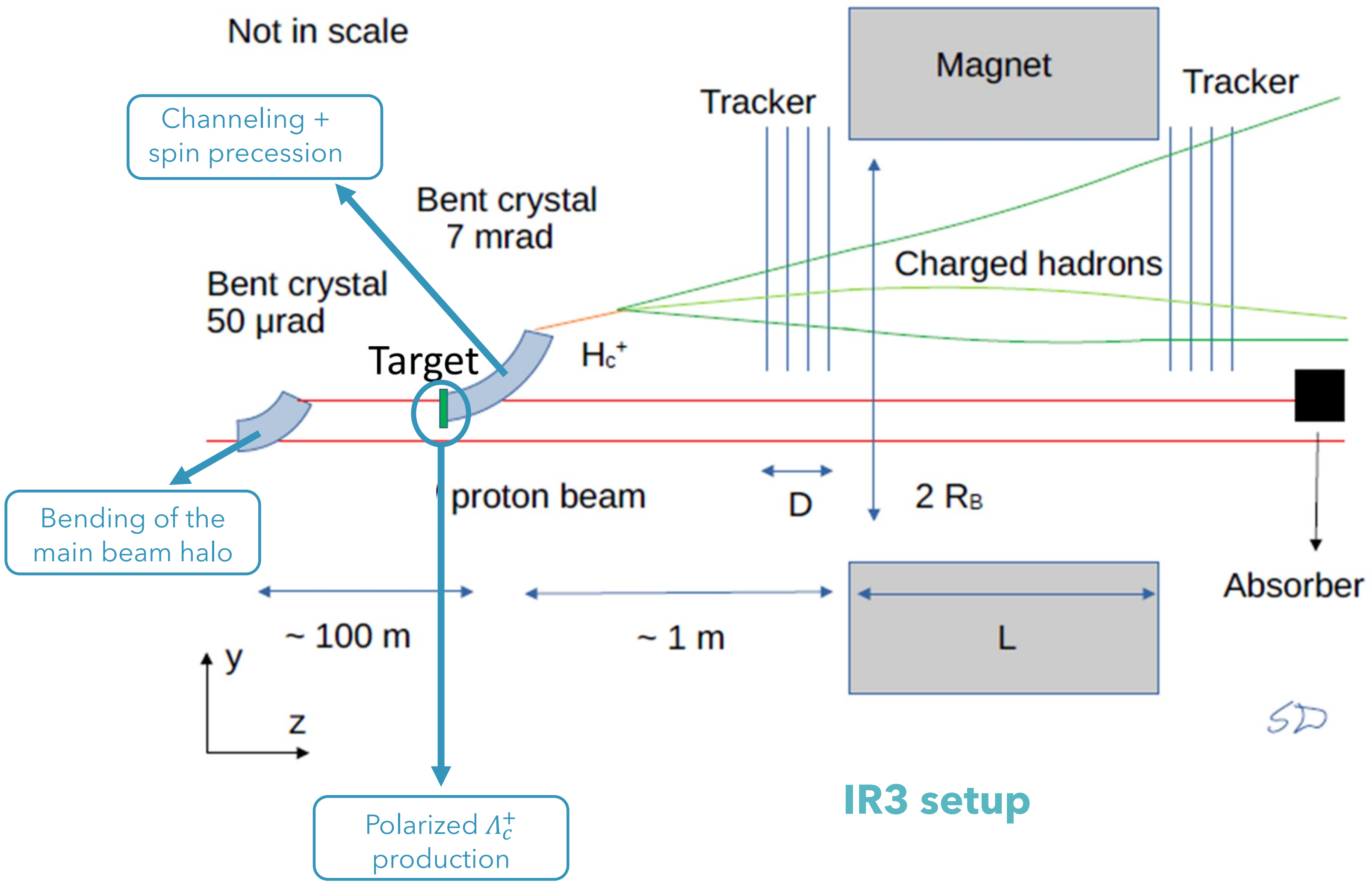
Fixed target experiment with bent crystals

Two alternative scenarios:

1. Target placed in front of the LHCb detector.
2. New independent experiment at IR3 (LHC).

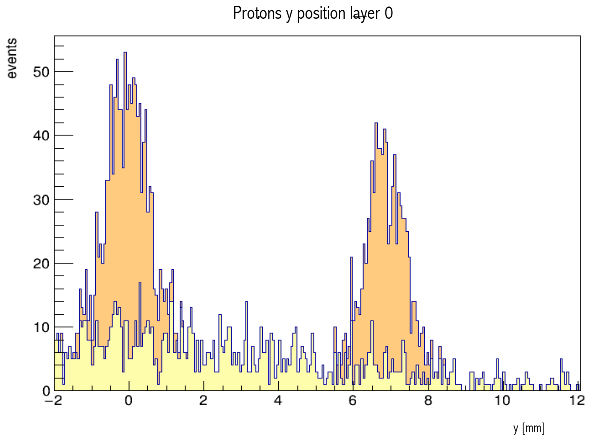
Additional physics opportunities due to the very forward acceptance:

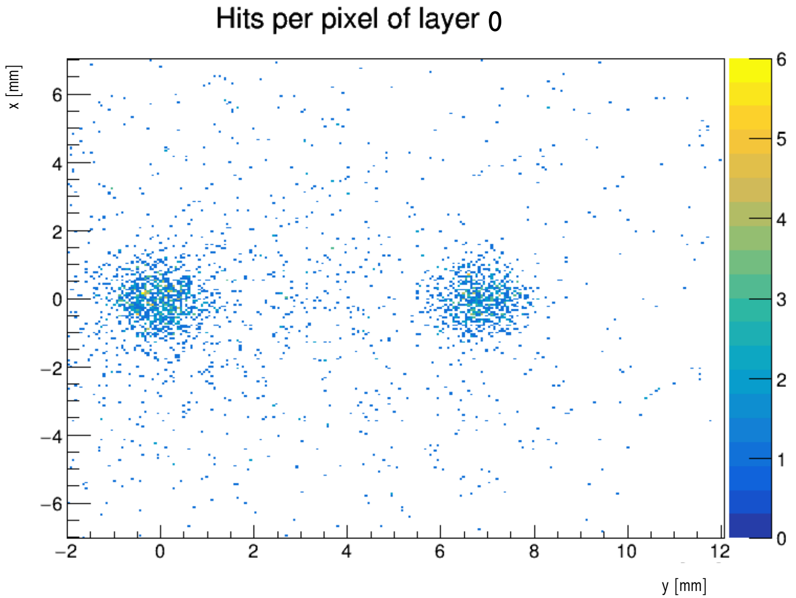
1. Forward charm baryons production
2. Pentaquark photoproduction

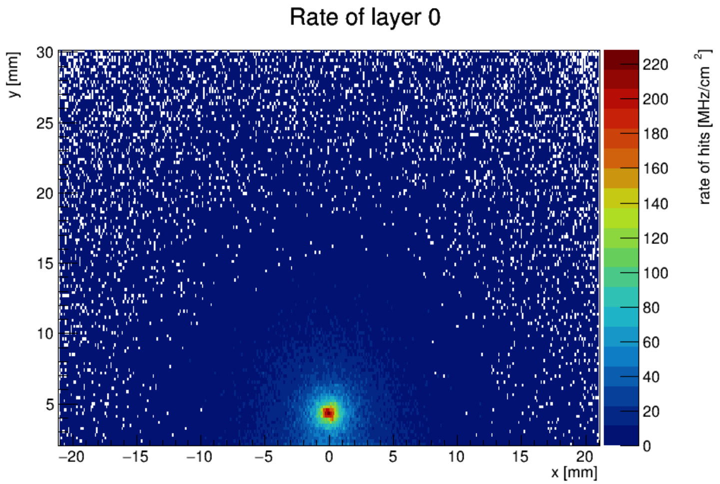


Measurement of the channeling efficiency

- Simulation studies of 1 TeV protons channeled with the double crystal setup
- Second crystal – tracker layer distance **d=1m**
- Need to measure both the channelled and unchannelled protons from the second crystal.





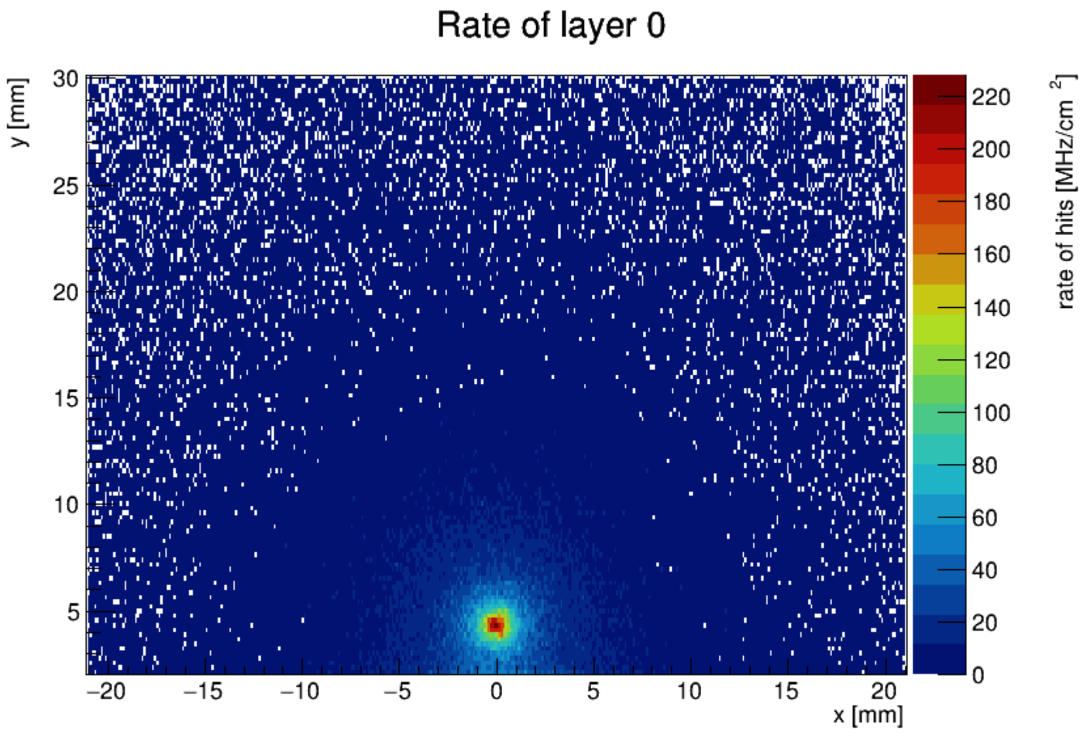


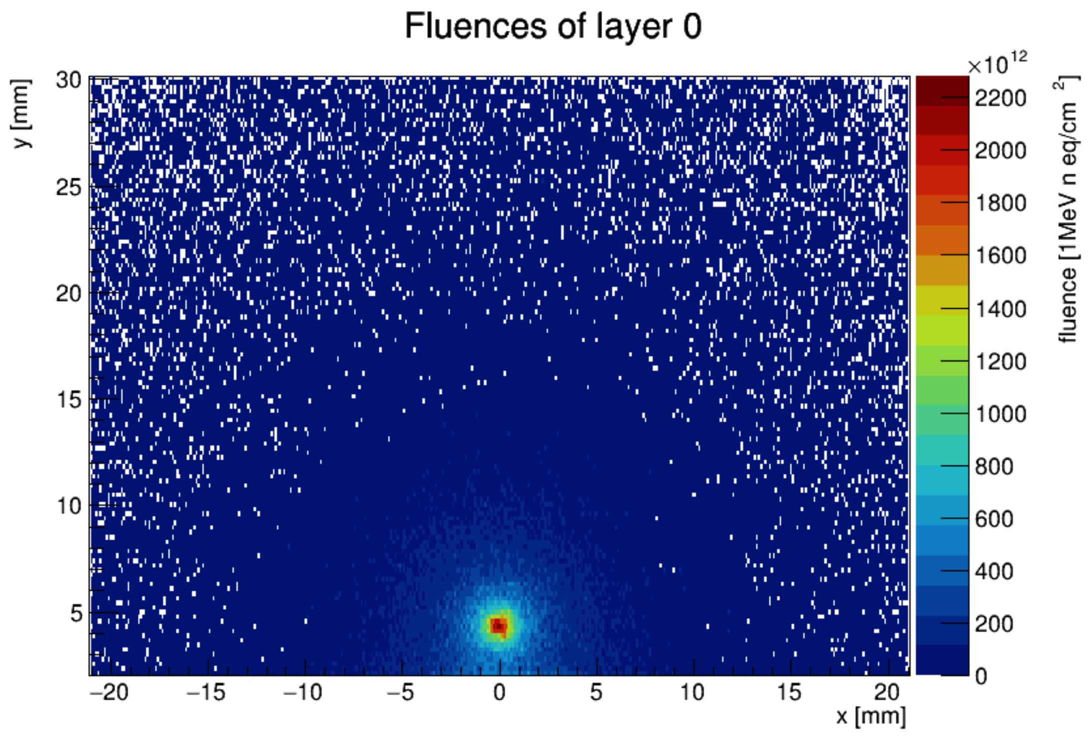
Background studies

- Tracks multiplicity in pW collisions (with target in place)

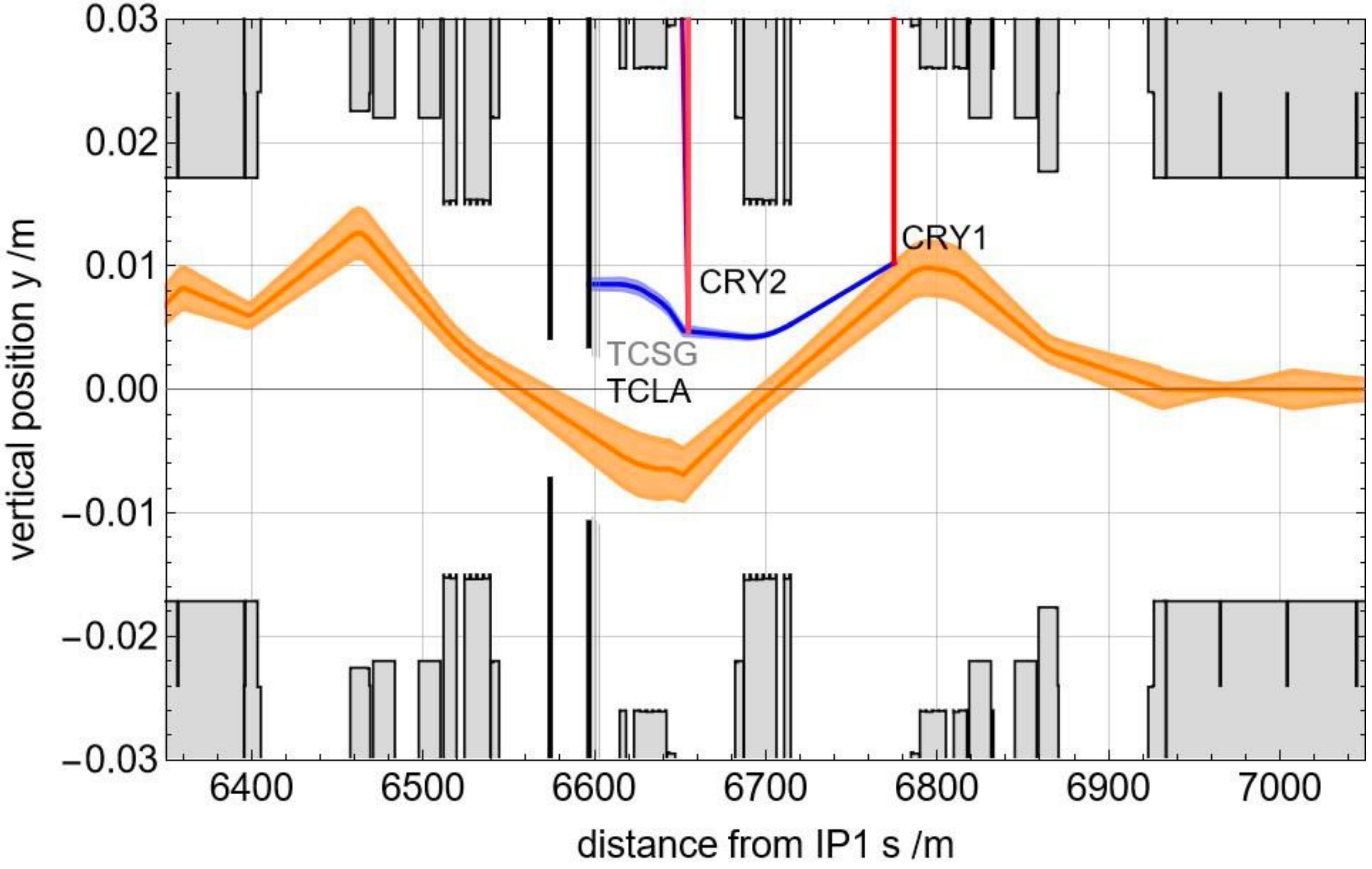
Long cables and services

- Fluences calculated for 2 years of data-taking ($1.37 \times 10^7 s$) for each super pixel (matrix of 2x4 pixels) with a flux of $10^6\ p/s$ → we would like to increase to $10^7\ p/s$
- In the plot the fluences for the first station after the crystal that is the one with the highest fluence.





Measurement of the channeling efficiency



Tiles Quality Assurance

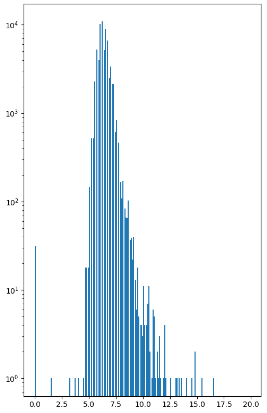
Functionality test of the ASIC

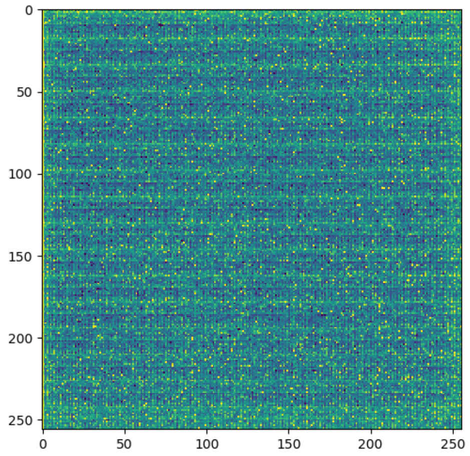
- power-up test
- register test
- ECS matrix test
- DAC scan
- Responses to TFC commands
- Fast equalisation and noise scan.

Scan each ASIC for:

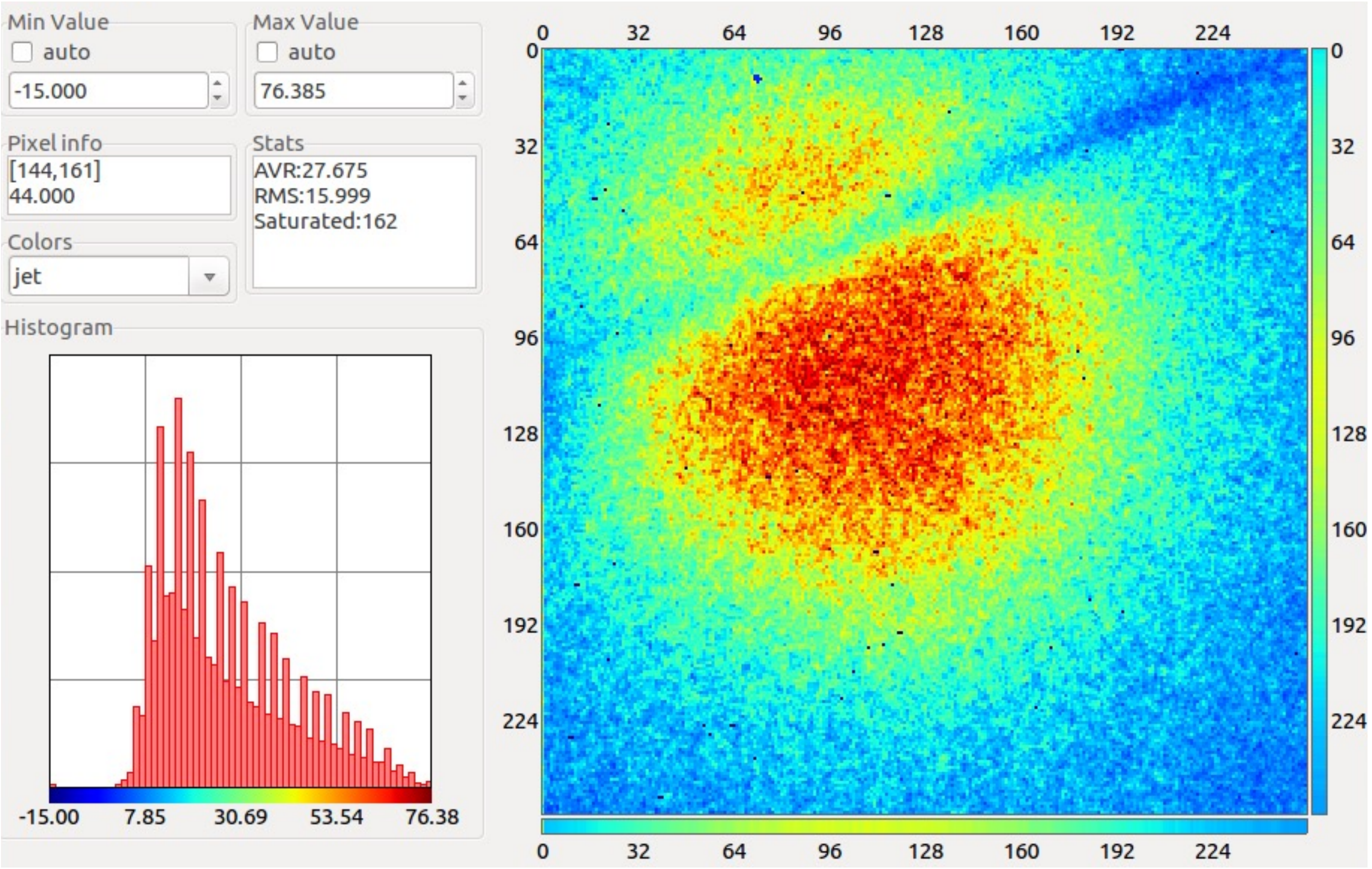
- Masked pixel (non-equalisable)
- Noise scan
- Shorted pixel
- Missing pixel

Noise scan





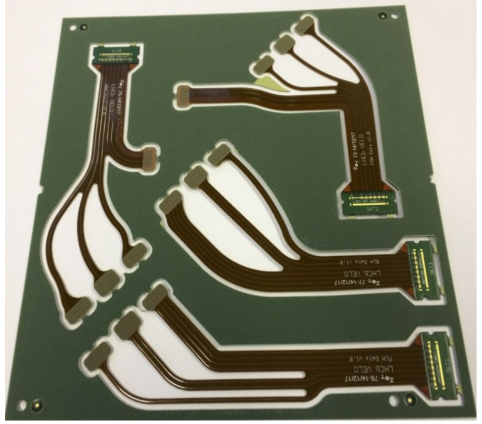
Source test with Sr90

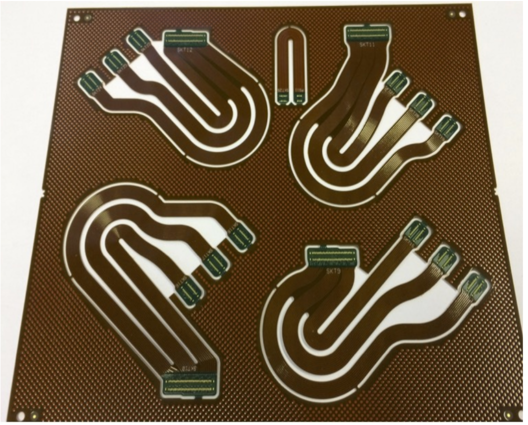


Flex cables

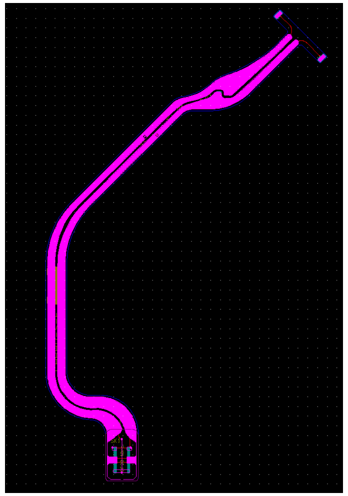
VELO SIGNALS

- ECS In, Out, Clock
- TFC Out, Clock
- Master Clock
- Reset





Interconnecting tapes



HV tapes

DATA cables

- Connect the velopix data output streams, uplink, down link, reset lines to the long data cables
- These are flexible, double sided, 100um track and gap, with controlled impedance, 100" differential traces.

New straight design of the flex cables in progress with the collaboration of the LumiTracker group of LHCb

https://edms.cern.ch/ui/#!master/navigator/document?P:1340134179:100310887:subDocs

FE and GBTx hybrids

Front End hybrid

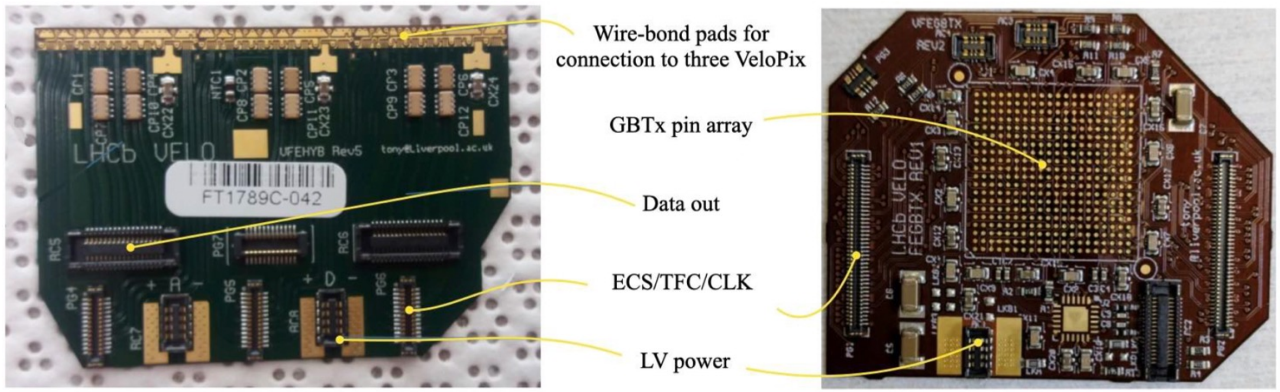
- Route the signals from the VeloPix ASIC
- Minimised material contribution – 4 copper layers
- Optimised for high speed signals

GBTx hybrid

- Provides control and timing information to the VeloPix FE
- Provides monitoring information back to the control room
- Each GBTx can operate two tiles

For the moment there will be 1 GBTx and 1 tile for each module

First units of GBTx and FE hybrids will be provided by the VELO group



Flex cables

DATA cables

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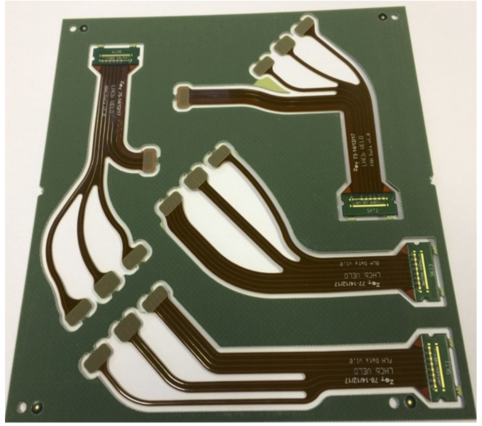

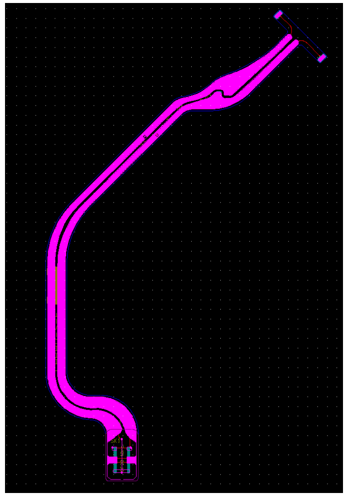

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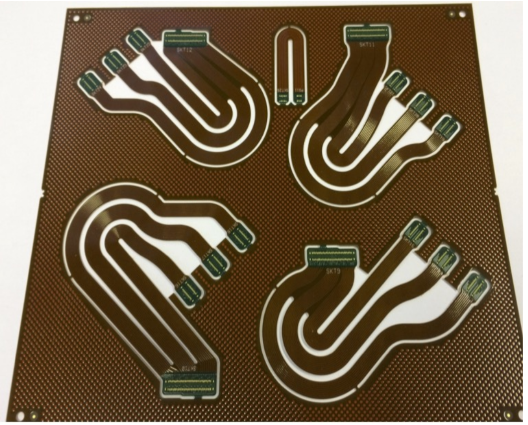
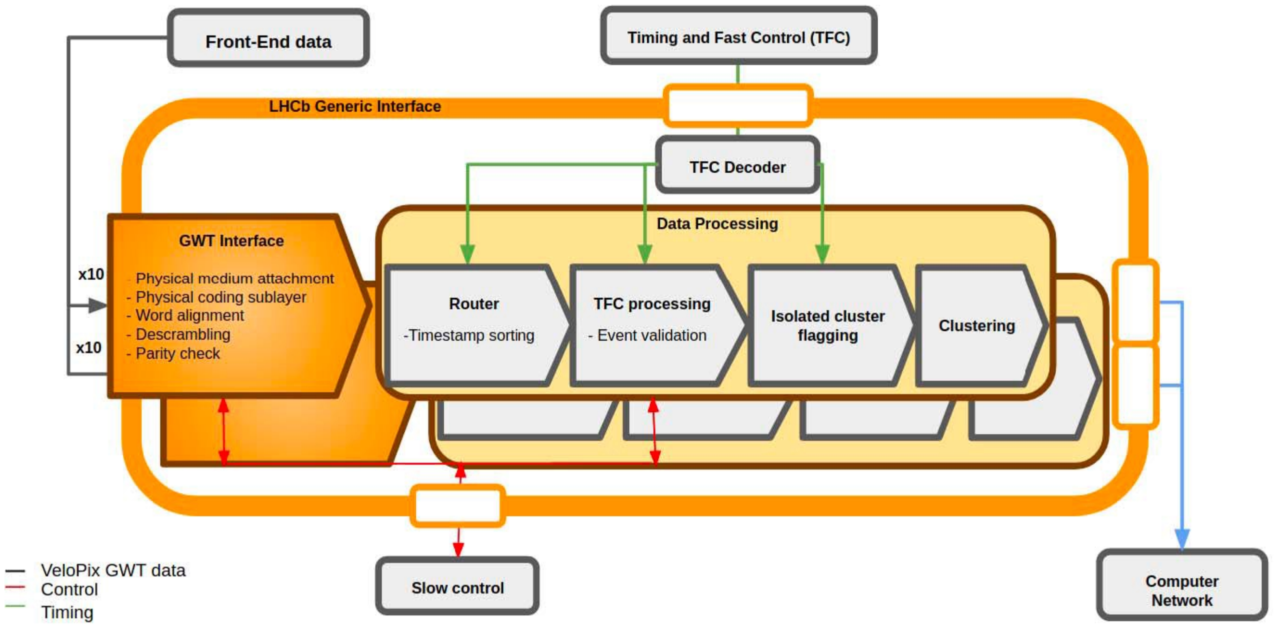


VELO firmware

- VELO has a specific control interface firmware to act as a bridge between PCIe and FE
- PCIe 40 card configured as cntrol interface
- 1 GBTx for commanding the OPB and monitoring temperature and analog signals
- 1 GBTx for up to 2 VeloPix tiles

The readout board firmware architecture



FERNÁNDEZ PRIETO et al.: PHASE I UPGRADE OF THE READOUT SYSTEM OF THE VERTEX DETECTOR AT THE LHCb EXPERIMENT

The experts from INFN Pisa are already in contact with the VELO group to learn how to operate the firmware + PCIe40 and minidaq are being purchased