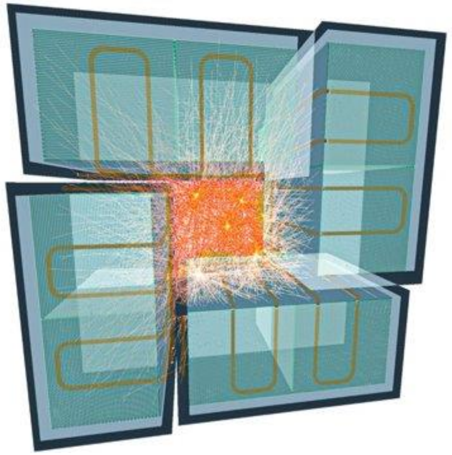
100 µPET: Multi-layer monolithic silicon pixel scanner for ultra-high-resolution molecular imaging

Thanushan Kugathasan
on behalf of the 100µPET collaboration



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100µPET
MOLECULAR IMAGING AT ULTRA-HIGH RESOLUTION

Swiss National Science Foundation

The 100μPET project

Molecular imaging with ultra-high resolution

- **SNSF SINERGIA** grant among **UNIGE** (scanner construction) **EPFL** (imaging) and **UNILU** (medical application studying atherosclerosis in ApoE+/- mice)
- **Deliverable:** Small-animal PET scanner with monolithic silicon pixel detectors

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- project P.I.

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- Sensor design
- Analog electronics

Didier Ferrere
- System integration
- Laboratory tests

Sergio Gonzalez-Sevilla
- System integration
- Laboratory tests

Mateus Vicente
- System integration
- Laboratory tests

Jihad Saidi
- Laboratory tests
- Data analysis

Yannick Favre
- Board design
- RO system

Stéphane Débieux
- Board design
- RO system

Franck Cadoux
- Mechanical design

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- Lead chip design
- Analog electronics

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- Sensor design
- Digital electronics

Antonio Picardi
- Chip design
- Firmware

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- Printed Circuit design

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- Translational imaging

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- Physical modeling

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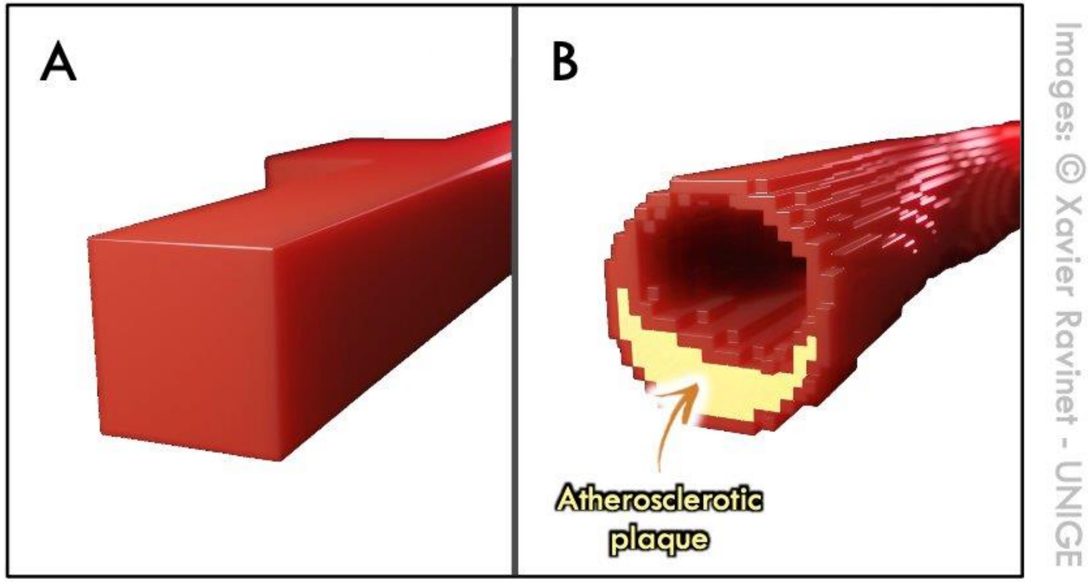
Molecular imaging with ultra-high resolution

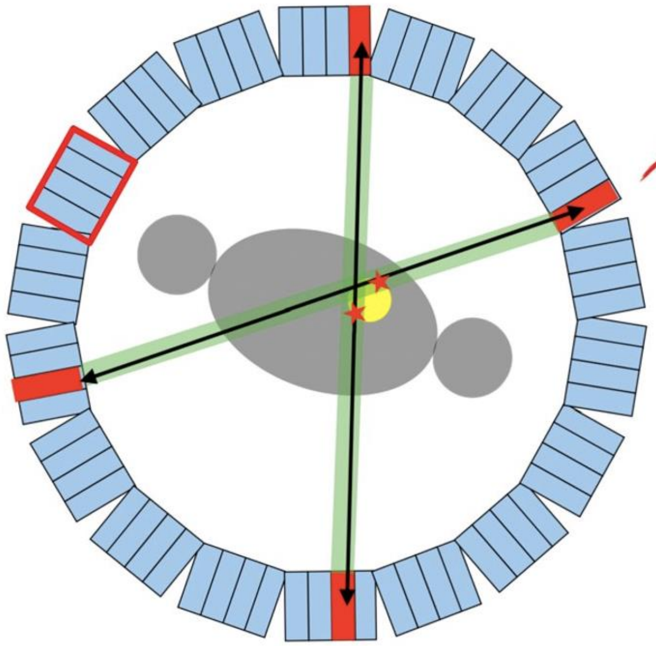


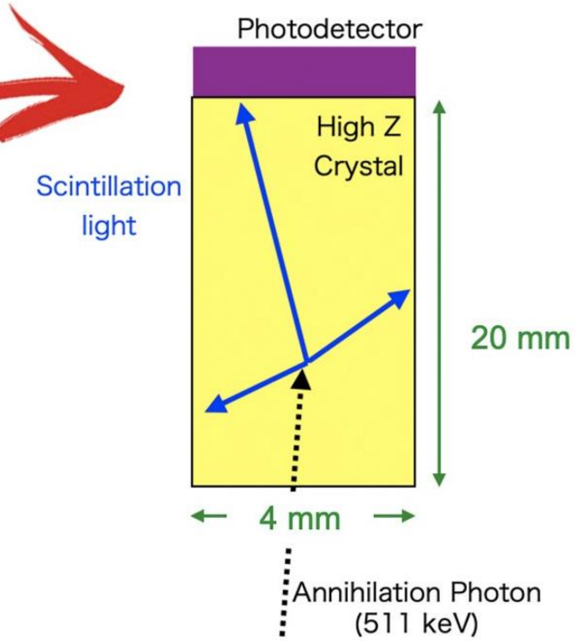
With today's PET technology, small blood vessels can only be visualized in their entirety (A). The proposed new PET technology will allow the study of changes in the walls of small blood vessels, such as atherosclerotic plaques (B).

Positron Emission Tomography (PET)

Positrons emitted from radiotracer decay annihilate with nearby electrons, producing back-to-back 511 keV photons.

- The detection of coincident photons defines the Line-of-Response (LoR) volume.
- Images reconstructed by intersection of LoR volumes.





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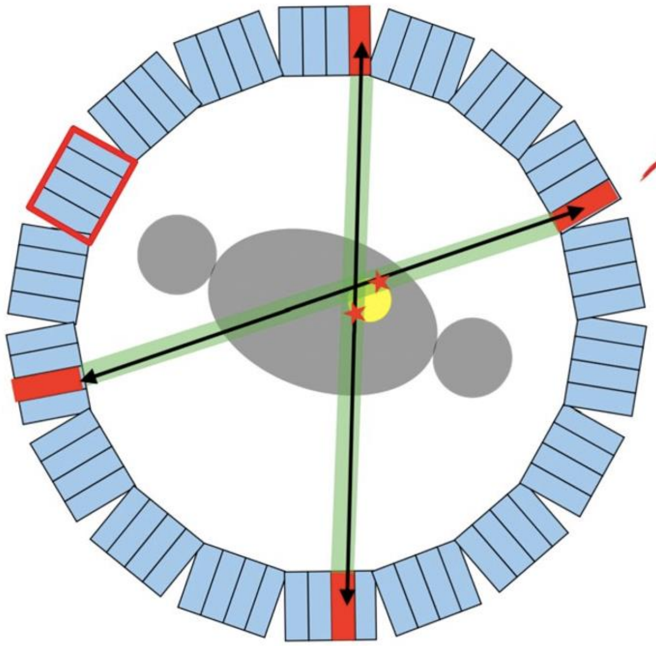
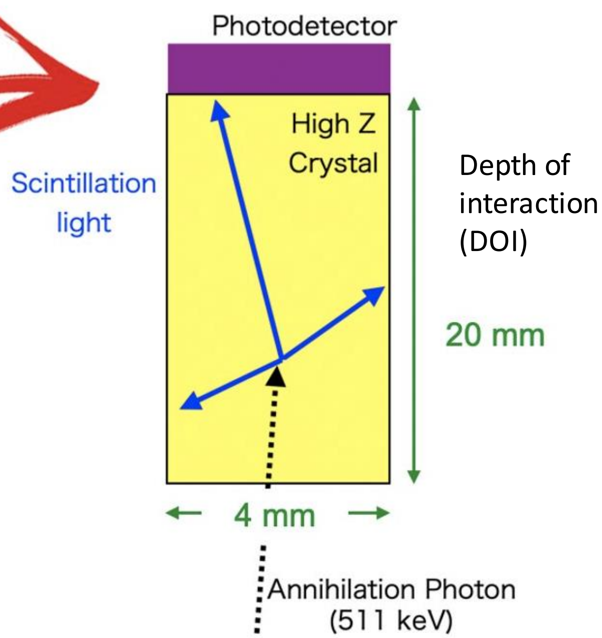
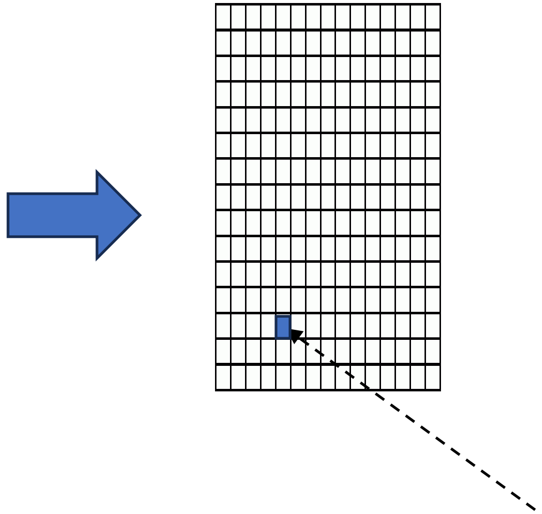




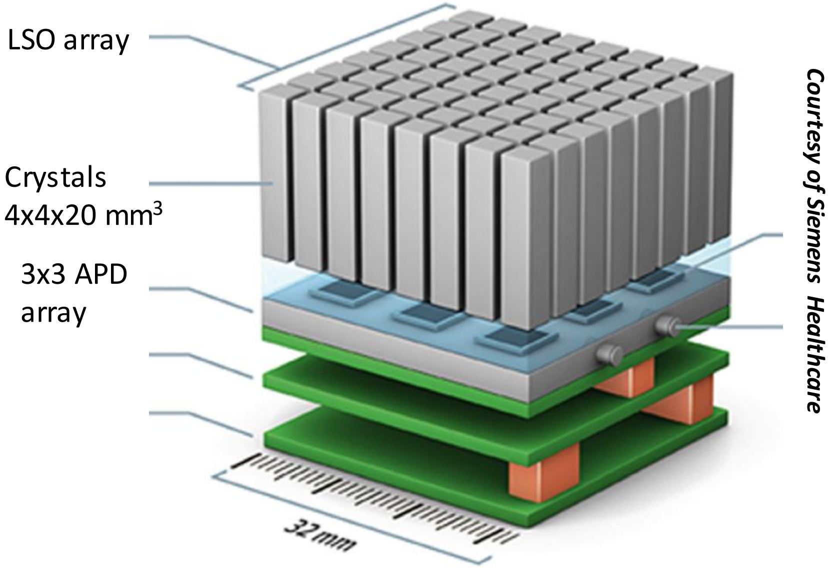
Higher resolution with smaller sensing volume



Positron Emission Tomography (PET)

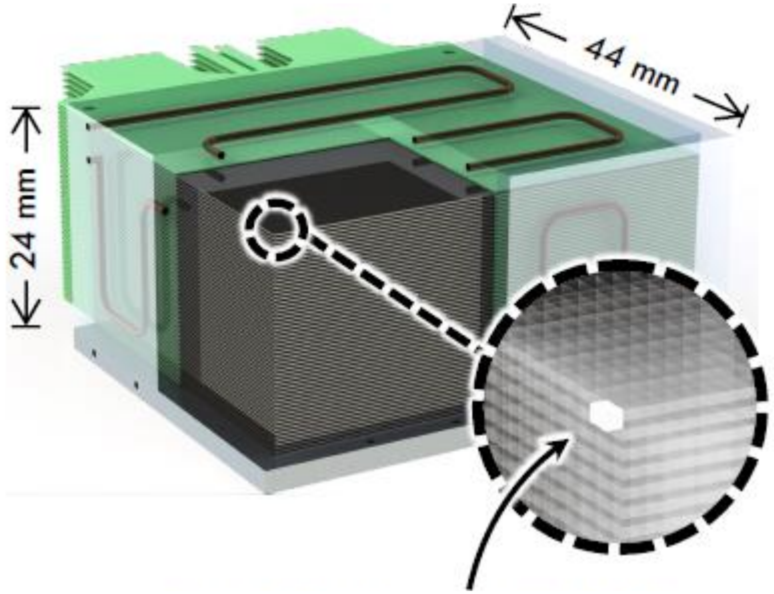
Ultra-high resolution obtained by increasing the granularity inside the detection volume

PET tower with LSO crystals



DOI: 20 mm
Sensor granularity: **320 mm³**

100µPET stack

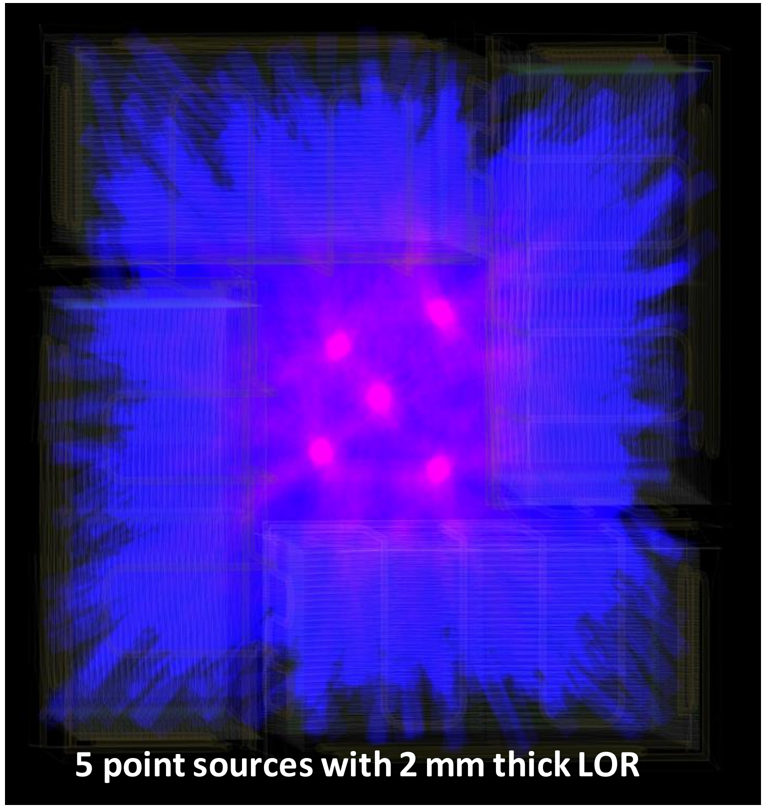


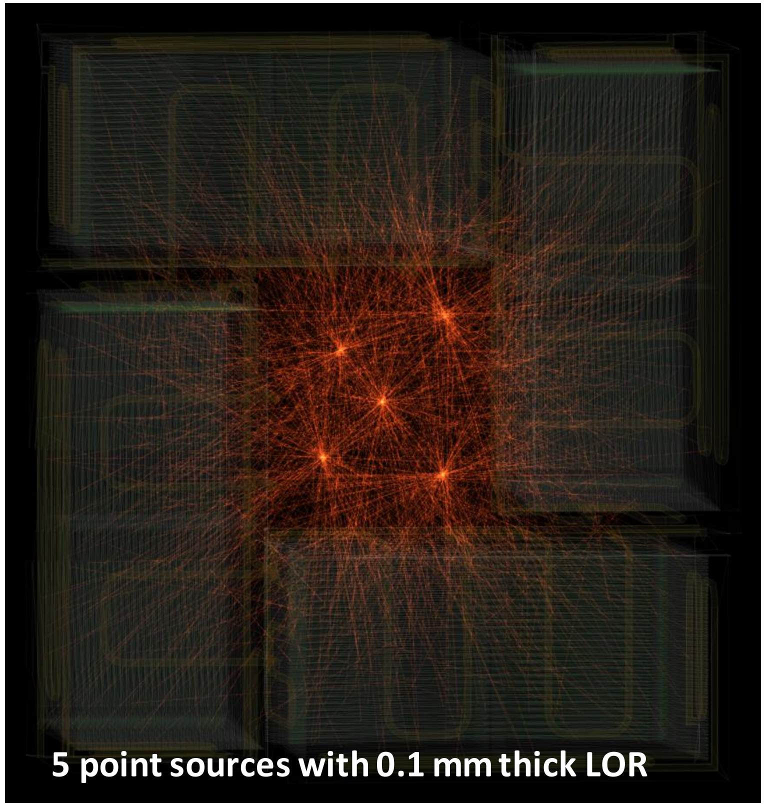
Pixel pitch: 150 µm | DOI: 550 µm
Sensor granularity: **0.012 mm³**

Scanner granularity: 27’000 times finer
LOR volume: 700 times smaller
DOI: 36 times smaller

Detector Granularity - DOI and LOR

Ultra-high resolution is obtained by increasing the granularity inside a detection volume thanks to small silicon pixel size (~100 microns)

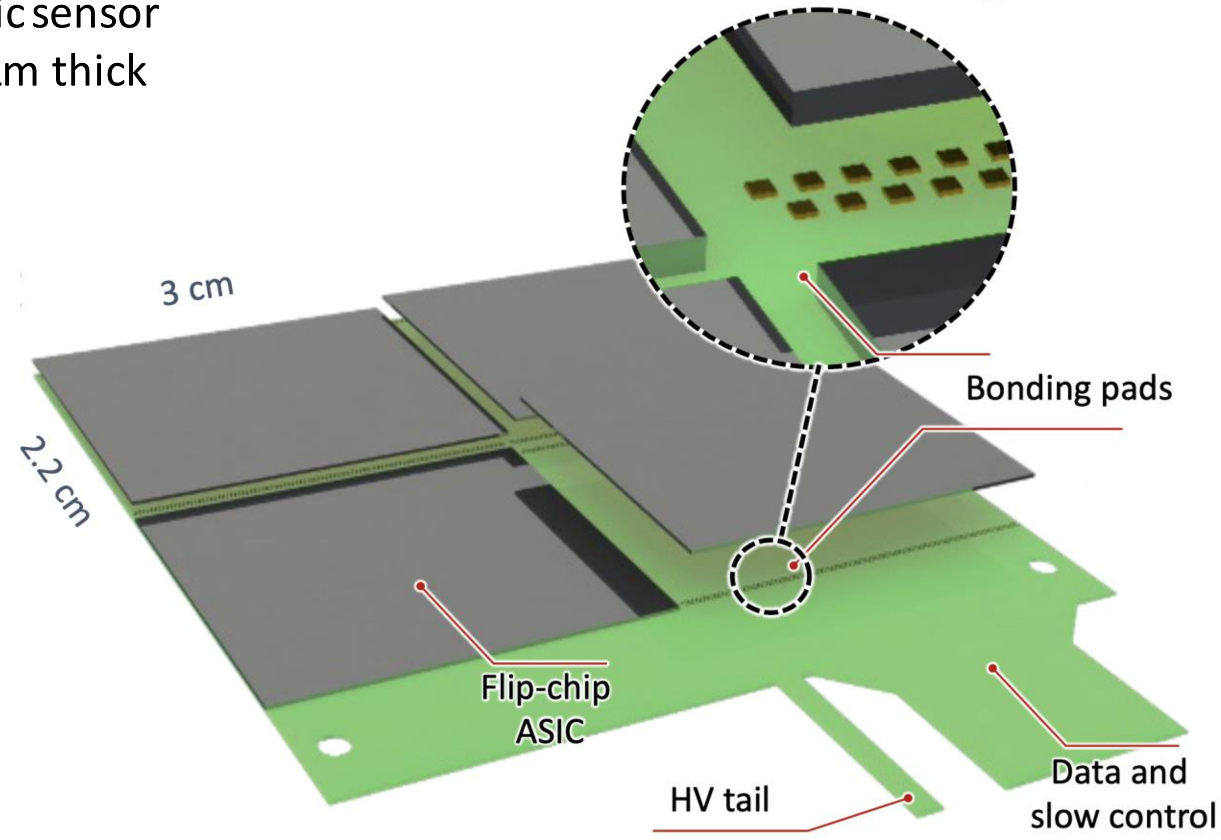




Only a factor of 20

100µPET module layer

Quad module monolithic sensor
4 x (30 x 22 mm^2), 270 µm thick



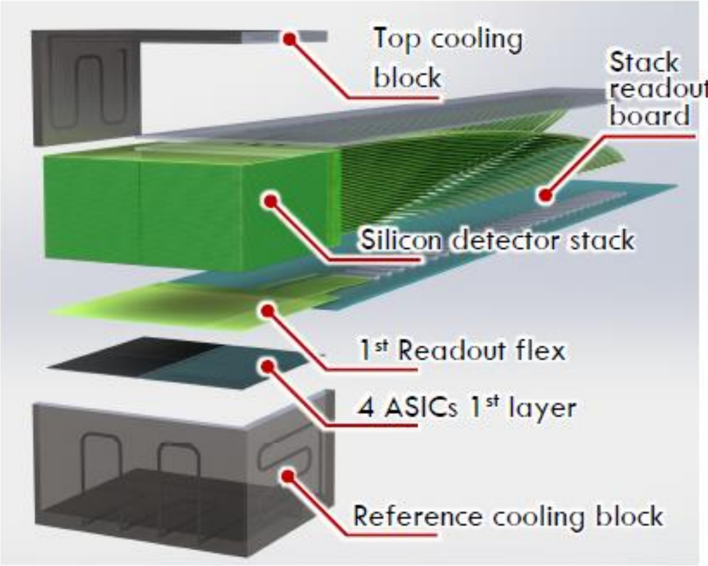
Flip-chip bonding to the Flexible Printed Circuit (230 µm thick)

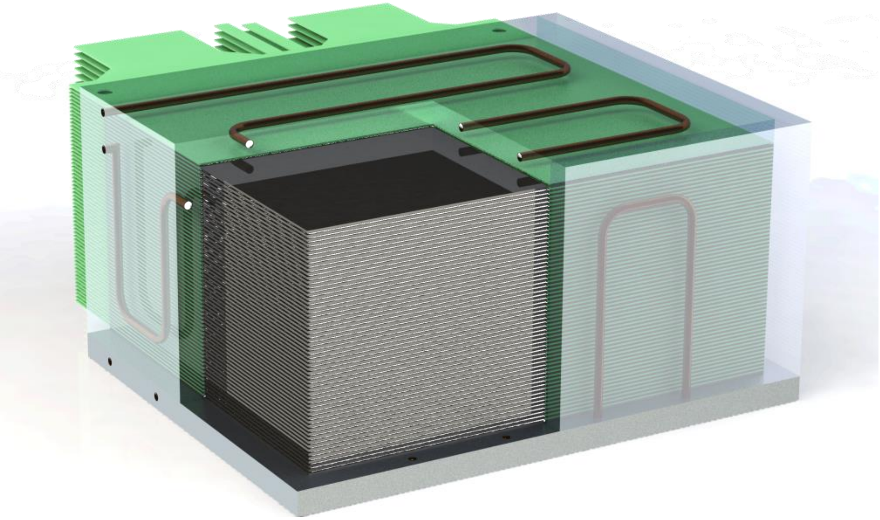
Chip readout daisy chained:
1 readout line for 4 chips

+ Optional 50 µm thick Tungsten layer to increase the photon conversion efficiency (w.r.t. only silicon)

100µPET scanner

Tower: 60 quad-module layers (240 chips)





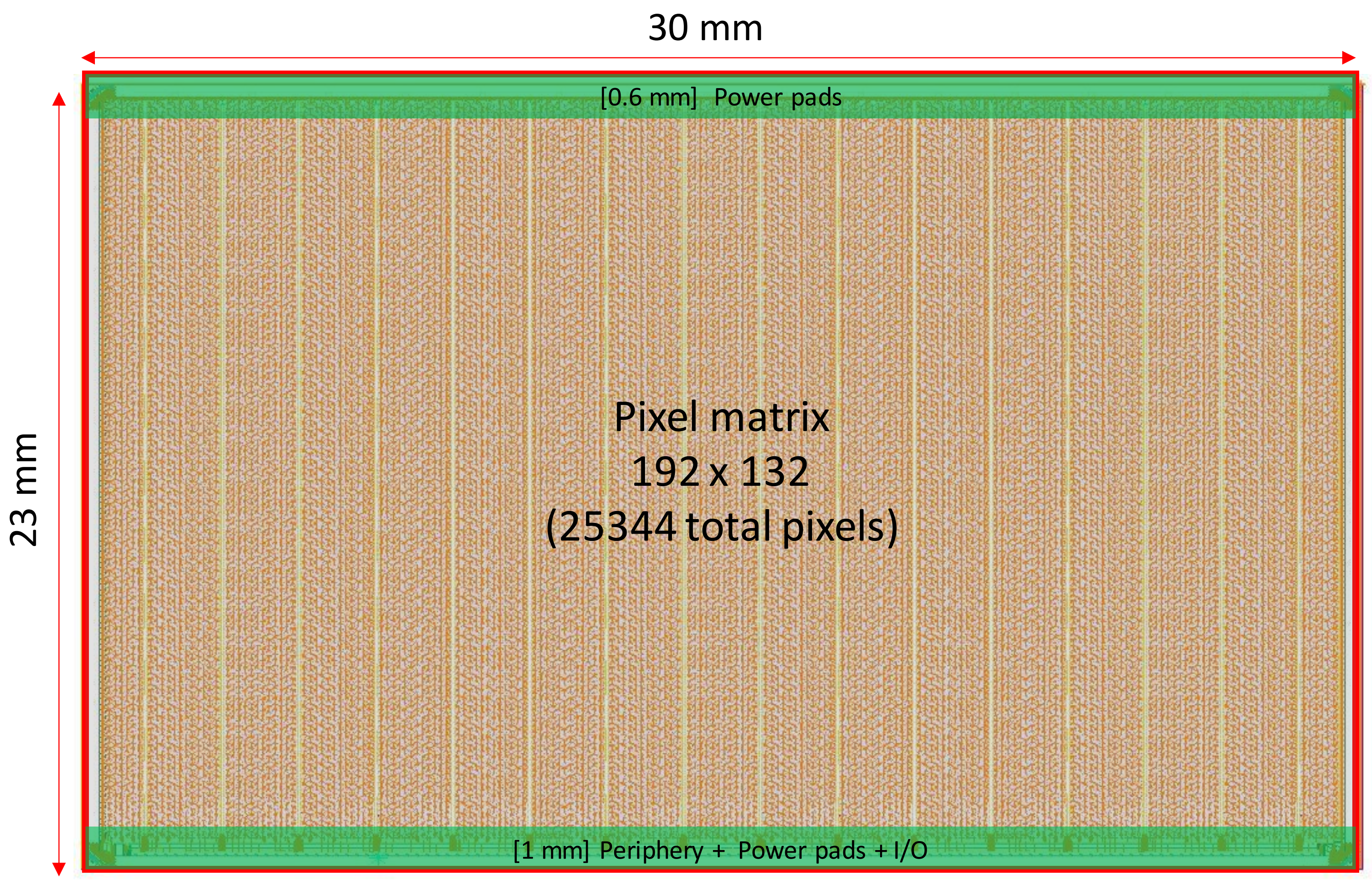
100µPET Scanner:
4 towers (960 chips)

ASIC requirements

Event size	1 cluster (< (5x5) pixels)
Event rate	10 kHz/cm^2
Equivalent Noise Charge (ENC)	200 [e-]
Operation Threshold	3000 [e-]
Time resolution RMS (Qin > 7 ke-)	200 [ps]
ToA	Yes, 1 pixel/event
ToT	Yes, for ToA time walk correction
Power consumption	< 100 [mW/cm^2]
Pixel pitch	150 µm

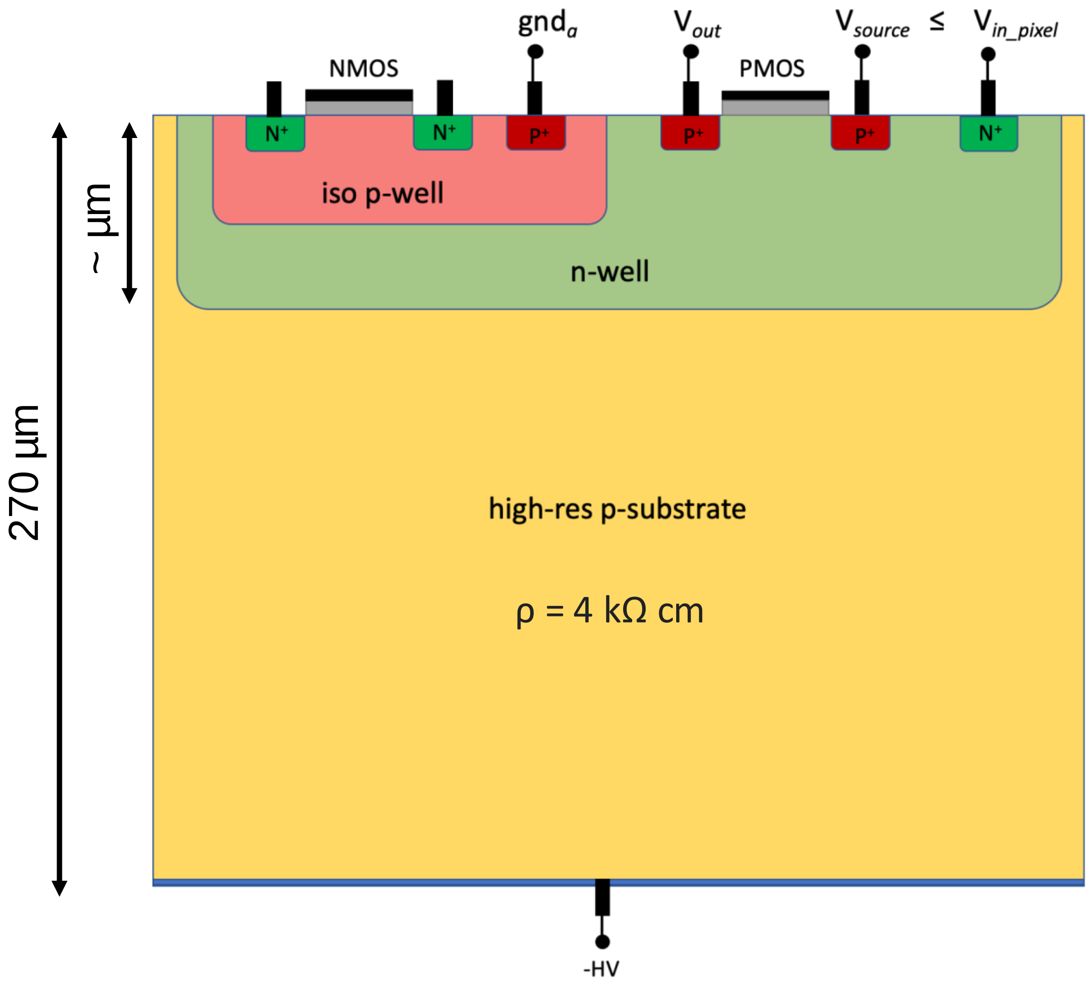
→ CMOS monolithic sensor in IHP SG13G2 BiCMOS, 130 nm process featuring SiGe HBT

100 µPET ASIC layout



Submitted for production in October 2023

Pixel cross-section



High resistivity substrate as detection volume.

Pixel electronics inside a large n-well electrode (uniform electric field)

- NMOS in isolated p-well

- PMOS in the collection n-well
  - Reverse bias condition on V_{source}-V_{in_pixel} junction: $V_{inpixel} \geq V_{source} = V_{ccA}$
  - Charge injection from output to input via $V_{out} - V_{in\_pixel}$ junction
  - Next step: implementation test of isolated PMOS in a iso n-well

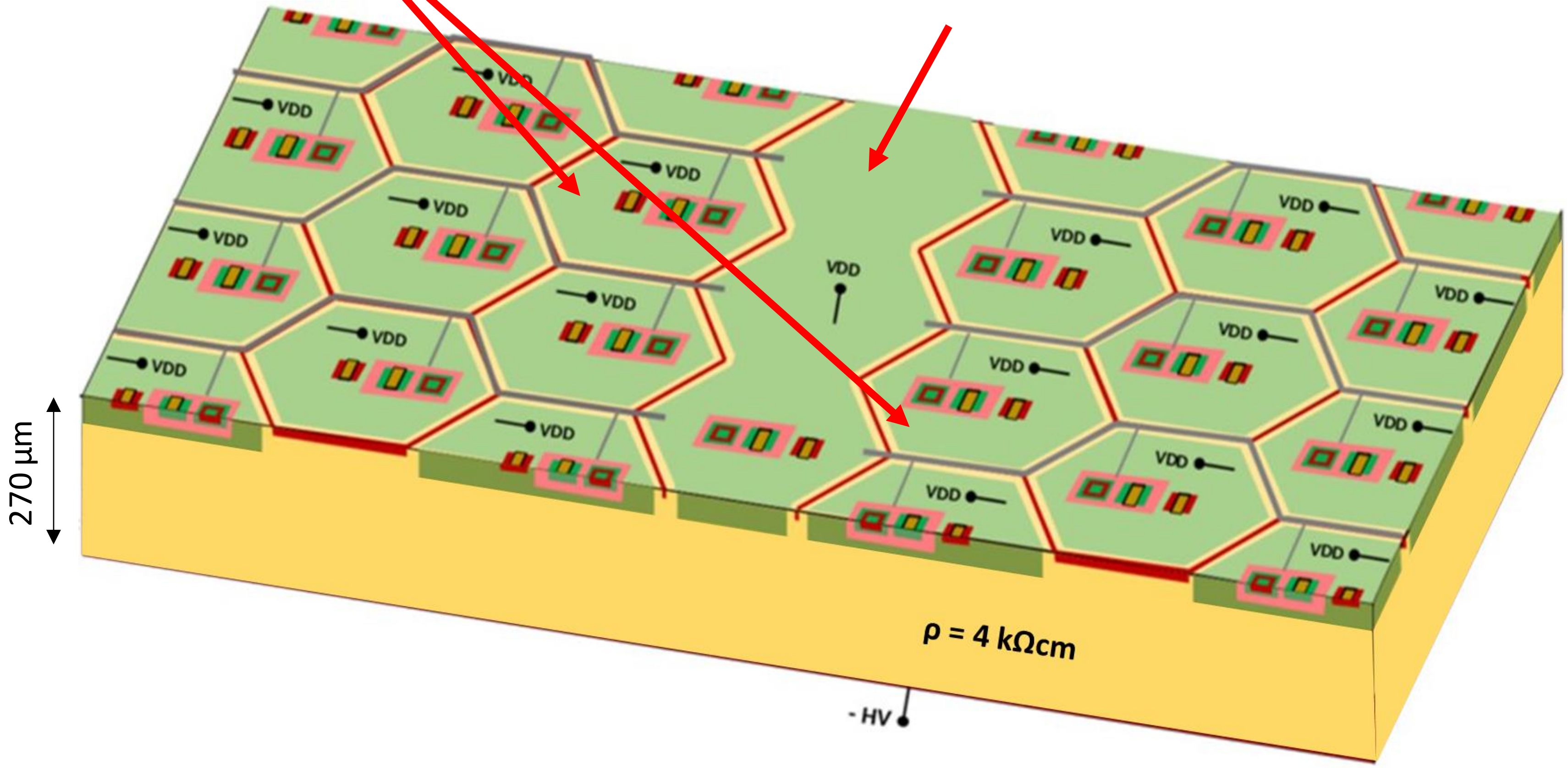
Input capacitance for a pixel of $(150\ \mu m)^2$: 360 fF

- 140 fF sensor pn junction (n-well to p-substrate)
- 220 fF electronics well junction (n-well to iso pwell)
  - Next step: low doped p layer around iso-pwell to reduce capacitance

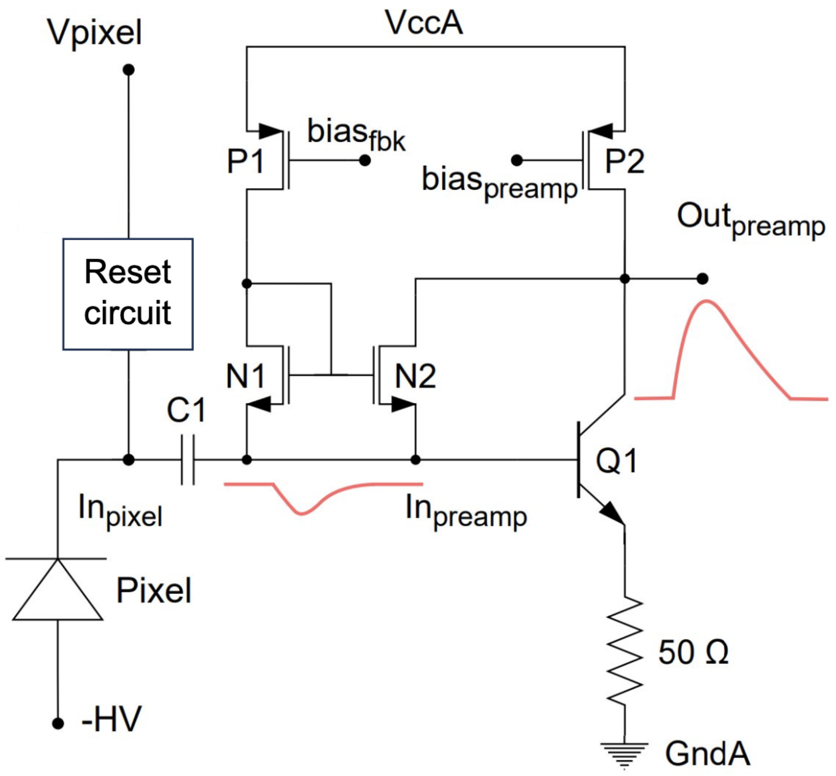
Pixel matrix cross-section

Analog electronics in pixel electrode deep-nwell (100% sensitive region)

Digital electronics placed in a separate deep-nwell to improve noise robustness (non-sensitive region)



Front-end



+ pixel level test-pulse

Front-end with input AC coupling to allow $V_{in\_preamp} < V_{ccA}$

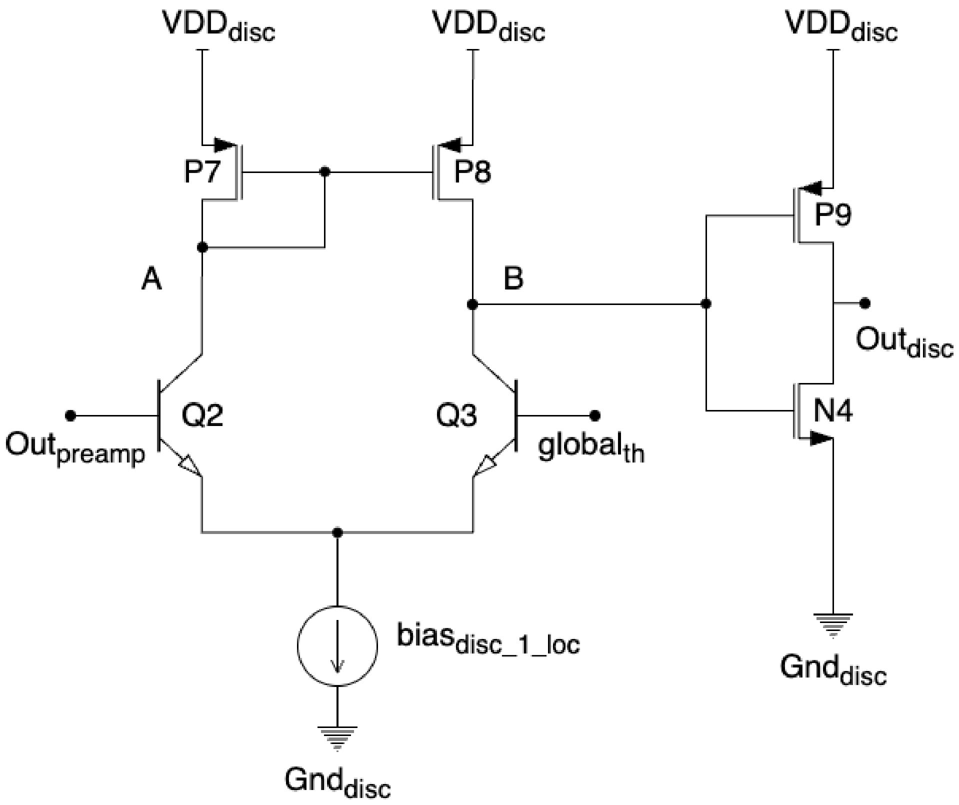
- $V_{in\_pixel} \approx V_{ccA} = 1.2$ V
- $V_{in\_preamp} \approx 0.7$ V

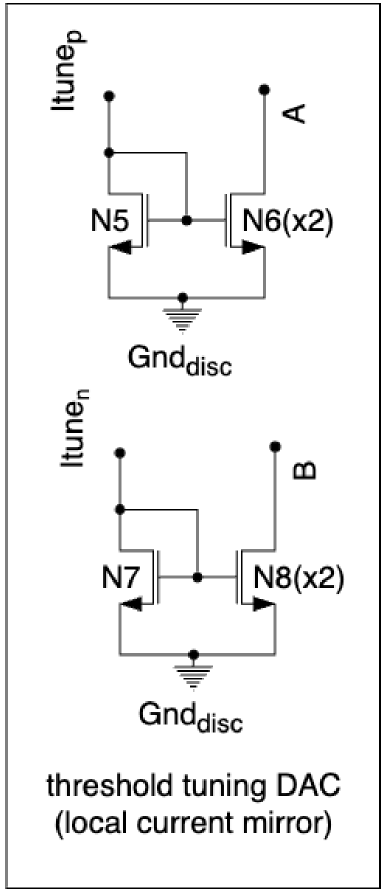
Input Hetero-junction Bipolar Transistor (HBT), good trade-off power vs gain & bandwidth

$I_{bias\_preamp} = 8.5$ µA

Gain ≈ 120 mV/fC

Discriminator





Input HBT pair, good for low mismatch

I_{bias_preamp} = 5 µA

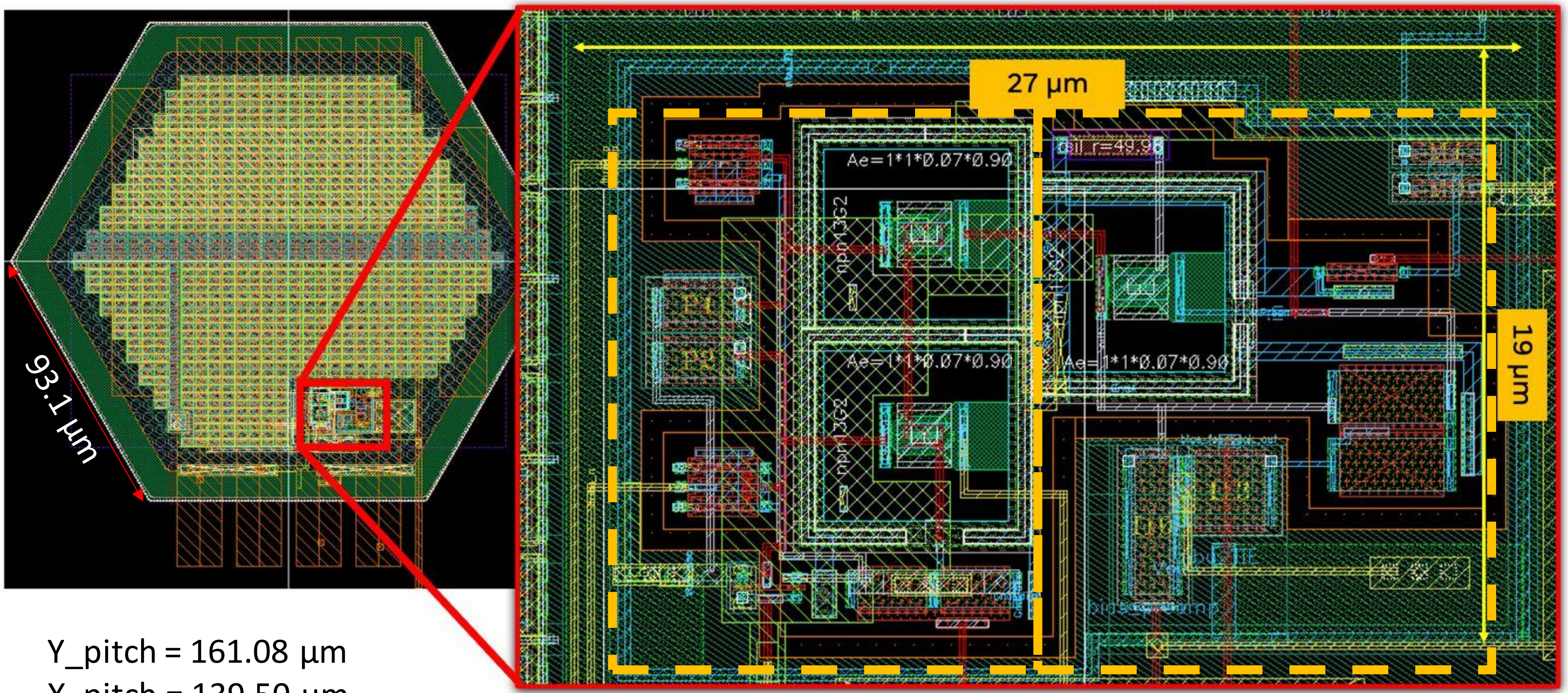
Pixel level masking

Pixel level threshold tuning (3 Bit DAC)

Mismatch in simulation before tuning ≈ 200 e^-

→ ToT measurement via periphery TDC

Pixel layout

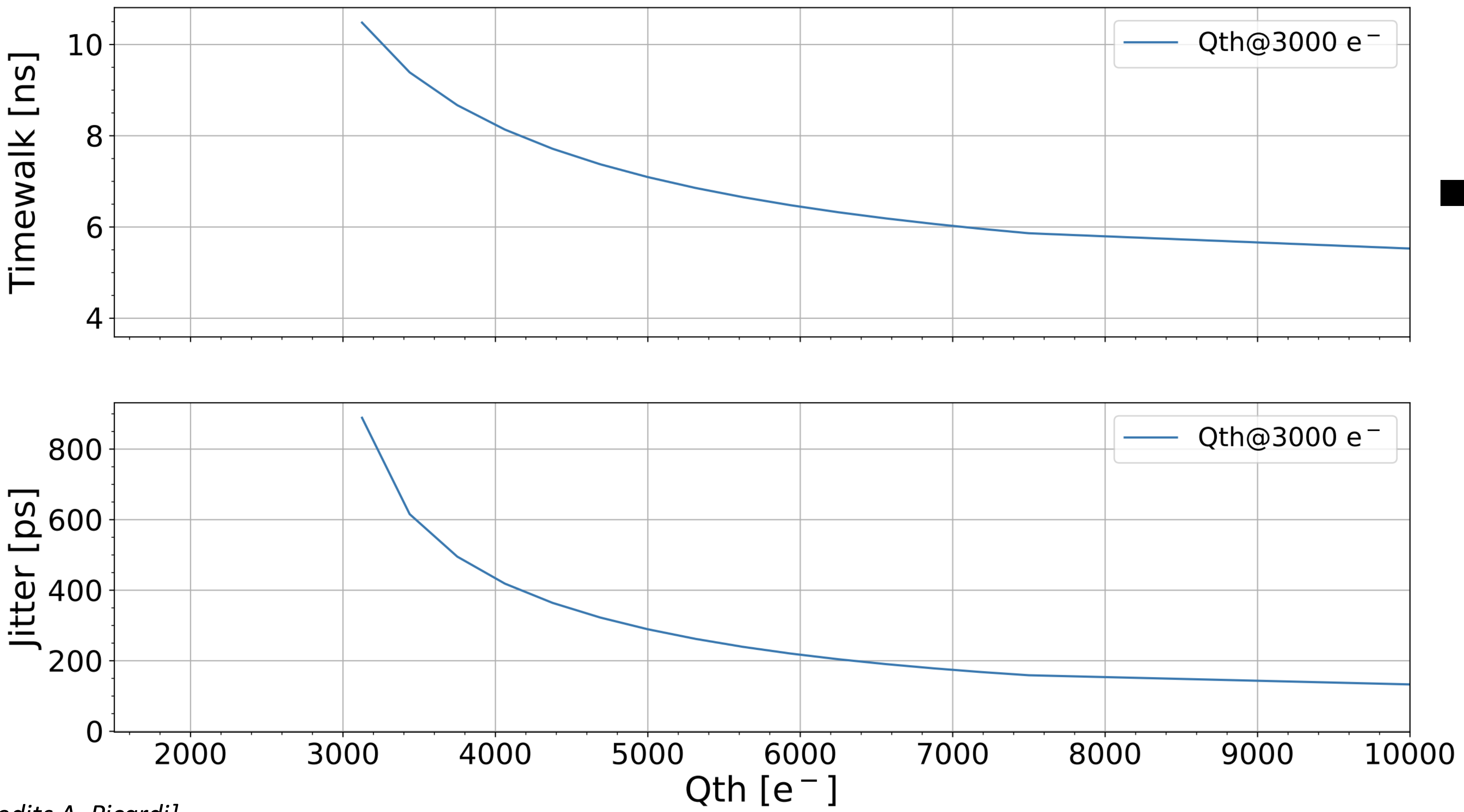


Discriminator

Front-end

Y_pitch = 161.08 µm
X_pitch = 139.50 µm
Area = (150 µm)^2

Front-end + Comparator Timing simulation

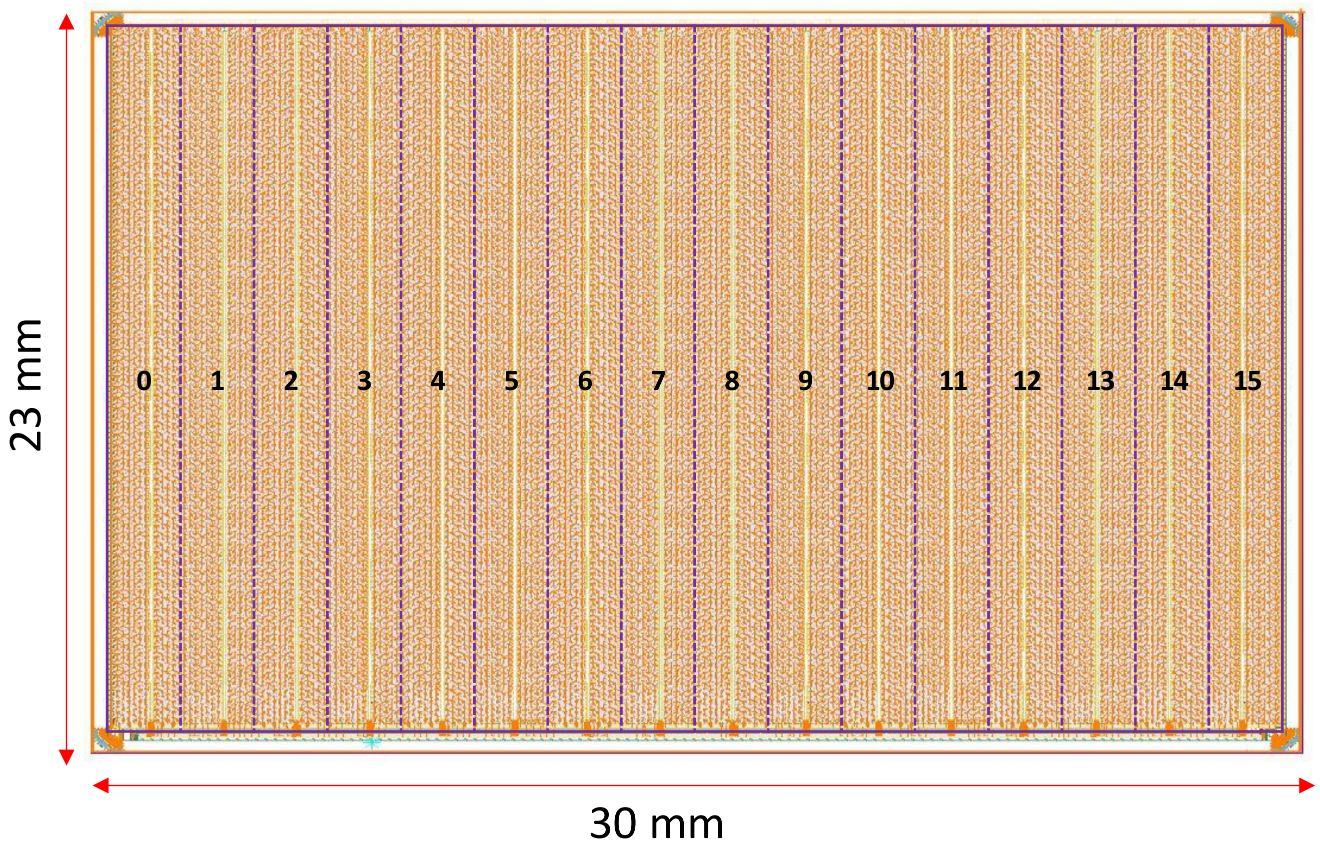


Timewalk correction with ToT

< 200 ps
for Qin > 6.5 ke^{-}

[Credits A. Picardi]

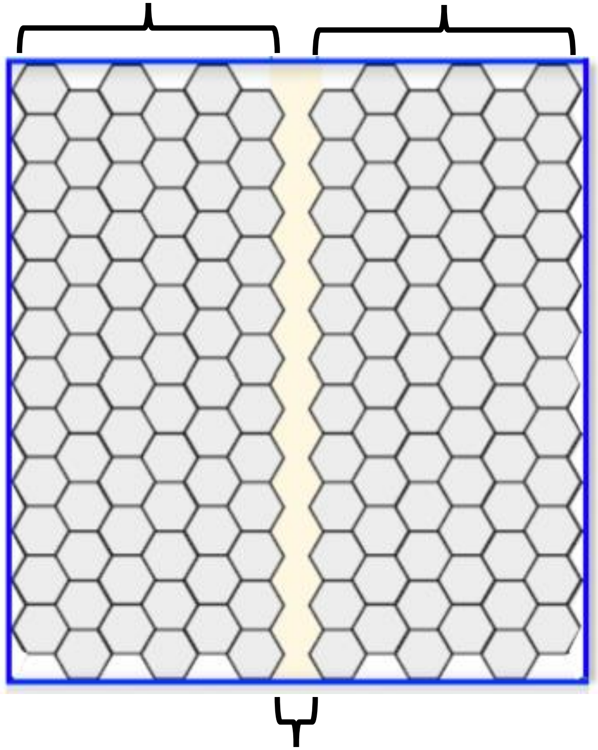
Pixel Matrix



Super Colum
11 Super Pixels

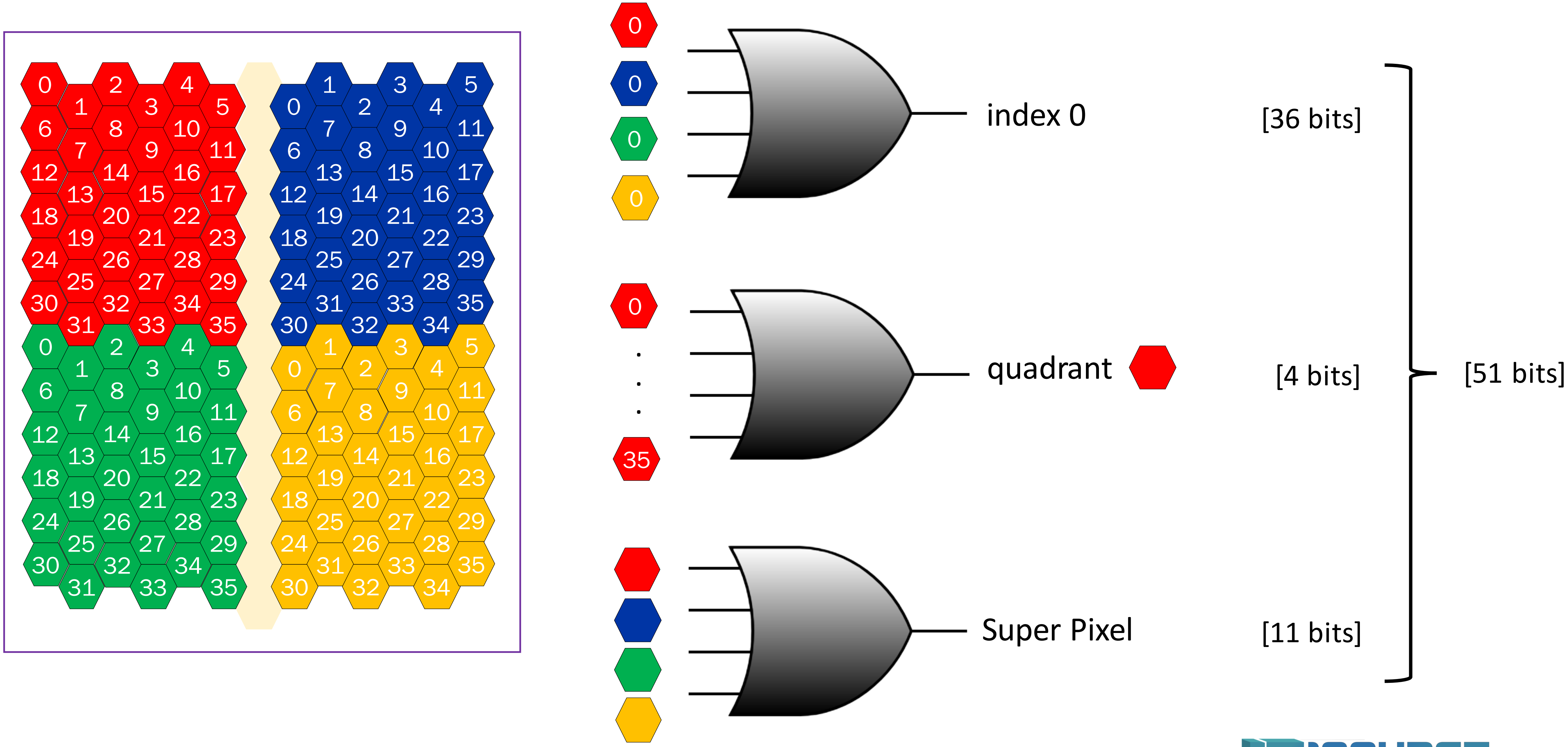
0
1
2
3
4
5
6
7
8
9
10

Super Pixel
12 x 12 pixels
(sensitive region)

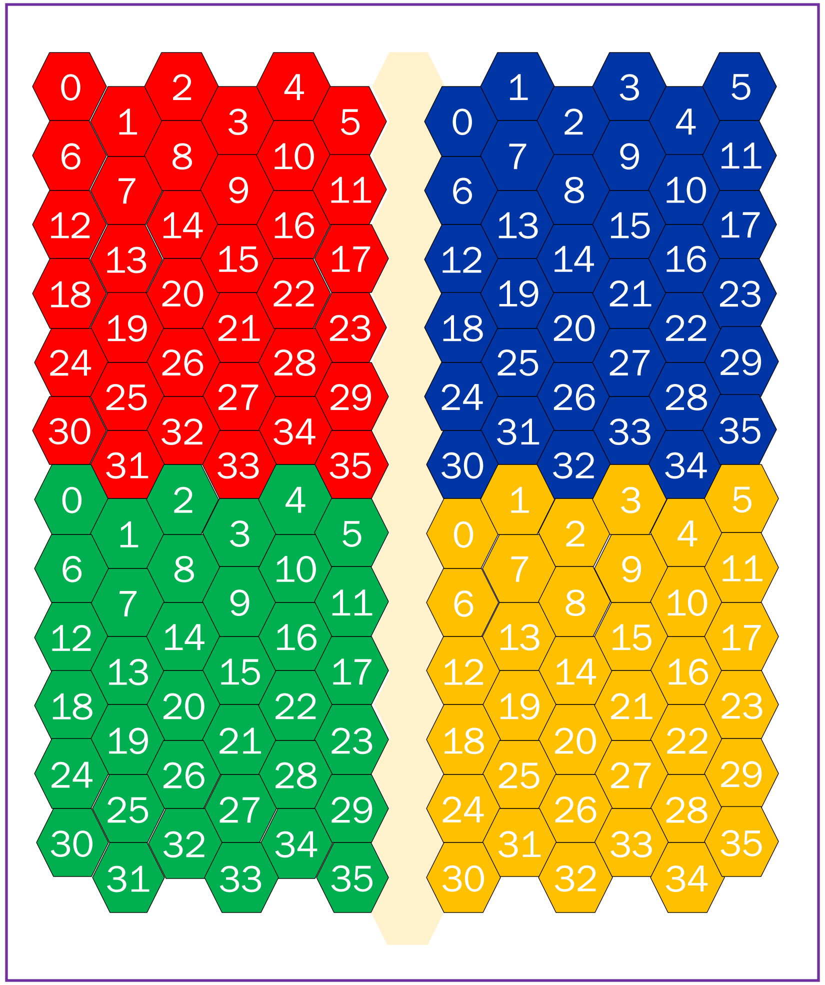


1 x 12 pixels
digital read-out and configuration
(non-sensitive region)
1/13 of matrix area (7.7%)

Pixel Address Encoding

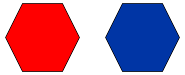


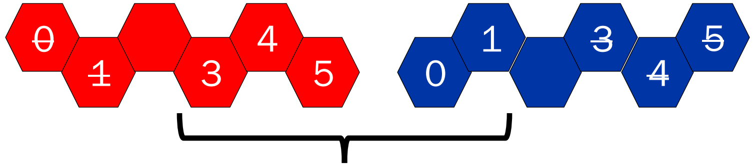
Pixel Address Encoding



Quadrants of 6x6 pixels [NxN]

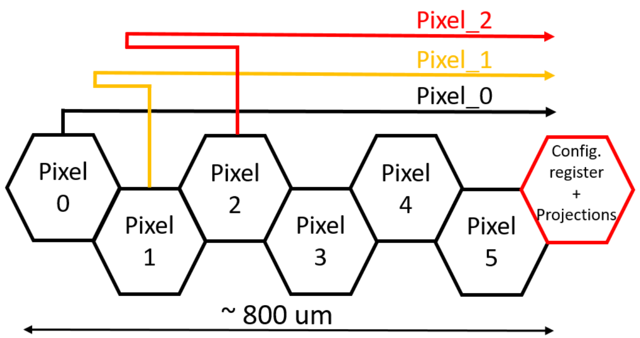
Maximum cluster size 5x5 pixels [(N-1)x(N-1)]

If we get: 0,1,3,4,5 & quadrants 

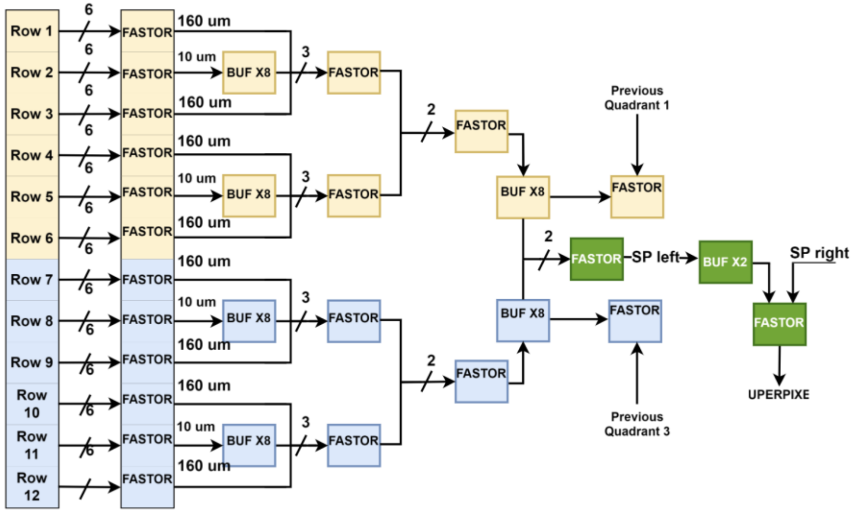


Asynchronous FAST-OR to TDC

Delay line matching

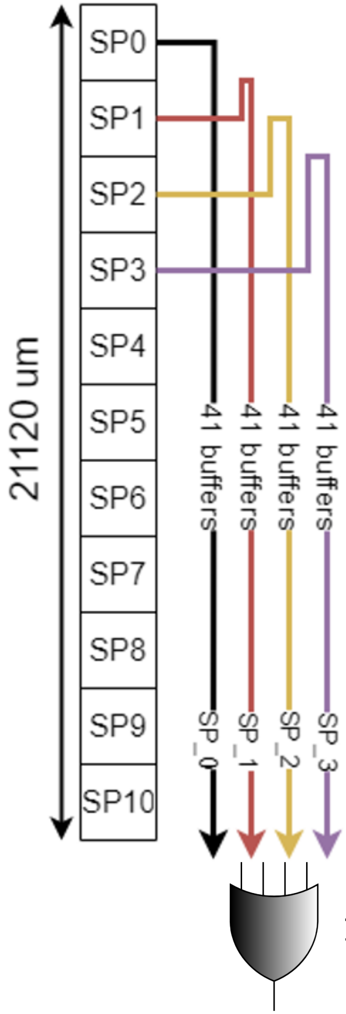


Super-pixel fast-OR tree



[Credits L.Iodice]

Super-column propagation



11 Super-Pixel output fast-OR

TDC [LSB 150 ps]

1 TDC channel/Super Pixel

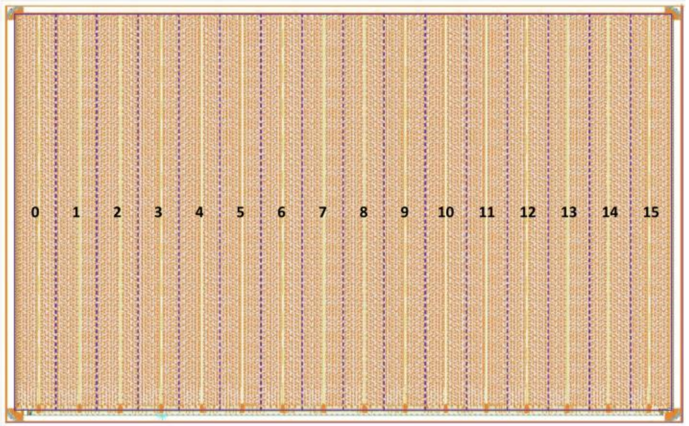
Simulation results

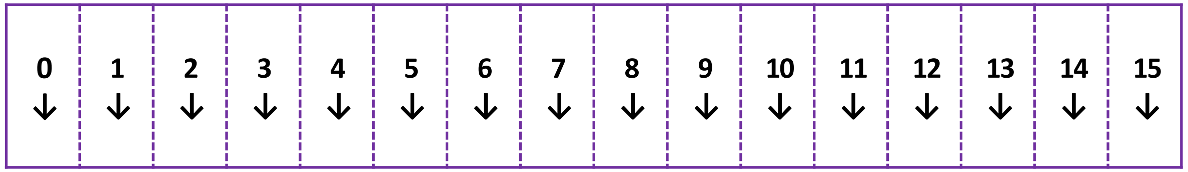
Max skew	67 ps
Mismatch rms	11 ps
Jitter rms	0.5 ps
T. coeff.	0.6 ps/C
V. coeff.	7.3 ps/mV

No pixel-to-pixel delay calibration required

Read-out

16 Super Columns

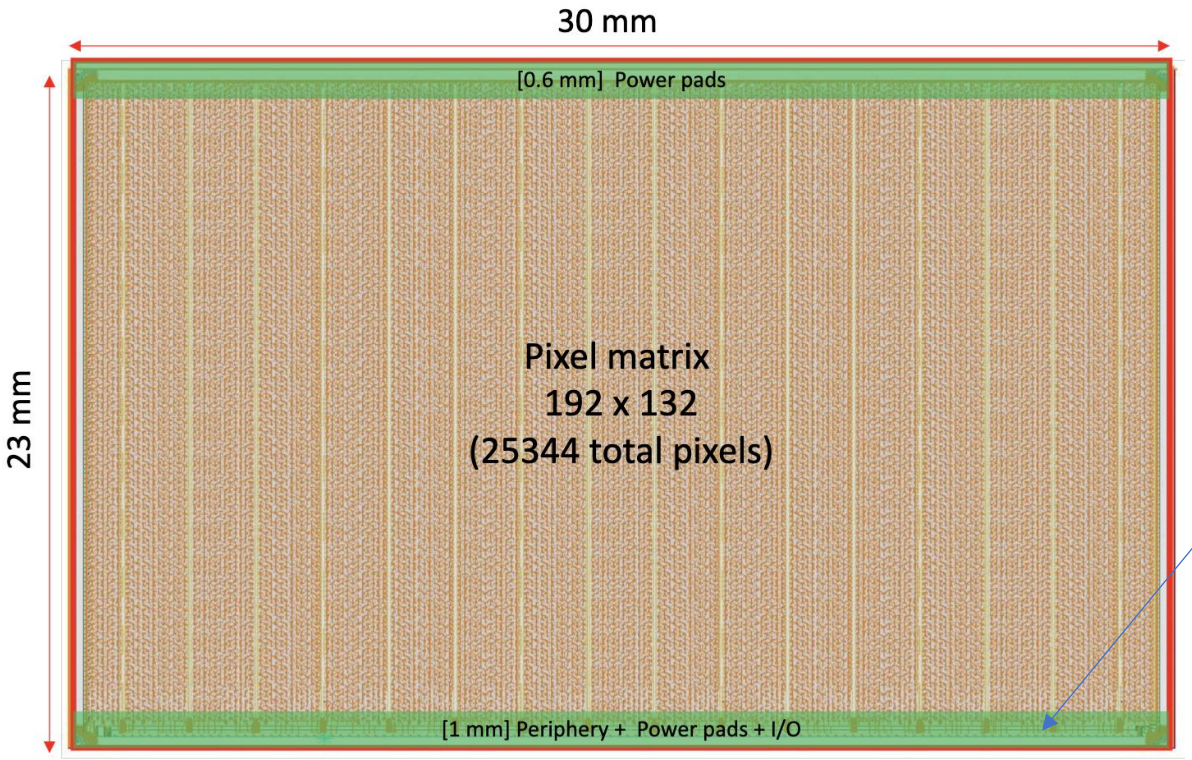




Each super-column provides pixel address and TDC data: event size of 143 bits

- No readout clock to the matrix. Only configuration.
  - Good noise immunity in the pixel region
  - Reduction of clock distribution power
- 3 level memory read-out buffers for hit de-randomization
- Chip-level global time stamping and synchronization with super-column level TDC
- Read-out speed 50 Mb/s (with 50 MHz clock)
  - Max read-out event rate 350 k events/s,
  - Maximum expected rate for quad module (24 cm^2 x 10 kHz/cm^2)=240 k events/s

ASIC periphery



- Read-out and configuration (SPI)
- Bandgap for analog reference current, independent from Process, supply Voltage, Temperature.
- Digital to Analog Converters (DACs)
- Low Voltage Differential Signal (LVDS)
  - In Read-out CLK (50 MHz),
  - Data Out 50 Mbit/s
  - Fast-OR Out for debugging
  - Data in for chip to chip data transfer

Power domains:

- **Digital:** for readout and TDC.
- **Oscillator:** only TDC ring oscillators. Shares ground with Digital.
- **Discriminator:** only for discriminator, low resistance, low current.
- **Analog:** only for amplifier, pixel bias and analog memory reference.

Conclusions

- **60-layer monolithic silicon pixel scanner for ultra-high-resolution PET**
  - Improved resolution, detection volume: $(150\ \mu m)^2$ pixel area and 550 µm DOI
  - 24.3 Mpixels

- **6 cm^2 Monolithic pixel sensor chip, 25 kpixels**
  - IHP 130 nm Bi-CMOS process from IHP
  - Submitted for production in October 2023, test start in June 2024

- **ASIC design and simulations:**
  - Design to detect single cluster events (max 5x5 pixles) up to 10 kHz/cm^2
  - Pixel jitter of 200 ps, system level coincidence window of 1 ns with no pixel level delay calibration.
  - Pixel level threshold-tuning, high SNR at 3000 e- threshold
  - Power < 75 mW/cm^2

- **Delivery of a proof-of-concept scanner for small animals in 2025**