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Test results of the monolithic ASIC for the upgraded preshower detector of the FASER experiment at the LHC

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The FASER experiment at the Large Hadron Collider (LHC) aims to detect new, long-lived fundamental particles and to study neutrino interactions. To enhance its discovery potential, a W-Si preshower detector is being built, targeting surface commissioning and then installation during the second half of 2024. The new preshower will enable the identification and reconstruction of electromagnetic showers produced by high-energy photon pairs with separations as fine as $200\text{ }\mu\text{m}$. The detector incorporates a cutting-edge monolithic ASIC with hexagonal pixels measuring $100\text{ }\mu\text{m}$ in pitch, designed to achieve an extended dynamic range for charge measurement and capable of storing charge information for thousands of pixels per event. The ASIC integrates fast front-end electronics based on SiGe heterojunction bipolar transistor technology, providing a $O(100)$ ps time resolution. Analog memories embedded within the pixel array facilitate frame-based event readout, minimizing dead areas. In this presentation, we detail the design and expected performance of the preshower detector, along with the results from lab characterisation of pre-production ASIC prototypes, and of the first module prototypes.

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