UNIVERSITÉ
DE GENÈVE
FACULTÉ DES SCIENCES
Département de physique
nucléaire et corpusculaire

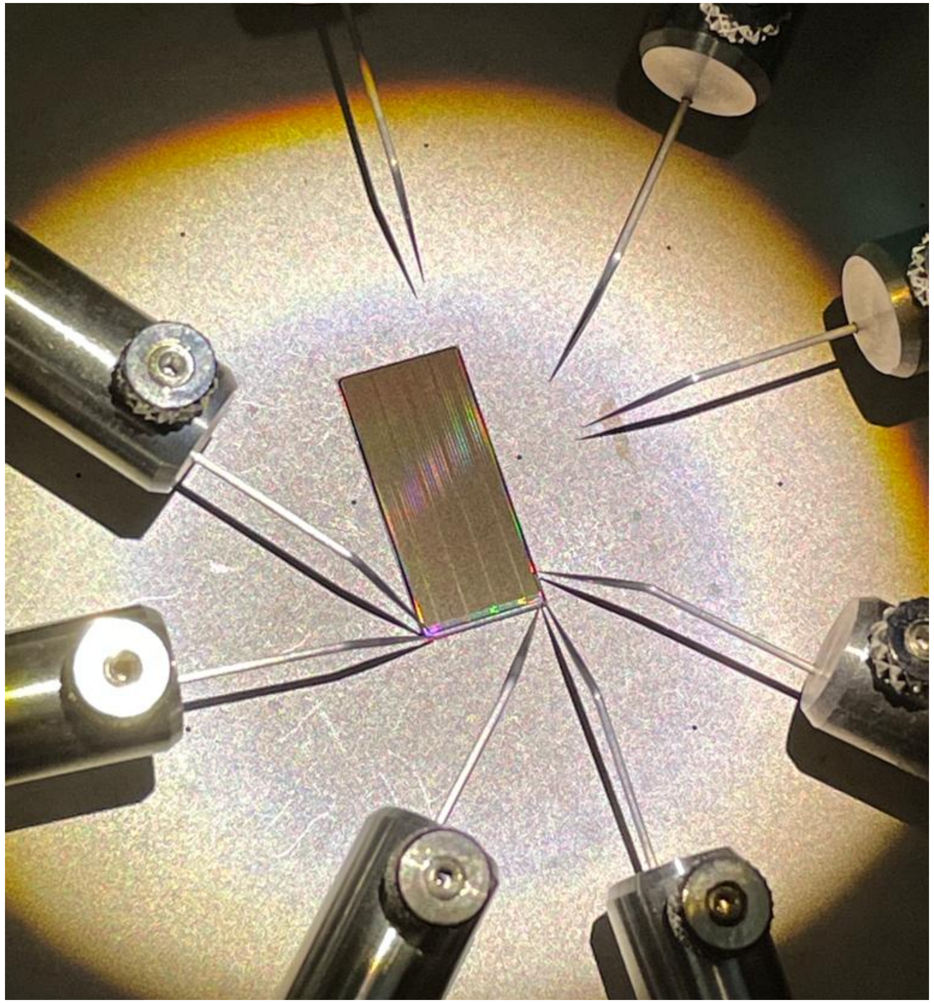
Test Results of the Monolithic ASIC for the Upgraded Preshower Detector of the FASER Experiment at the LHC

CHIARA MAGLIOCCA
on behalf of the FASER Preshower Upgrade Team

TREDI 2024, Turin

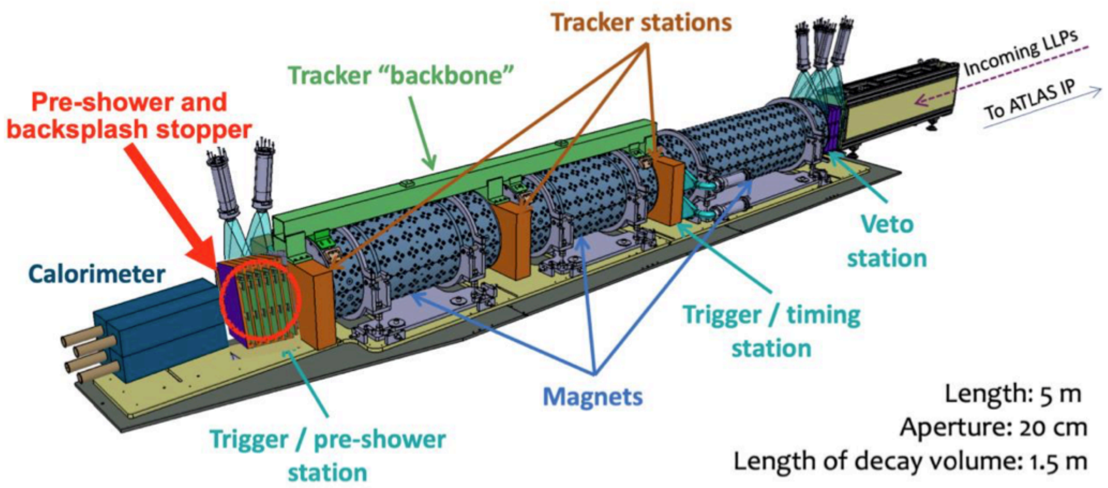
Outline

1. Introduction: FASER Experiment
2. Preshower Upgrade: the Monolithic Silicon Pixel ASIC
3. Tests and Results on the Pre-production Chip



THE FASER EXPERIMENT

The FASER Experiment at LHC



Forw**A**rd **S**earch **E**xpe**R**iment

- Designed to search for **light and weakly-interacting particles (LLPs)** + study the **interactions of high-energy neutrinos** (FaserNu)

- Fluxes of high-energy SM particles are supressed
- Muons and neutrinos only exception
- FASER can probe **Axion-Like-Particles** (ALPs) model

Zero degrees angle → huge LLPs flux

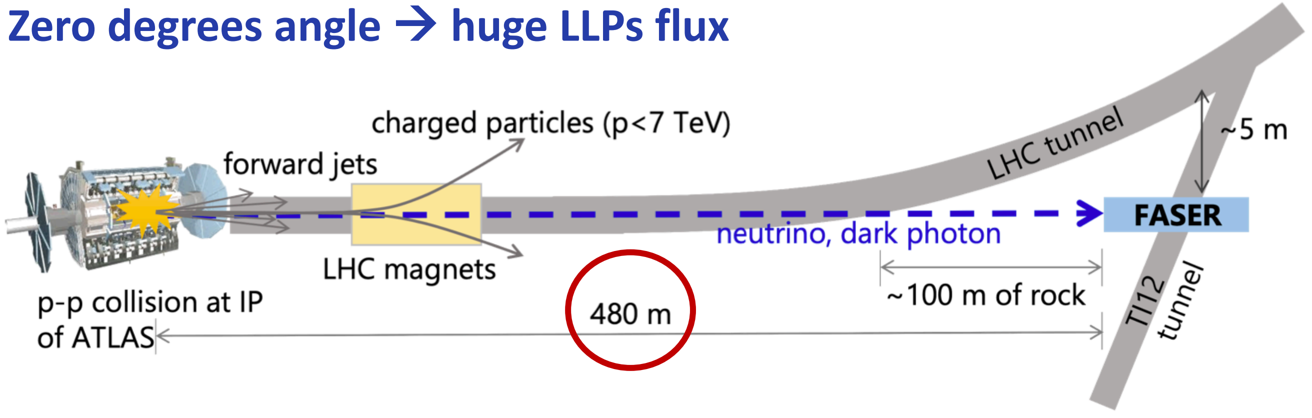
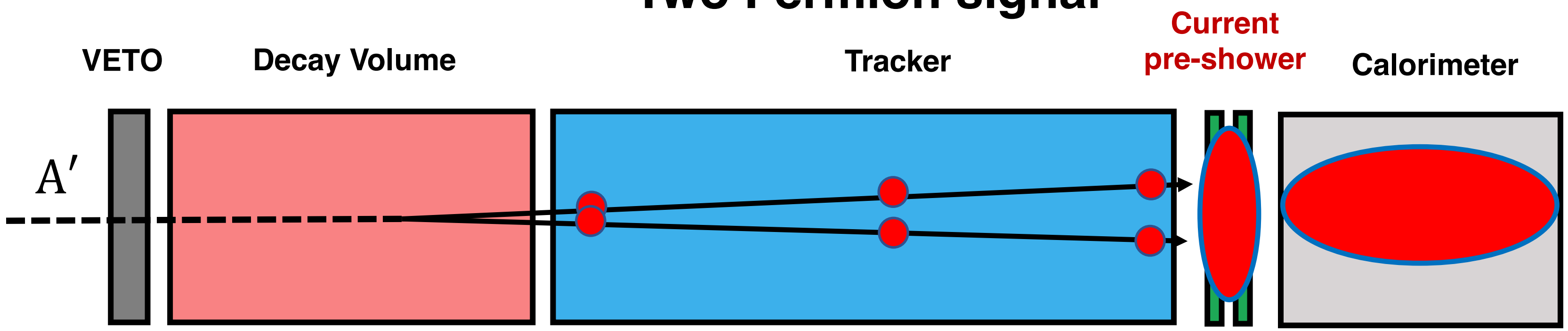


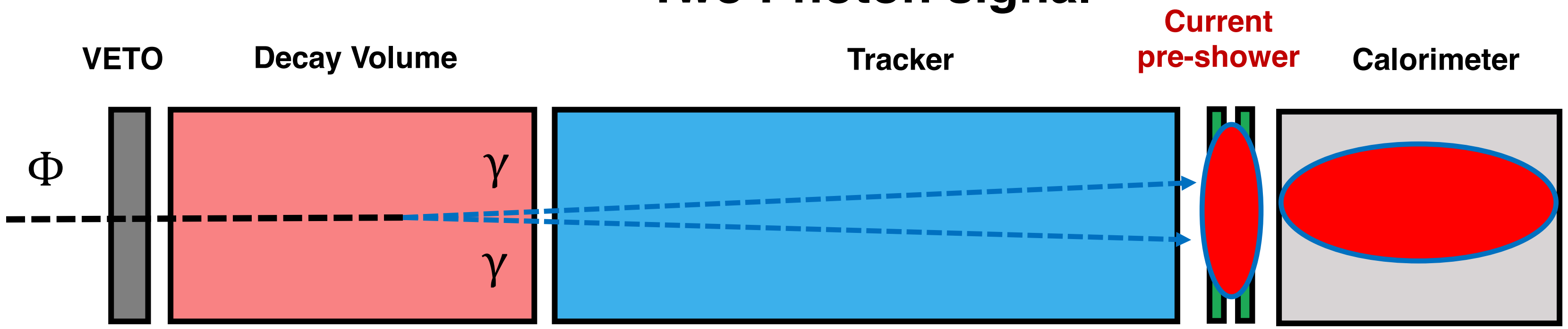
Figure: Location of FASER in the tunnel - schema is not in scale.

Current Detection Capabilities

Two Fermion signal



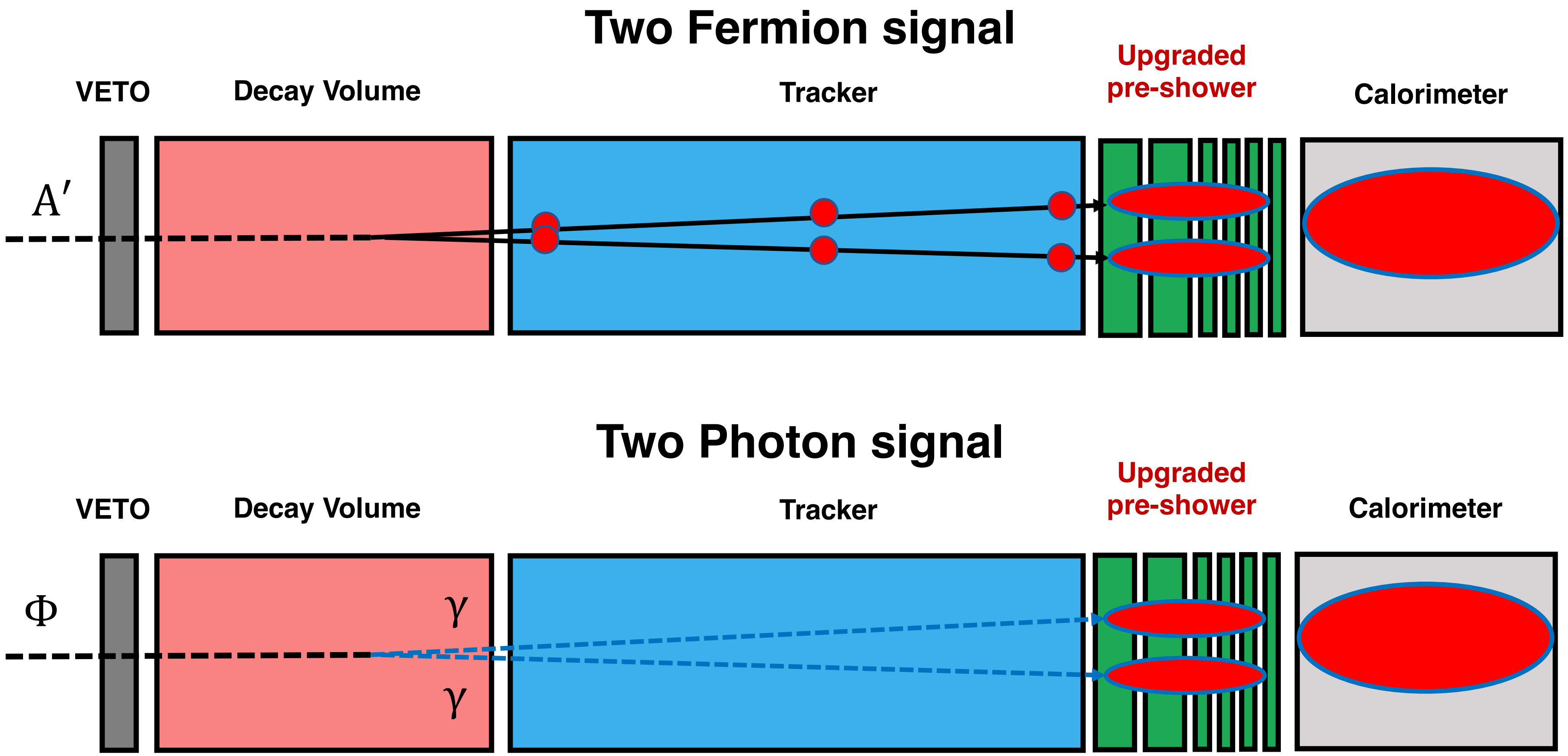
Two Photon signal



NO XY GRANULARITY

unable to resolve diphoton events!

Desired Detection Capabilities



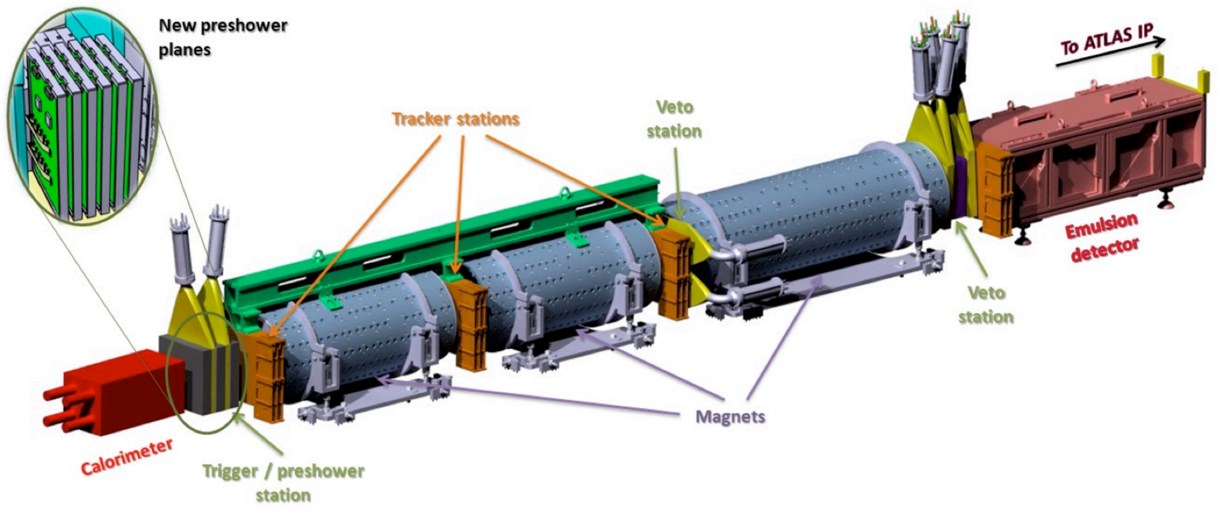
HIGH XY GRANULARITY

The FASER Pre-shower Detector Upgrade

Main Challenge:
Independent measurement of two very collimated high energy photons before the calorimeter

Current preshower:

2 layers of tungsten (1X0) + scintillating detectors
⇨ no XY granularity



The upgrade:

- **High granularity/high dynamic range** pre-shower based on monolithic silicon pixels sensors
- Discriminate **TeV scale electromagnetic showers**
- Targeting data-taking during last year of LHC Run 3 and HL-LHC

Pre-shower Upgrade Design

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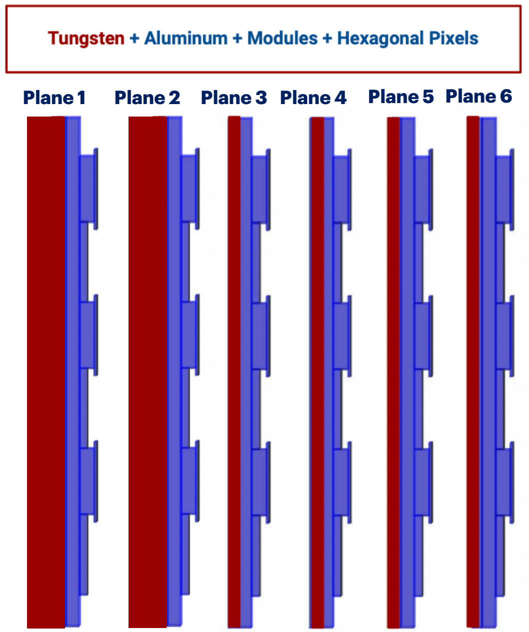
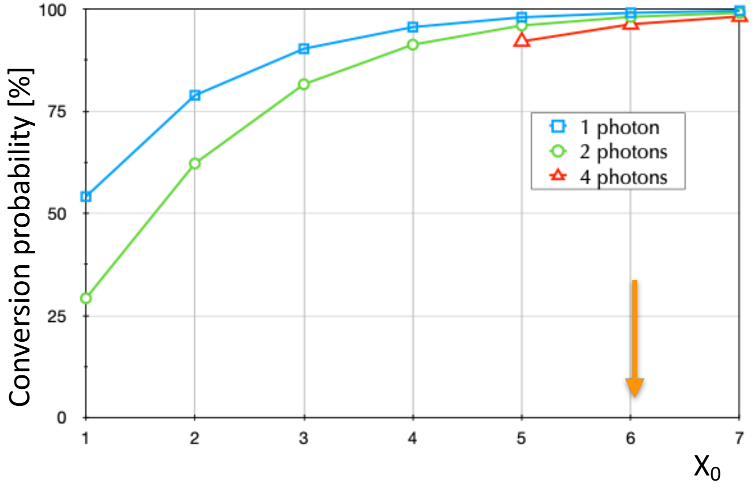
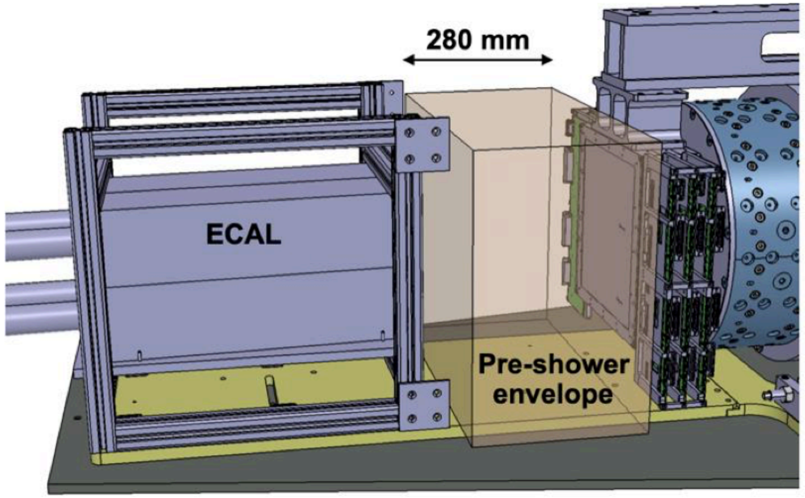
- 6 detector planes
- **$6X_0$ of tungsten in total**
- One plane of **monolithic Si-pixel sensors** after each tungsten layer

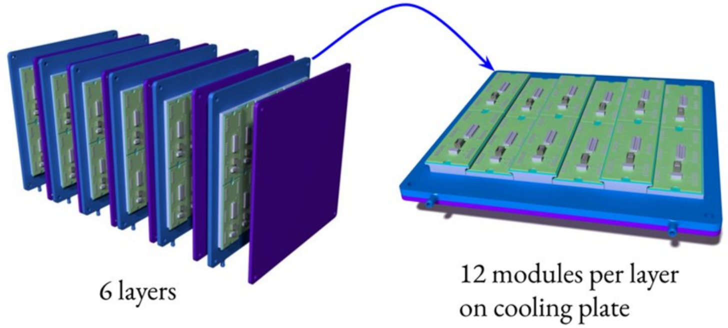


2*(1.70 X_0 of W + Si plane) + 4*(0.65 X_0 of W + Si plane)

More tungsten in the first two layers to force early photon conversion

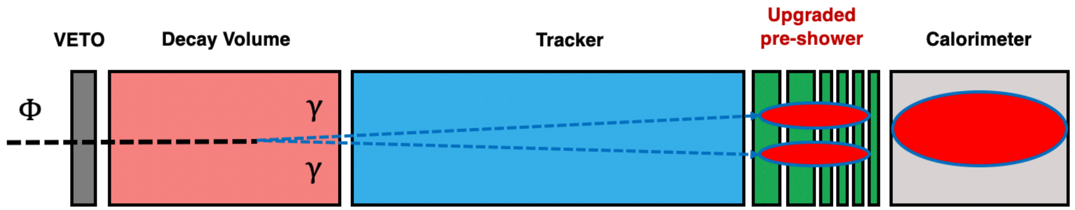




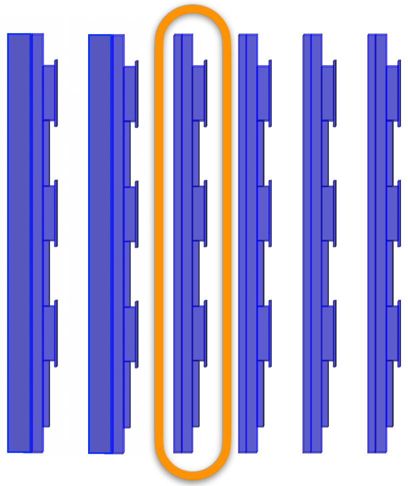


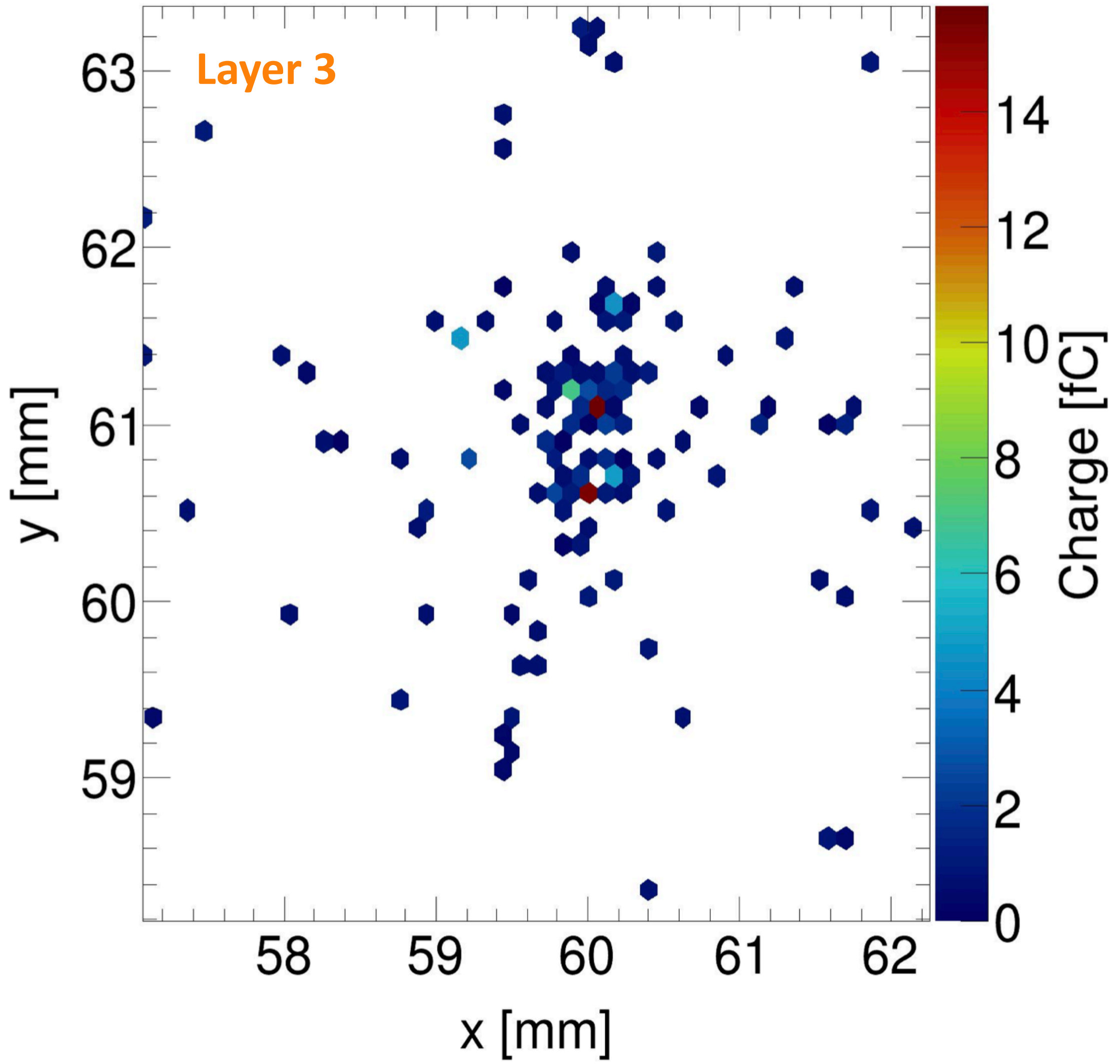
Pre-shower Simulation: Diphoton Signature

Why 6 planes?
Why pixelated sensors?



E1= 1 TeV
E2= 1 TeV
d=500um





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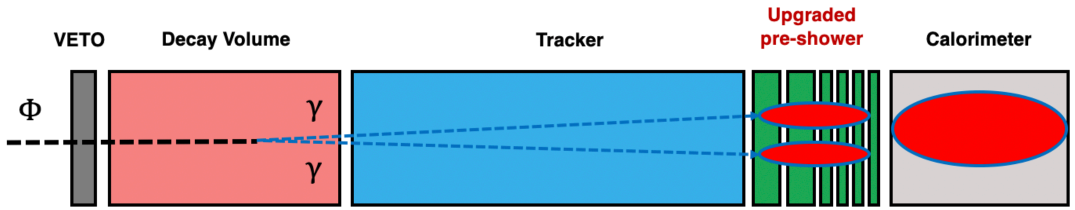

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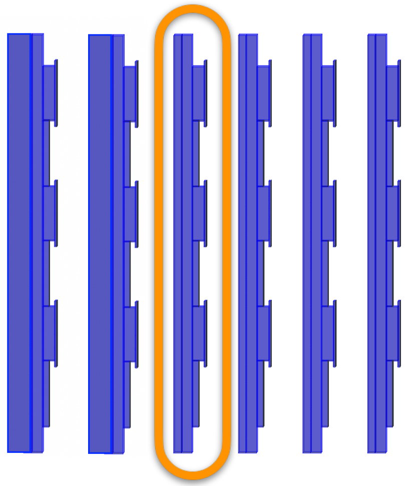

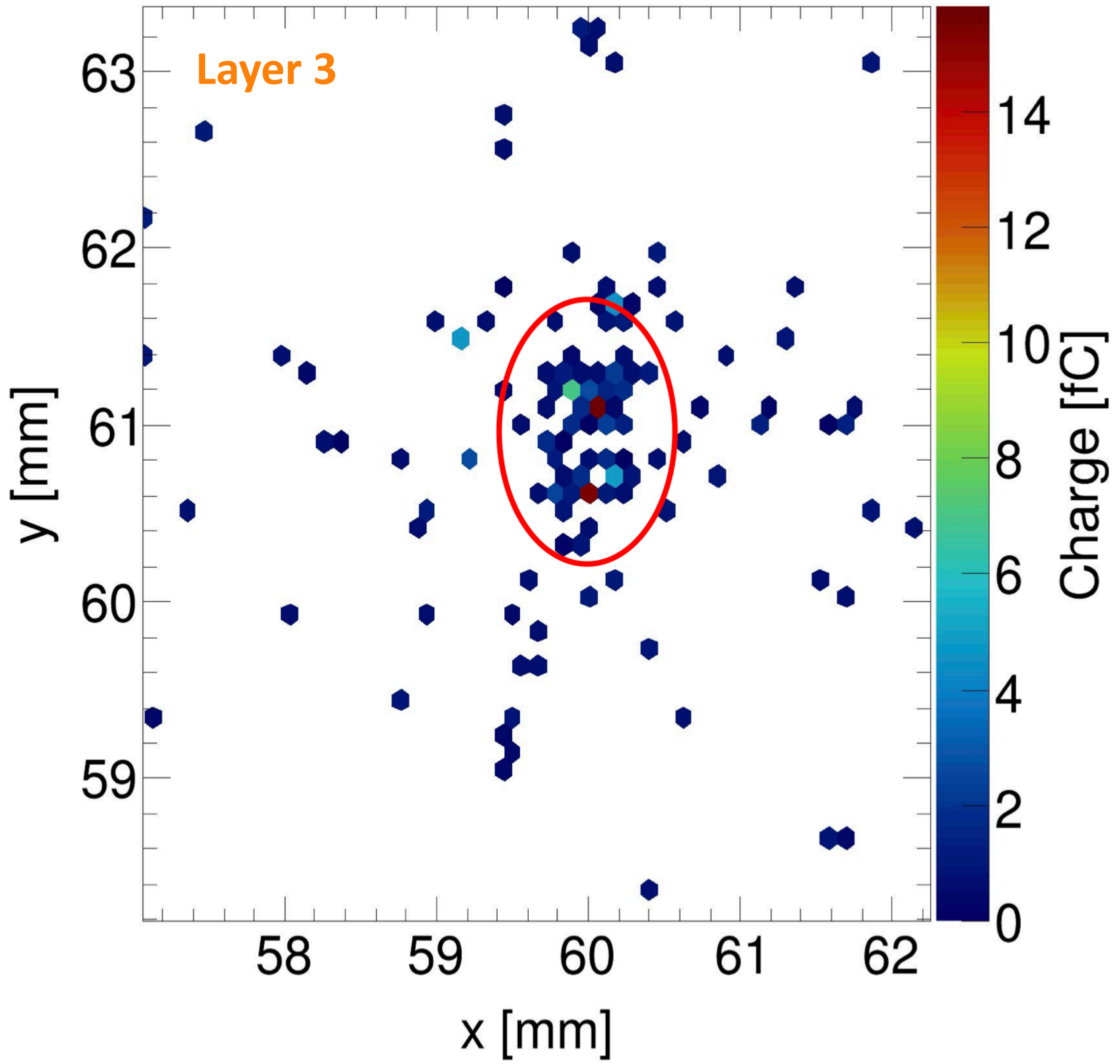

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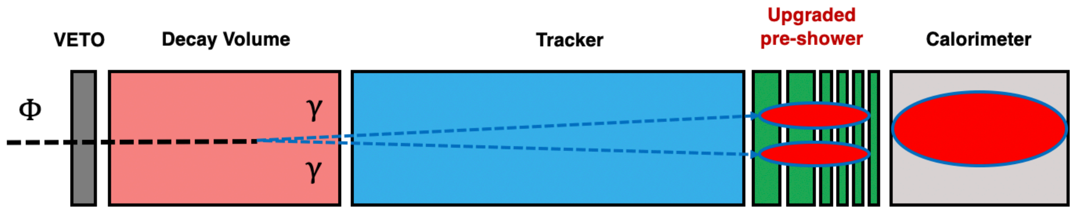

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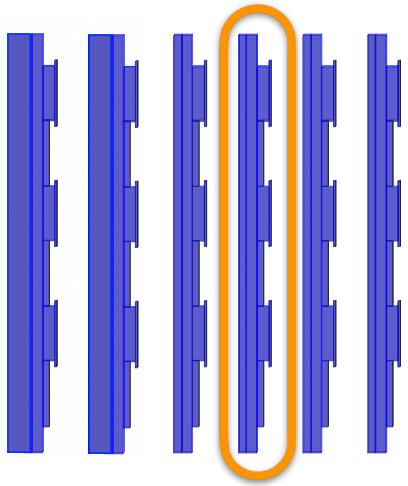

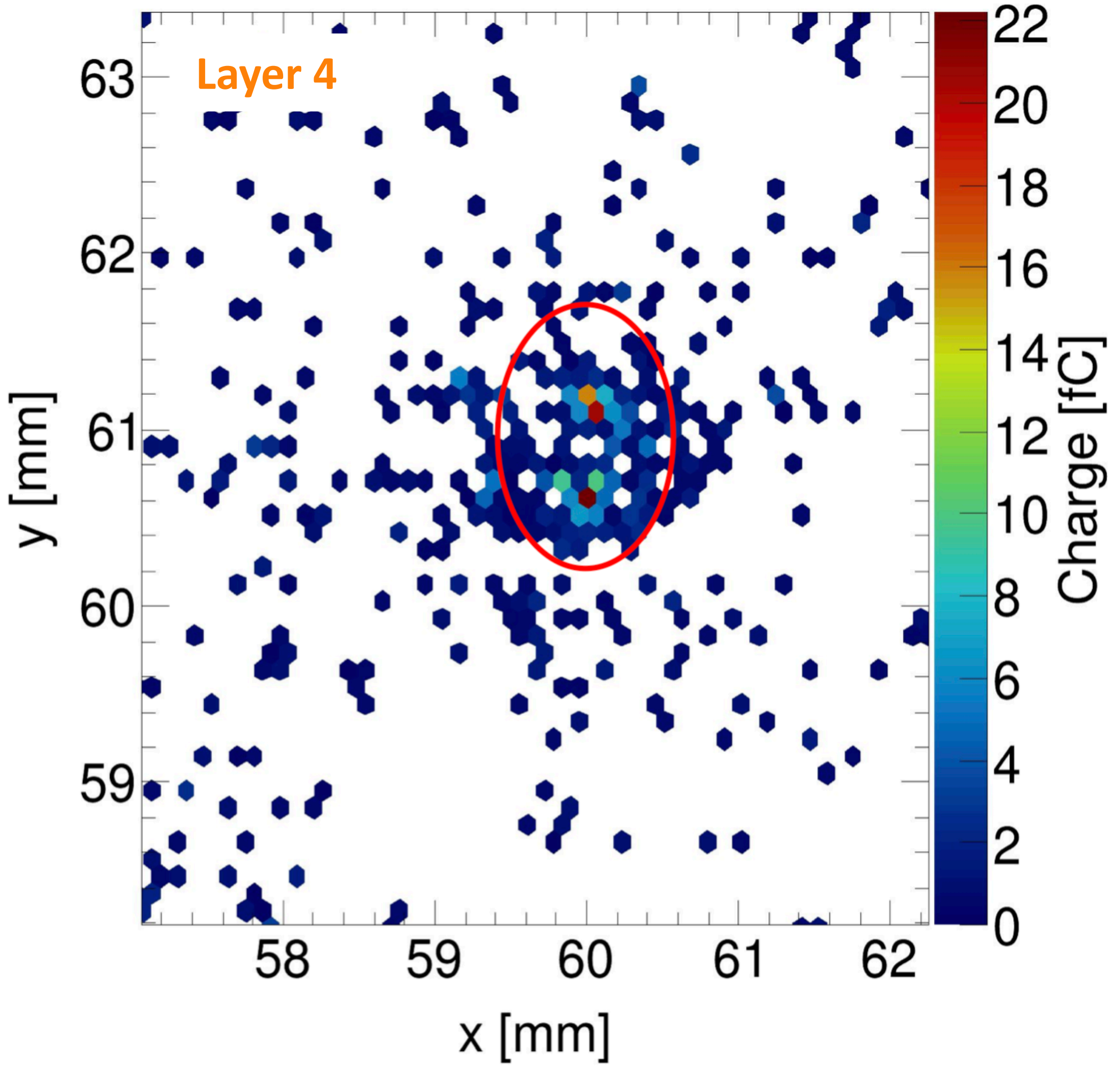

Pre-shower Simulation: Diphoton Signature

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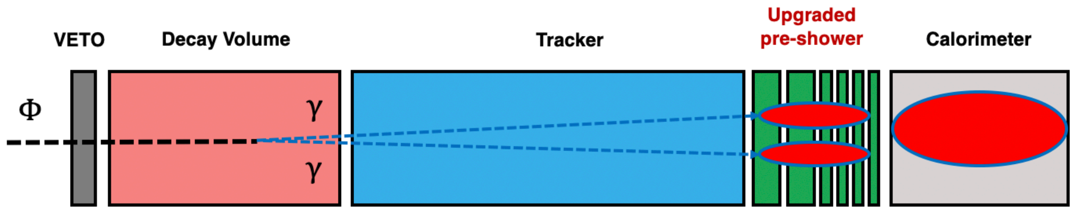

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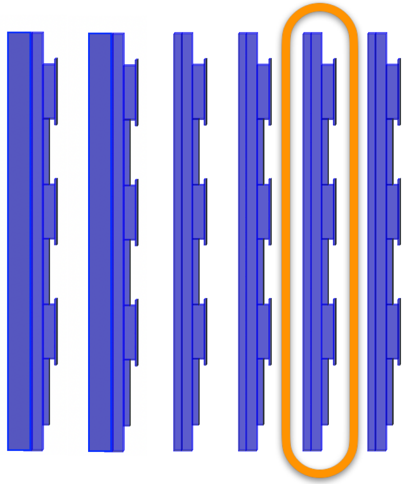

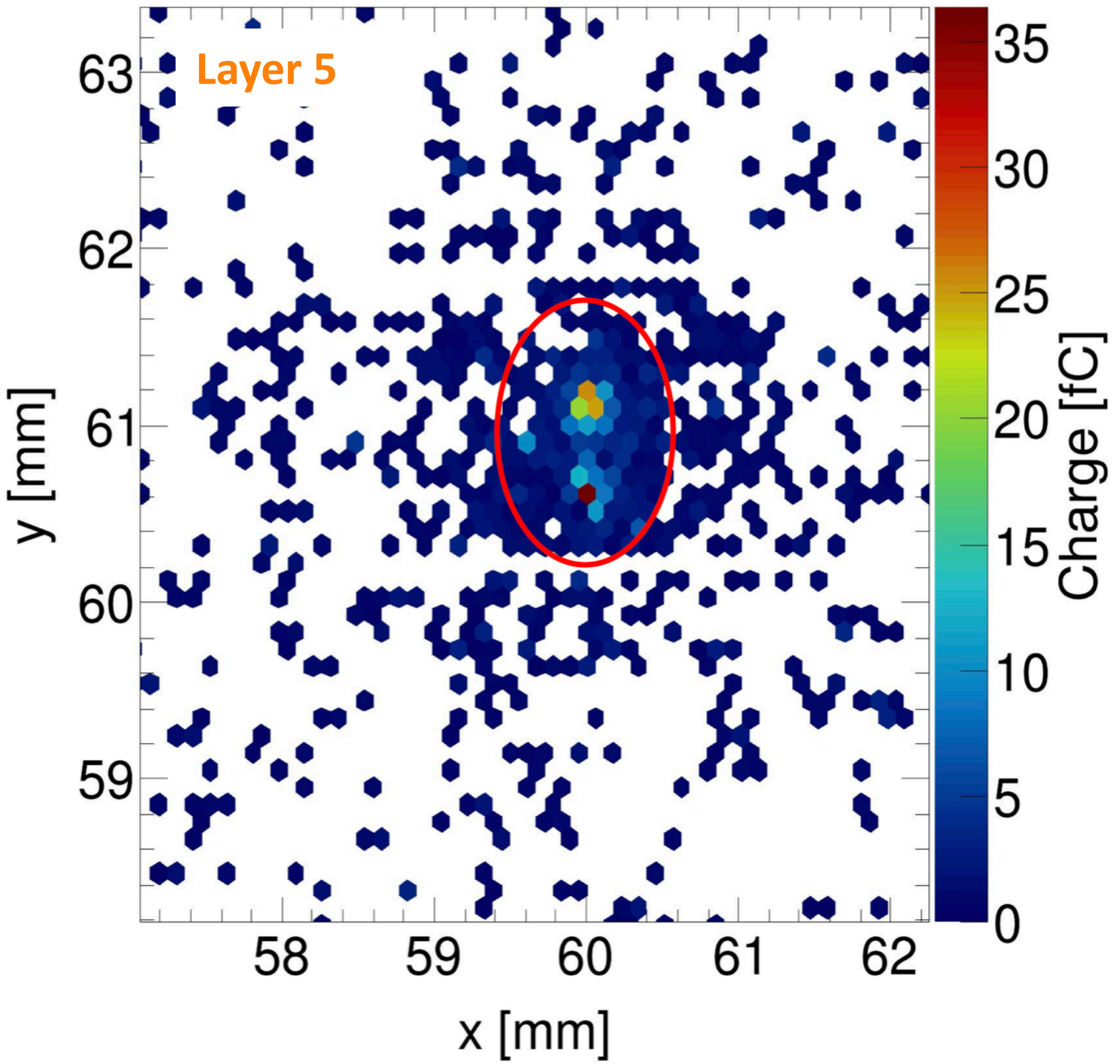

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Pre-shower Simulation: Diphoton Signature

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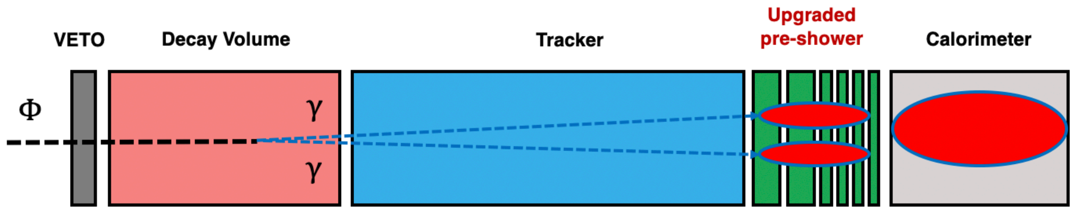

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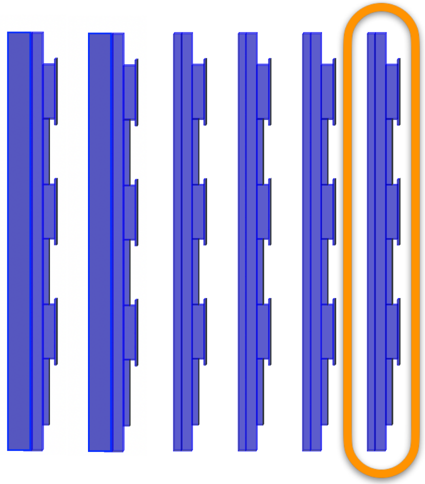
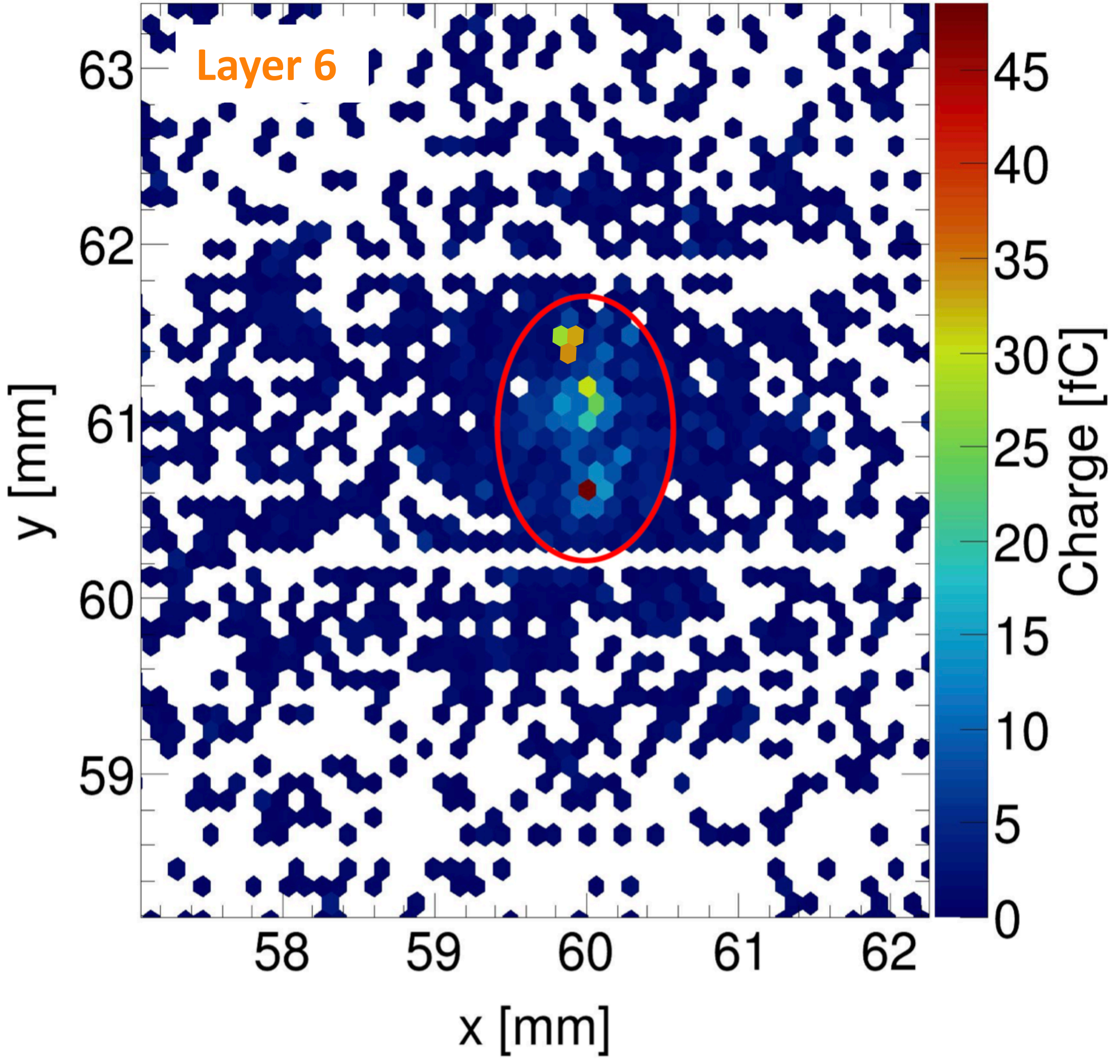


Layer 6



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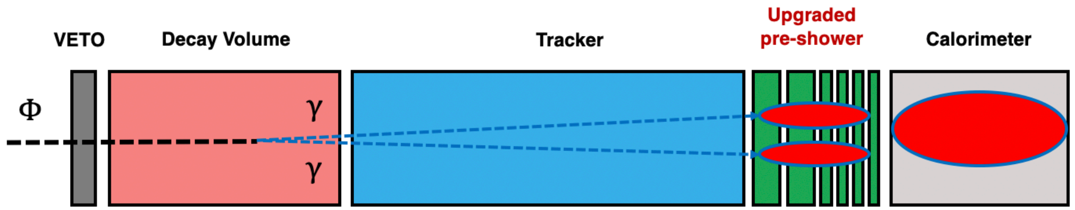

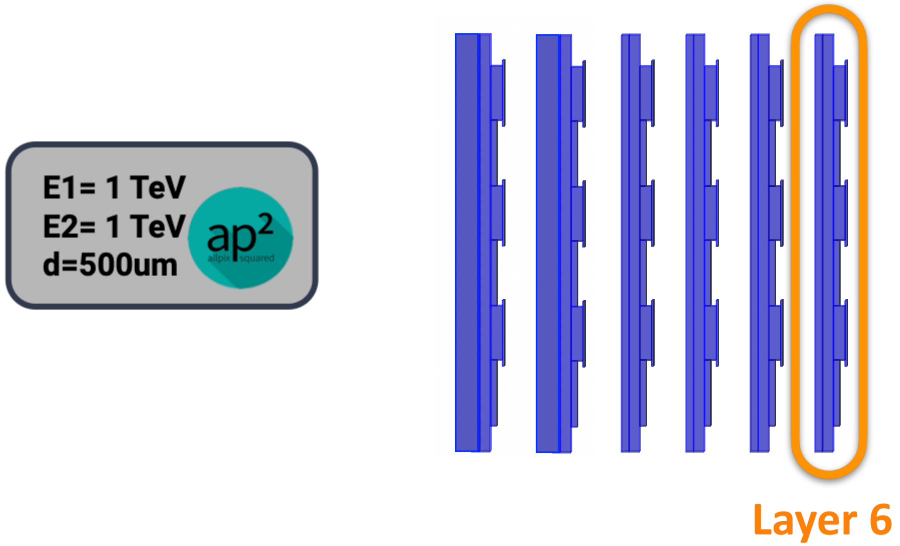

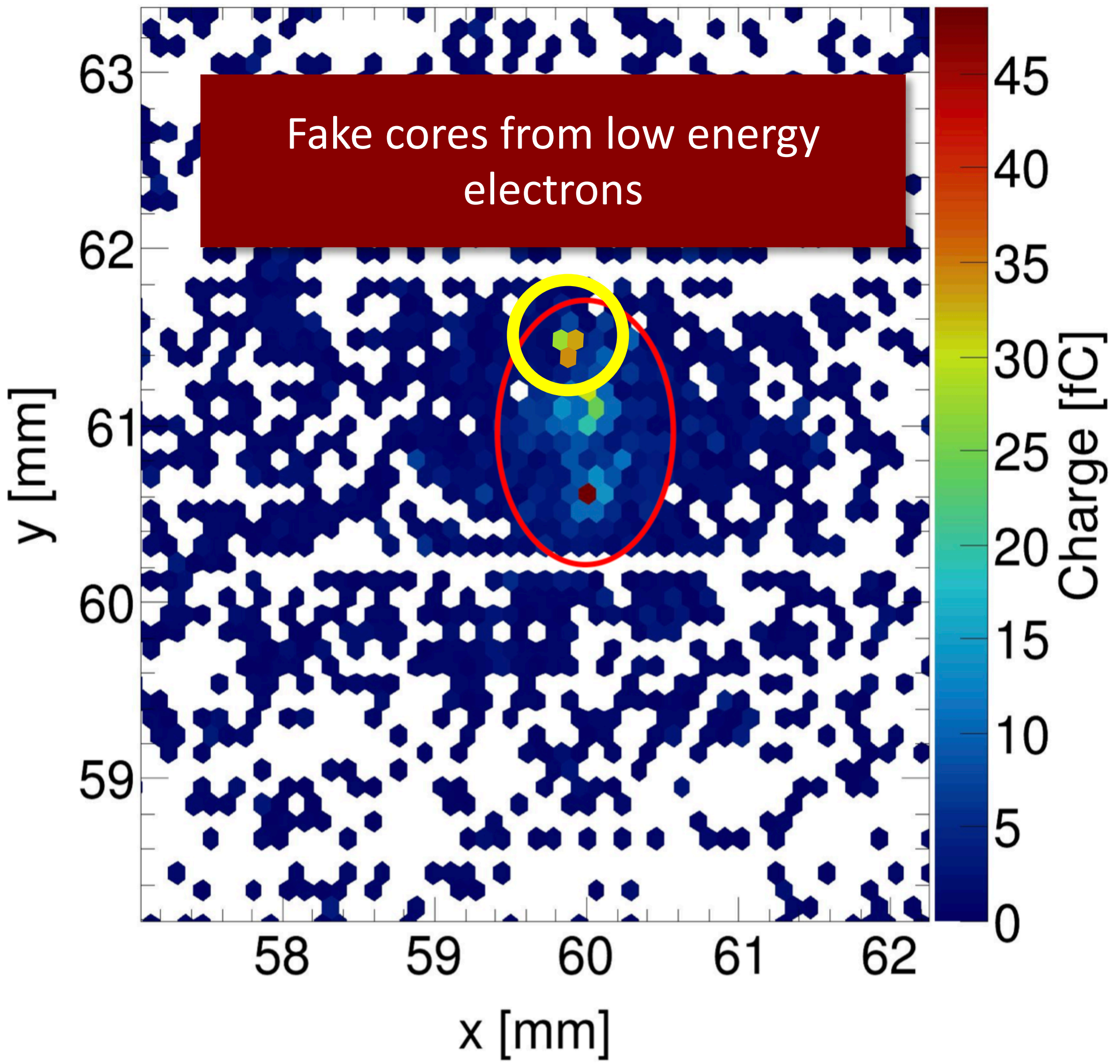

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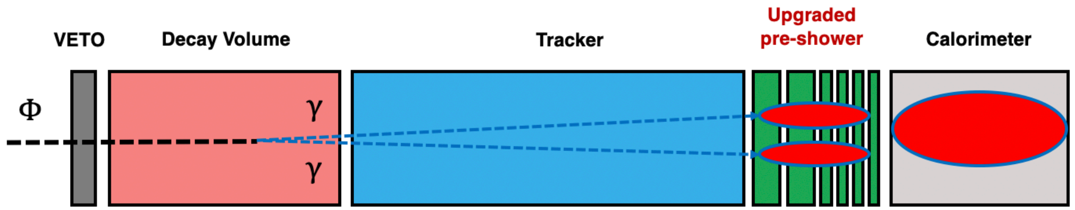
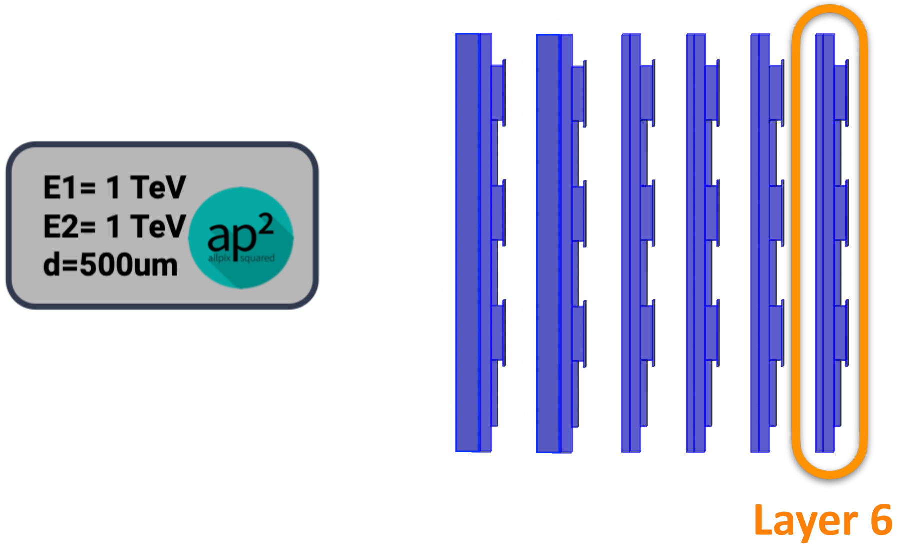
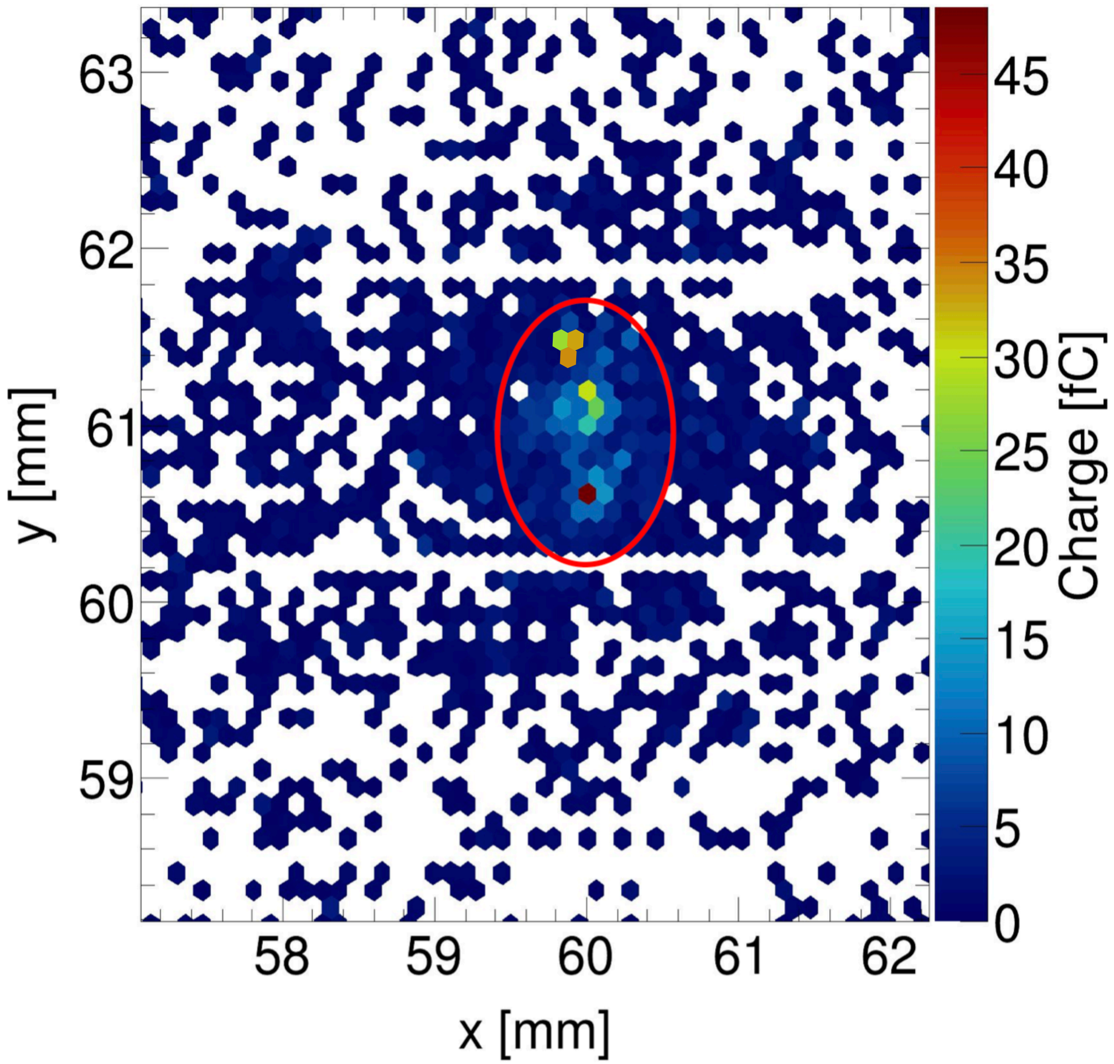




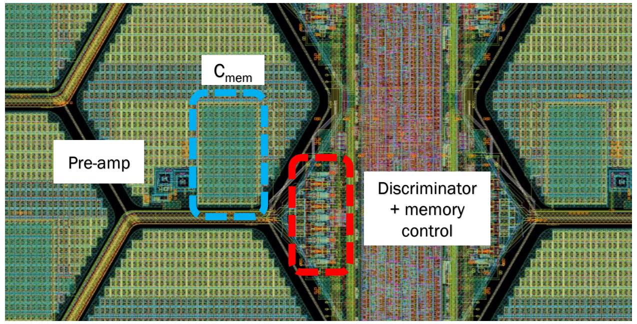
Very large occupancy

High dynamic range for charge measurements



THE MONOLITHIC PIXEL ASIC

The Sensor

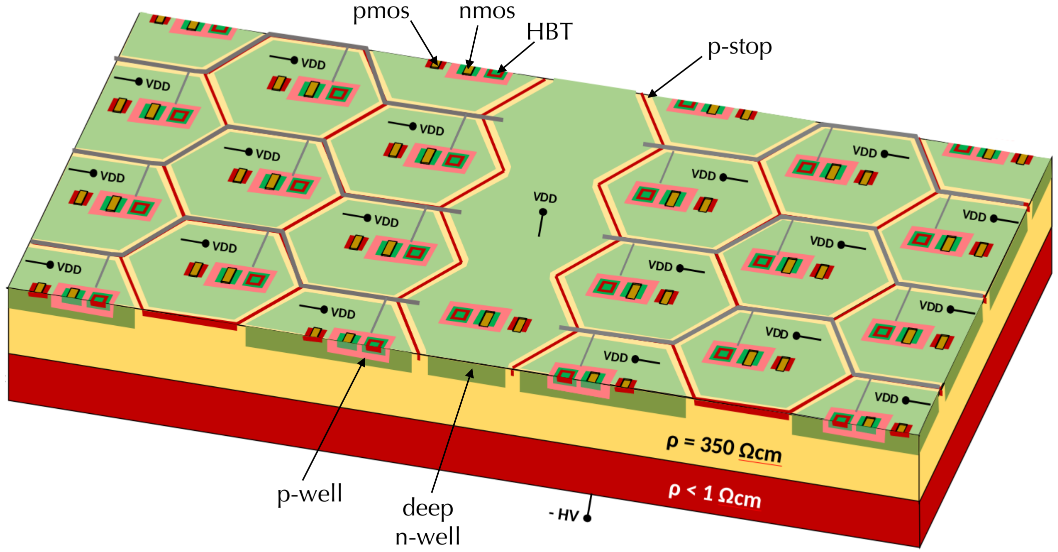


Monolithic active pixel sensor

130 nm SiGe BiCMOS technology (SG13G2 by IHP microelectronics)

- High-resistivity (220 Ωcm) substrate, about 130 μm thickness
- Hexagonal 65 μm side pixels integrated as triple well; 80fF pixel capacitance
- **High dynamic range** for charge measurement (0.5 ÷ 65 fC)
- **Ultra fast readout** with no digital memory on-chip (to minimize dead area)
- **Local analog memories** to store the charge in pixel

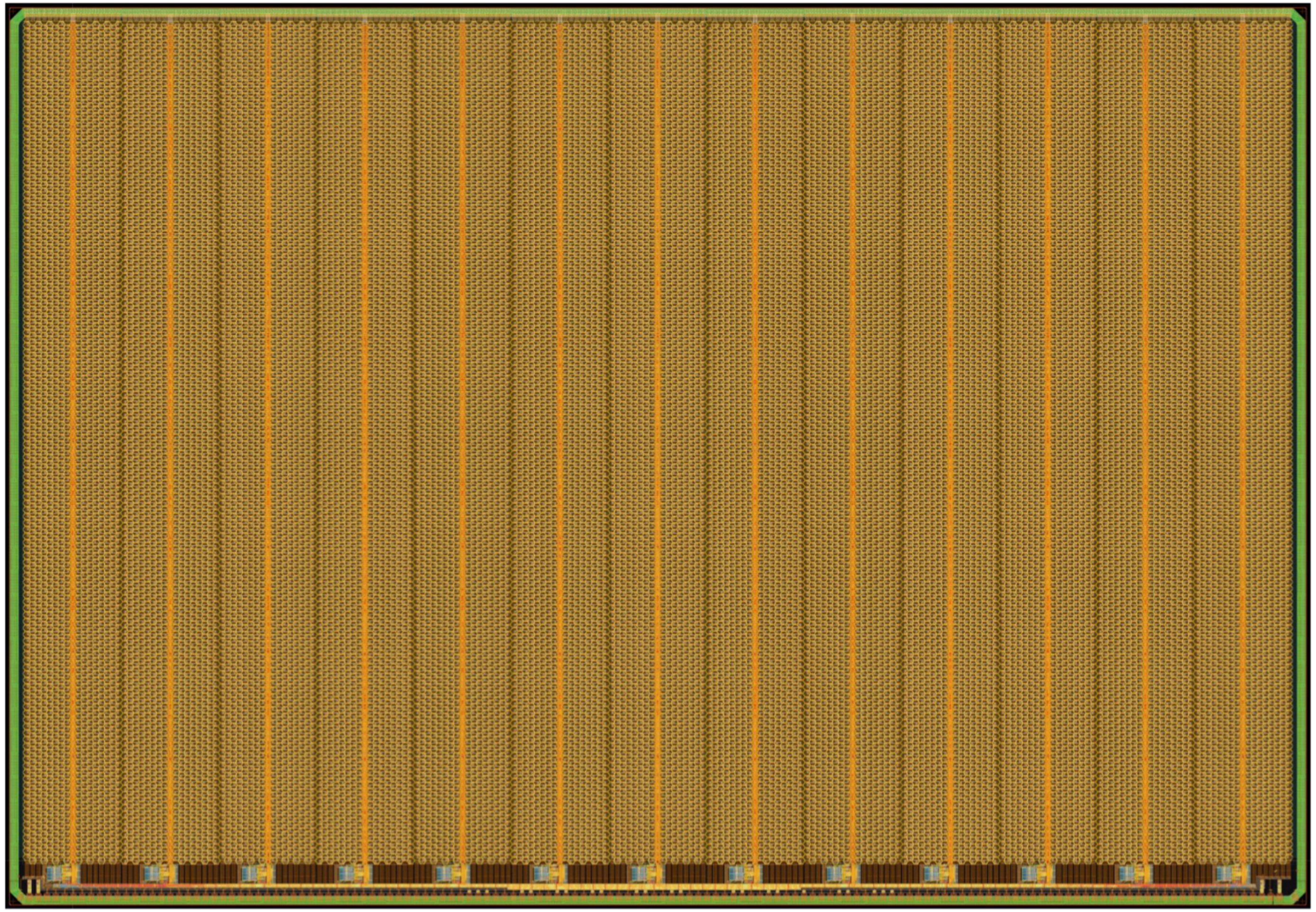
Main specifications	
Pixel Size	65 μm side (hexagonal)
Pixel dynamic range	0.5 ÷ 65 fC
Cluster size	O(1000) pixels
Readout time	< 200 μs
Power consuption	< 150 mW/cm^2
Time resolution	< 300 ps



In between an imaging chip and a HEP detector
Final Production Chip submitted in May 2023

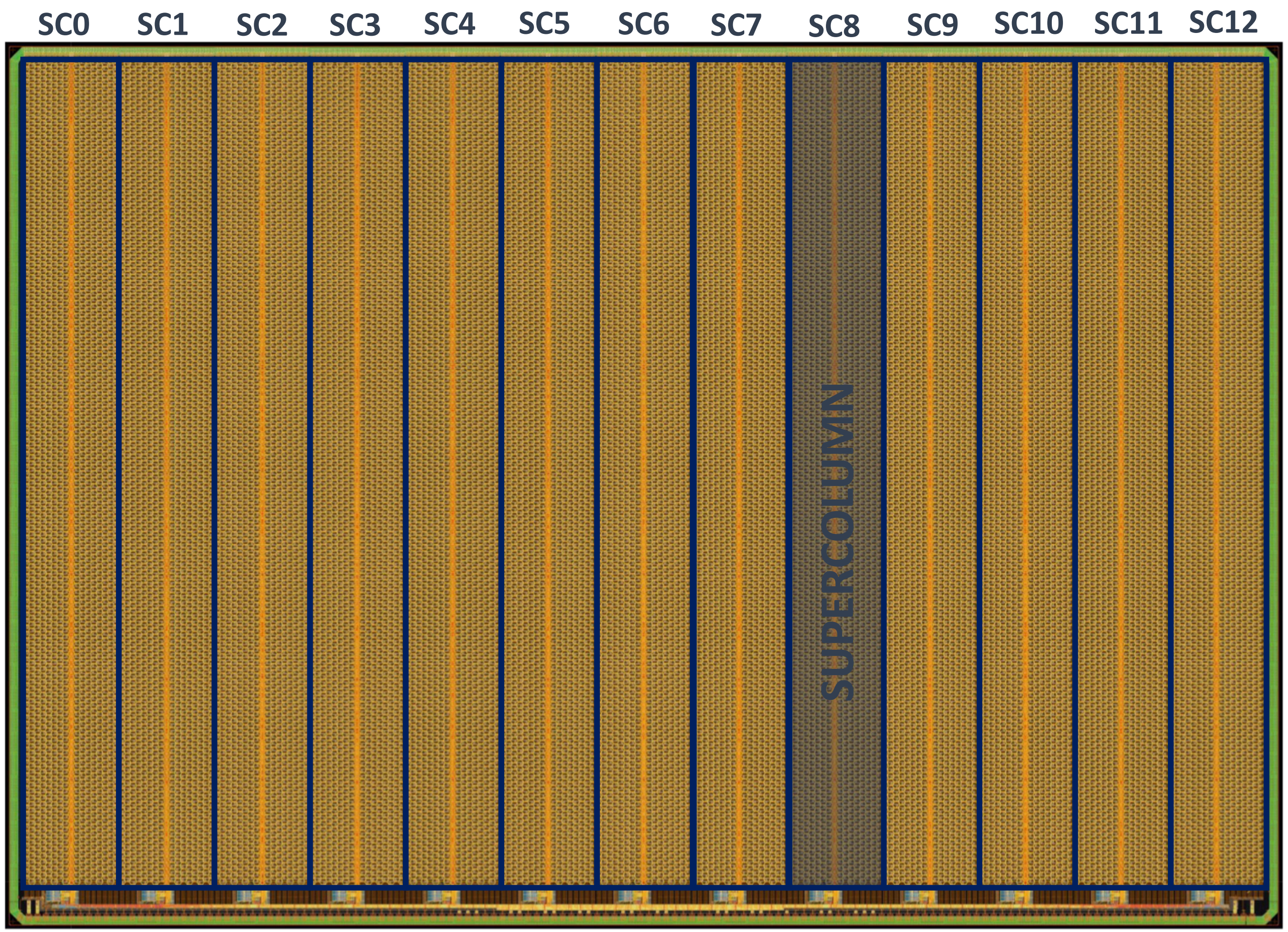
Modular Architecture

- Chip size: 2.2 x 1.5 cm^2 with matrix of 208x128 pixels (**26’624 pixels in total**)



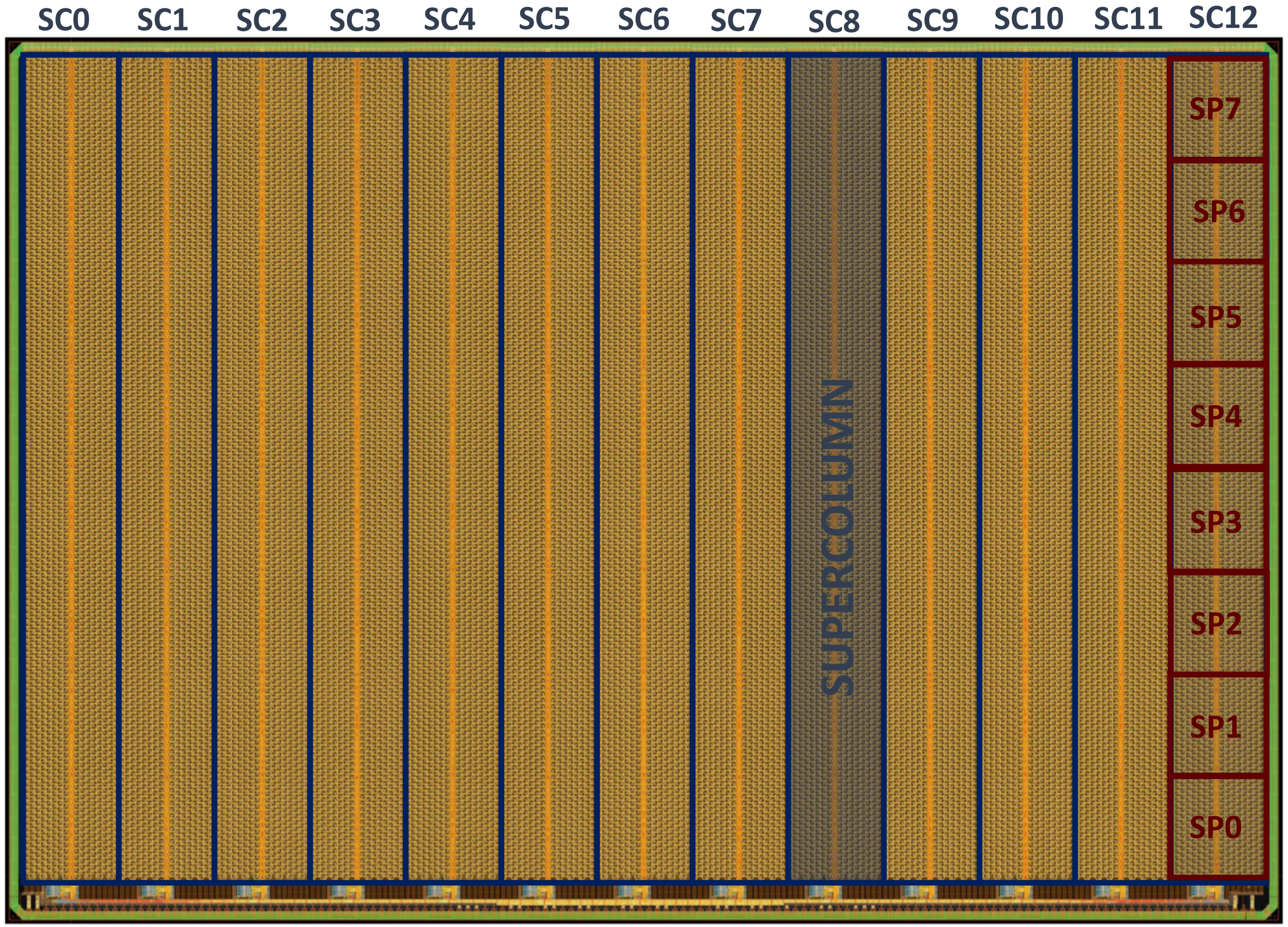
Modular Architecture

- Chip size: 2.2 x 1.5 cm^2 with matrix of 208x128 pixels (**26’624 pixels in total**)
- 13 **Supercolumns** (SC)



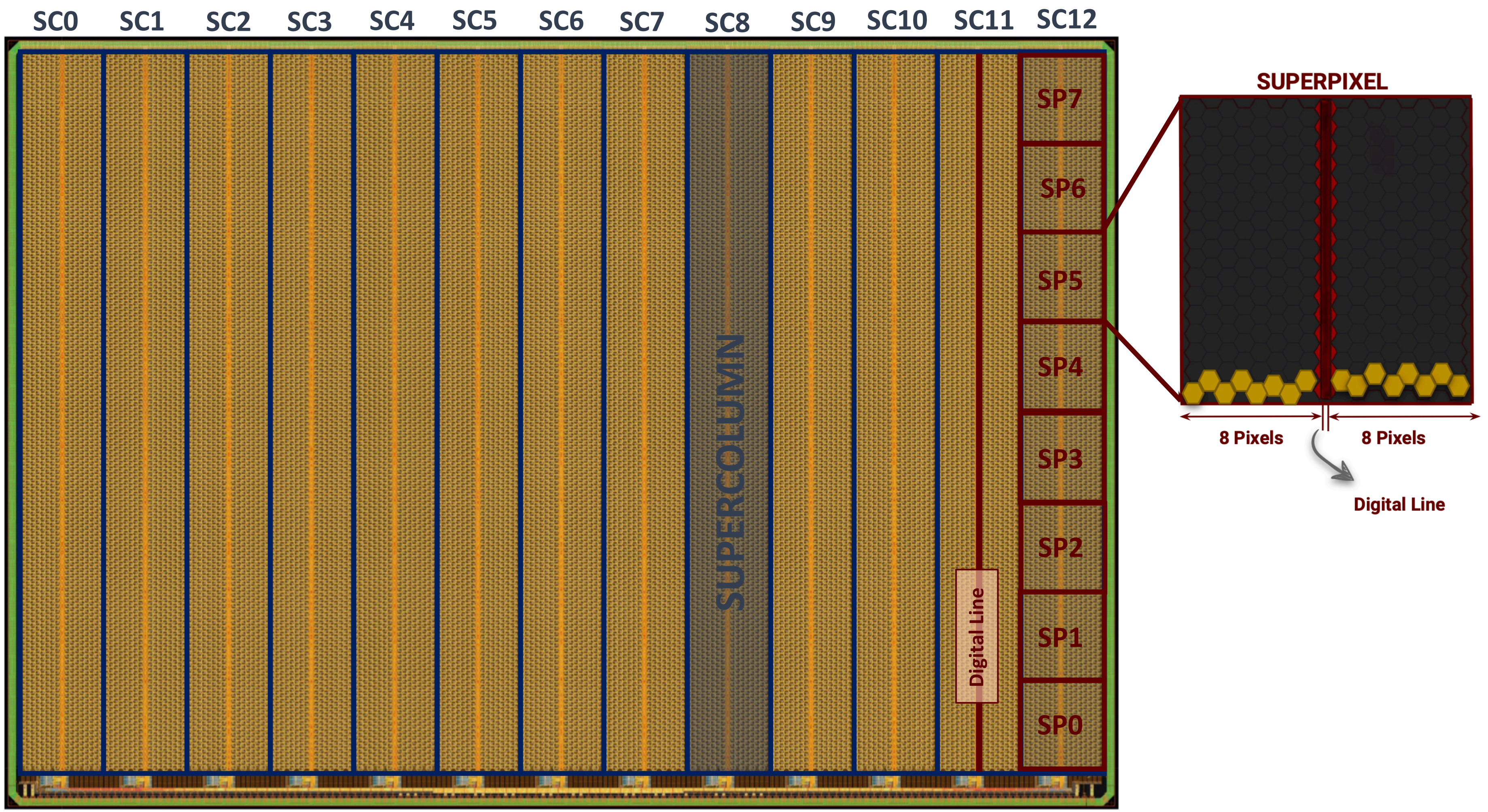
Modular Architecture

- Chip size: 2.2 x 1.5 cm^2 with matrix of 208x128 pixels (**26’624 pixels in total**)
- 13 **Supercolumns** (SC)
- Each Supercolumn has 8 **Superpixels** (SP) (16x16 pixels)



Modular Architecture

- Chip size: 2.2 x 1.5 cm^2 with matrix of 208x128 pixels (**26’624 pixels in total**)
- 13 **Supercolumns** (SC)
- Each Supercolumn has 8 **Superpixels** (SP) (16x16 pixels)
  - **Analog multiplexer**
  - **4-bit flash ADC**
  - **3 fast-OR lines**
  - **Local bias circuit**
  - **Programming logic to mask pixels**



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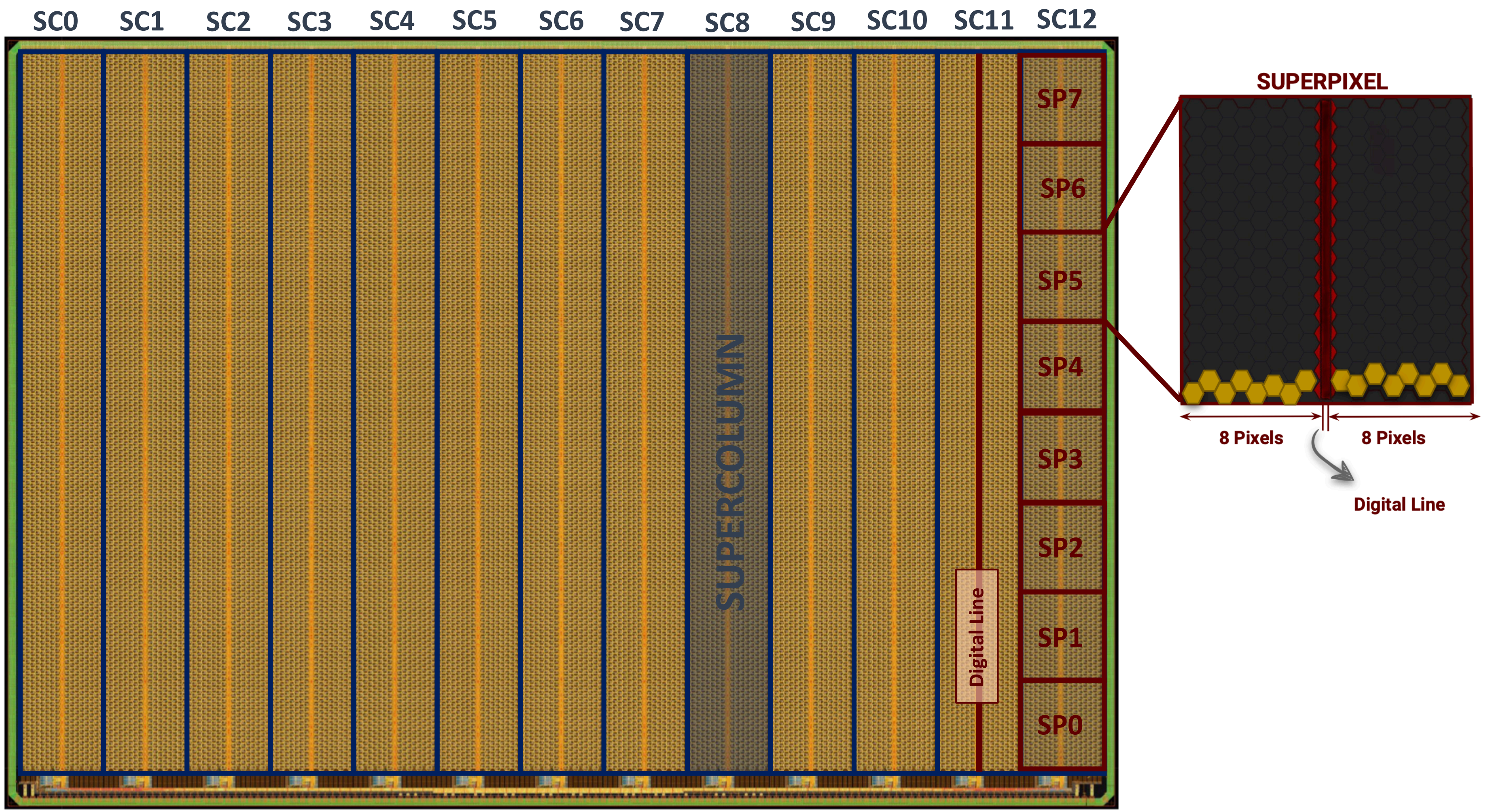
- Chip size: 2.2 x 1.5 cm^2 with matrix of 208x128 pixels (**26'624 pixels in total**)
- 13 **Supercolumns** (SC)
- Each Supercolumn has 8 **Superpixels** (SP) (16x16 pixels)
- and 1 **Digital Line** (40 µm)



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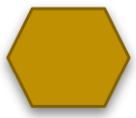

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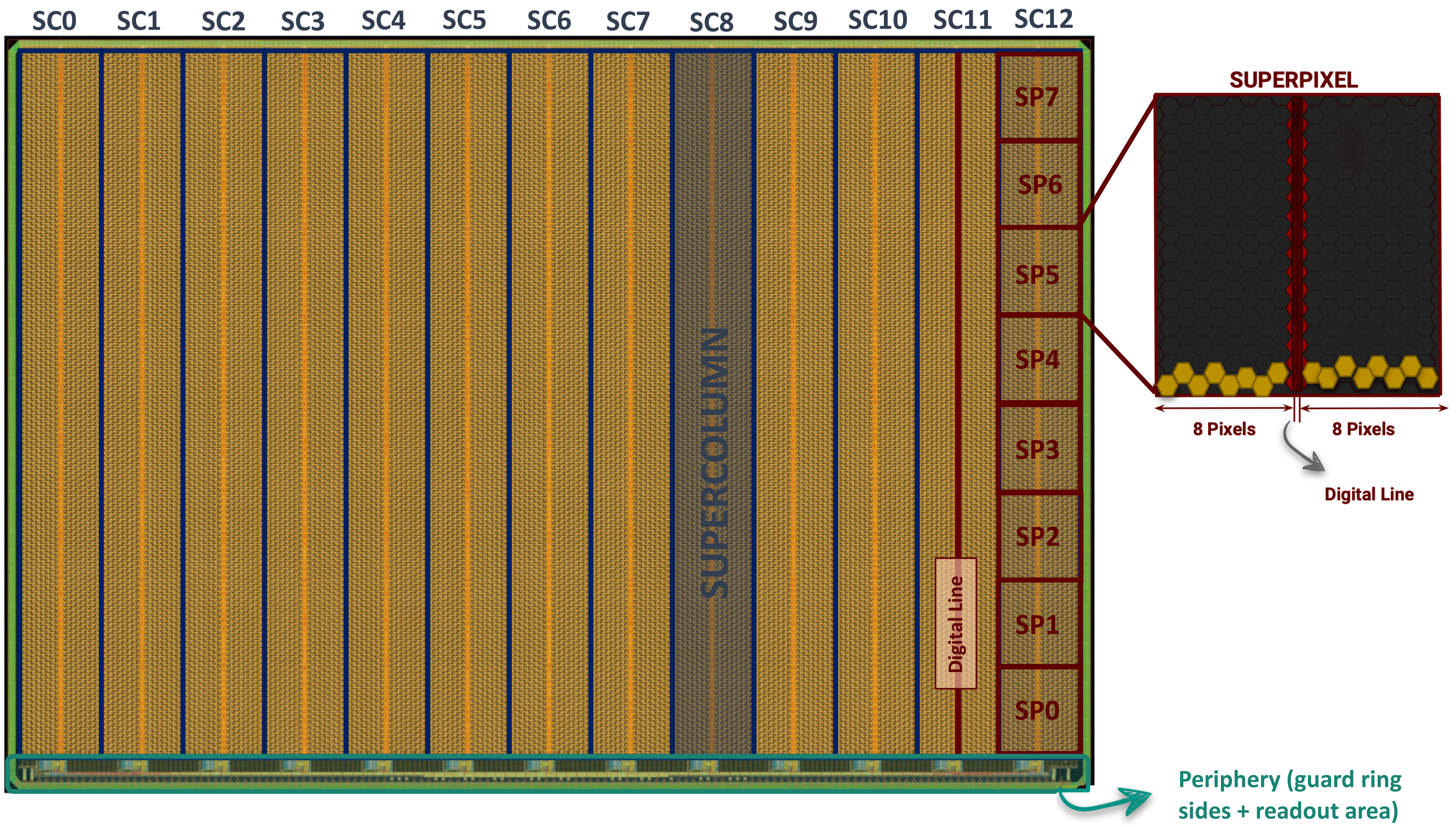
- 13 **Supercolumns** (SC)
- Each Supercolumn has 8 **Superpixels** (SP) (16x16 pixels)
- and 1 **Digital Line** (40 µm)
- **Periphery** (I/O and arbitrary logic) with dead area
  - 720 µm on the readout side
  - 270 µm for the guard ring



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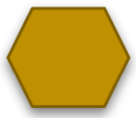

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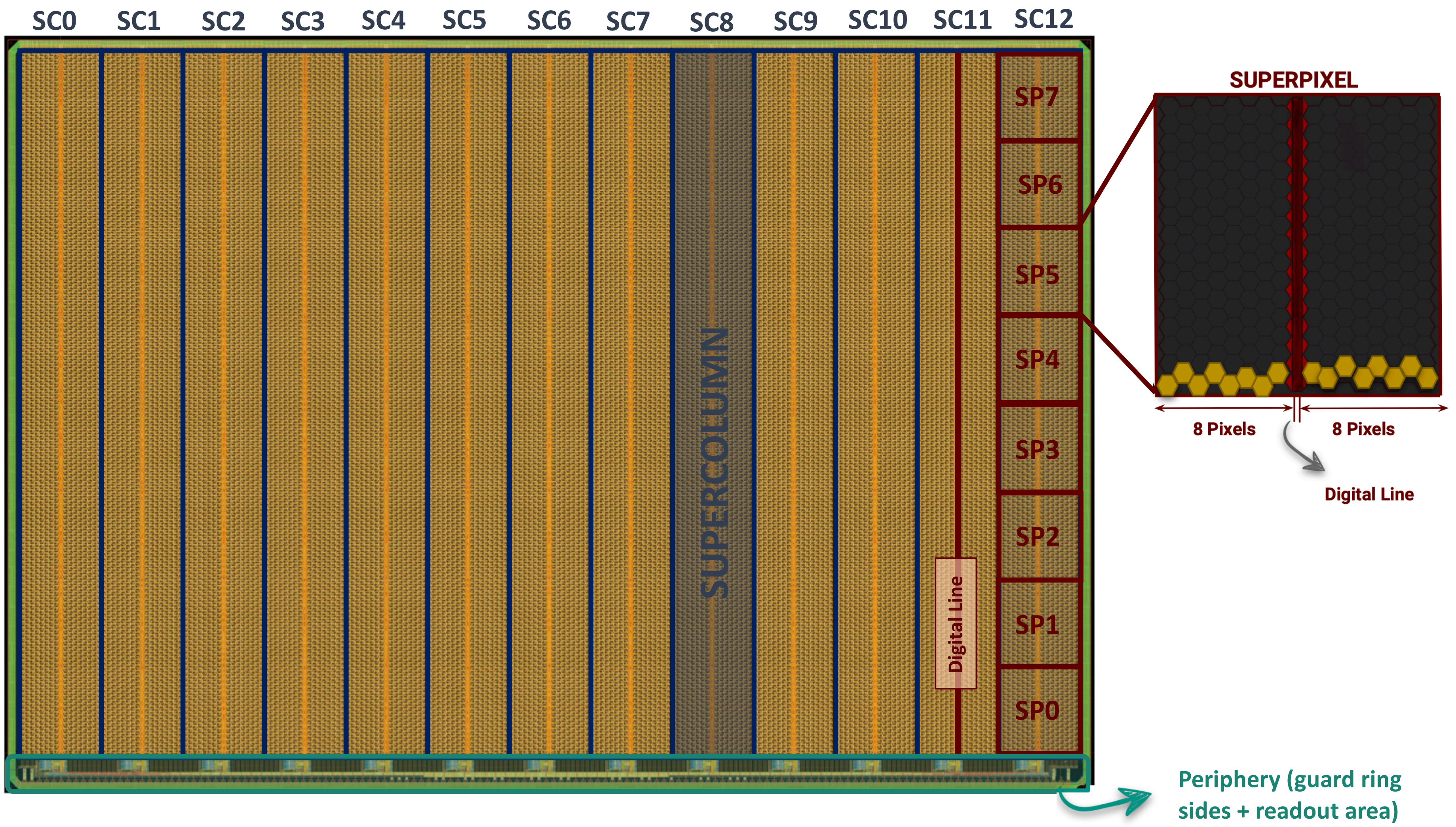
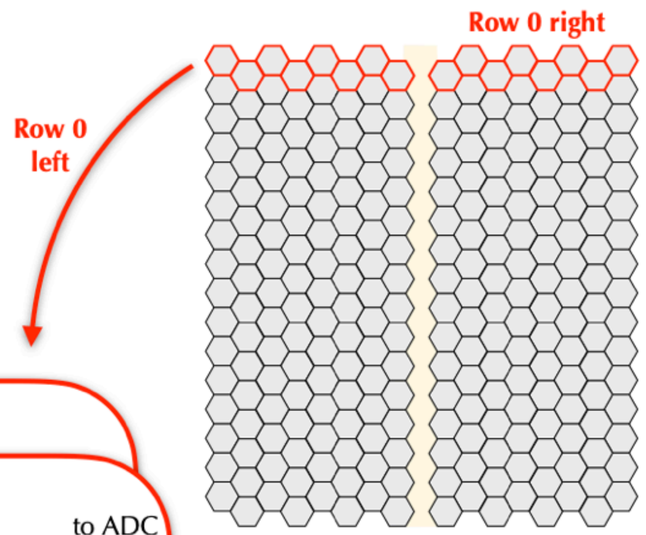
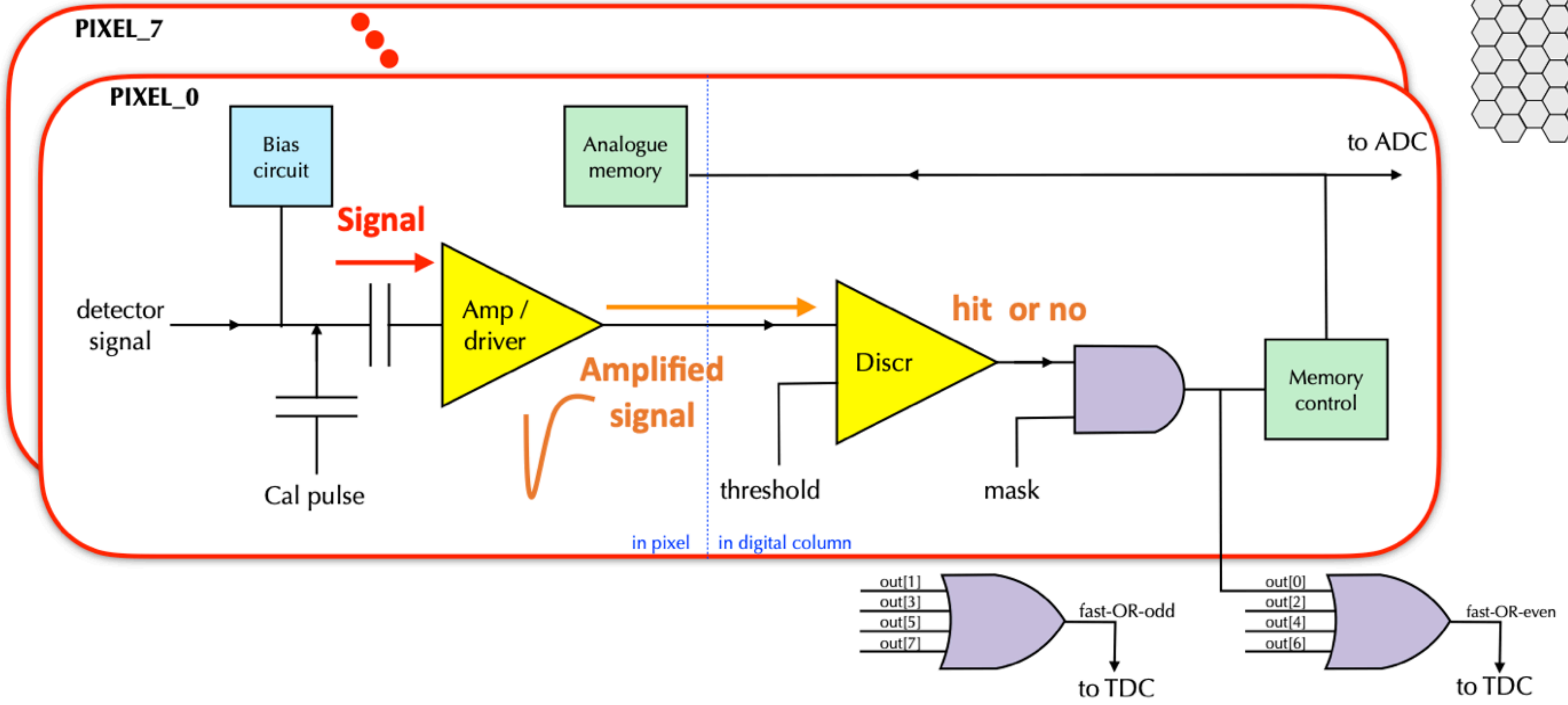
- Each Supercolumn has 8 **Superpixels** (SP) (16x16 pixels)
- and 1 **Digital Line** (40 µm)
- **Periphery** (I/O and arbitrary logic) with dead area
  - 720 µm on the readout side
  - 270 µm for the guard ring
- **Dead area** < 5%



Pixel Circuitry

Charge measured per-pixel, simultaneously for different superpixels

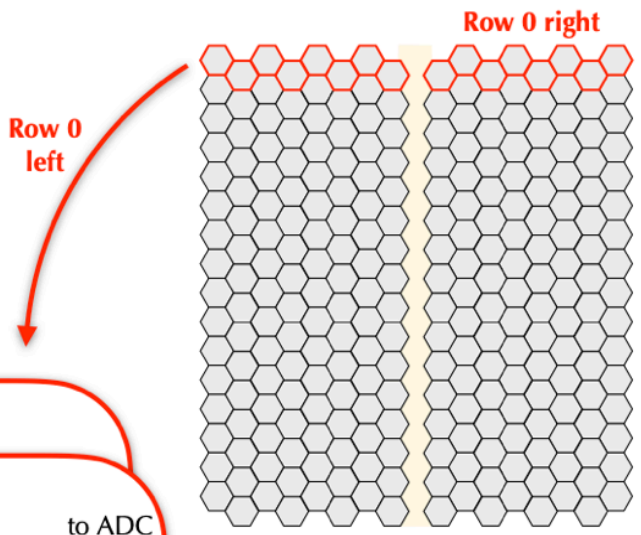


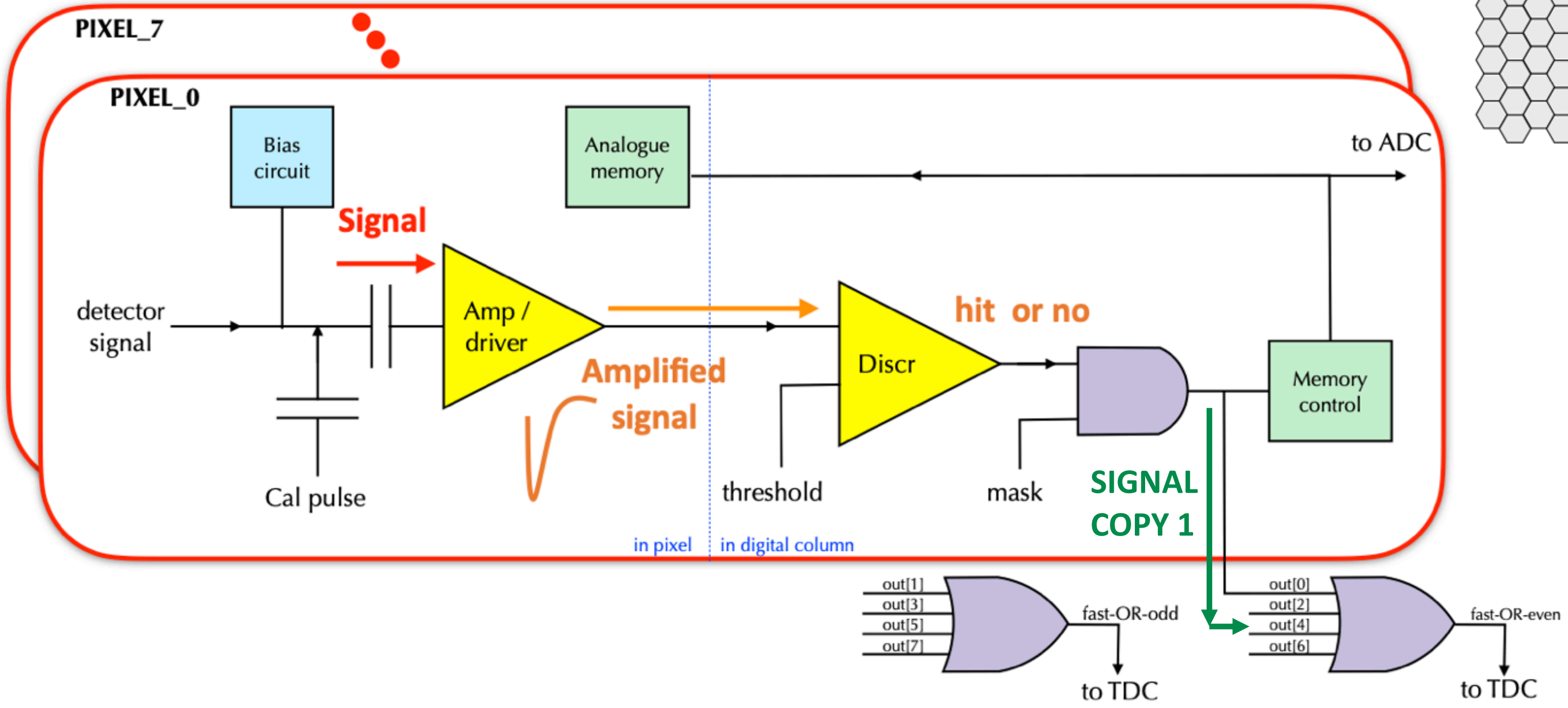


Pixel Circuitry

Charge measured per-pixel, simultaneously for different superpixels

➡ Hit above threshold generates a signal that is sent to the periphery via fast-OR





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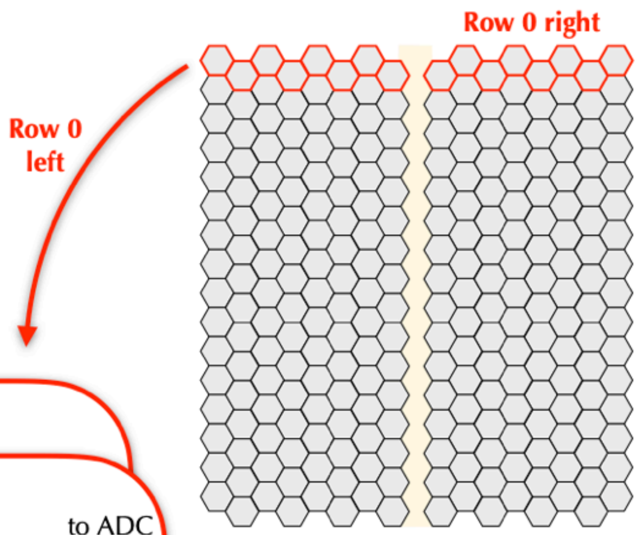
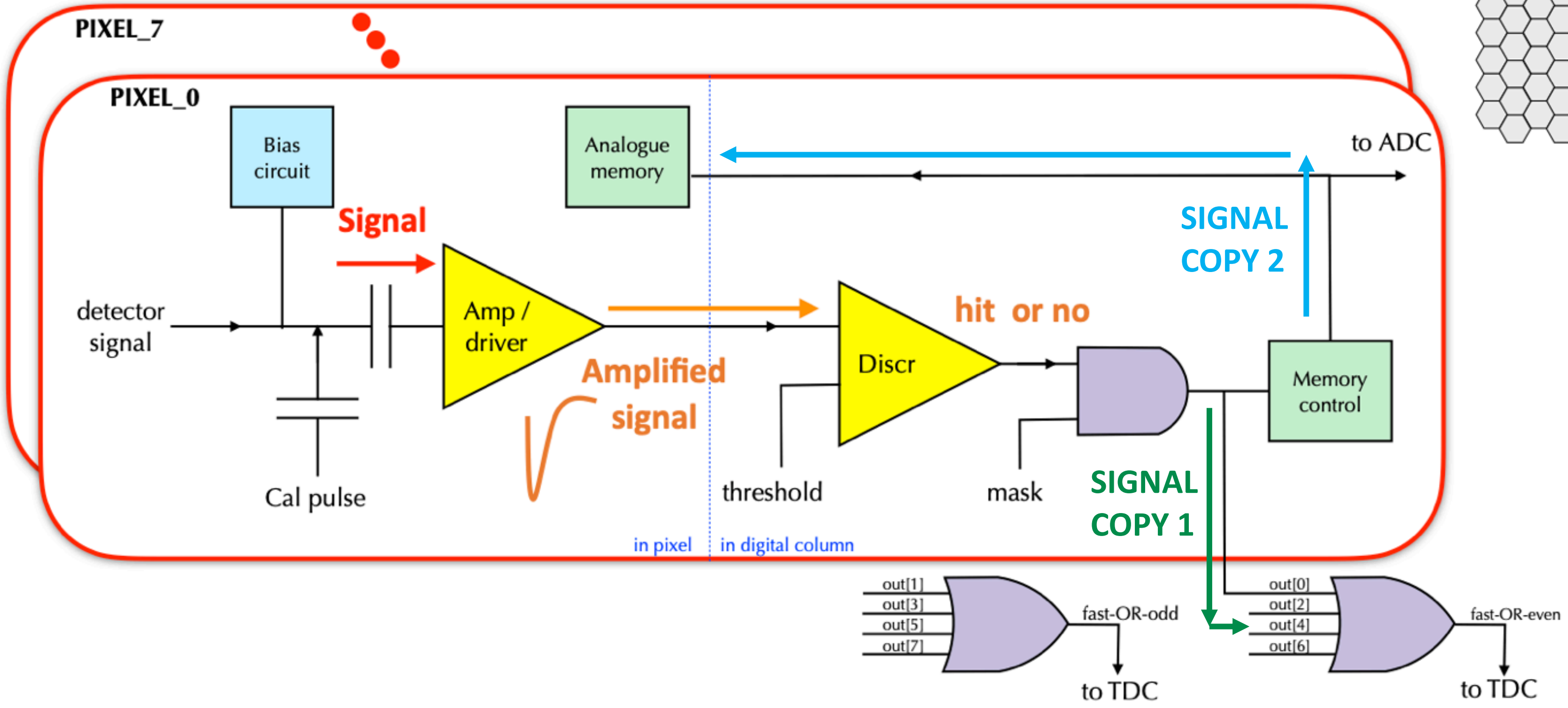
Pixel Circuitry

Charge measured per-pixel, simultaneously for different superpixels

- Hit above threshold generates a signal that is sent to the periphery via fast-OR
- A charge proportional to the TOT is stored into the pixel's analog memory

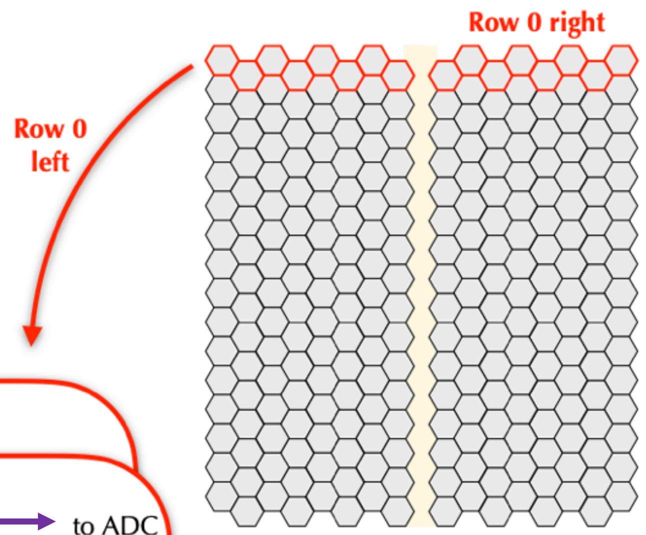


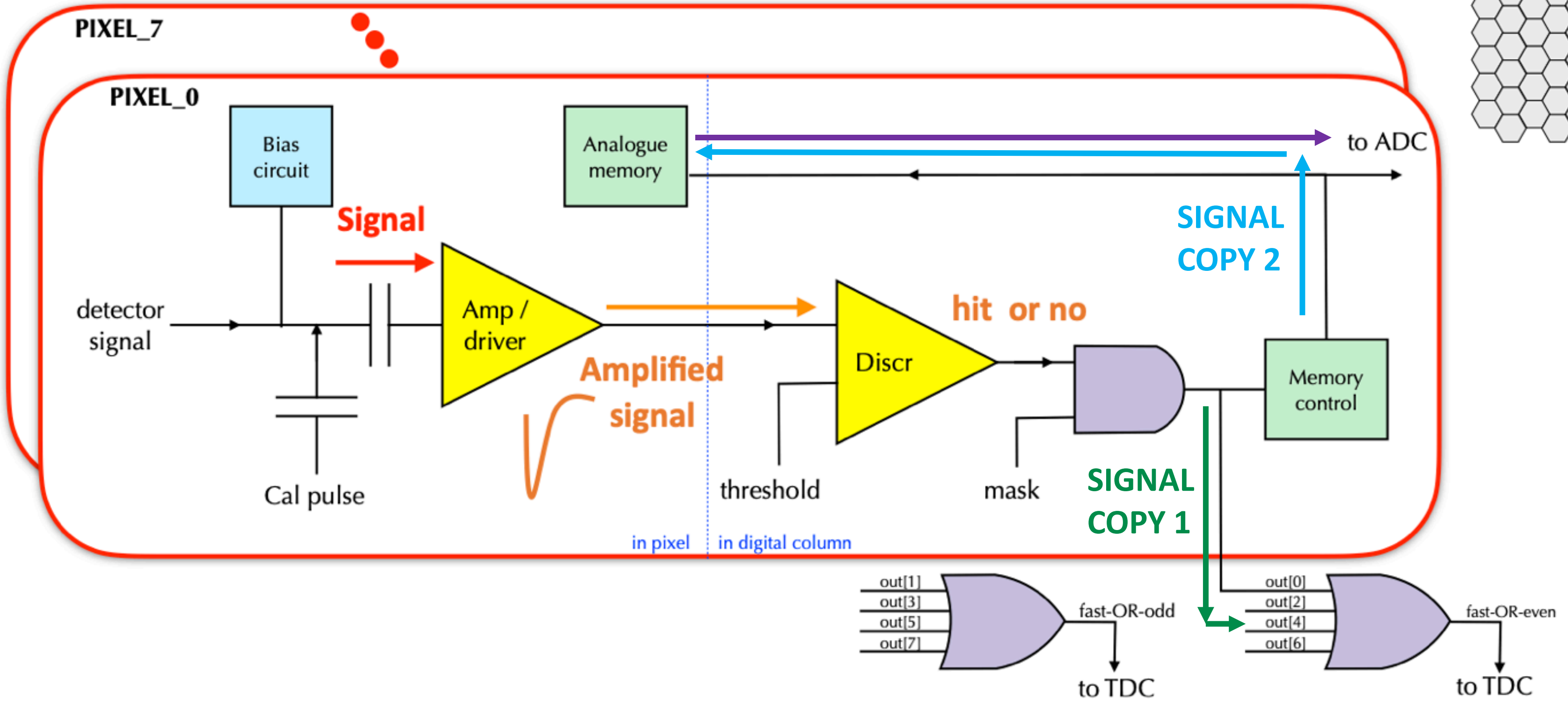


Pixel Circuitry

Charge measured per-pixel, simultaneously for different superpixels

- Hit above threshold generates a signal that is sent to the periphery via fast-OR
- A charge proportional to the TOT is stored into the pixel's analog memory
- After a configurable delay, the readout starts supercolumn after supercolumn



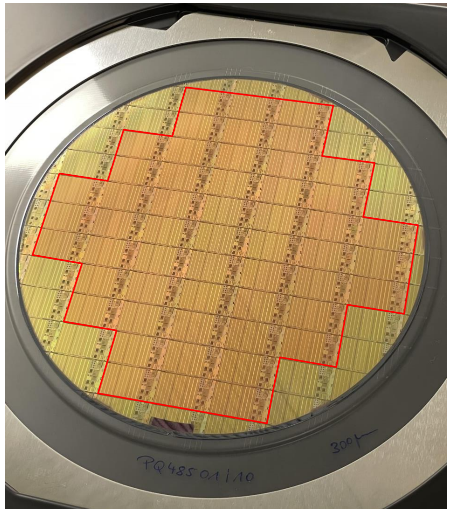


TESTS ON THE PRE-PRODUCTION CHIP

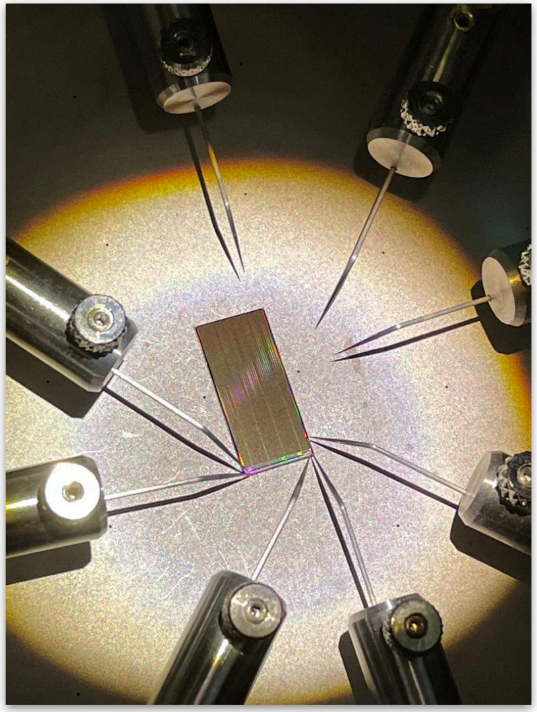
The Pre-production ASIC

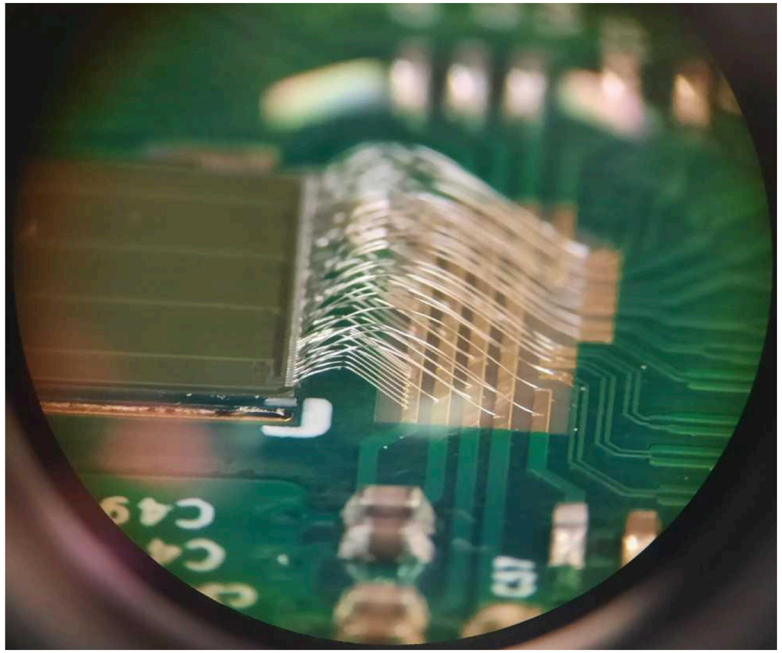
Wafers received in June 2022, tested in the laboratory
- I-V characteristics measured at probe station
- Charge response scrutinised with ^{109}Cd and IR laser
- Stress-tests for digital electronics and readout

Reticle: 2.4 x 1.5 cm^2
53 reticles per wafer
Thickness 300 µm

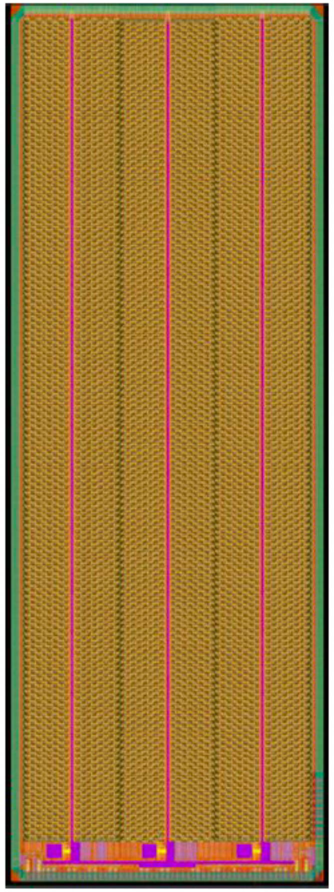


CHIP @ probe station





Pre-production ASIC



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Tests with ^{109}Cd source: gain and ENC

Aim of the measurements:

- Test **sensitivity to small charges**
- Identify **the best** Front-End **working point**
- Study the **gain** and **ENC** mismatch

^{109}Cd has three peaks of emission:

- **22.1 keV (around 1 fC)**
- **25 keV (around 1 fC)**
- **88 keV (around 4 fC)**

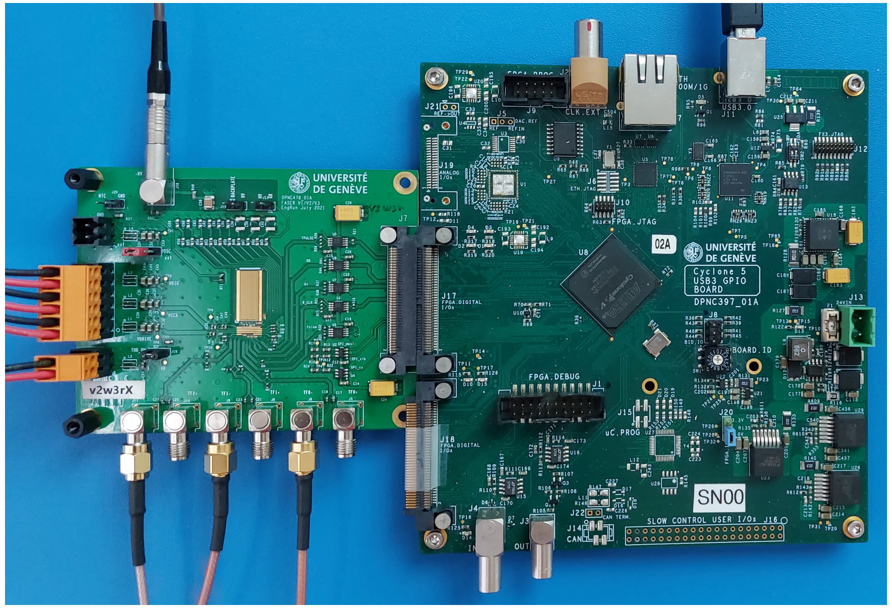
plus Auger electrons at low energy

Measurement principle:

- **Threshold scan** to measure the **hit rate** and build the S-curve
- Fit the S-curve to obtain the **gain** and **ENC**

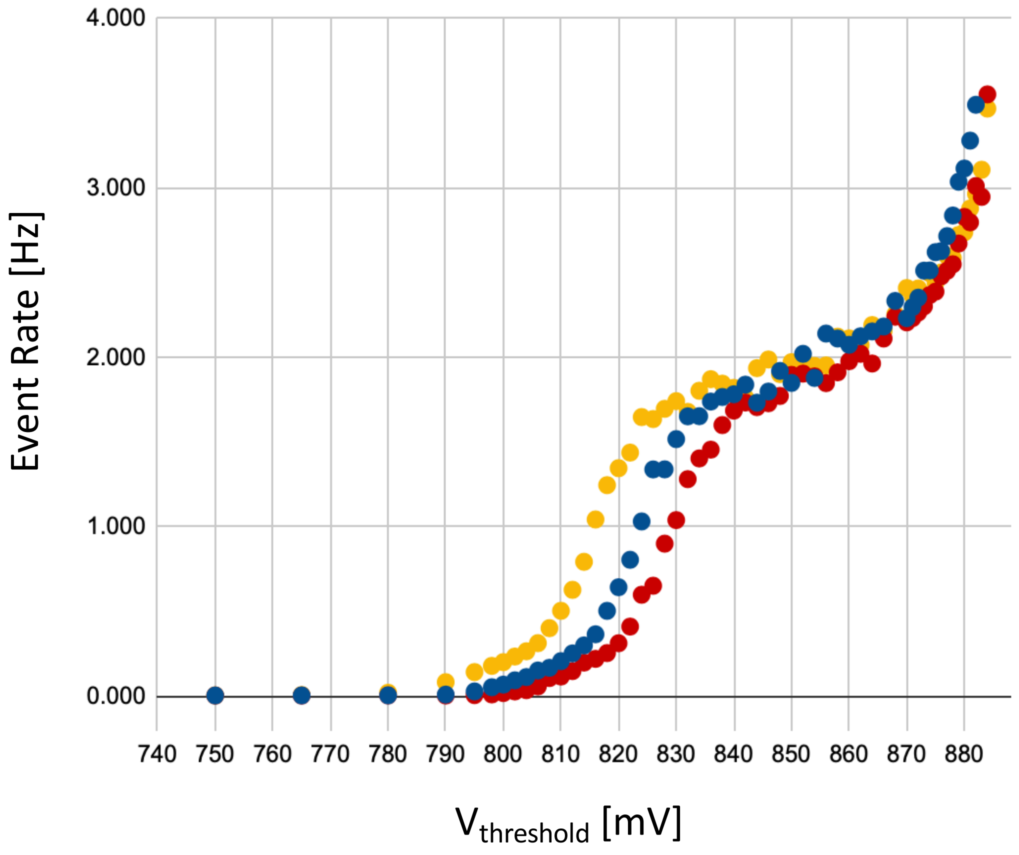
The idea is to identify **two different working points:**

- **First two planes** of the preshower where we aim to be **more sensitive to smaller charges**
- **Rest of the planes**, in which we have **more charge deposited per pixel:** be sensitive to smaller charges is not a priority

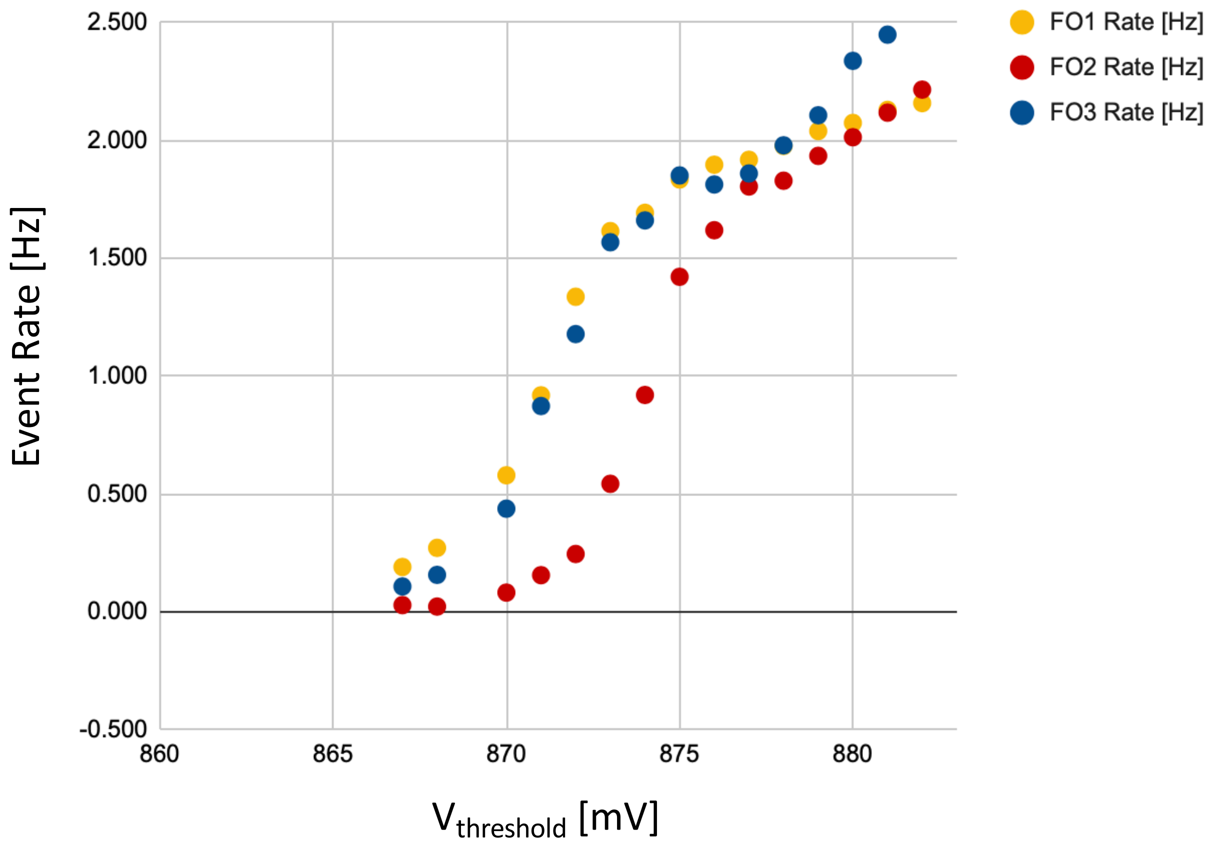


Tests with ^{109}Cd source: gain and ENC

WP: **Small charges sensitivity**
preamplifier current = 0.714 µA



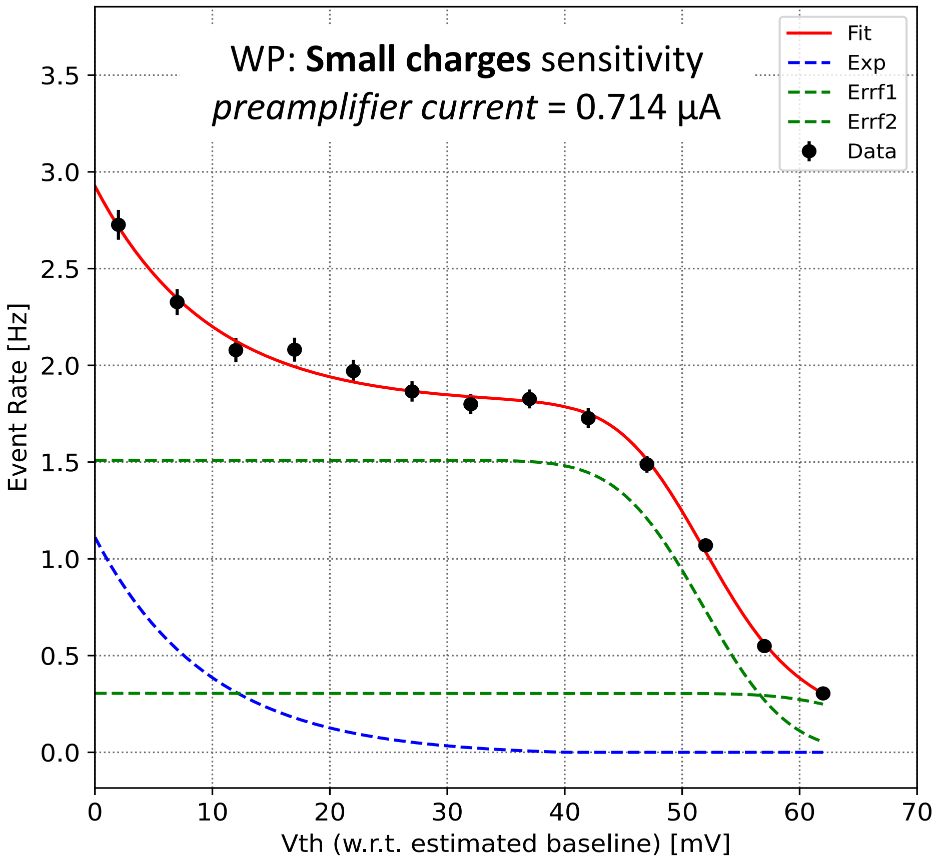
WP: **Large charges sensitivity**
preamplifier current = 1.268 µA

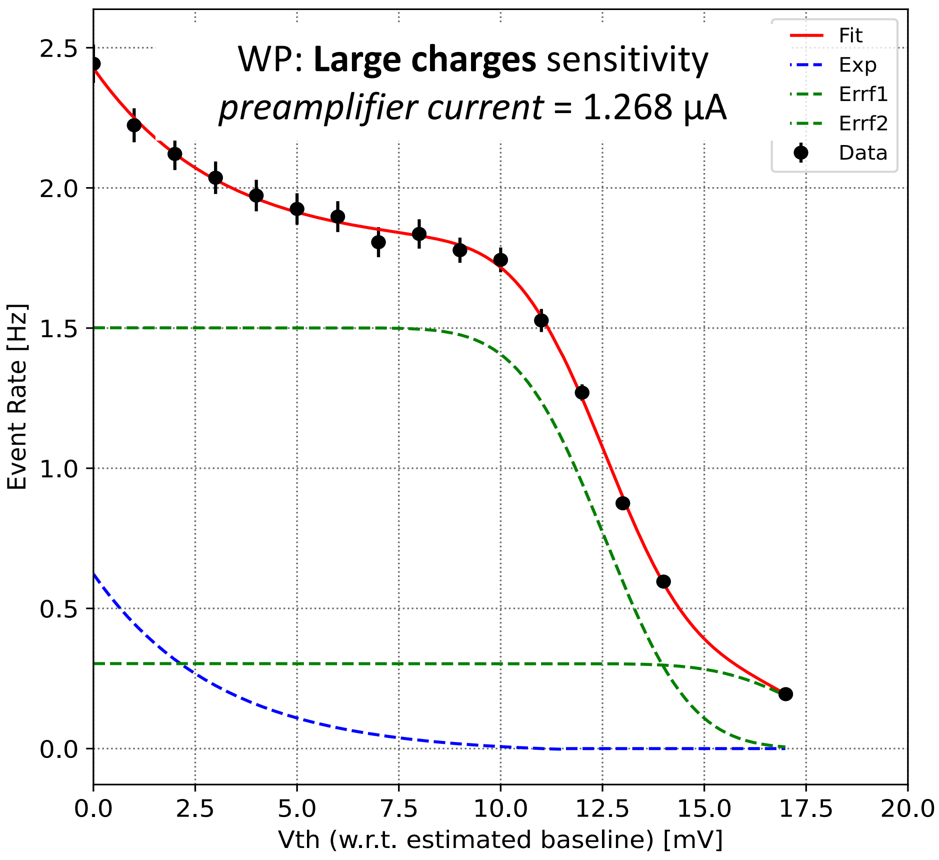


Tests with ^{109}Cd source: gain and ENC

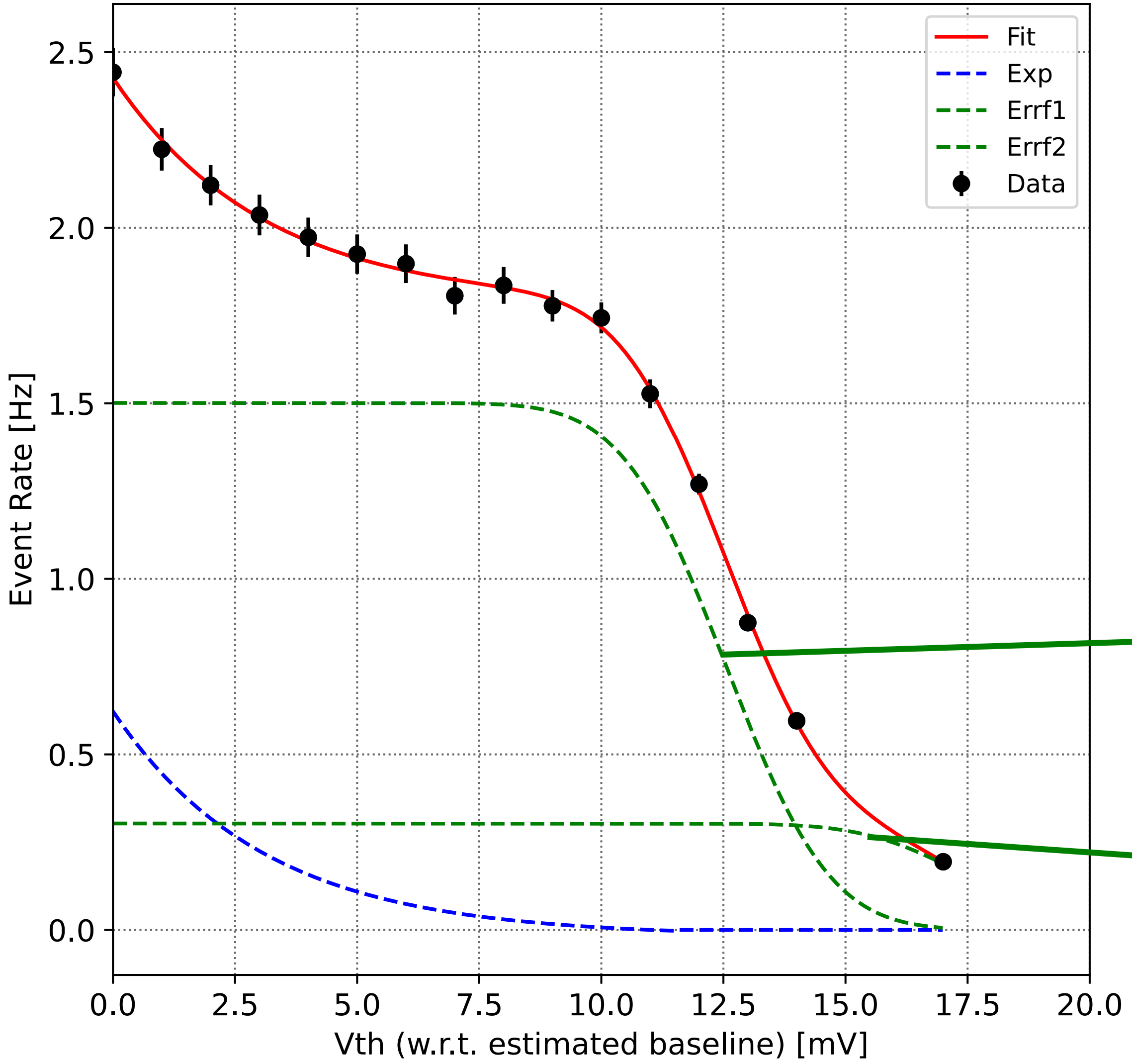
Fitting function:

- Exponential function modeling Auger electrons
- Two gaussian error functions describing emissions from the two close-by peaks of emission



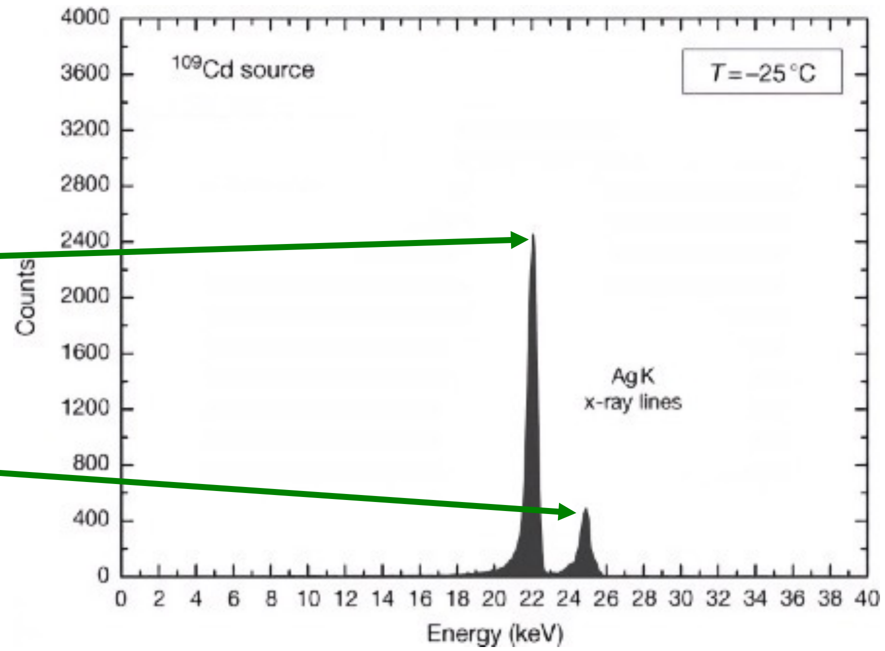


Tests with ^{109}Cd source: gain and ENC

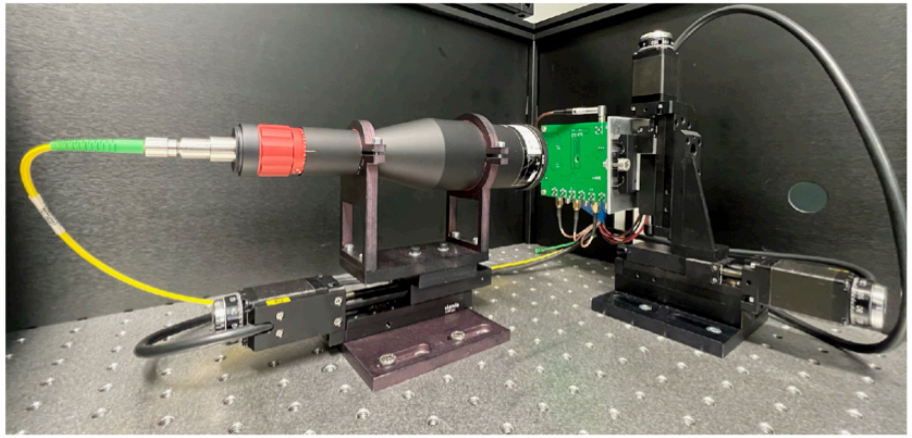


Extract the gain and ENC from the fit parameter for the 22.1 keV peak

Gain = 21.0 ± 0.5 mV/fC **ENC** = 502 ± 20 electrons



Tests with the 1060nm IR Laser: TOT Mismatch



Aim of the measurements:

- Test the **mismatch** in measured charge **pixel-to-pixel**
- The charge is **measured through TOT** of the induced signal, a **difference in gain** pixel-to-pixel can cause **mismatch**

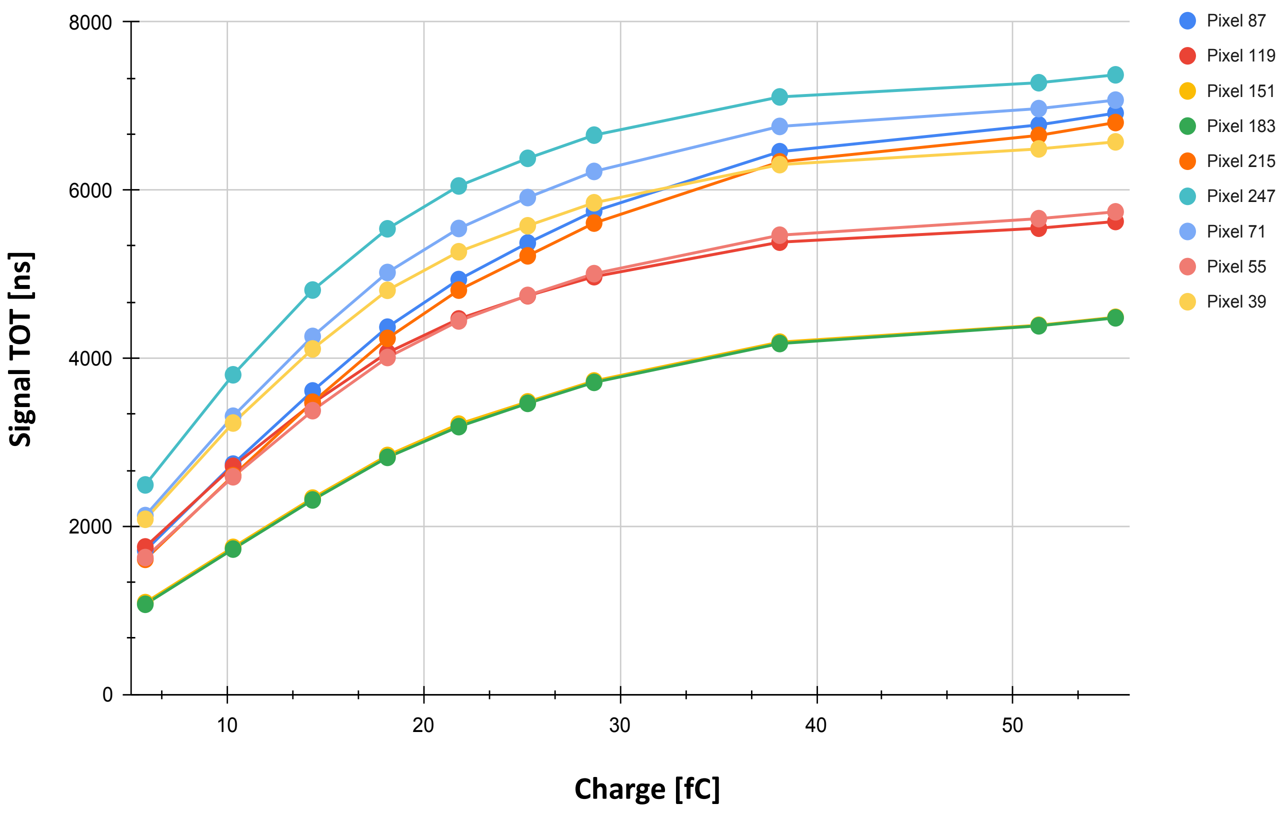
Measurement principle:

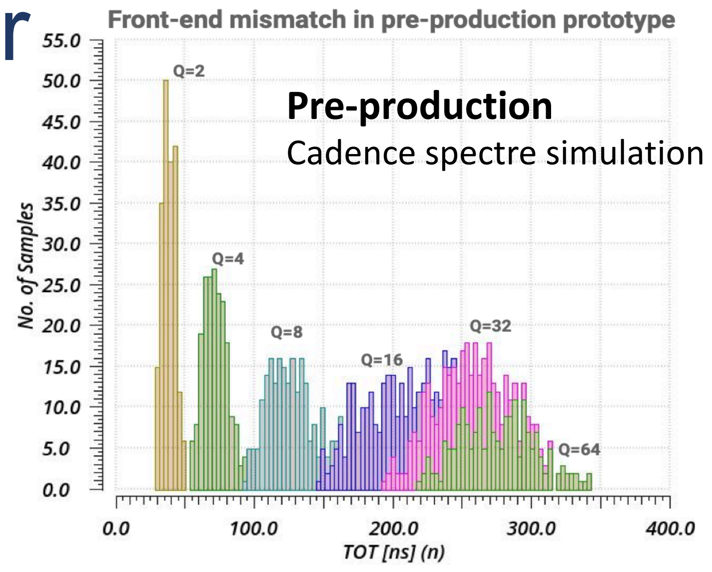
- Measuring TOT via fast-OR signal on the oscilloscope
- Varying per-pixel injected charge via laser attenuation

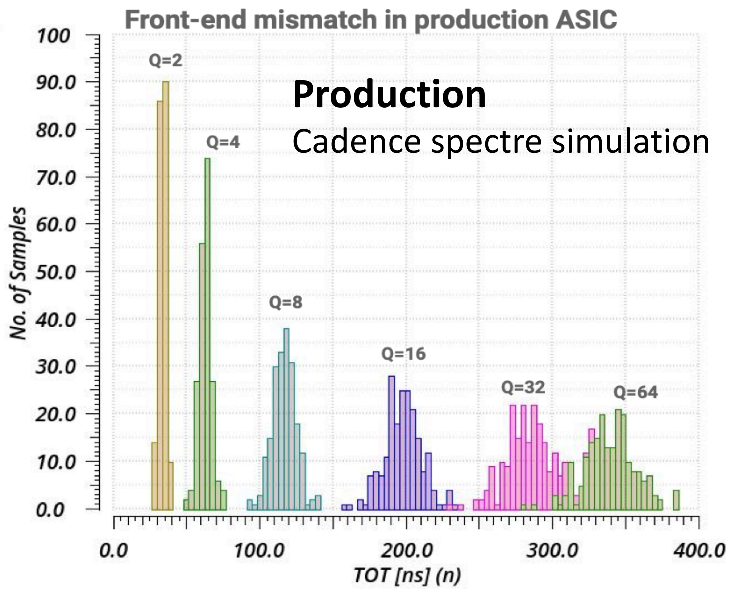
The injected charge as a function of the chosen laser intensity was calibrated using the internal ASIC testpulse

Measurement of the TOT as a function of the injected charge for same pixels probed with the 109Cd source

Tests with the 1060nm IR Laser

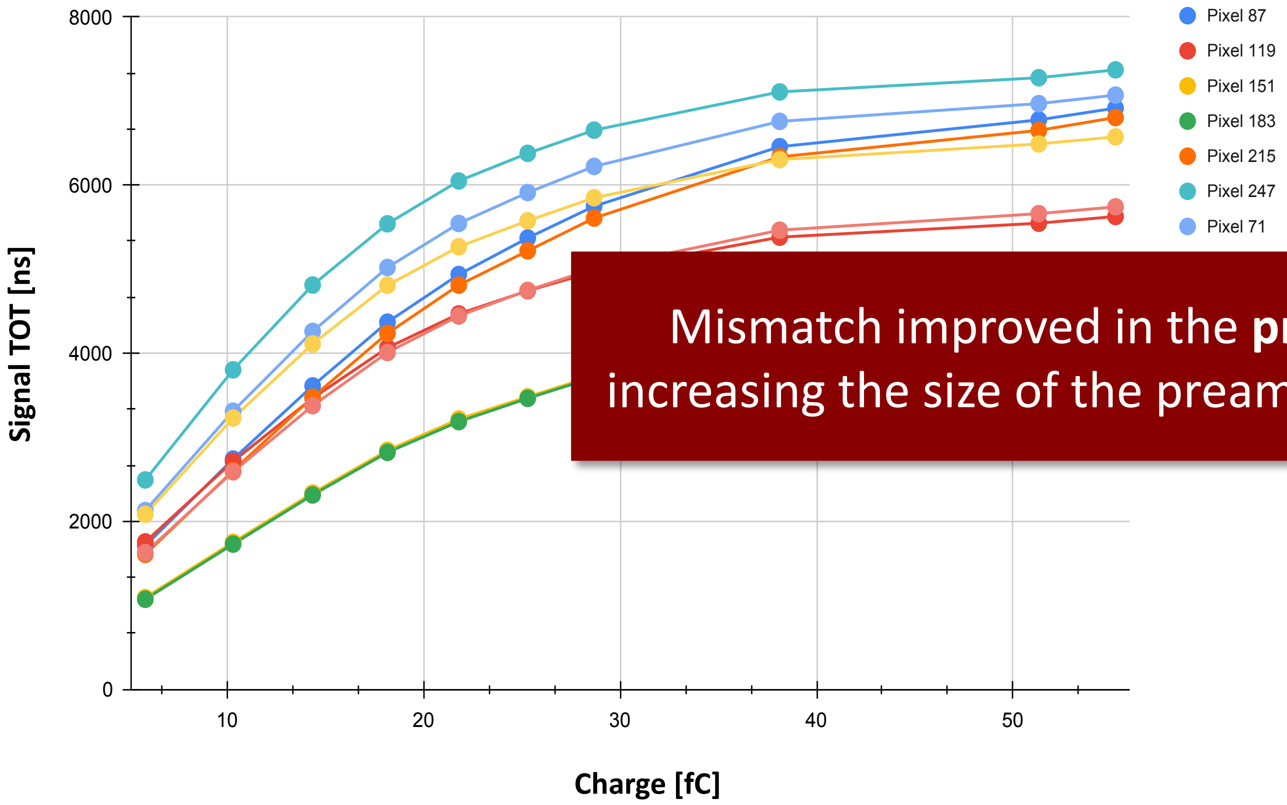


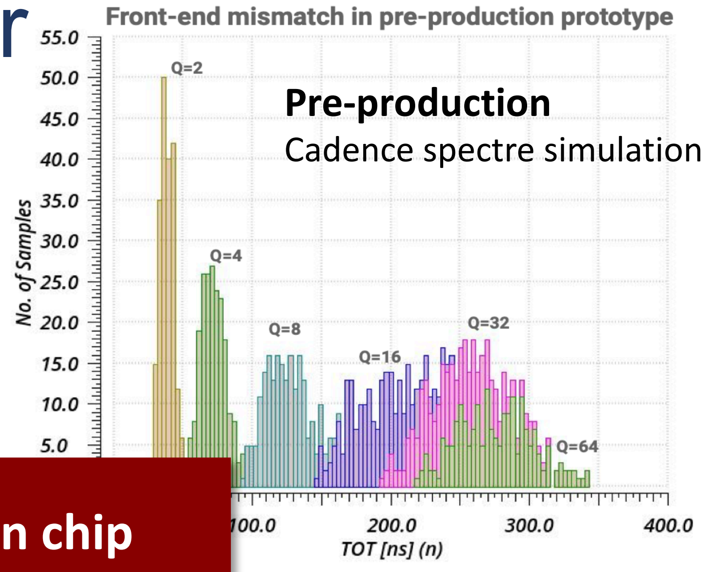




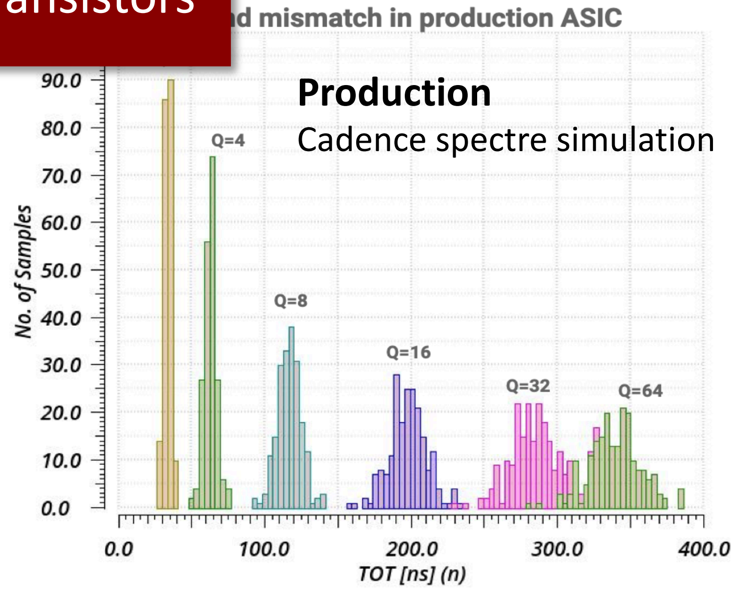
Large mismatch on the pre-production chip from amplifier response

Tests with the 1060nm IR Laser





Mismatch improved in the production chip increasing the size of the preamplifier transistors



Large mismatch on the pre-production chip from amplifier response

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Tests on the ADC Response

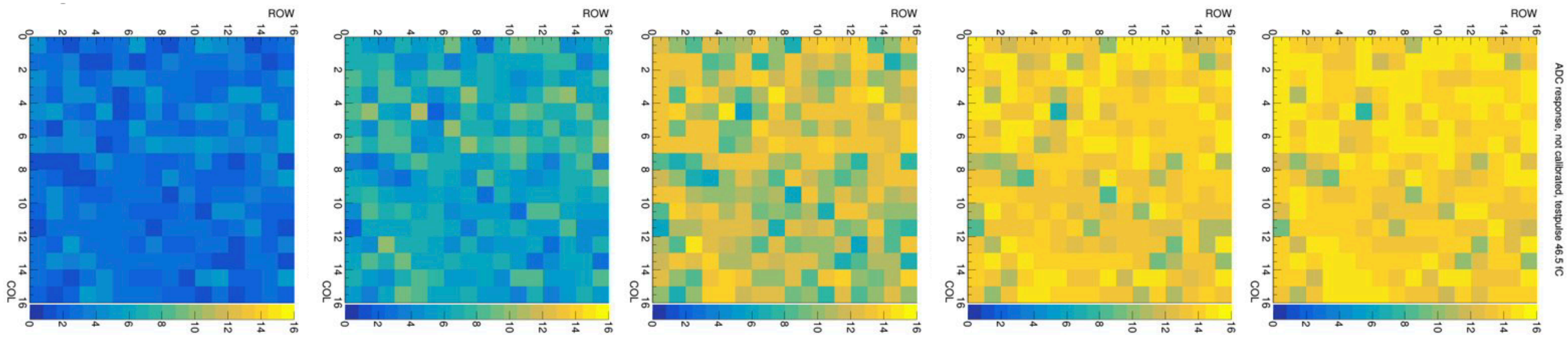
Aim of the measurements:

- Characterize **the mismatch of the full electronic chain**, mostly analog **MUX and ADC**

Measurement principle:

- Study of the chip response for different value of injected charge

One SP

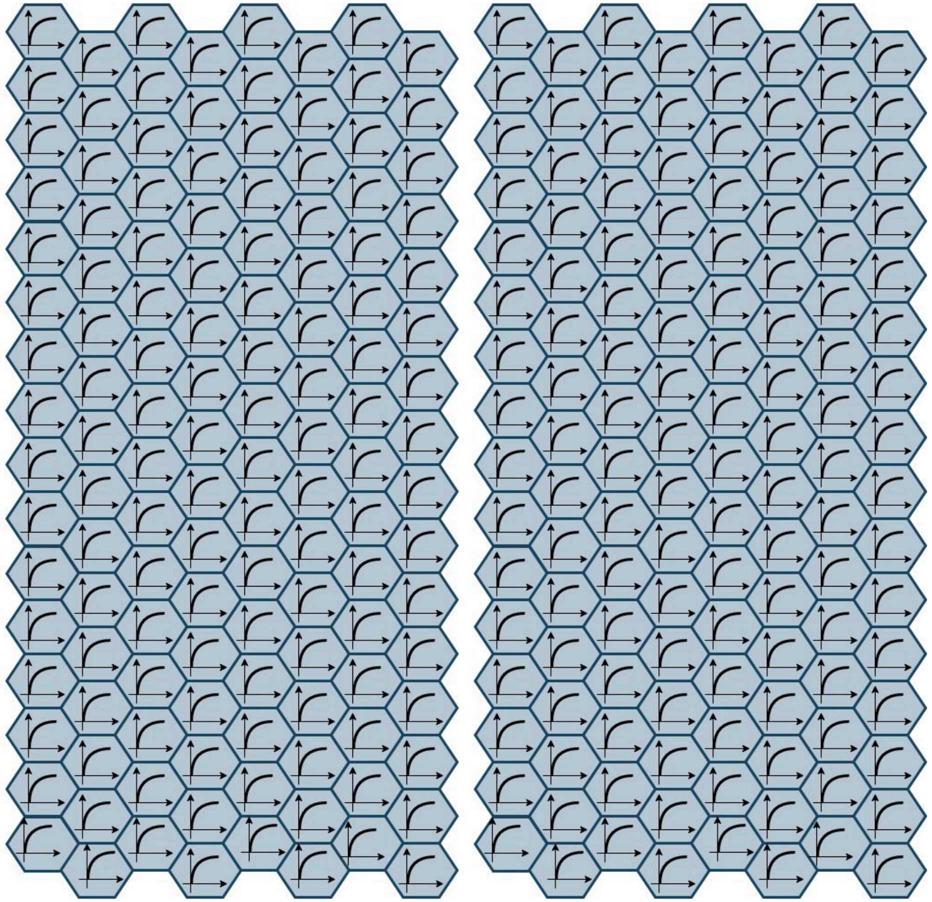


Increasing injected charge via testpulse

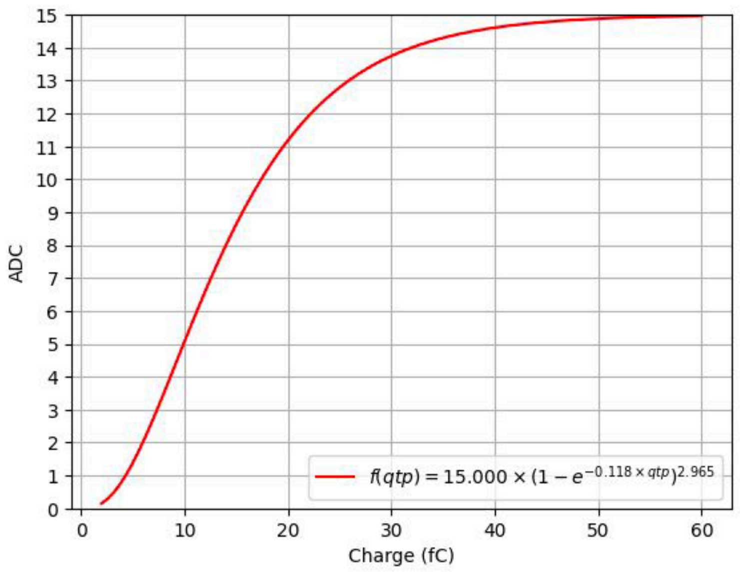
Mismatch can be compensated with an offline calibration procedure

Charge Calibration Procedure

- **Goal of the charge calibration**: from the digitized data information, reconstruct the charge the particle deposited in each pixel



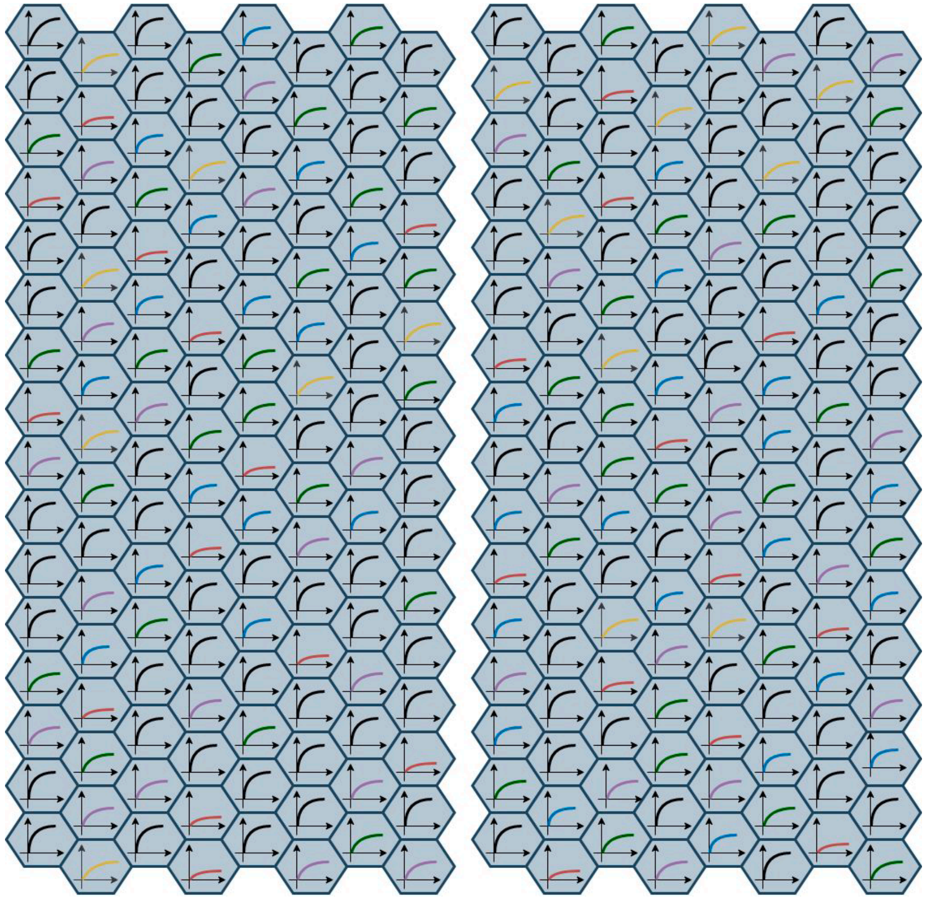
Our logarithmic response

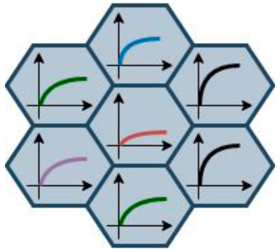


Ideal case in which all pixels have the same response and same saturation point

Charge Calibration Procedure

- **Goal of the charge calibration**: from the digitized data information, reconstruct the charge the particle deposited in each pixel,





- Mismatch in TOT response of the amplifier
- Mismatch on voltage saturation value in analog memory
- Mismatch on threshold voltages of the flash ADC

Each pixel has its own calibration curve, describing its ADC response

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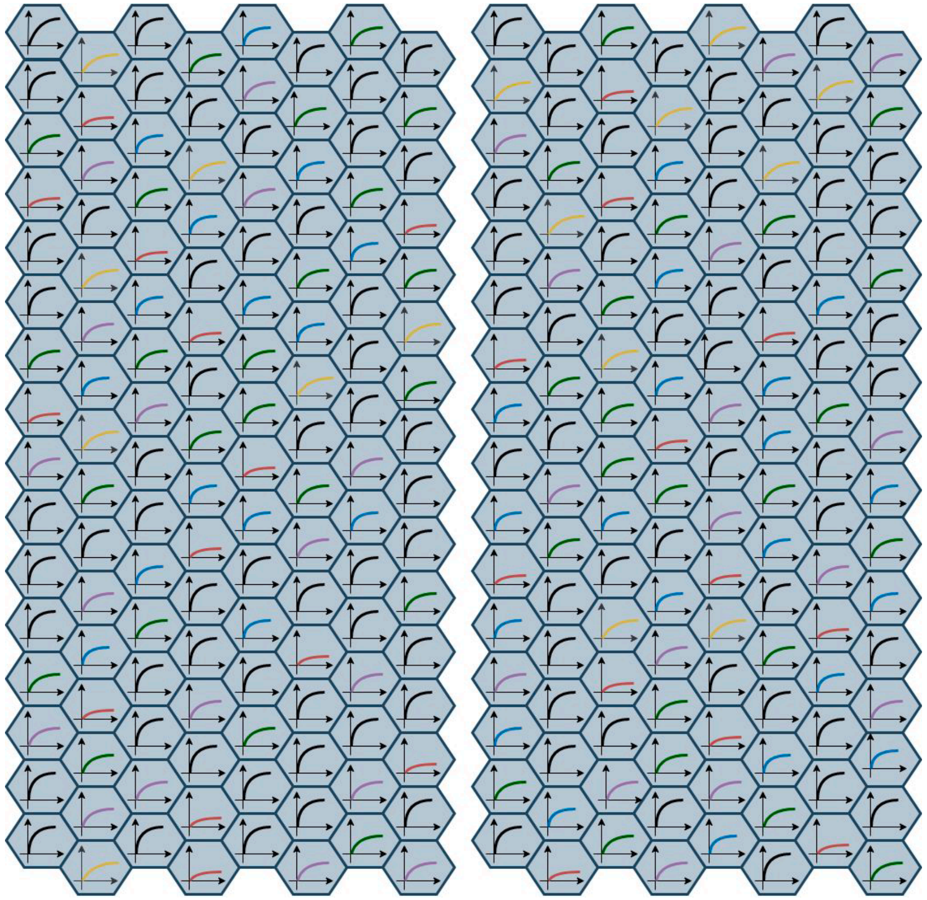
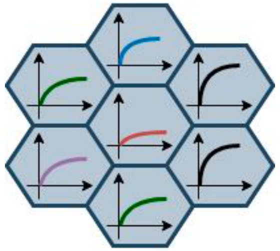
Charge Calibration Procedure

- **Goal of the charge calibration**: from the digitized data information, reconstruct the charge the particle deposited in each pixel, considering the response of each pixel





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Each pixel has its own calibration curve, describing its ADC response

Charge Calibration Procedure

- **Goal of the charge calibration**: from the digitized data information, reconstruct the charge the particle deposited in each pixel, **considering the response of each pixel**

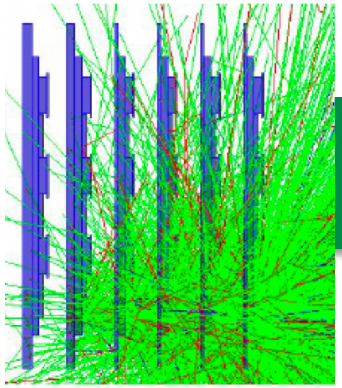
Pre-processing

1 — ADC vs injected charge
Get the values of ADC bin per pixel for different values of injected charge using the testpulse

2 — Fit
Fit the ADC vs injected charge curve for each pixel to retrieve the calibration curve

3 — Invert f
Invert the calibration curve and save the parameters for each pixel

Data reconstruction

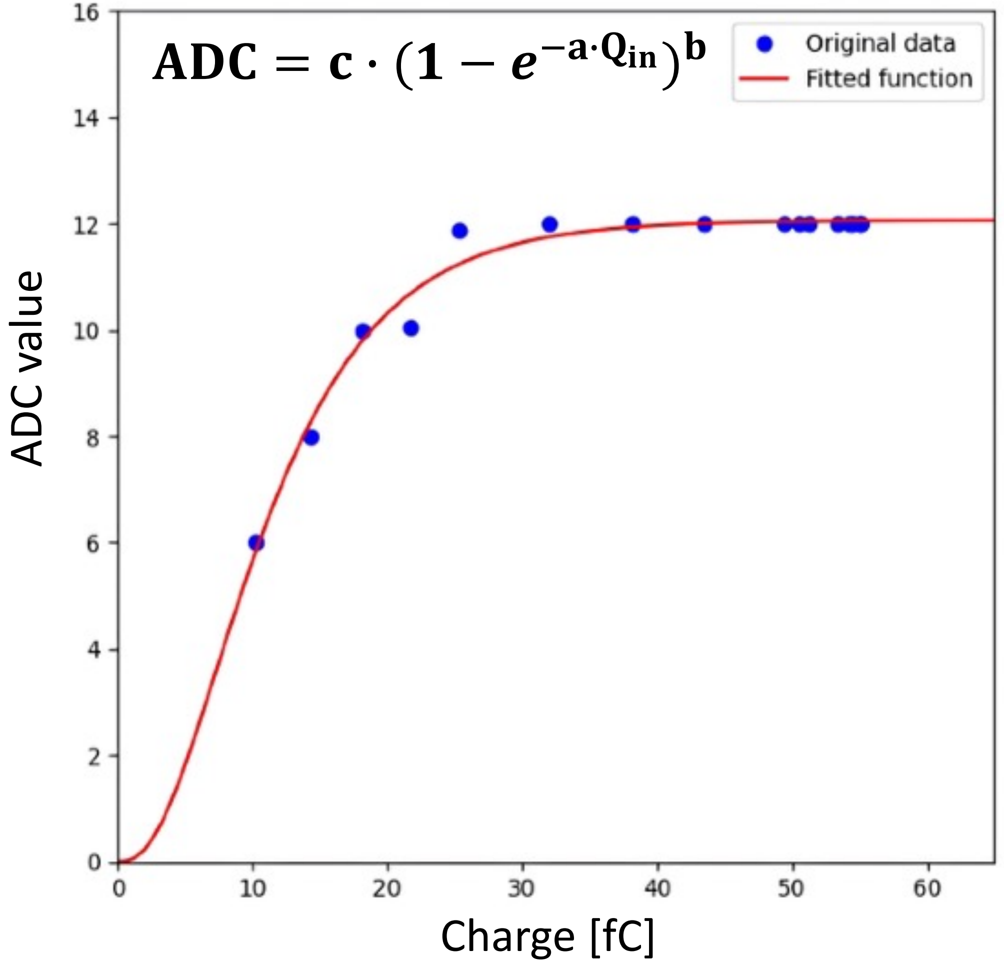


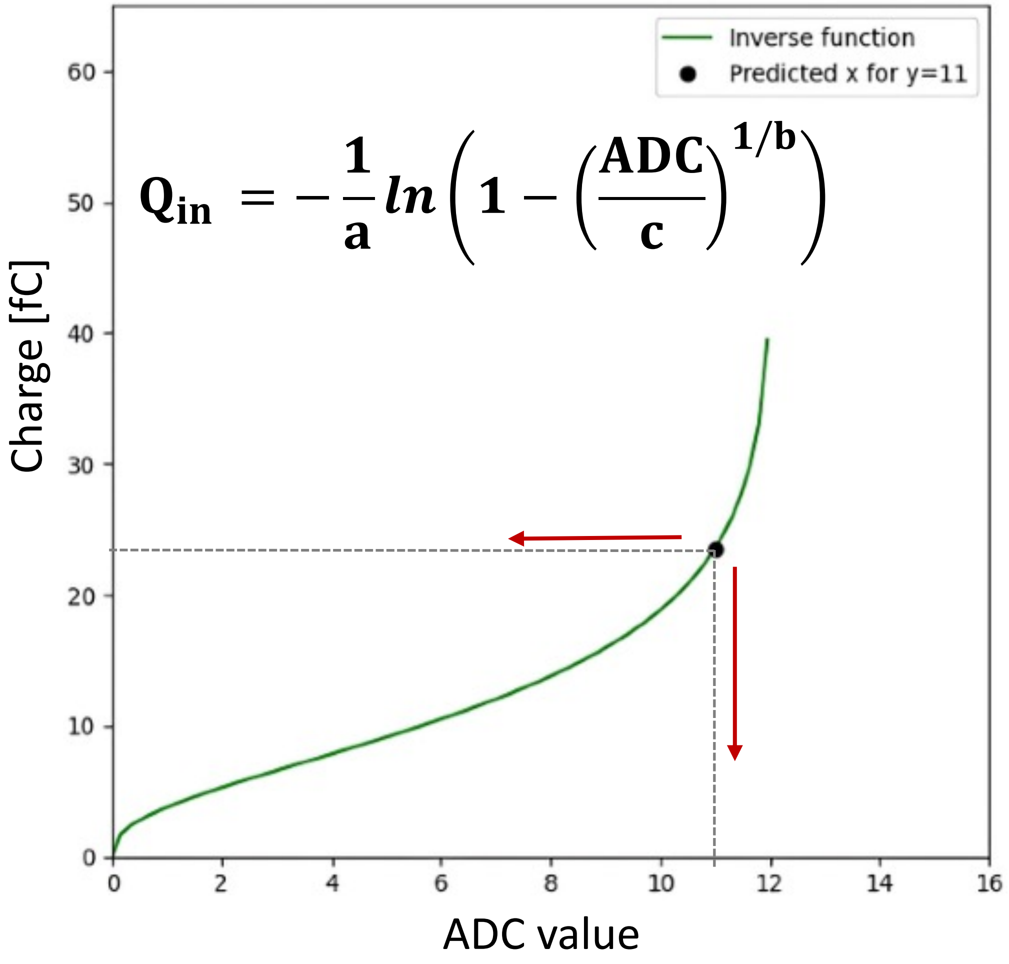
4 — Measured ADC
Collect the data for each event

5 — Use inverted f
Insert the ADC value in the previously saved inverted function

6 — Reconstruct Charge
Project to get the reconstructed charge value

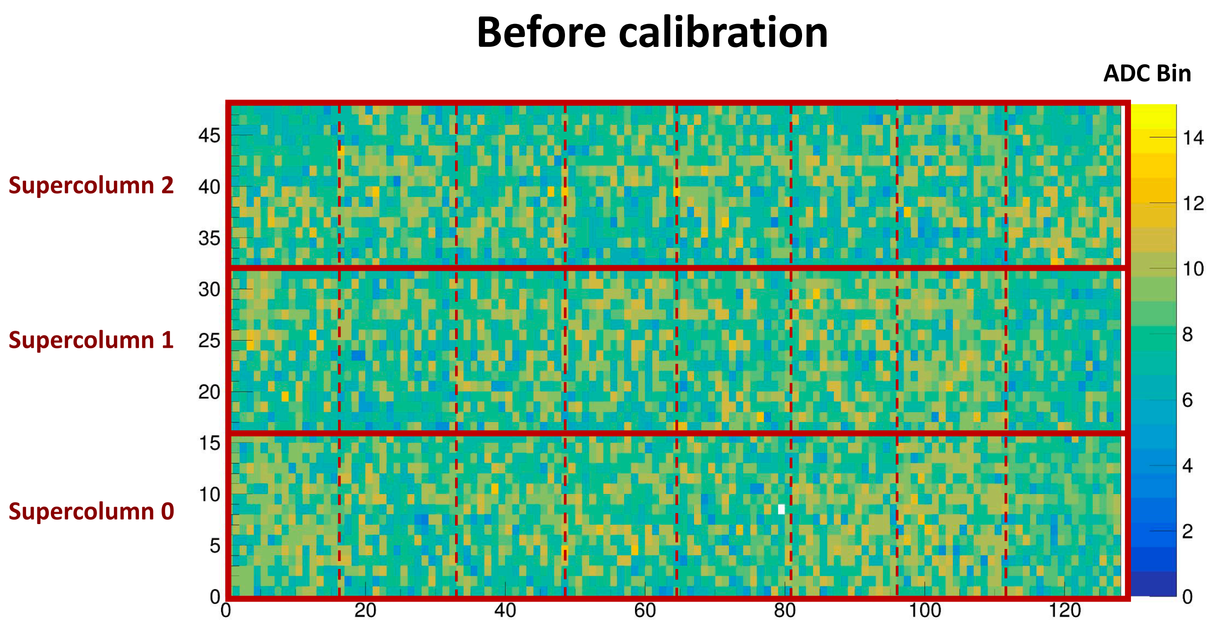
Calibration curve for one pixel

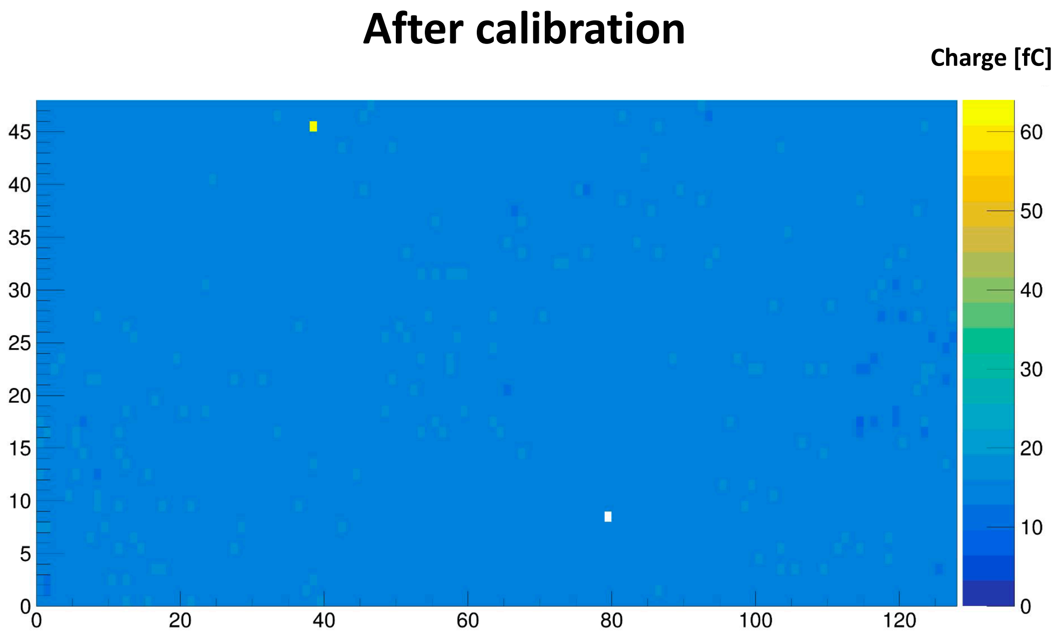




Calibration of the whole ASIC matrix

Q = 14 fC injected

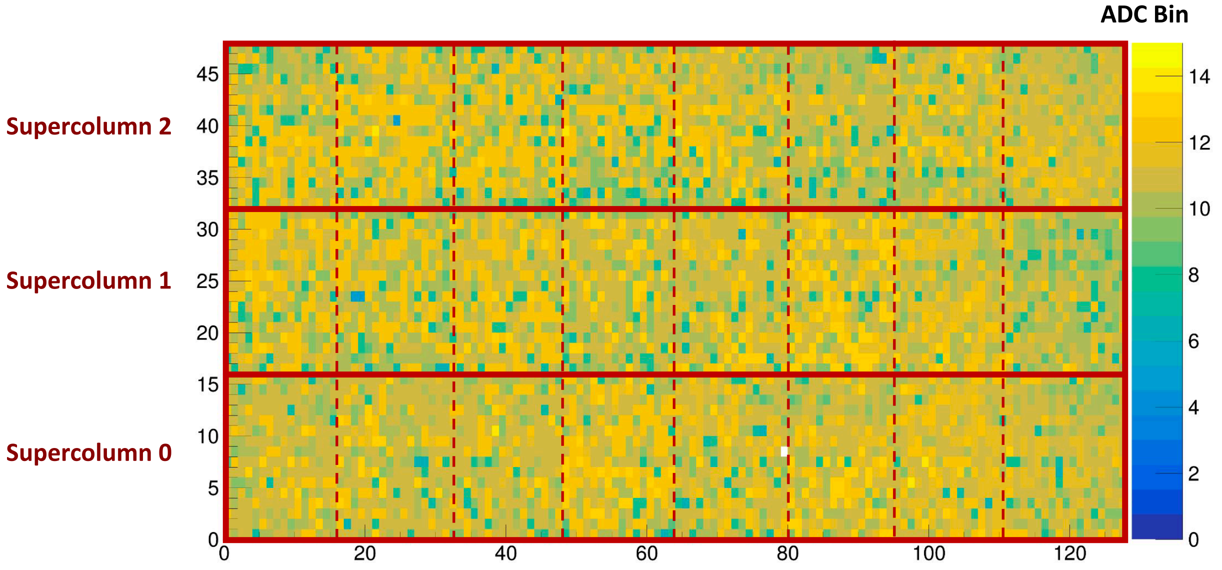




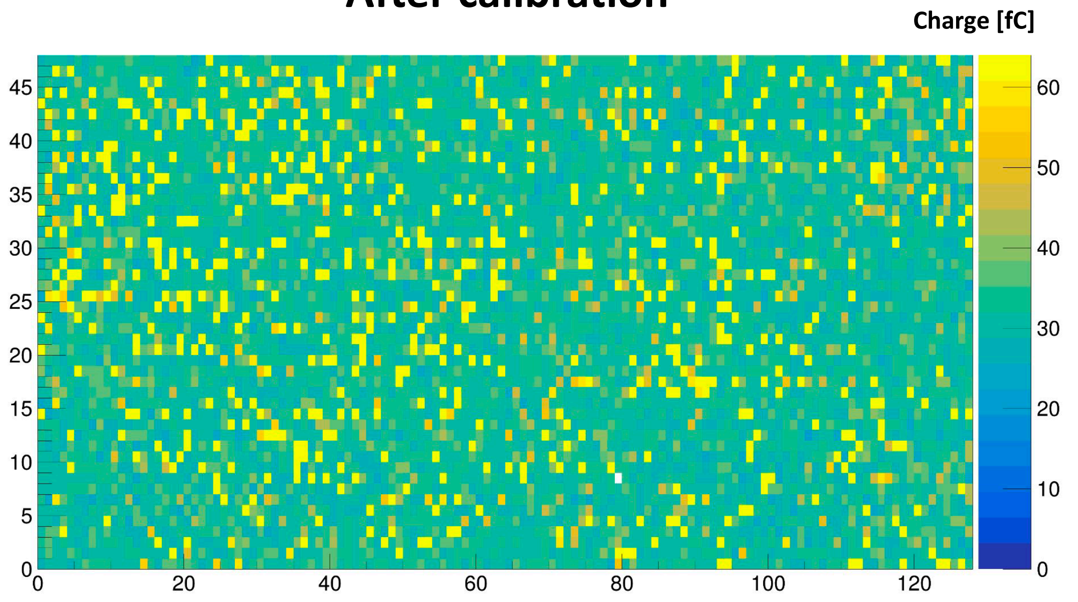
Calibration of the whole ASIC matrix

Q = 32 fC injected

Before calibration



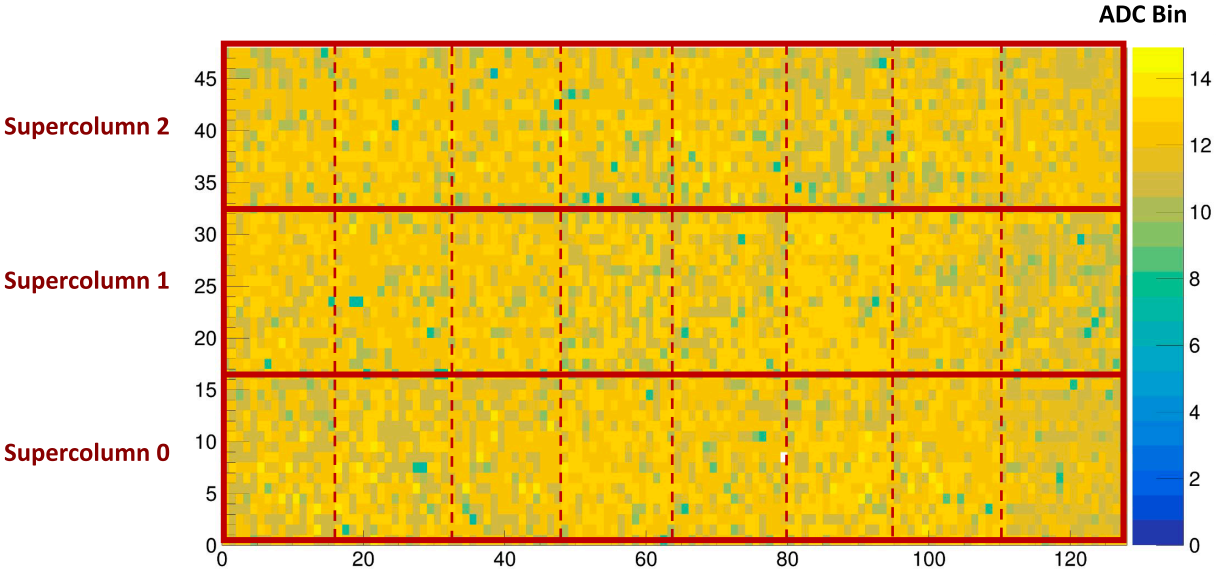
After calibration



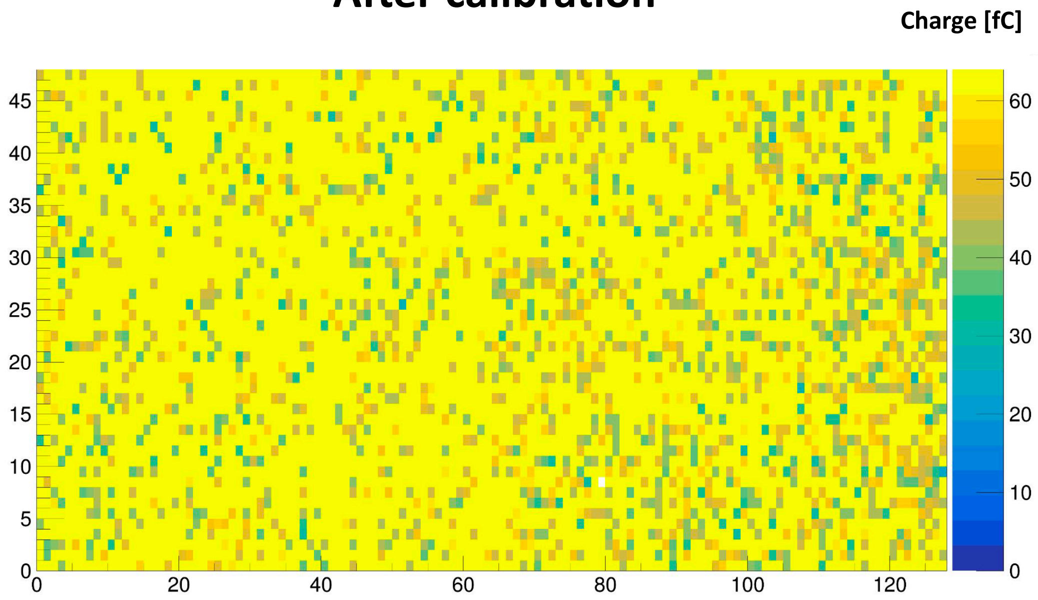
Calibration of the whole ASIC matrix

Q = 51 fC injected

Before calibration



After calibration



Calibration of the whole ASIC matrix

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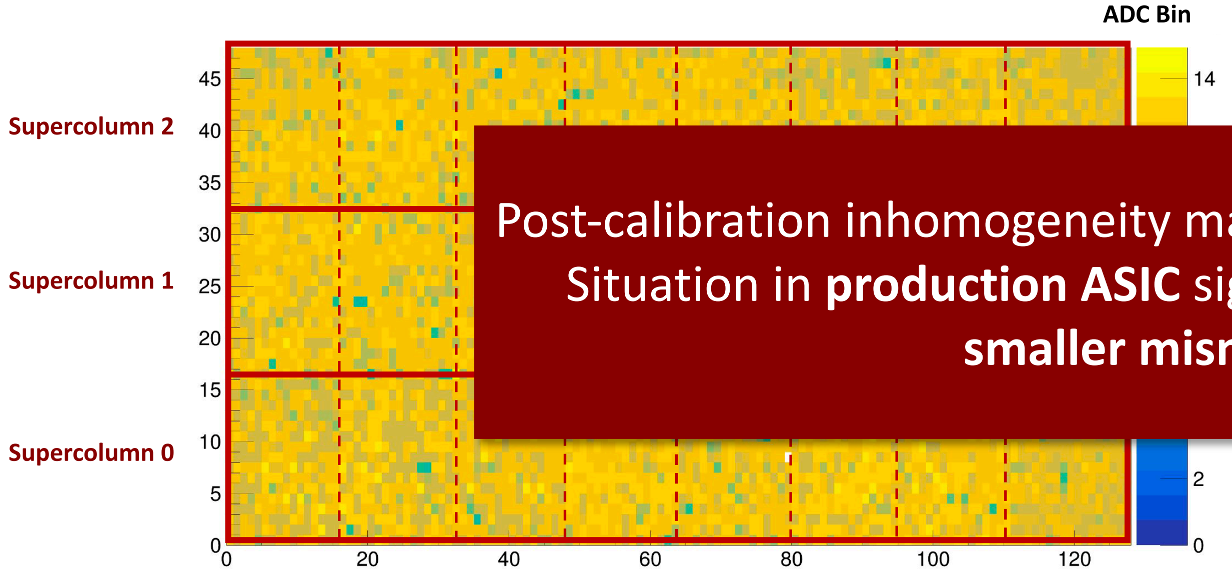
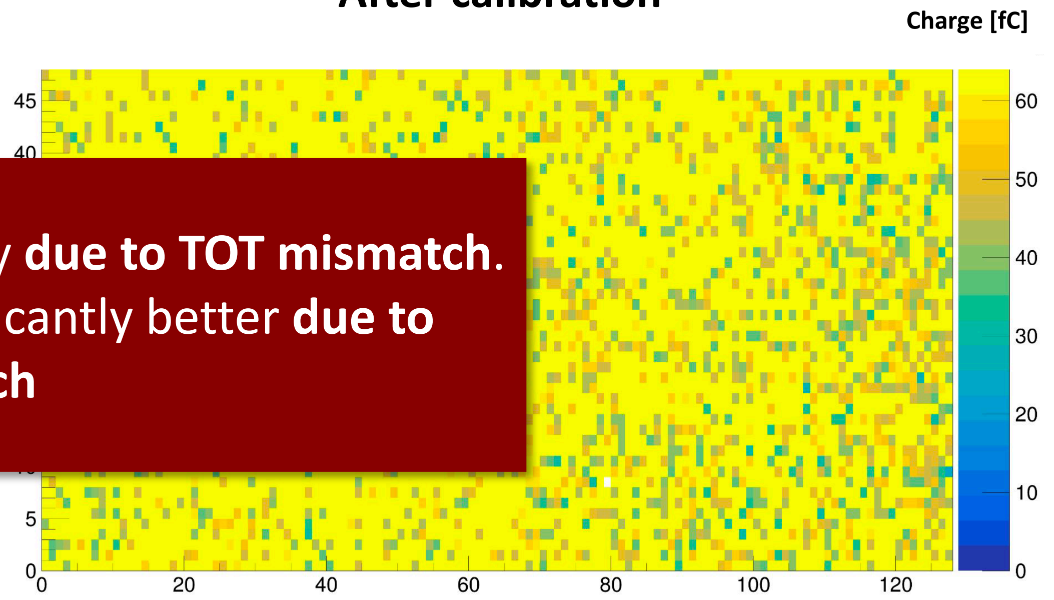
Q = 51 fC injected

Before calibration



After calibration



Post-calibration inhomogeneity mainly **due to TOT mismatch**.
Situation in **production ASIC** significantly better **due to smaller mismatch**

Summary and Conclusions

- A **new preshower detector** is being developed for the **FASER experiment** at the LHC
  - Enabling the discrimination of ultra-collimated TeV diphoton events from LLP decays
  - 130 nm SiGe BiCMOS Technology MAPS designed and developed at the University of Geneva, with support from KIT and CERN
  - Targeting installation in December 2024 and data-taking during last year of LHC Run 3 and HL-LHC

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  - Minor bugs have been identified and corrections have been implemented in the production chip
  - Some tests with respective results have been presented, but many more have been done (time limitation)
  - A paper on the characterization of the pre-production chip will be published soon

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  - A paper on the characterization of the pre-production chip will be published soon

- **Final production chip submitted in May 2023**
  - Expected delivery: end of February 2024
  - Test beam at SPS (CERN) planned for August 2024

The FASER Collaboration

FASER Collaboration Members

Henso Abreu (Technion), John Anders (CERN), Claire Antel (Geneva), Akitaka Ariga (Chiba/Bern), Tomoko Ariga (Kyushu), Jeremy Atkinson (Bern), Florian Bernlochner (Bonn), Tobias Boeckh (Bonn), Jamie Boyd (CERN), Lydia Brenner (NIKHEF), Franck Cadoux (Geneva), Roberto Cardella (Geneva), Dave Casper (UC Irvine), Charlotte Cavanagh (Liverpool), Xin Chen (Tsinghua), Andrea Coccaro (INFN), Sergey Dmitrievsky (JINR), Monica D'Onofrio (Liverpool), Yannick Favre (Geneva), Deion Fellers (Oregon), Jonathan Feng (UC Irvine), Carlo Alberto Fenoglio (Geneva), Didier Ferrere (Geneva), Stephen Gibson (Royal Holloway), Sergio Gonzalez-Sevilla (Geneva), Yuri Gornushkin (JINR), Yotam Granov (Technion), Carl Gwilliam (Liverpool), Daiki Hayakawa (Chiba), Shih-Chieh Hsu (Washington), Zhen Hu (Tsinghua), Peppe Iacobucci (Geneva), Tomohiro Inada (Tsinghua), Luca Iodice (Geneva), Sune Jakobsen (CERN), Hans Joos (CERN), Enrique Kajomovitz (Technion), Hiroaki Kawahara (Kyushu), Alex Keykan (Royal Holloway), Felix Kling (DESY), Daniela Köck (Oregon), Umut Kose (CERN), Rafaella Eleni Kotitsa (Geneva), Susanne Kuehn (CERN), Thanushan Kugathasan (Geneva), Helena Lefebvre (Royal Holloway), Lorne Levinson (Weizmann), Ke Li (Washington), Jinfeng Liu (Tsinghua), Jack MacDonald (Mainz), Chiara Magliocca (Geneva), Josh McFayden (Sussex), Andrea Pizarro Medina (Geneva), Matteo Milanesio (Geneva), Theo Moretti (Geneva), Mitsuhiro Nakamura (Nagoya), Toshiyuki Nakano (Nagoya), Friedemann Neuhaus (Mainz), Laurie Nevay (Royal Holloway), Ken Ohashi (Bern), Hidetoshi Otono (Kyushu), Lorenzo Paolozzi (Geneva), Hao Pang (Tsinghua), Brian Petersen (CERN), Markus Prim (Bonn), Michaela Queitsch-Maitland (Manchester), Hiroki Rokujo (Nagoya), Elisa Ruiz Choliz (Mainz), Jorge Sabater-Iglesias (Geneva), Osamu Sato (Nagoya), Paola Scampoli (Bern), Kristof Schmieden (Mainz), Matthias Schott (Mainz), Anna Sfyrla (Geneva), Savannah Shively (UC Irvine), Yosuke Takubo (KEK), Noshin Tarannum (Geneva), Ondrej Theiner (Geneva), Eric Torrence (Oregon), Svetlana Vasina (JINR), Benedikt Vormvald (CERN), Di Wang (Tsinghua), Eli Welch (UC Irvine), Stefano Zambito (Geneva)

International laboratory covered by a cooperation agreement with CERN

The development and construction of the W-Si pre-shower of the FASER experiment was funded by the **Swiss National Science Foundation (SNSF)** under the **FLARE grant 20FL21-201474** at the University of Geneva. Additional financial contributions from **KEK**, **Kyushu University**, **Mainz University**, **Tsinghua University** and the **Heising-Simons Foundation** are also acknowledged

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FACULTÉ DES SCIENCES
Département de physique nucléaire et corpusculaire

FASER

Thank you !

Chiara Magliocca
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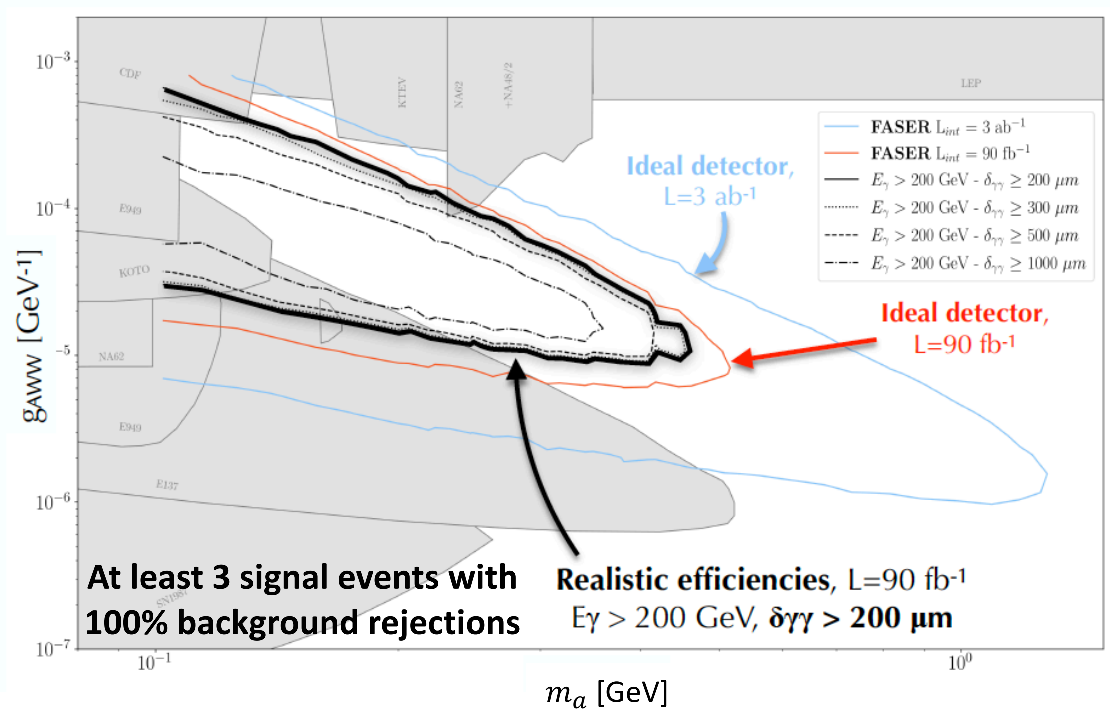
List of publications on the Preshower Upgrade:

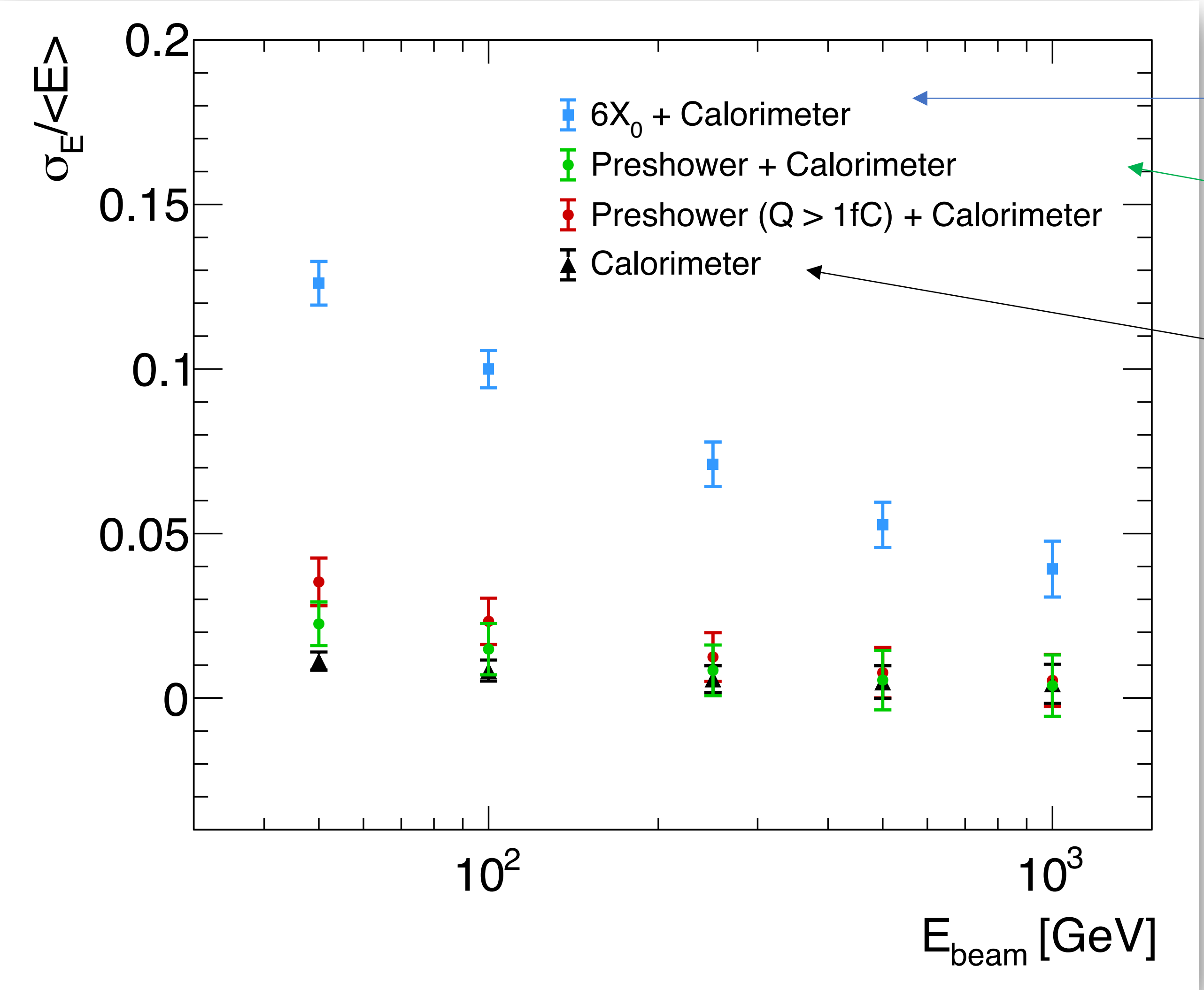
- The FASER Detector
  arXiv: 2207.11427: Accepted for publication in JINST
- The FASER W-Si High Precision Preshower Technical Proposal
  CERN-LHCC-2022-006
- Measurements and analysis of different front-end configurations for monolithic SiGe BiCMOS pixel detectors for HEP applications
  F. Martinelli *et al* 2021 *JINST* **16** P12038

Discovery potential for ALP



BACKUP SLIDES

Energy resolution



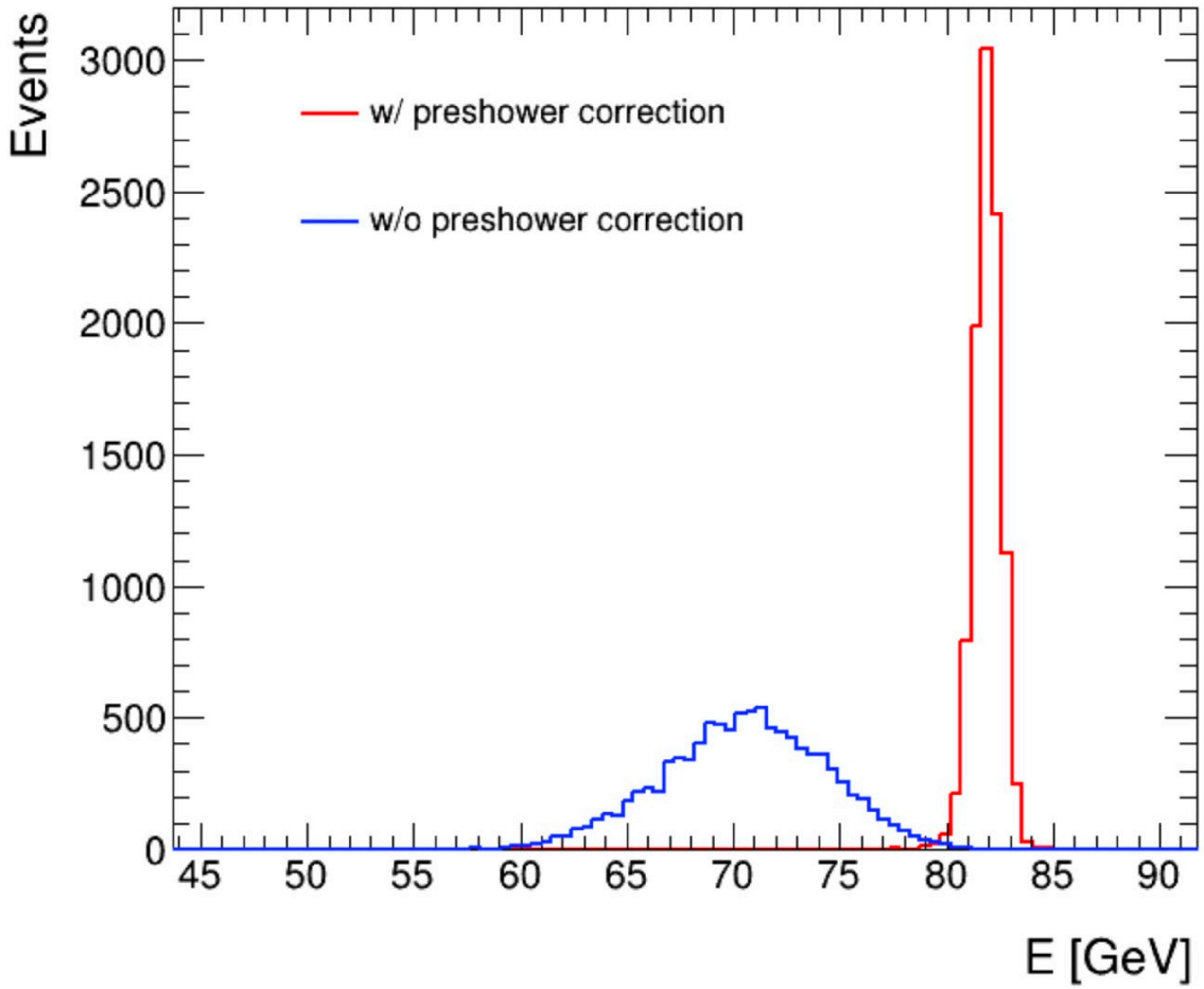
Only looking at the calorimeter (not using the preshower information)

Correcting with the Preshower measurement

Calorimeter only

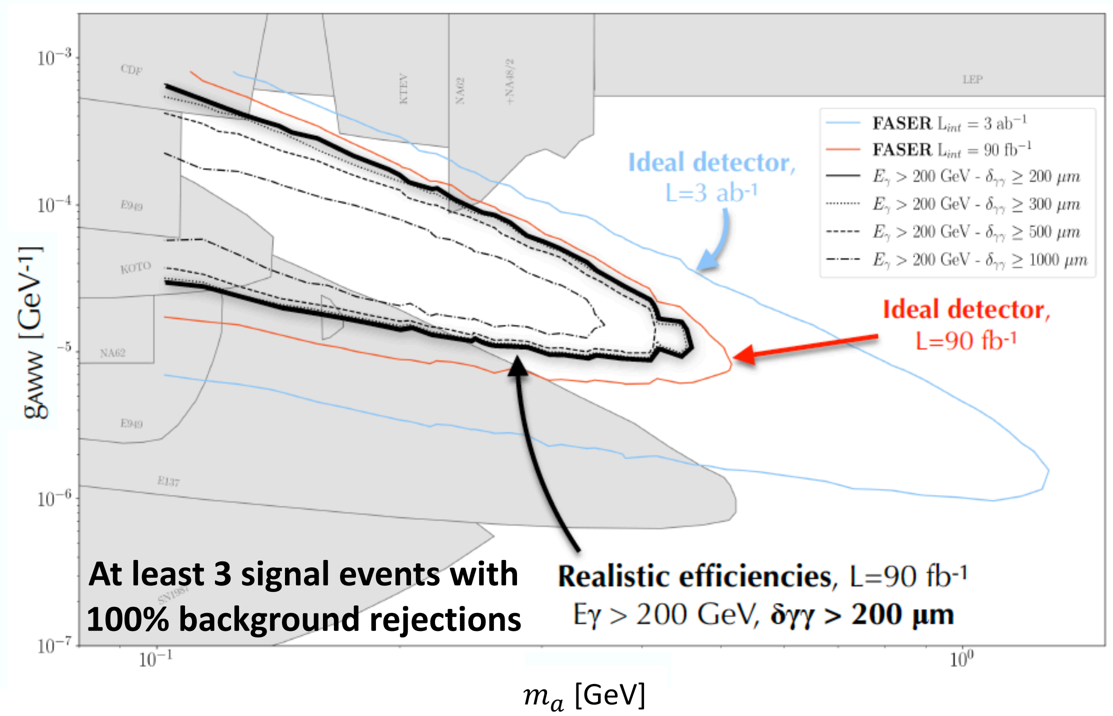
Energy resolution

For 500 GeV photons



Motivations for a new pre-shower detector

Discovery potential for ALP



H. Abreu et al. "The FASER W-Si High Precision Preshower Technical Proposal"
CERN-LHCC-2022-006 ; LHCC-P-023
https://cds.cern.ch/record/2803084

- **Enables measurements:**
  - Axion-Like-Particles (ALP) produced via aWW coupling
  - LLP with neutral pions in the final state
  - Neutrino background suppression
- **Reinforces measurement:**
  - Dark photon and other LLPs decaying into charged fermions
  - LLP with charge and neutral pions in the final state

Detector requirement:
Discriminate photons down to **200 µm separation** to exploit the full potential of the experiment

The FASER Small Prototype Chip (2021)

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

Purpose

study **different level of INTEGRATION OF THE FRONT-END** electronics inside the sensitive area of the pixels

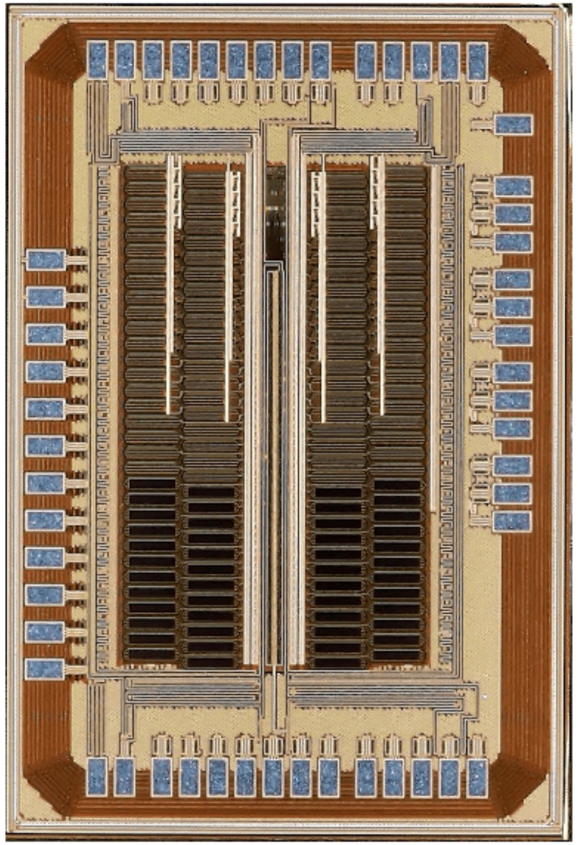
Final aim

identify the BEST FRONT-END CONFIGURATION for the pre-production chip of the FASER Pre-shower (submitted in June 2021)

200 µm x 50 µm PIXELS
shape to reduce the electric field at the edge of the sensitive areas

Tested in 2021

2 superpixels
16x4 pixels each



2.6 mm

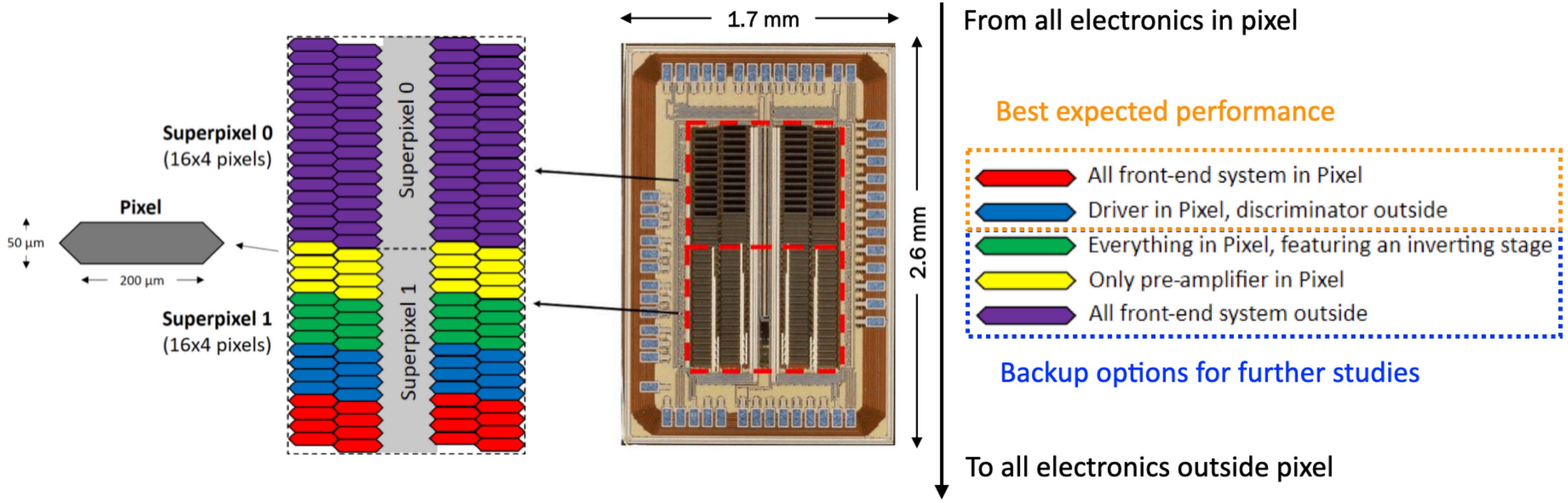
1.7 mm

Small Prototype: Front-end Configurations

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

First chip prototype tested in 2021

- designed to study different levels of integration of the front-end electronics
- simultaneous goals: minimize dead area and routing capacitance, maximize stability



Small Prototype: Results and Comments

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

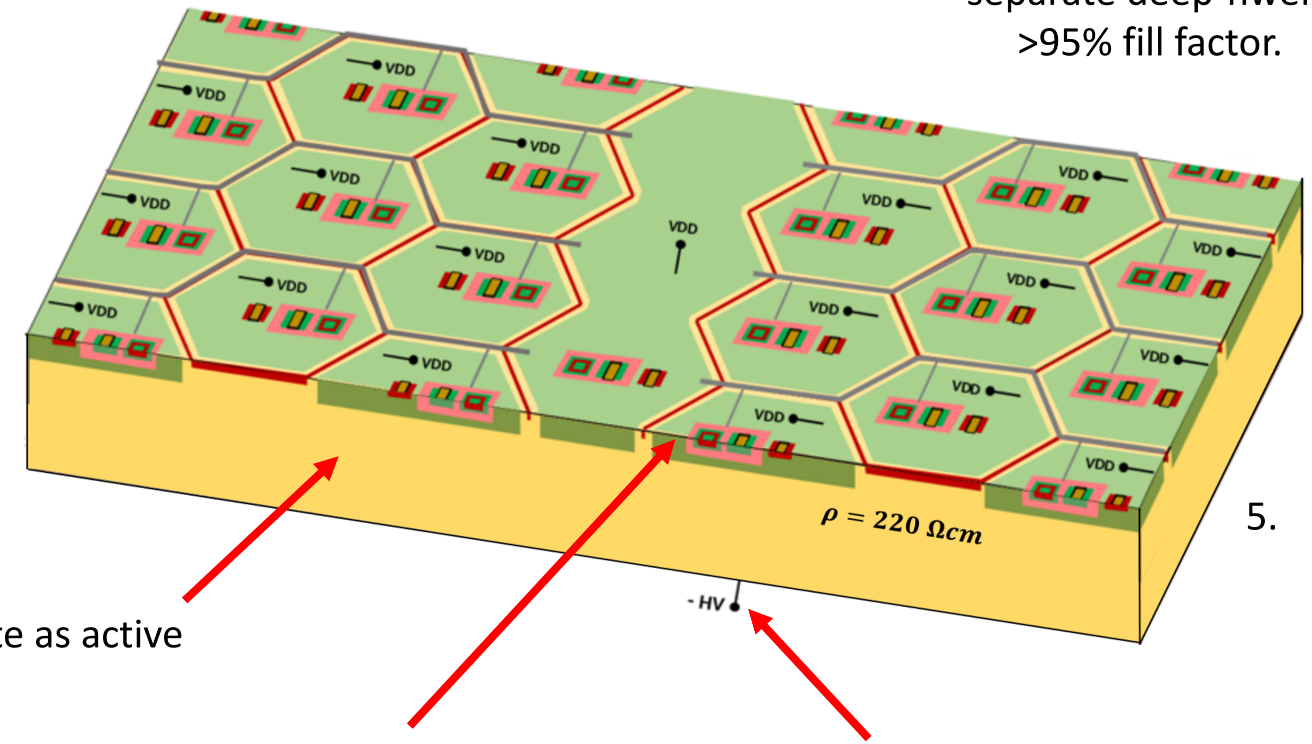
- All front-end system in Pixel
- Driver in Pixel, discriminator outside
- Everything in Pixel, featuring an inverting stage.
- Only pre-amplifier in Pixel
- All front-end system outside

Configuration	σ_v [mV]	G_c [mV/fC]	ENC [e$^-$]	$\sigma_{V_{th}}$ [mV]
All f.e. outside pixel	4.2 ± 0.2	159 ± 1.0	165 ± 9	32.3
Only pre-amp. in pixel	2.5 ± 0.1	96.8 ± 0.5	161 ± 9	26.9
All f.e. in pixel, inv. stage	6.9 ± 0.5	179 ± 1.0	241 ± 19	30.8
Pre-amp. and driver in pixel	3.8 ± 0.2	133.7 ± 0.6	178 ± 9	23.4
All f.e. in pixel	5.4 ± 0.4	148 ± 1.0	228 ± 20	27.1

Last two configurations represent a good compromise between *comptacness* and *performance*: adopted for the pre-production prototype

Monolithic Pixel ASIC: Sensor

7. Digital electronics can be placed in pixel or in a separate deep-nwell to improve noise robustness.
   >95% fill factor.



6. Analogue electronics in pixel.

1. CMOS die thinned to 130 µm

5. Pixel and electronic deep n-wells are kept at positive low voltage.

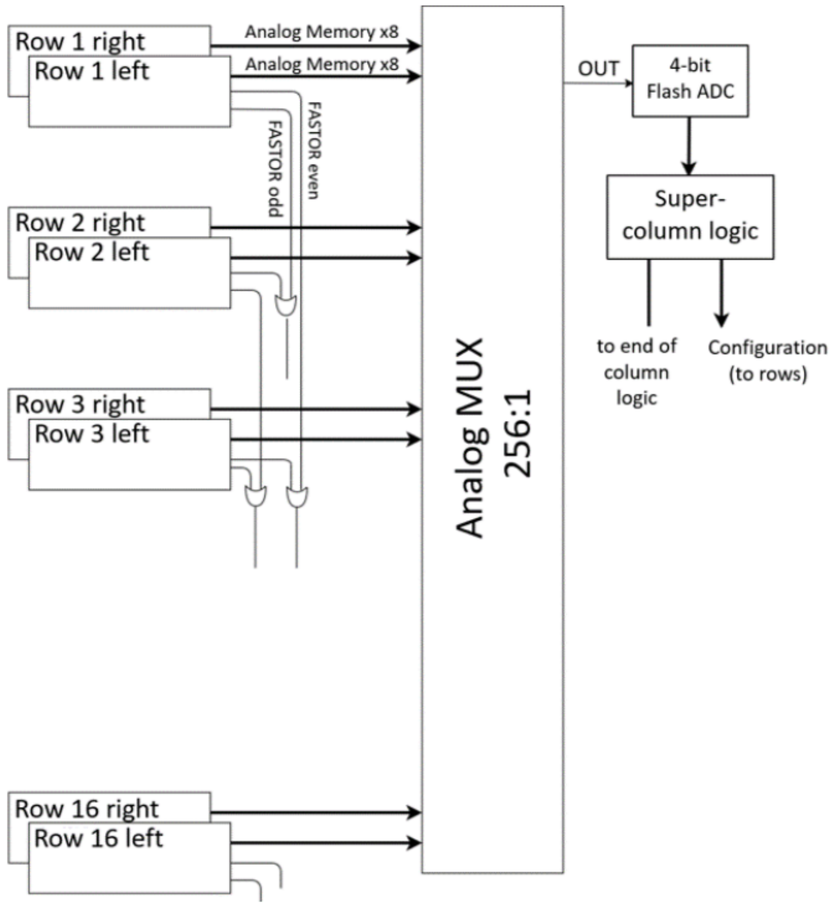
2. High resistivity substrate as active volume.

Depletion: 50 µm

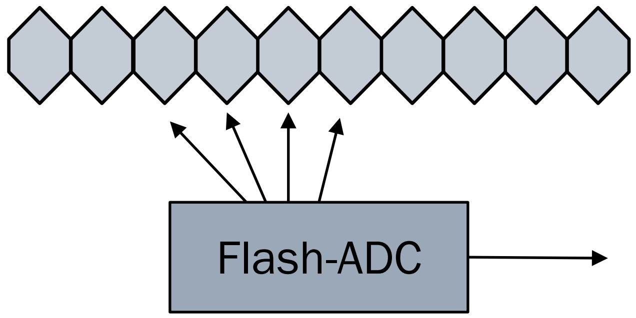
3. Electronics inside the guard-ring, isolated from substrate using deep n-well.

4. Negative High Voltage applied to the substrate from front-side contact.

Super-pixel Architecture



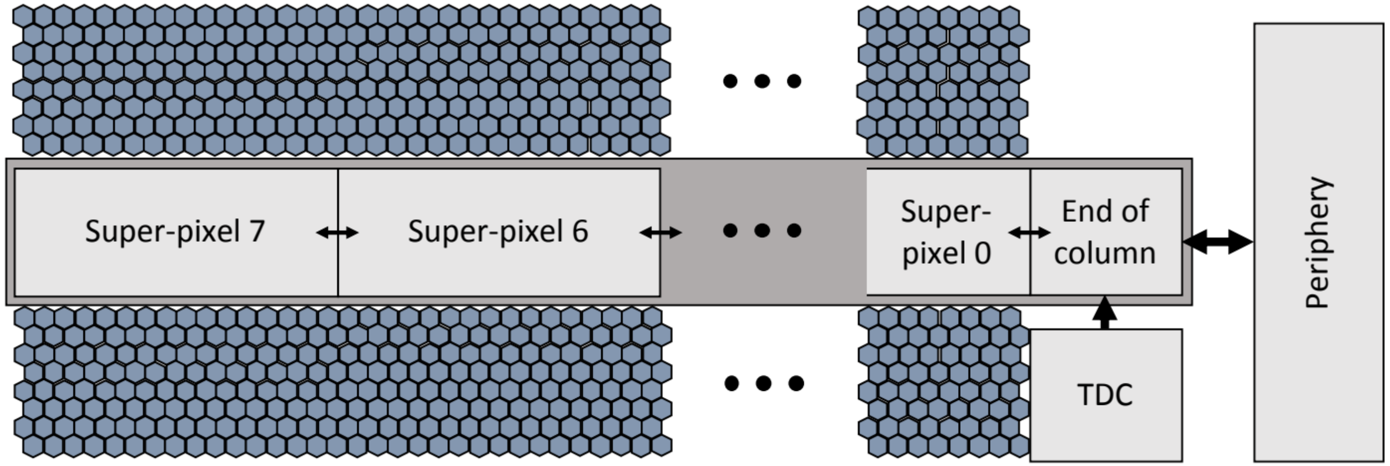
- Charge needs to be measured for each pixel: **acts as an imaging device.**
- Data is stored on the **capacitor in each pixel** and converted on the fly with a **flash ADC** at the output of a **256-to-1 MUX**.
- The capacitor is charged with a **constant load current** during the TOT.
- The **same ADC** will poll all pixels in a Super Pixel (SP) and convert them as needed.

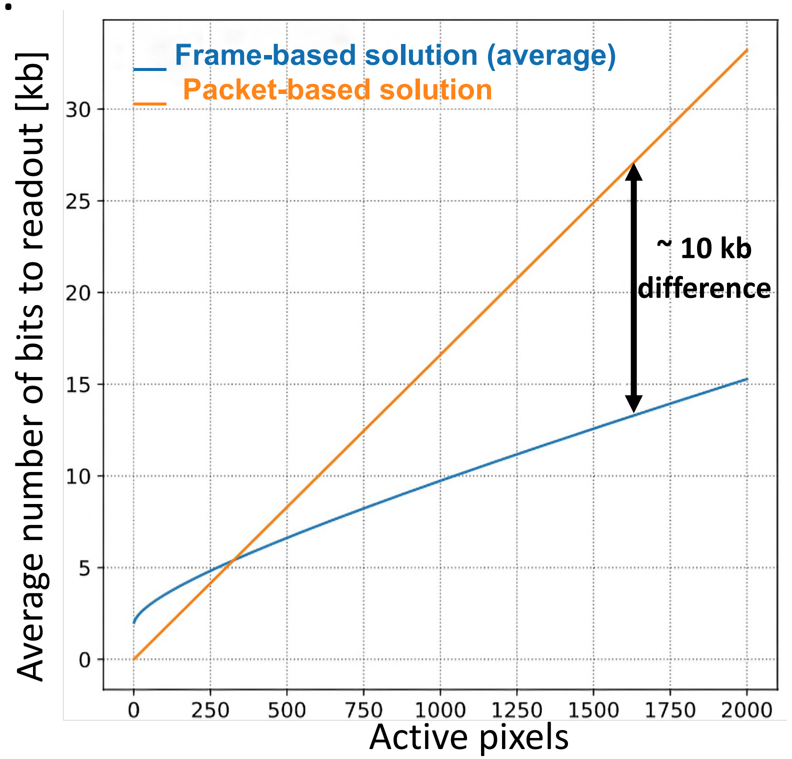


Super-column Architecture

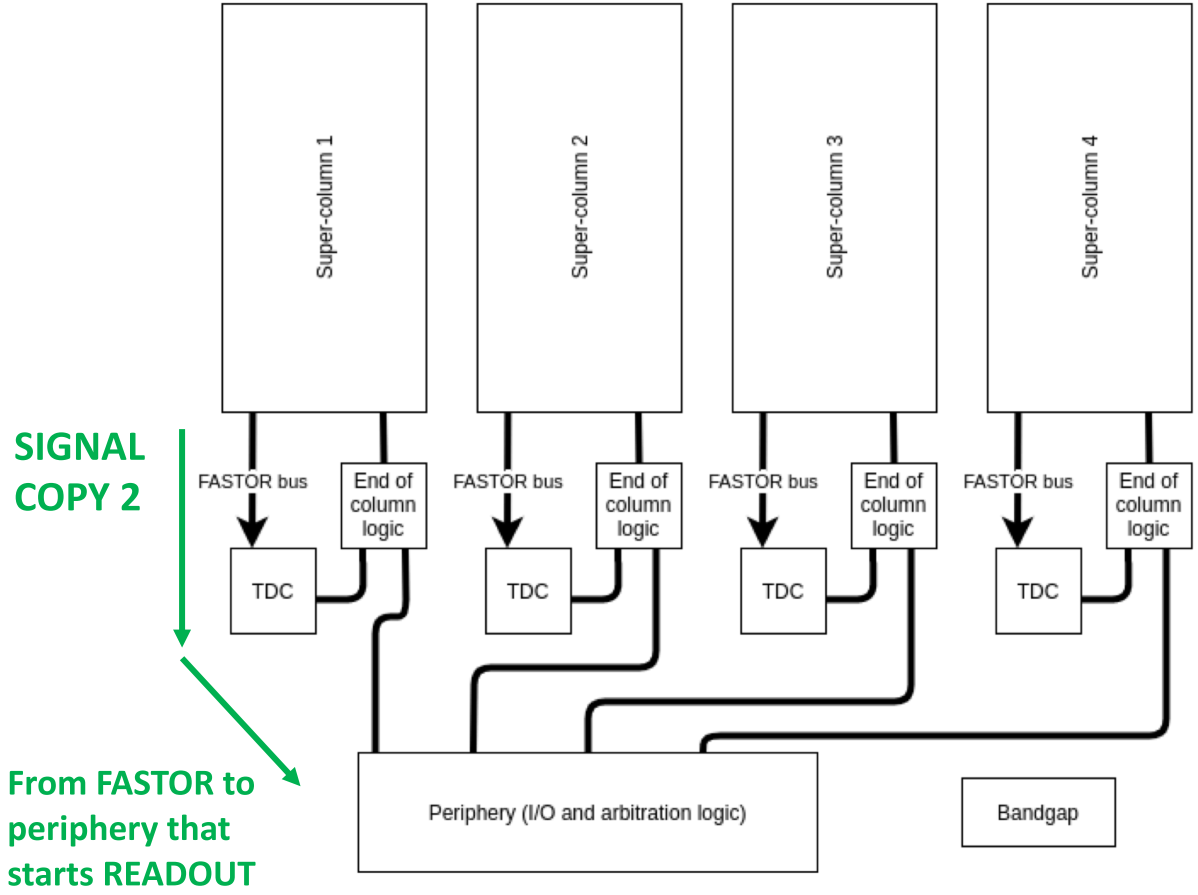
- Super-column (SC) logic: mask the pixels, generates the test-pulse (TP), drives the analog MUX, handles readout and communication with the periphery.

- SC are read out **only if they register a hit**.
- SC level **frame-based** solution for readout logic in the periphery.



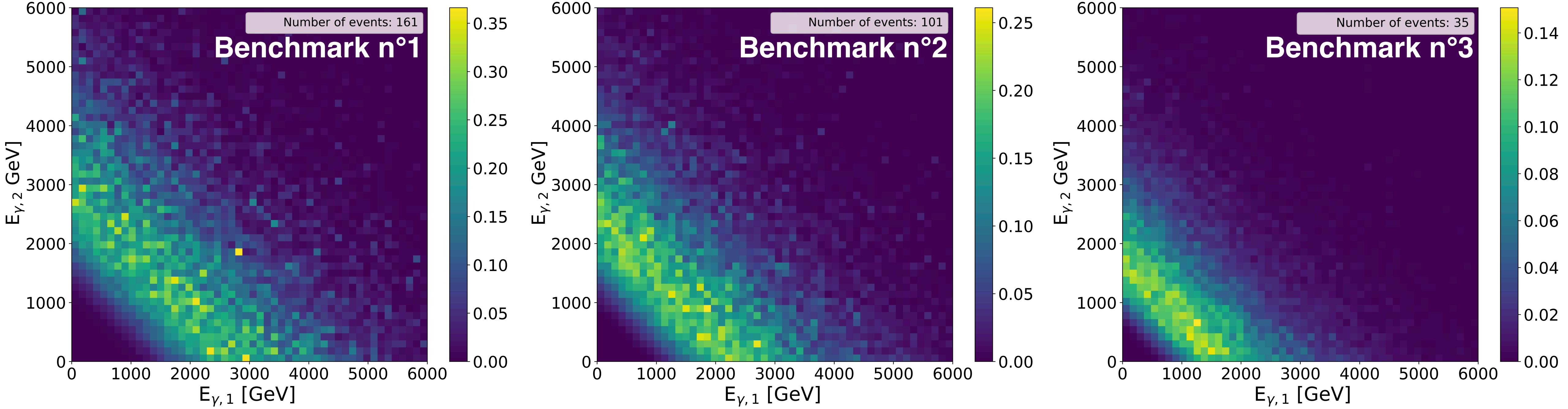


ASIC Structure and Readout



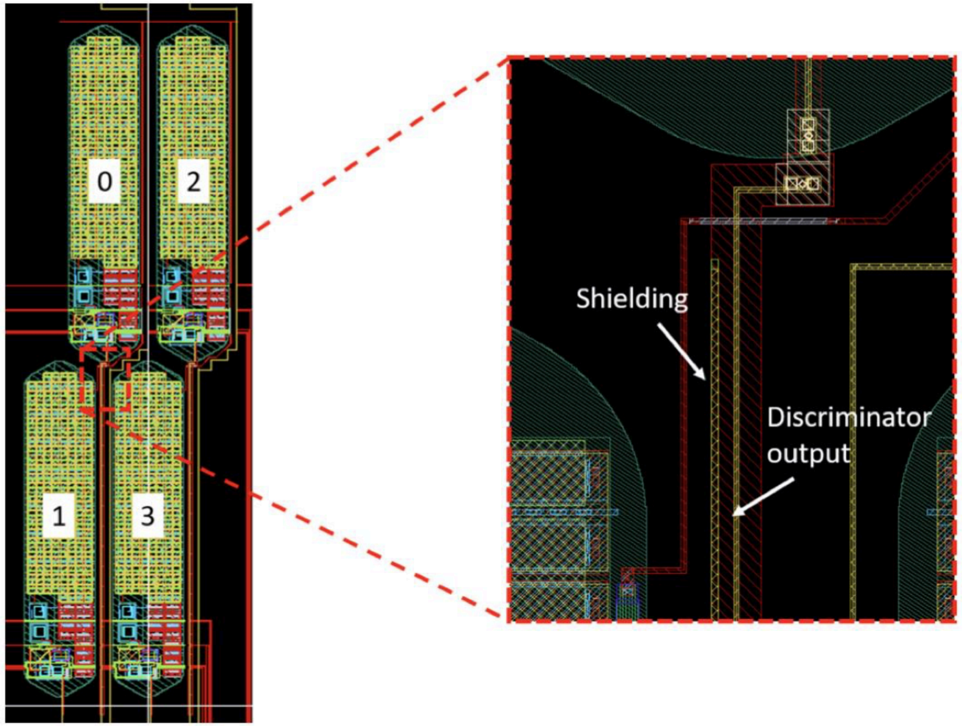
- A copy of the signal exit **IMMEDIATELY** the pixel through the FASTOR
- Each FASTOR send a signal to the perifery to start the READOUT
- To be sure we collected the charge entirely, the **perifery waits a bit before starting the READOUT**
- **Readout time max 200 µs**
- If in a super-pixel **zero FASTOR** are **active, zero bit are sent to the periphery (optimization)**

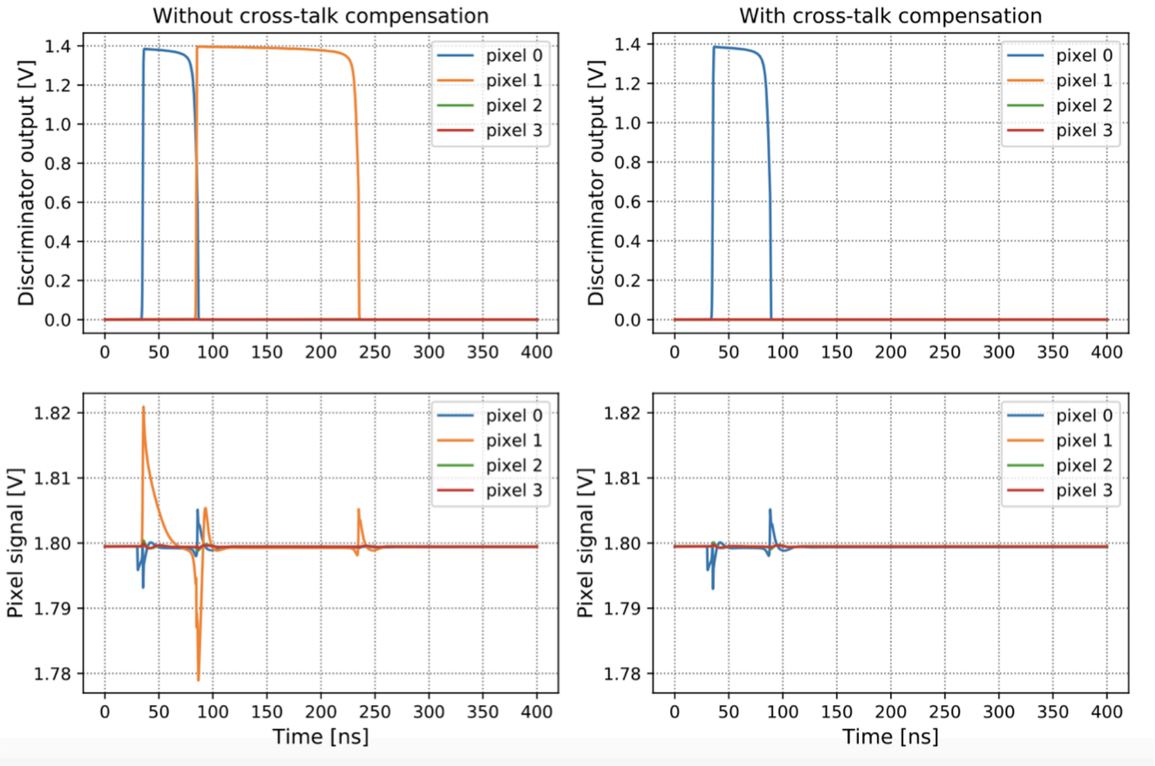
Di-photon Signal Energy Distributions



Signal Routing and Crosstalk Suppression

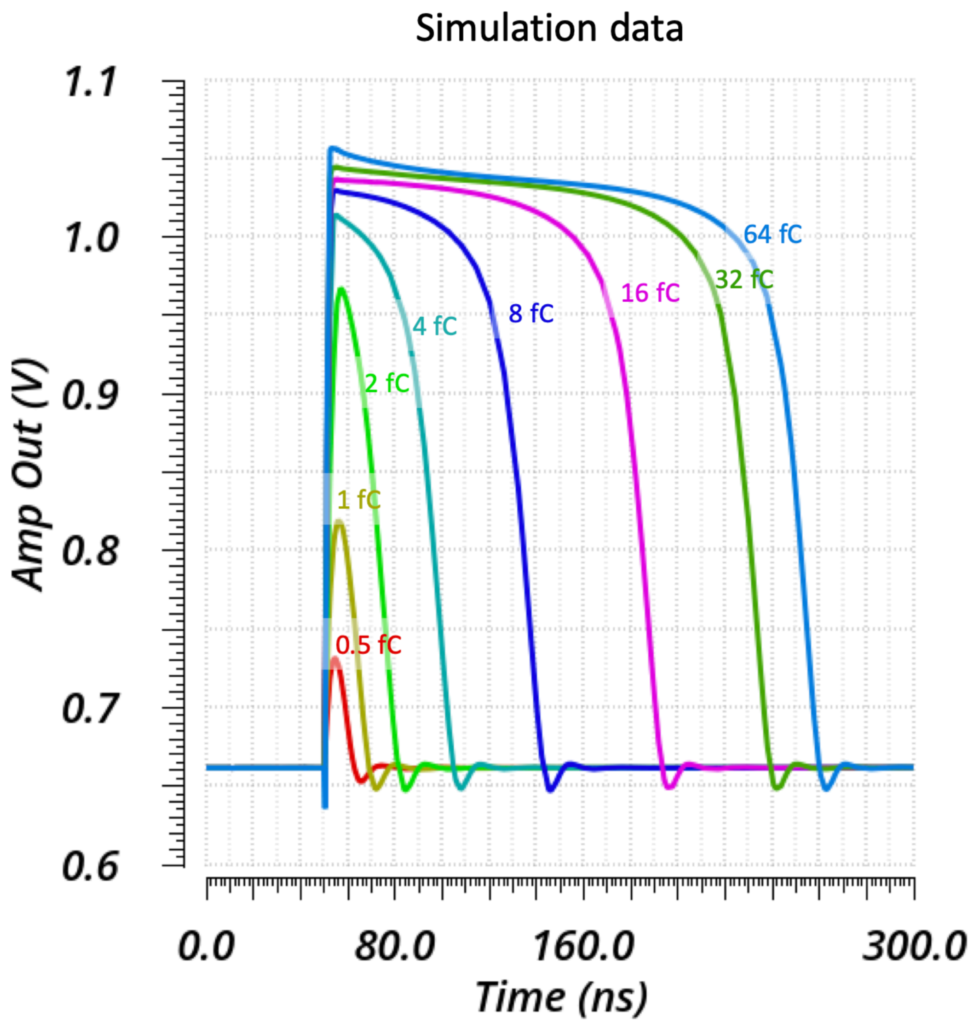
- Signal routed in a **shielded bus** to **minimize crosstalk between neighboring pixels**



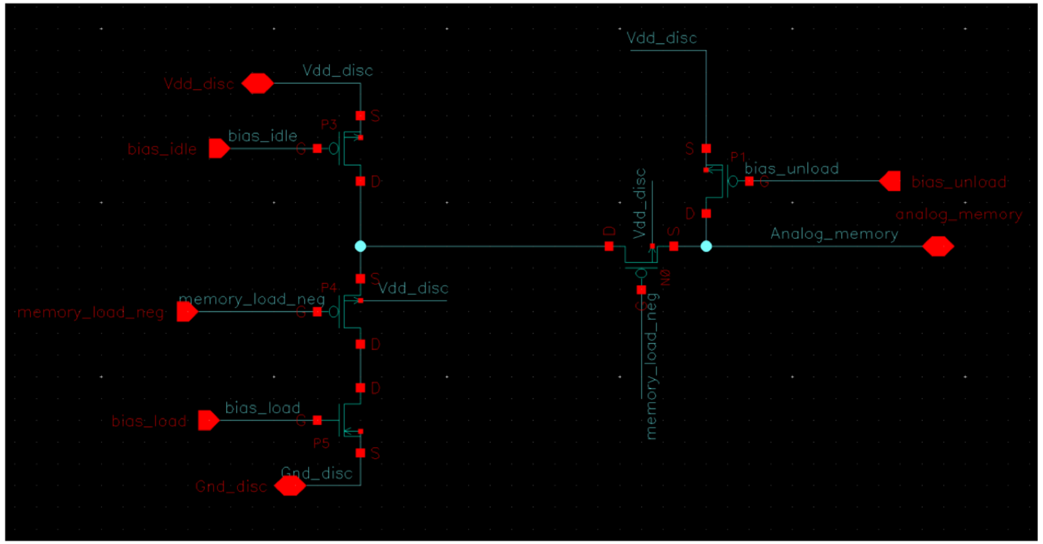


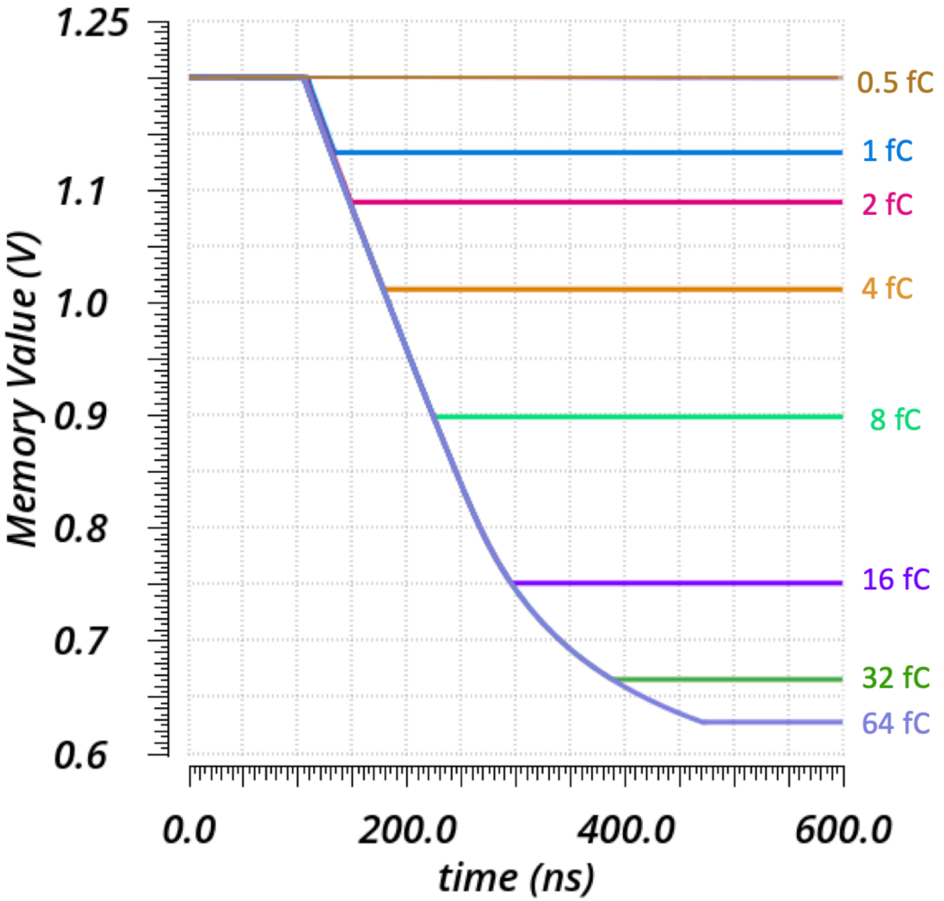
Amplification Stage

- Since we want to measure high charges we convert the charge information to Time Over Threshold
- **For different charges, if the charge increases also the TOT increases but not linearly (almost logarithmic relation)**
- **Saturation at 64 fC (intrinsic saturation of the pixel)**



Memory Control and Analog Memories





- When signal returns below threshold, memory is disconnected and left floating until read by the flash ADC
- Current leakage even if the switch is opened
- It takes 200 µs to degradate the memory value of 30 mV (= 1 bin of our ADC)

After 200 µs we still measure something but we are less precise

Di-Photon Reconstruction Efficiencies

$E_{\gamma 1}$= 1 TeV
$E_{\gamma 2}$= 1 TeV