

# Quality Assurance / Quality Control of the LGAD sensors for CMS ETL

#### 20.2.2024

Federico Siviero on behalf of the CMS ETL group







- ➤ The CMS MIP Timing Detector (MTD)
  - The Endcap Timing Layer (ETL)
  - $\circ \quad \text{Sensors for ETL} \quad$
- The ETL sensor QA/QC strategy
  - Process Quality Check
  - Sensor Quality Check







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# The CMS MIP Timing Detector (MTD)



- > MTD will provide accurate timing of charged tracks during the High-Luminosity phase of the LHC (HL-LHC)
- > It will be divided into 2 sections:
  - BTL: Barrel Timing Layer
  - ETL: Endcap Timing Layer







# **Endcap Timing Layer (ETL)**



- ETL will be mounted on the nose of the CMS CE calorimeter
- 2 double-sided disks on each side of CMS (+z / -z)



Endcap region of the CMS detector



# **Endcap Timing Layer (ETL)**



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ETL disk

- 2 double-sided disks on each side of CMS (+z / -z)
- Coverage:
  - $\circ$  z ~ 3 m from pp interaction
  - ~0.3 m < R < ~1.2 m
  - $\circ$  1.6 <  $|\eta|$  < 3.0
  - $\circ$  Surface ~ 14 m<sup>2</sup>





# **Sensors for ETL: LGAD**



- ETL will be instrumented with LGAD sensors, with a 16x16 pad array
  - $\circ$  ~~ 1.3 x 1.3 mm^2 pads for a total surface of 21.4 x 21.6 mm^2
- ETL LGADs can achieve:
  - Single hit time resolution < 50 ps
  - Delivered Charge > 8 fC
  - Maintain performance up to the end of detector operation ( $\Phi \sim 1.5$ -2.5e15 n<sub>eq</sub>/cm<sup>2</sup> in the most irradiated regions of ETL)





• LGADs will be bump-bonded to the ETL read-out ASIC (ETROC)



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#### The LGAD schedule

- 2023: Market Survey completed, we identified 3 potential vendors
- ➤ 2024: Freeze LGAD specifications + define quality management (QA/QC) procedures for the sensors production → Invitation to Tender and final selection of the vendor(s)
- 2025: Beginning of the sensor production for ETL



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Today I will focus on this







- > The CMS MIP Timing Detector (MTD)
  - The Endcap Timing Layer (ETL)
  - Sensors for ETL

#### The ETL sensor QA/QC strategy

- Process Quality Check
- Sensor Quality Check







- ETL will comprise ~ 35k LGAD sensors (20% spare sensors included)
- How do we ensure they are working and within specifications? → that's the purpose of the quality management procedures described in this presentation
- Quality management is split in Quality Assurance (QA) and Quality Control (QC)
  - **QA:** actions taken to ensure the sensor meets specifications
  - **QC:** monitor results after the sensor is produced
- QA/QC to be carried out both at vendors and at the ETL testing sites





## LGADs production schedule

- Sensors will be delivered in **batches**, starting August 2025
- A pre-production series (5% of the total) will be delivered a few months in advance, will be used to set the sensors acceptance ranges, based on the parameters discussed in the following



Batch	Delivery date
Pre-production (5%)	February 2025
Face 1 (20%)	August 2025
Face 2 (25%)	December 2025
Face 3 (25%)	March 2026
Face 4 (25%)	July 2026

A wafer of the FBK UFSD4 production











- **Process Quality Check (PQC)**: check quality of all the process steps
- 16x16 LGADs on-wafer testing:
  - **Optical Inspection:** no scratches or any other visible damage
  - Sensor Quality Check (SQC): on-wafer characterization of the sensors







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## **Process Quality Check (PQC)**



Aim of the PQC: check quality of the process steps using test arrays that will be placed on wafer

#### The test array will comprise

- Process Control Monitor (PCM) structures to measure oxide charges and thicknesses, resistivities
   Acceptance ranges on PCM defined internally by vendors
- A single LGAD to perform a CV: measure gain implant profile and gain layer depletion voltage (VGL)
   Acceptance ranges on implant profile and VGL will be fine-tuned after pre-production



Example of a test array



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  - $\rightarrow$  If all the parameters are within acceptance ranges, the wafer can proceed to the SQC phase



Example of a test array







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The aim of the SQC is twofold:

#### 1) Identify sensors not working or with parameters not in the acceptance ranges

- We identified 3 main parameters to achieve this:
  - Breakdown Voltage (VBD)
  - Leakage Current in the sensor operation range
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#### **SQC Parameter 1: VBD**



- To compute the Breakdown Voltage (VBD), we identified the <u>k-factor</u> method [1]
- The k variable measures the relative increase of the sensor current (for a fixed ΔV) normalized to the absolute value of V and I
  - $\circ \quad \mathsf{k}(\mathsf{I},\mathsf{V}) = (\Delta\mathsf{I} \ / \ \Delta\mathsf{V})^*(\mathsf{V} \ / \ \mathsf{I})$

 $\begin{cases} k~1 \text{ Ohmic resistor} \\ \text{VBD defined as first voltage at which } k > k_{THR} \end{cases}$ 

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- $\circ ~~$  k  $_{\rm THR}$  to be fine tuned, it will be in the 15-25 range
- This method does not depend on the compliance set during the IV measurement
- To fully exploit the k-factor method, we will request on-wafer IVs with a variable voltage step size:
  - We require fine steps (2 to 5 V) from 0 V to full depletion and as close to the BD.
  - 10 V steps are suitable in the intermediate region

#### SQC Parameter 1: VBD → requirements

2500

- For a given vendor, the VBD distribution
   (@ room T) is computed over a large statistics of sensors
  - Sensors going in BD outside μ ± 3σ will be rejected, where μ, σ are the mean and the std. deviation of the distribution
- We will use pre-production data to fine-tune this acceptance range



VBD HPK2 split4

Measurements performed at room T

An example of VBD distribution, from the HPK2 production (on-wafer tests on single pads, room T)



9620

243.3

HPK2 split4

Entries

Mean

27







- For the sensors leakage current check:
  - An **upper limit I**<sub>MAX</sub> is set on the total sensor leakage current (all pads + guard-ring at room T)
  - The maximum voltage of operation V<sub>MaxOp</sub> is defined as the voltage up to which the sensor noise ~ electronics\_noise and no micro-discharges are present (see backup for details)







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  - If the leakage current exceeds I MAX at any voltage lower than V MaxOp, the sensor is rejected
- A rough estimate for I <sub>MAX</sub> based on available sensors:
  - I<sub>MAX</sub> ~ 10-20 uA for designs with carbonated
     Gain Layer
  - I<sub>MAX</sub> ~ 1-5 uA for designs without carbonated
     Gain Layer









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- Pad-by-pad tests can provide the position of the bad pad(s):
  - These investigations are time-consuming, will not be not requested to the vendors
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Early BD of the whole array

the sensor going in BD earlier



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#### Why grouping?



ETL module: Four LGADs bump-bonded to the ETROC ASIC, arranged between the module PCB and a baseplate

- LGADs will be assembled in modules (4 sensors/module) on the ETL disks: they will have a common bias voltage line → need to ensure that sensors have a similar doping
- 2) Modules comprising sensors with a higher doping will be used to instrument regions more exposed to radiations (because of their higher radiation hardness)





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- Straightforward when using a reticle. Otherwise, careful placement to be implemented in the mask layout







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Test structures mapping the wafer in the same way as the  $16x16 \rightarrow$  **no need to extract VGL from the 16x16 sensors, use the PQC CV results** (from the single LGAD) instead





#### **Outcome of the SQC**



- The outcome of the SQC will be summarized in the wafer quality maps:
  - Breakdown Voltage (VBD)
  - $\circ$  Leakage current measured at V<sub>MaxOp</sub>
  - Presence of noisy pad(s) [0= no noisy pads; 1= presence of noisy pads]





## **Sensors categories**



Based on the SQC parameters, the 16x16 sensors will be divided into categories, reflecting their quality

- **GOOD:** sensors working as expected, all parameters within acceptance ranges
- **BAD:** sensors with one or more parameters out of acceptance ranges
- MEDIUM: Breakdown and leakage current level within specifications, but a bad pad is present
  - Only a very small fraction of the 16x16 will fall into this category: a bad pad usually causes the sensor to be tagged as BAD



Categories will be summarized in the wafer quality map

(this map for illustrative purposes only, not realistic)



# **Sensors categories**



After the wafer post-processing:

- GOOD sensors will be grouped according to their VGL and will go to testing sites / bump-bonding
- BAD sensors will be discarded
- MEDIUM sensors will be stored for backup or further investigations





# **Summary & Outlook**



- ETL will be installed in the CMS detector during HL-LHC, providing accurate timing of charged tracks for the entire lifetime of the detector
- ETL will be made of 16x16 pad array LGADs  $\rightarrow$  the first production sensors will be ready in 2025
- We need to test ~35k LGADs and ensure their quality and performance!
- That's the purpose of the QA/QC procedures described in this presentation:
  - In the <u>PQC</u> phase, test structures will be used to check the quality of the process steps and the gain implant
  - During the <u>SQC</u>, the breakdown voltage and leakage current of the 16x16 will be measured, checking also for the presence of bad pads
    - All the above parameters can be extracted from a total IV (256 pads + guard-ring grounded)
  - Qualified sensors will be grouped based on their gain layer doping and will be used in the further steps
    - Grouping based on CV tests performed during the PQC on single LGADs
- After post-processing, a fraction of diced sensors will be re-tested at the testing sites → QA/QC procedures for this step to be finalized soon!

**Thank You!** 





#### **Test array**

- The test arrays will also include structures for the QA/QC at the testing sites (*not covered in this talk*) :
  - $\circ~$  1x2 LGAD array: inter-pad width (TCT)
  - $\circ~$  LGAD-PiN pair: gain curve (TCT) and charge/timing performance
- Only a small fraction of the test arrays (<1%) will be tested
- A subset will be sent to irradiation and re-tested afterwards







#### **SQC** Parameter 1: VBD $\rightarrow$ an example





- VBD as measured by different k thresholds
- k = 15, 20, 25
- VBD goes from ~275 V (k=15) to ~ 295 V (k=25)



## **Micro-discharges**





- In LGAD arrays with a correct design of the inter-pad region, micro-discharges are observed a few Volts before breakdown
- Sensors cannot be reliably operated when the micro-discharges show up



#### Effect of a bad pad in a 16x16

- In this test, we measured the total current, the guard-ring (GR) and the 16 pads of a column, one of which is bad
- The total current is determined by the bad pad, while good pads have the expected IV
- This sensor shows very high current much before  $V_{MaxOp}$  and early BD  $\rightarrow$  would be rejected







VGL will be measured on the single LGAD with a standard method: intercept of two linear fits on the 1/C<sup>2</sup> curve





#### VGL-CV on-wafer - global



- Relative uncertainty on the VGL extraction method,  $\sigma/\mu = 0.02\%$
- This result was achieved by measuring many times the pads of a single 16x16 LGAD, to rule out the contribution from doping non-uniformity





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- Relative uncertainty on the VGL extraction method,  $\sigma/\mu = 0.02\%$
- This result was achieved by measuring many times the pads of a single 16x16 LGAD, to rule out the contribution from doping non-uniformity
- Given its very low relative uncertainty, this method allows distinguishing sensors with a 1-2% doping difference
- By performing a CV on the test structures, we can group the 16x16 based on their doping