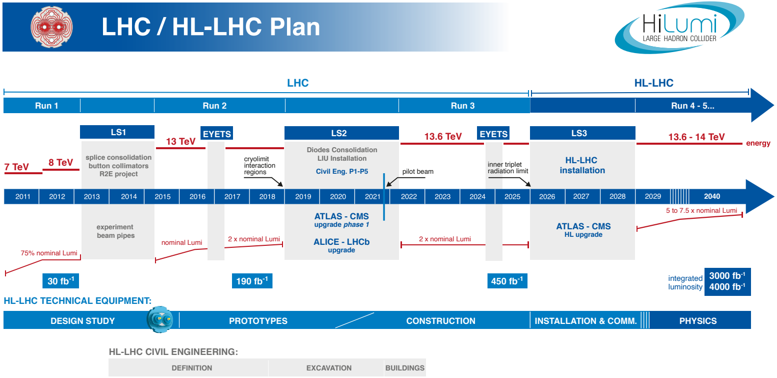
ATLAS ITk Pixel Detector Overview

Silke Möbius on behalf of the ATLAS ITk Pixel Collaboration
University of Bern- Laboratory for High Energy Physics

2024-02-20
TREDI 2024, Torino

High Luminosity LHC upgrade

- LHC and LHC experiments are currently running in Run 3
- HL-LHC period will start in 2029 and is supposed to accumulate $\int Ldt \approx 4000\,\mathrm{fb}^{-1}$

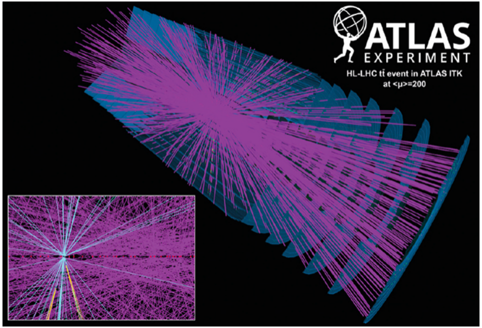


https://hilumilhc.web.cern.ch/content/hl-lhc-project

High Luminosity LHC upgrade

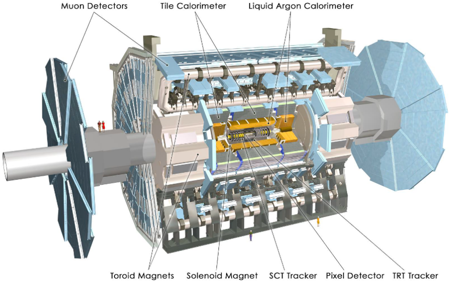
Upgrade to enhance physics reach: higher luminosity (L) and energy (E) → HL-LHC

	LHC	HL-LHC (2026)
E	7 - 13.6 TeV	14 TeV
L	$2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$	$7.5 \times 10^{34}\,\mathrm{cm}^{2}\mathrm{s}^{-1}$
pile-up $< \mu >$	≈ 50	≈ 200



https://twiki.cern.ch/twiki/bin/view/AtlasPublic/UpgradeEventDisplays

Present Inner Detector pixel technology cannot cope with HL-LHC challenges

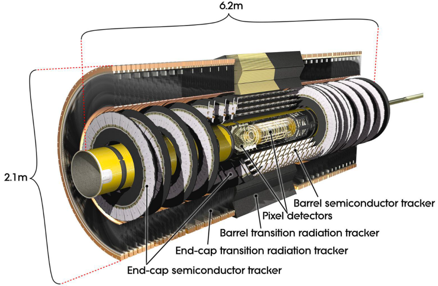


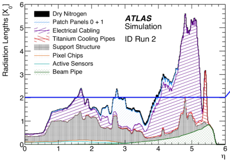
⇒ Replacement of detectors of the experiments to

- have higher granularity
- have higher bandwidth
- be $4 - 10\times$ radiation harder

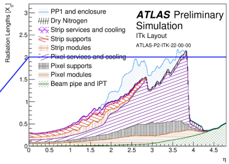
Tracker Upgrade

Upgrade of current ATLAS Inner Detector



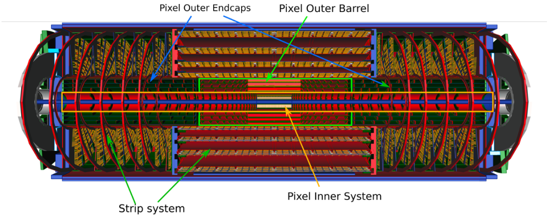


CERN-LHCC-2017-021



ATL-PHYS-PUB-2021-024

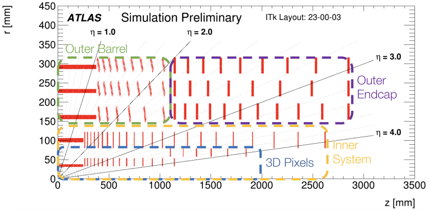
to all-silicon Inner Tracker (ITk) ATL-PHYS-PUB-2021-024



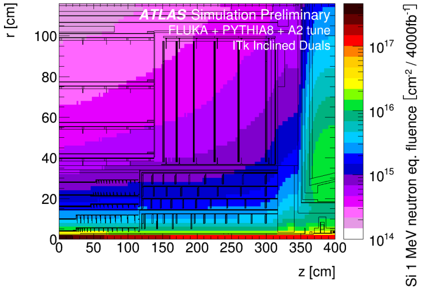
	ID Pixel	ITk Pixel
# pixels	92 M	1.4 G
# modules	≈ 2000	≈ 19400
Active area	$1.9\,\mathrm{m}^2$	$13\,\mathrm{m}^2$
η	2.5	4.0

- Increased granularity to maintain occupancy $< 1\%$
- Low mass mechanics, cooling and serial powering
- Increased radiation hardness up to $2 \times 10^{16}\,\mathrm{n/cm}^{-2}$

ATLAS ITk Pixel Detector



ATL-PHYS-PUB-2021-024



ATLAS Public Radiation Simulation

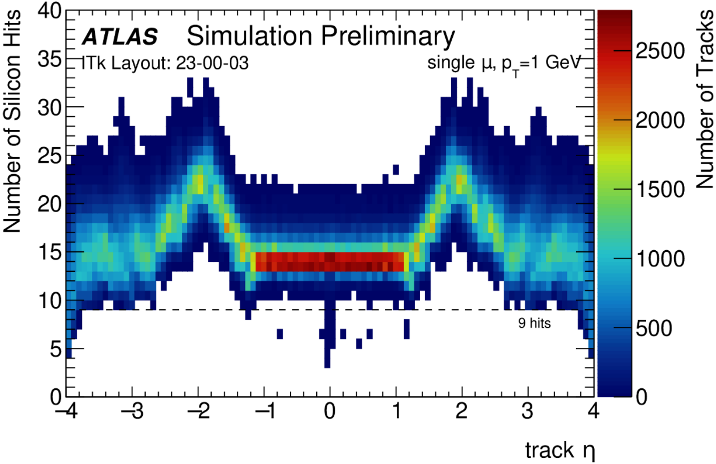
- Outer Barrel:
  - 3 layers of flat staves and inclined rings
  - n-in-p planar quad modules, 6.94 m^2 active area
  - 2.3×10^{15} n/cm^{-2}, 1.7 MGy @ 4000 fb^{-1}
- Outer End Cap
  - 3 layers of rings
  - n-in-p planar quad modules, 3.64 m^2 active area
  - 3.1×10^{15} n/cm^{-2}, 3.5 MGy @ 4000 fb^{-1}

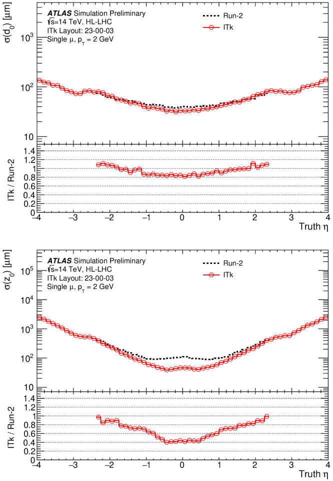
→ in total 7116 modules with 150 µm sensor and ASIC

- Inner System (Replacable)
  - 2 layers of flat staves and rings
  - L0: 3D single modules
    and L1: n-in-p thin planar quad modules
  - 2600 modules, 2.4 m^2 active area
  - 9.2×10^{15} n/cm^{-2}, 7.3 MGy @ 2000 fb^{-1}

ATLAS ITk Pixel Detector Performance

There will be at least nine hits per track



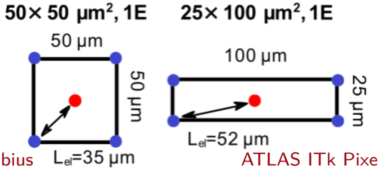


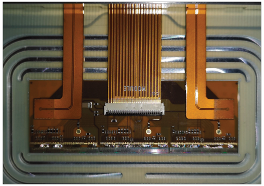
All plots: ATL-PHYS-PUB-2021-024

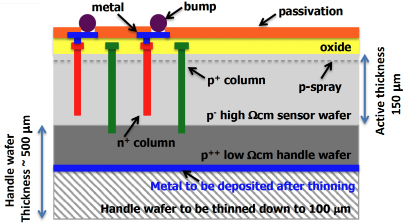
ITk Pixel 3D Sensors

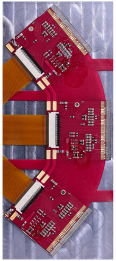
- 3D sensors are used in L0 (FBK, SINTEF, CNM)
- 150 µm thickness
- Radiation hard to $\approx 10^{16}\,\mathrm{n/cm^{-2}}$
- Operating voltage $< 250\,\mathrm{V}$
- $> 97\,\%$ hit efficiency at end of life
- $25 \times 100\,\mu\mathrm{m}^2$ pixel size in L0 barrel, $50 \times 50\,\mu\mathrm{m}^2$ pixel size for L0 rings

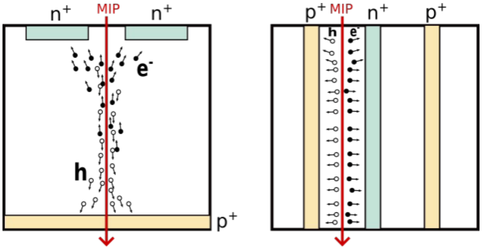
See dedicated talk of Martina Ressegotti tomorrow at 5:15 pm







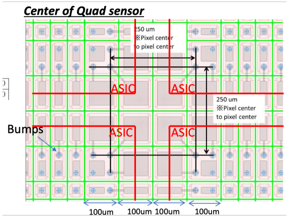


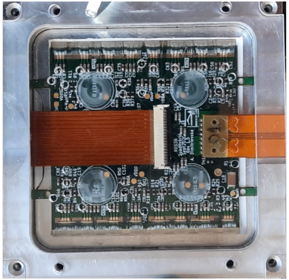


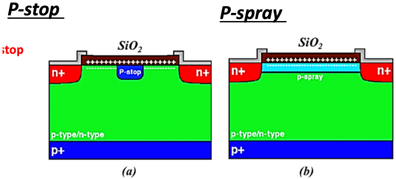
ITk Pixel Planar Sensors

- Thin planar sensors in L1 (100 µm thickness)
- Thick planar sensors in L2-L4 (150 µm thickness)
- Radiation hard to $\approx 3.1 \times 10^{15}\,\mathrm{n/cm^{-2}}$
- Dies of $4 \times 4\,\mathrm{cm}^2$ for quad modules
- Bias voltage up to 600 V (at end of life)
- $> 97\,\%$ hit efficiency at end of life
- $50 \times 50\,\mu\mathrm{m}^2$ pixel size
- Various design details left up to vendor:
  - p-stop vs p-spray insulation
  - Polysilicon bias or punch-through
  - Guard-ring geometry

⇒ Requirements defined on performance



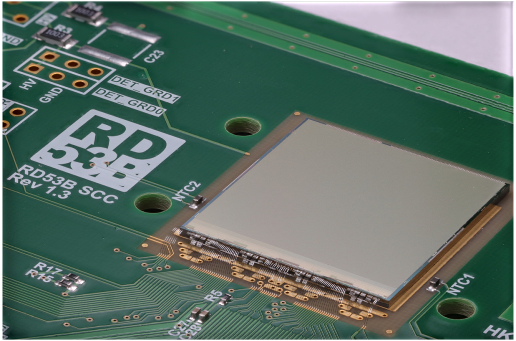




FE-chip ITkPixV2

All pixels read out with same ASIC ITkPix (ATLAS flavour of common RD53 ATLAS-CMS ASIC):

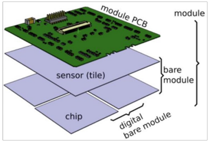
- 152800 pixels per chip (384 rows, 400 columns)
- 65 nm technology, $50 \times 50\,\mu\mathrm{m}^2$, total area $2 \times 2\,\mathrm{cm}^2$
- Power: $0.56\,\mathrm{W/cm}^2$
- 4 data links per chip at 1.28 Gbps
- Threshold: 1000 e, noise: 40 e
- Digital readout with Time over Threshold = ToT
- Column readout, data encoding
- Shunt Low Drop Output regulators (I = const.)
- 40 MHz clock with 780 ps phase adjustment
- Data merging: FE readout via another FE

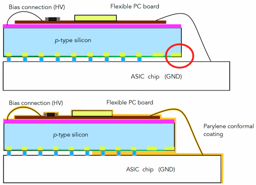


https://cds.cern.ch/record/2771271

Modules

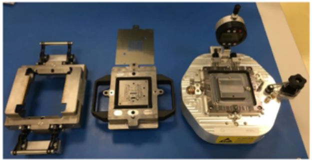
- Hybridisation → low pitch bump bonding $50 \times 50\,\mu\text{m}^2$
- Wire bond protection by CFRP roof and HV protection with Parylene coating
- Module assembly (gluing of flex PCB to bare module) with 100 µm precision, using stencil + precision tools, curing of glue (Araldite) at room temperature
- Large temperature range: operating at −25 °C to −10 °C, warmed up to 20 °C during maintenance → thin metal flex circuit to avoid delamination of bumps

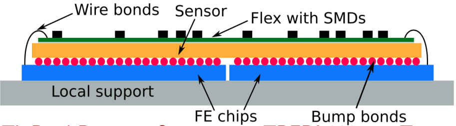




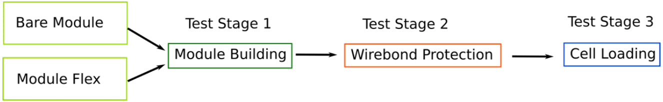
Japanese Tooling

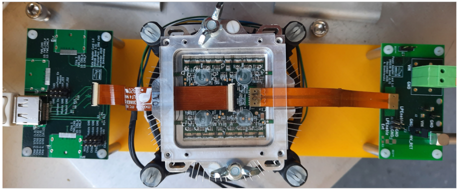
Göttingen and Bern v2 tooling





Module Electrical Testing





QC process for all modules to catch low quality modules:

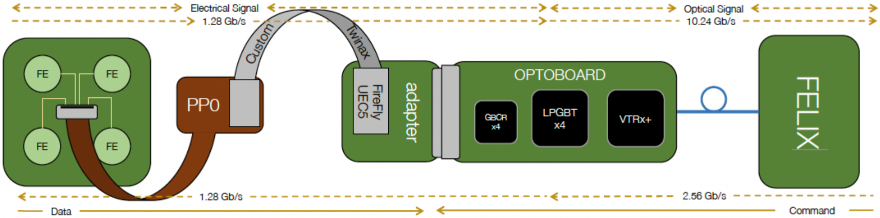
- x-ray images of flip-chip assemblies
- Sensor IV at several stages: on wafer, after flip-chip, after assembly, after thermal cycles
- Electrical tests and disconnected bump tests: as assembled (weak bonds), after thermal cycles (defects induced by thermal stress (delamination))
- Cold test at operating temperature ($-15\,^{\circ}$C)
- Burn-in for 48 h at room temperature ($20\,^{\circ}$C) on module: look for sensor and chip early failure

⇒ 3 categories of tests:

- Test of module quality;
- Check that module still functional after process step
- Module characterization and final working point setup

Data Transmission

- Readout of FE-chip at 1.28 Gbps with up to 4 links per chip depending on position in system
- Uplink sharing on module used on all layers to reduce material, sharing of downlinks
- Up to 6 data links per lpGBT from 1-6 modules sharing one 10.24 Gbps fibre, downlink 2.56 Gbps per lpGBT
- Custom low-mass 34AWG twinax cable for transmission from detector to optoboxes, up to 6 m
- Losses below 20 dB from FE-chip to GBCR including connectors, flexes and cable
- Signal recovered on Optoboard in Optobox by GBCR
- Aggregation of electrical signals and electro-optical conversion by lpGBTx and VTRx+
- Optical fibres to readout PCs with FELIX boards PRR Oct. 2024



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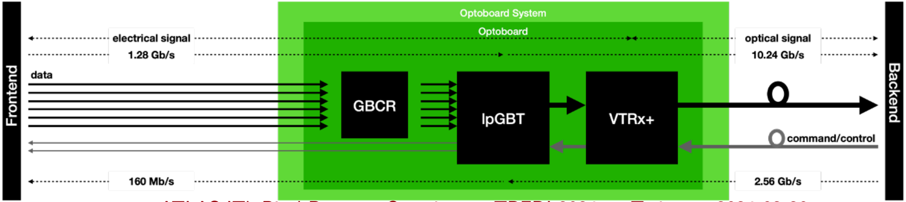
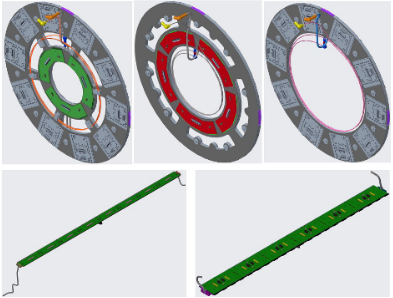
PRR Oct. 2024



Loaded Local supports

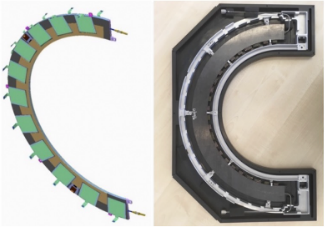
- Local support prototypes with carbon fibre and carbon foam to minimize mass and maximize thermal performance
- Different geometries dependent on the layers and regions of the pixel detectors:
  - Inner system: two layers of staves and double-sided rings in the endcaps
  - Outer Barrel: three layers of longerons and inclined half-rings
  - Outer Endcap: three layers of endcap rings composed by 2 half-rings (HR)

Inner System



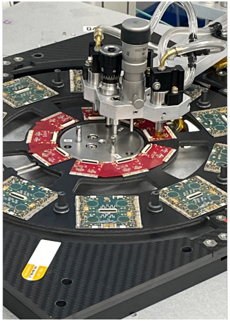
Outer Barrel

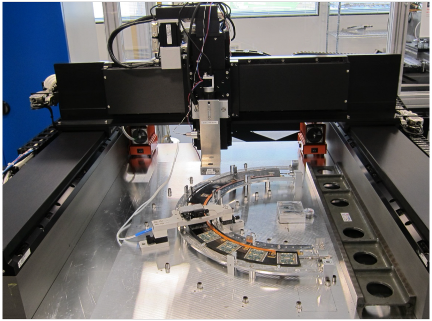
Outer Endcap

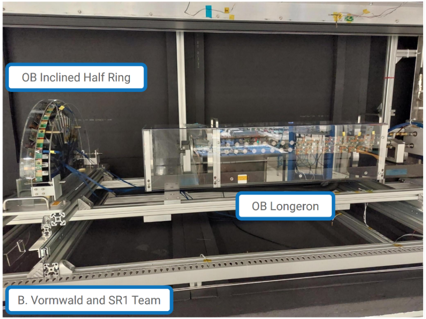


System Test Setups

- Multiple System Test Setups at different institutes
- Loaded Local support tests: 5 OB sites, 4 EC sites, 1 IS site
- Each site gets one loaded local support and an Optobox with up to 4 Optoboards
- Currently demonstrator setups in use

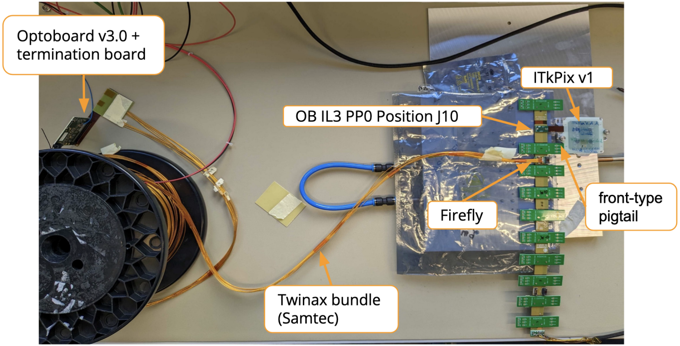






B. Vormwald and SR1 Team

Outer Barrel IL3 PP0 - Setup at Bern



Optoboard v3.0 + termination board

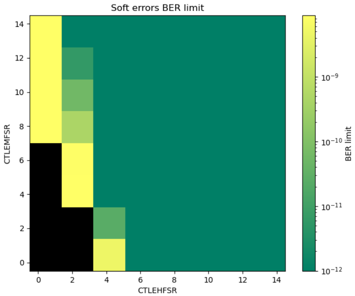
ITkPix v1

OB IL3 PP0 Position J10

Firefly

front-type pigtail

Twinax bundle (Samtec)



BER tests with 95% CL BER limit $< 10^{-12}$ for varying GBCR equaliser settings, using 64b/66b ITkPix idle signal

- Almost final Optoboard and ITkPix pre-production module
- Manually assembled 6 m long twinax bundle (10 cables) with off the shelf connector (firefly) and termination board

Conclusions

- ITk will have increased acceptance up to $\eta \approx 4$ and more than 9 hits per track with high granularity and radiation hardness
- ITk Pixel project is now moving into production and pre-production
- Production of $\approx$ 9000 modules will start this year (over 2 years in 20 assembly sites)

Next steps:

- Qualify 20-25 sites for production ongoing
- Set up and commission the system tests at local support level
- Integration at CERN of all subsystems
- Demonstrate to be able to produce on time all the required modules
- Demonstrate to be able to correctly place on local supports, connect and test
- Create a culture of consistent quality check in a distributed production model

Thank you for your attention.