The MONOLITH project: towards **picosecond timing** with monolithic silicon

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UNIVERSITÉ DE GENÈVE

Swiss National Science Foundation

European Research Council
Established by the European Commission

The MONOLITH Project

Funded by the H2020 ERC Advanced grant 884447,
July 2020 - June 2025

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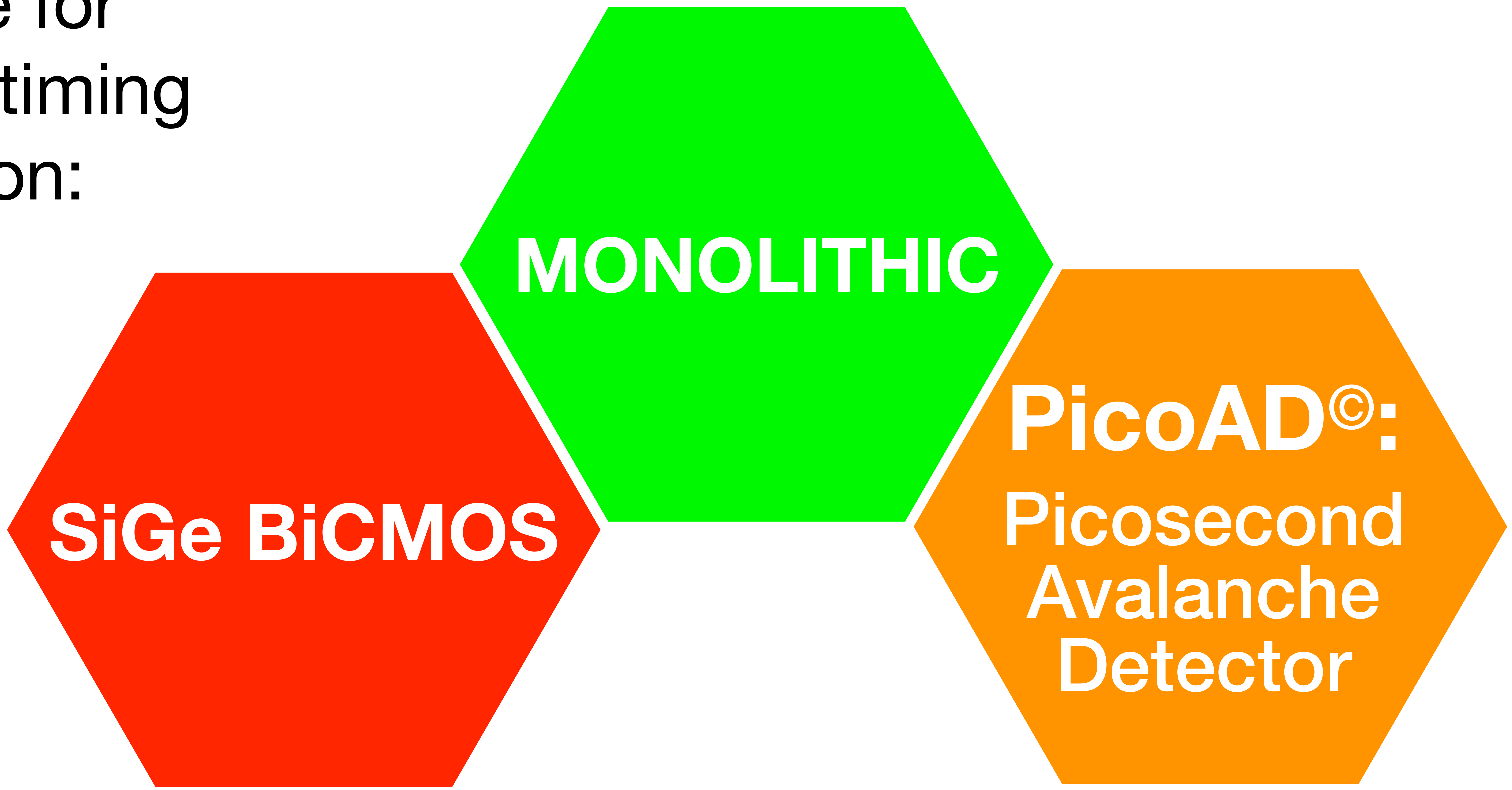
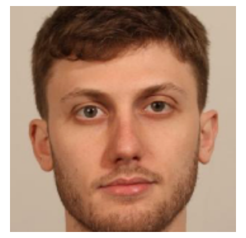
Our recipe for picosecond timing with silicon:



The UniGe Silicon Team

Giuseppe Iacobucci
- project P.I.

Thanushan Kugathasan
- Lead ASIC design
- Analog electronics

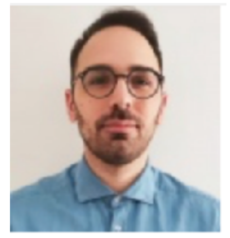


Leonardo Cecconi
- ASIC design
- Digital electronics

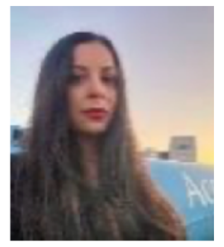
Stefano Zambito
- Laboratory tests
- Data analysis

Jordi Sabater Iglesias
- Detector simulation
- Laboratory tests

Matteo Milanesio
- Laboratory tests
- Data analysis



Antonio Picardi
- ASIC design
- Analog electronics

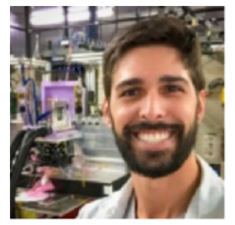


Rafaella Kotitsa
- Sensor simulation
- Data analysis

Carlo Alberto Fenoglio
- Digital electronics
- ASIC test

Lorenzo Paolozzi
- Sensor design
- Analog electronics

Roberto Cardella
- Sensor design
- Analog/Dig electronics



Mateus Vicente
- System integration
- Laboratory tests

Chiara Magliocca
- Laboratory tests
- Data analysis

Théo Moretti
- Laboratory tests
- Data analysis

Jihad Saidi
- Laboratory tests
- Data analysis

Luca Iodice
- Analog electronics
- ASIC test

Andrea Pizarro Medina
- Data analysis
- Laboratory tests

Ivan Semendyaev
- Data analysis
- Laboratory tests

Didier Ferrere
- System integration
- Laboratory tests

Sergio Gonzalez-Sevilla
- System integration
- Laboratory tests

Yannick Favre
- Board design
- RO system

Stéphane Débieux
- Board design
- RO system

Main research partners:

Roberto Cardarelli
INFN Rome2 & UNIGE

Holger Rücker
IHP Mikroelektronik

Marzio Nessi
CERN & UNIGE

Matteo Elviretti
IHP Mikroelektronik

Funded by:

Swiss National Science Foundation

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Sinergia

ATTRACT

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The MONOLITH Project

European Research Council
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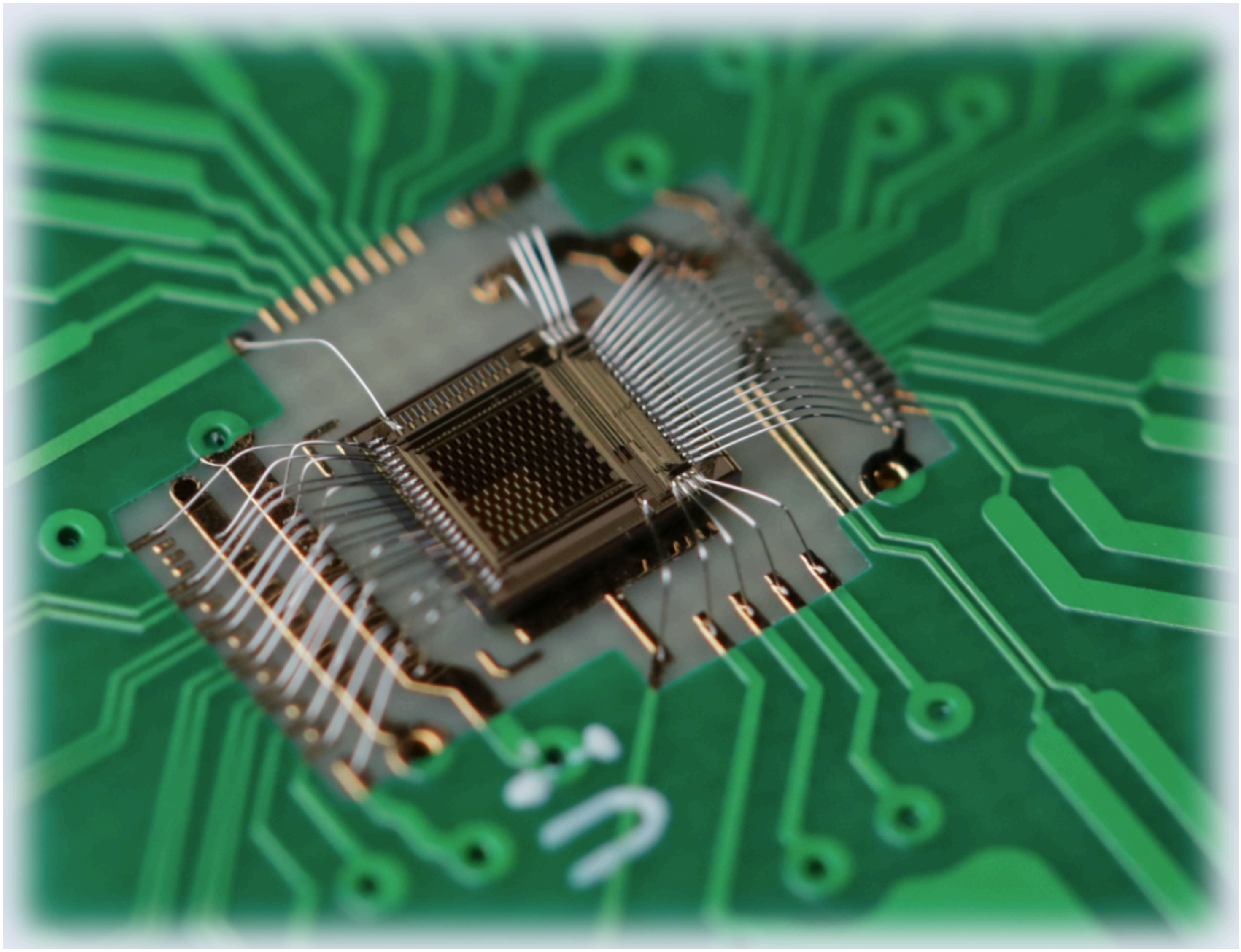
Selection of results that I will show today:

1. the **2022 prototype WITHOUT GAIN LAYER**,
   - testbeam **efficiency** and **time resolution** for proton irradiation up to **1×10^{16} 1MeV n_{eq}/cm^2**
     - ➡ *JINST* **18** P03047 (2023), *JINST* **19** P01014 (2024) + **preliminary results** presented here
   - time resolution vs. signal amplitude with a **femtosecond laser** to extract Landau noise
     - ➡ ArXiv:2401.01229 – accepted by JINST
2. the **PicoAD:** the **proof-of-concept**, and the **first batch of prototypes**
   - ➡ *JINST* **17** P10032 (2022), *JINST* **17** P10040 (2022) + **preliminary results** presented here

All ASICs were produced in the **130nm SiGe BiCMOS SG13G2** process by

ihp
innovations for high performance microelectronics
Leibniz-Institut für innovative Mikroelektronik



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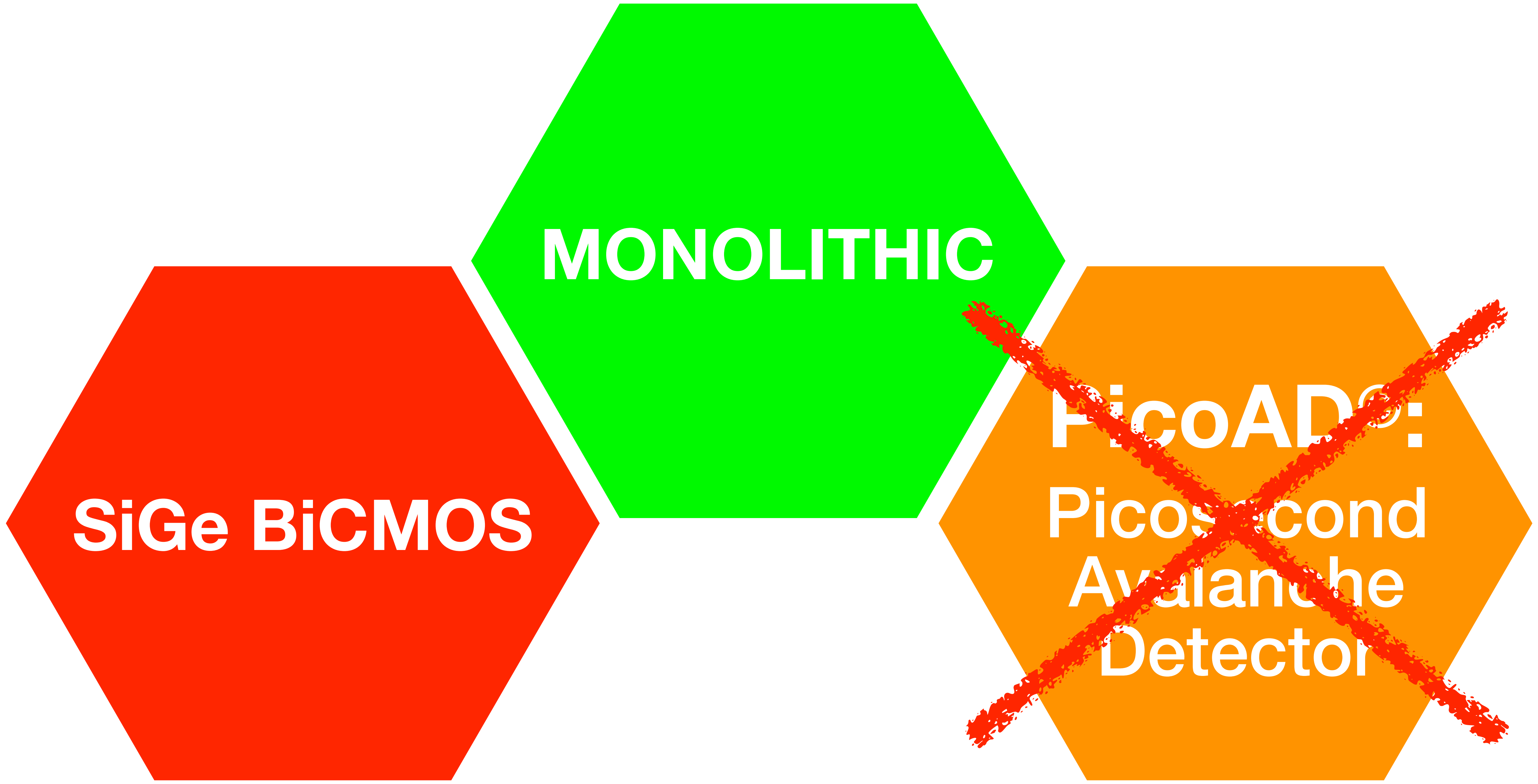
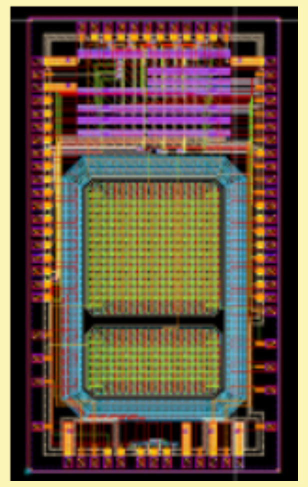
2022 prototype
no gain layer



MONOLITH Project prototypes

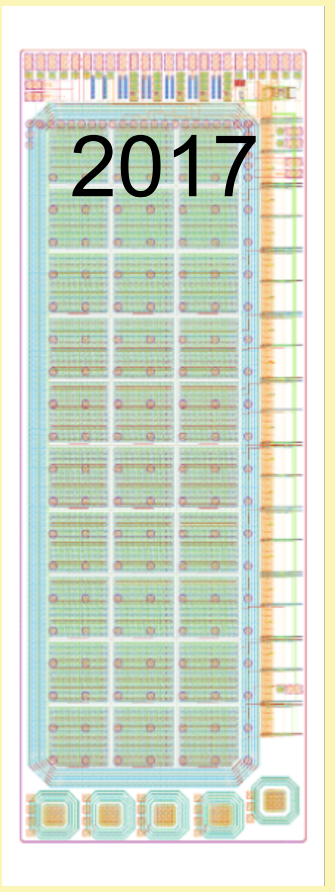
Monolithic prototypes in SiGe BiCMOS (without internal gain layer)

2016



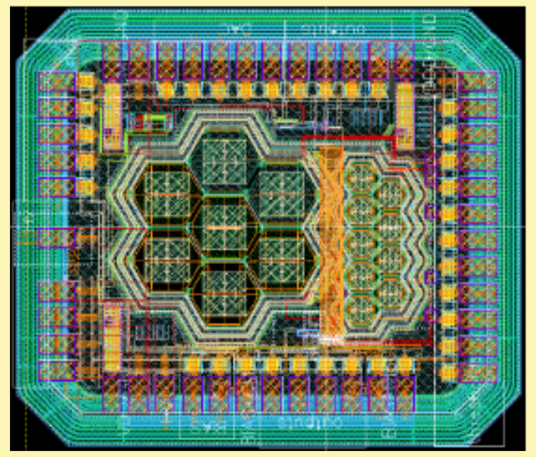
200ps
- 1 mm² pixel
- Discriminator

2017



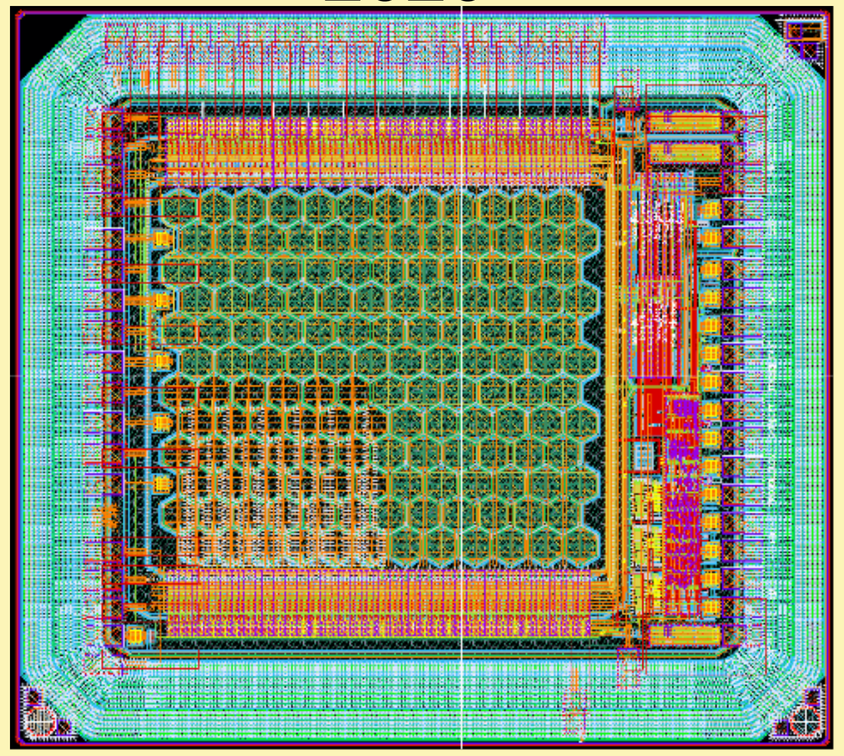
110ps
- 30 pixels 500x500μm²
- 100ps TDC +I/O logic

2018



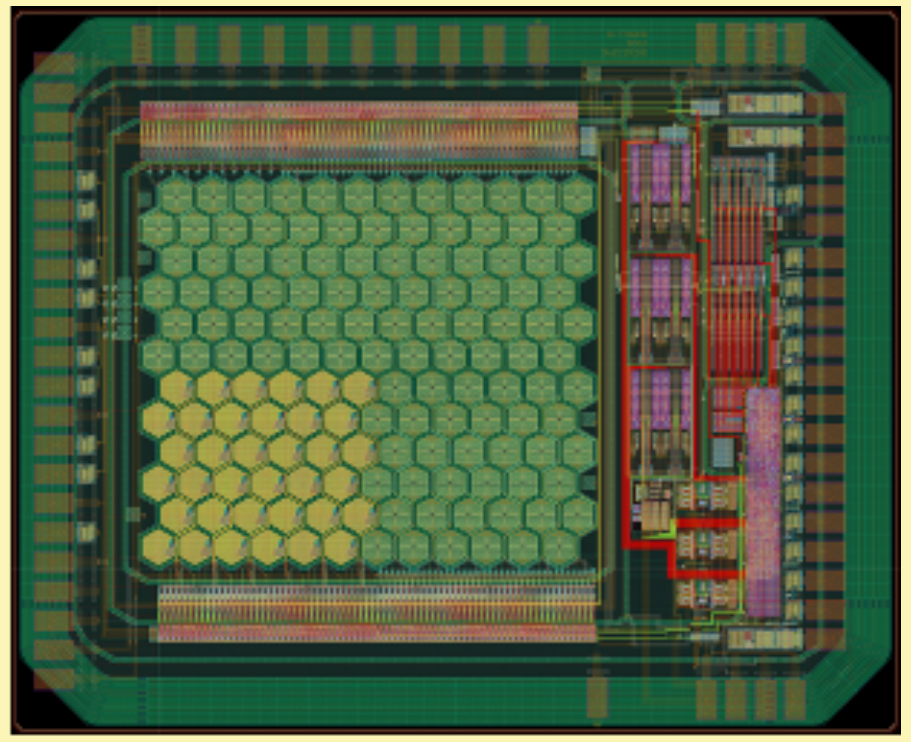
50ps
- Hexagonal pixels 100μm and 200μm pitch
- Discriminator output

MONOLITH prototype 1
2020



36 ps
- Hexagonal pixels 100μm pitch
- 30ps TDC + I/O logic
- 4 analog channels

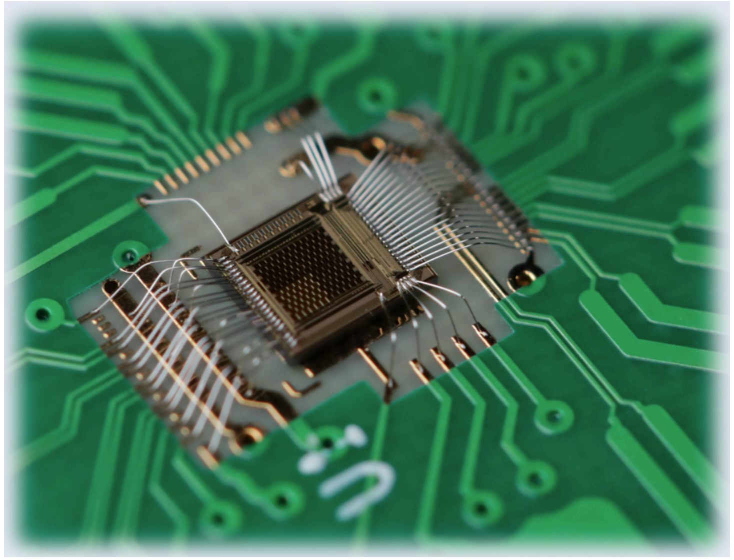
MONOLITH prototype 2
2022



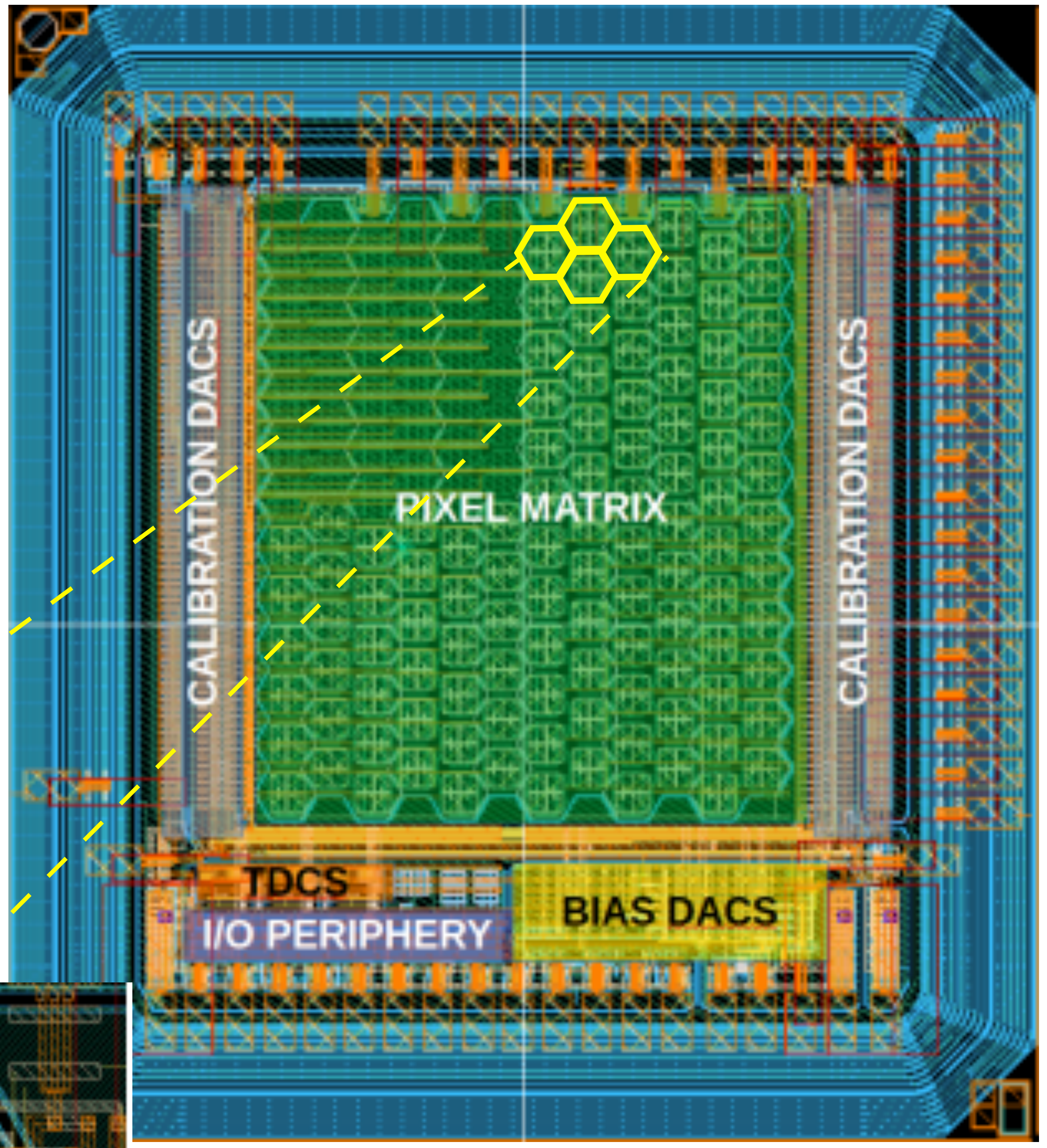
20 ps
- Evolution of 2020 prototype
- improved electronics
- 50μm epitaxial layer (350Ωcm)

evolution of 2020 prototype

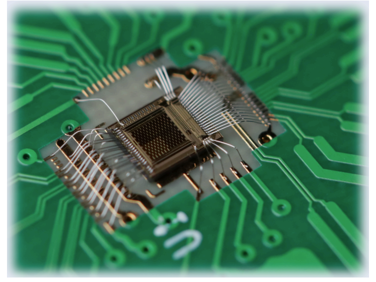
prototype2 — no gain layer



- Same matrix configuration as prototype1, but
  - **Substrate**: 50Ωcm → 350Ωcm epilayer, 50μm thick on low-res (1Ωcm)
    - ➡ smaller pixel capacitance
    - ➡ depletion 23μm → 50μm
    - ➡ larger voltage plateau
    - ➡ that allows operating sensor with v_{drift} saturated everywhere
  - **Preamp and driver voltage decoupled**
    - ➡ was limiting optimal amplifier operation
    - ➡ was creating cross-talk; removed
  - **Optimised FE layout**, **differential output**, high-frequency cables
    - ➡ better rise time (600ps → 300ps)

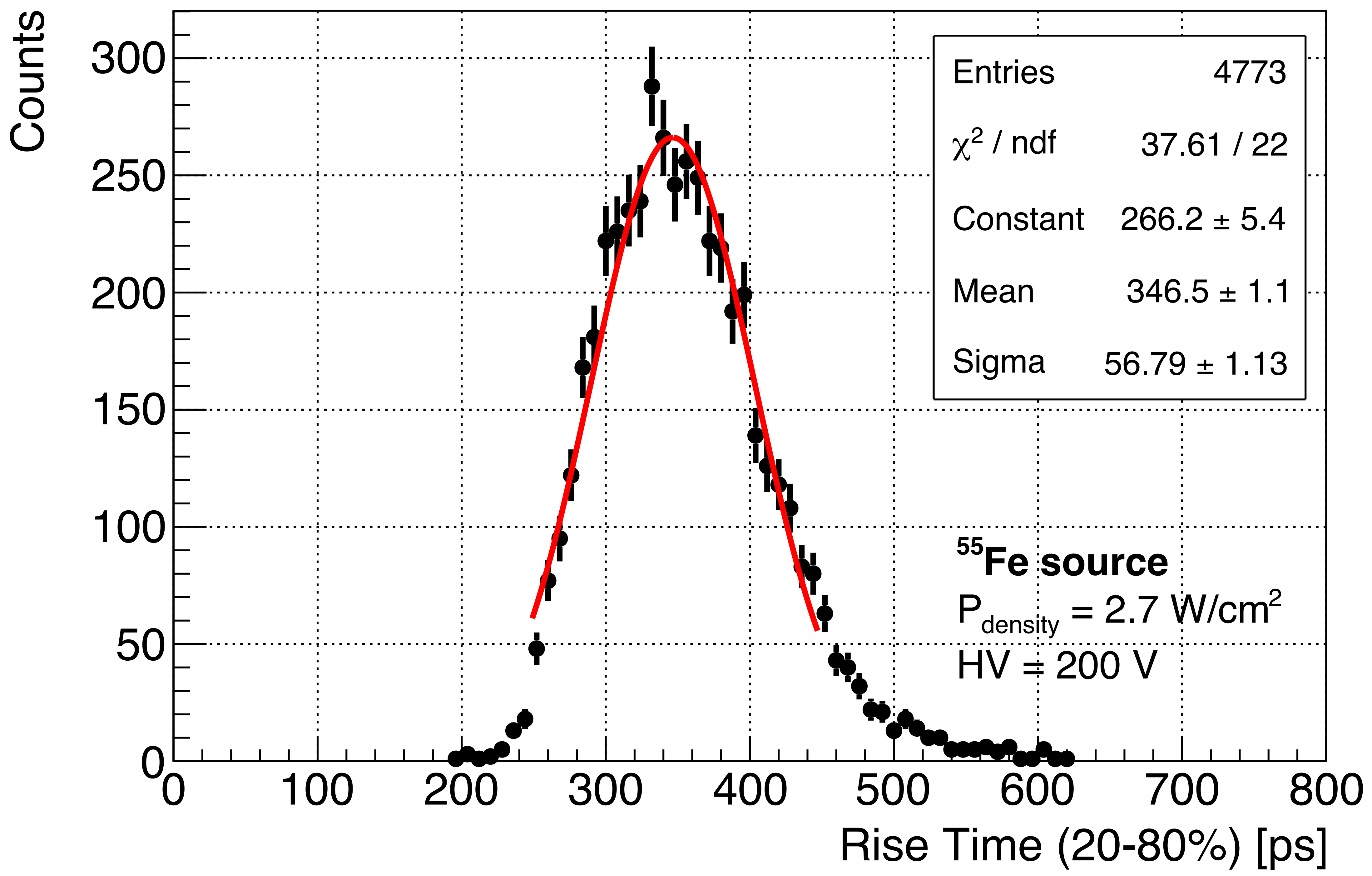


prototype2 — no gain layer

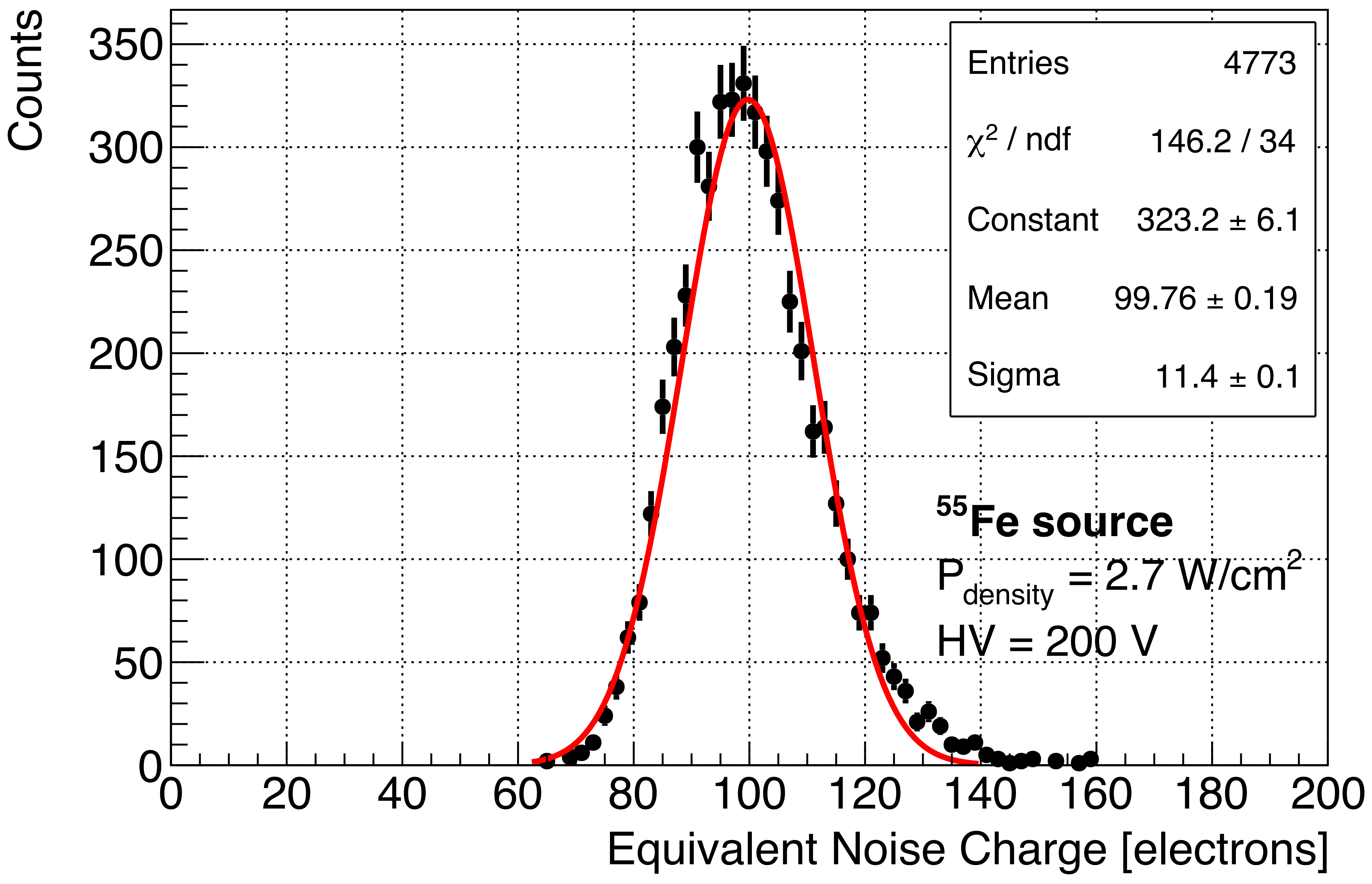


^{55}Fe measurements in cleanroom:

Risetime (20%–80%) ≈ 350 ps

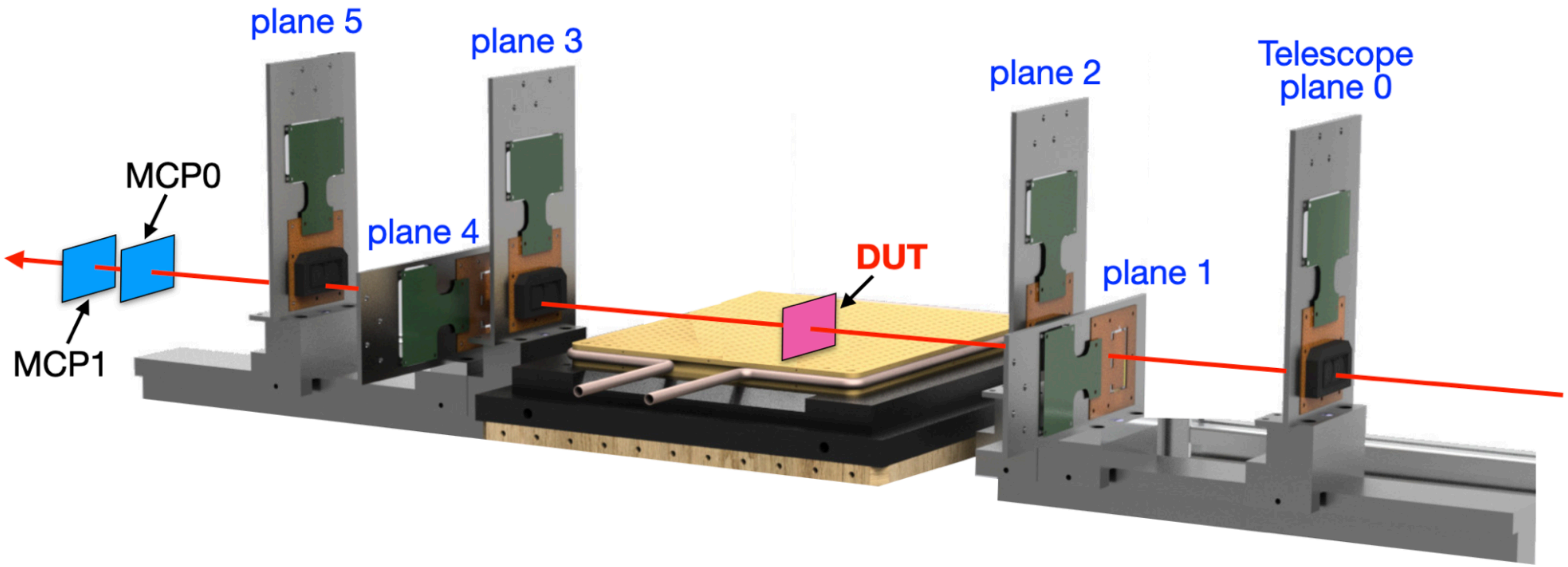


ENC ≈ 100 e⁻



Test Beam: Experimental Setup

SPS testbeam in 2023 with 120 GeV/c pions to measure **efficiency** and **time resolution**



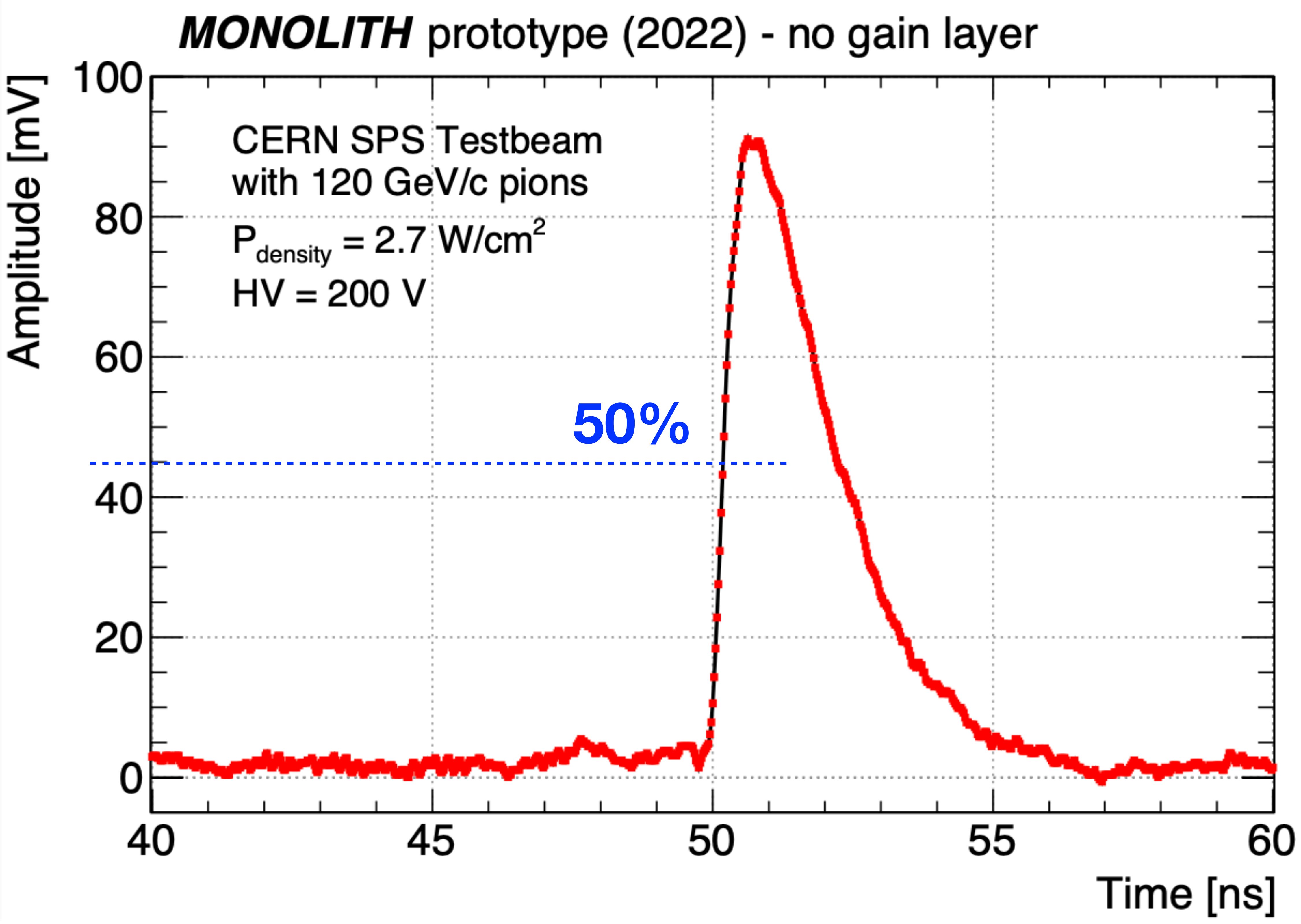
UNIGE FE-I4 telescope to provide spatial information ($\sigma_{x,y} \approx 10$ μm)

Two MCPs ($\sigma_t \approx 5$ ps) to provide the timing reference

Remark on the time resolution measurements

We performed a very simple analysis of the data taken with the **analog channels**:

1. **Linear interpolation** of oscilloscope samplings (25ps)
2. Time Of Arrival taken at **50% of signal height**
3. **No further time-walk correction applied**



Radiation hardness

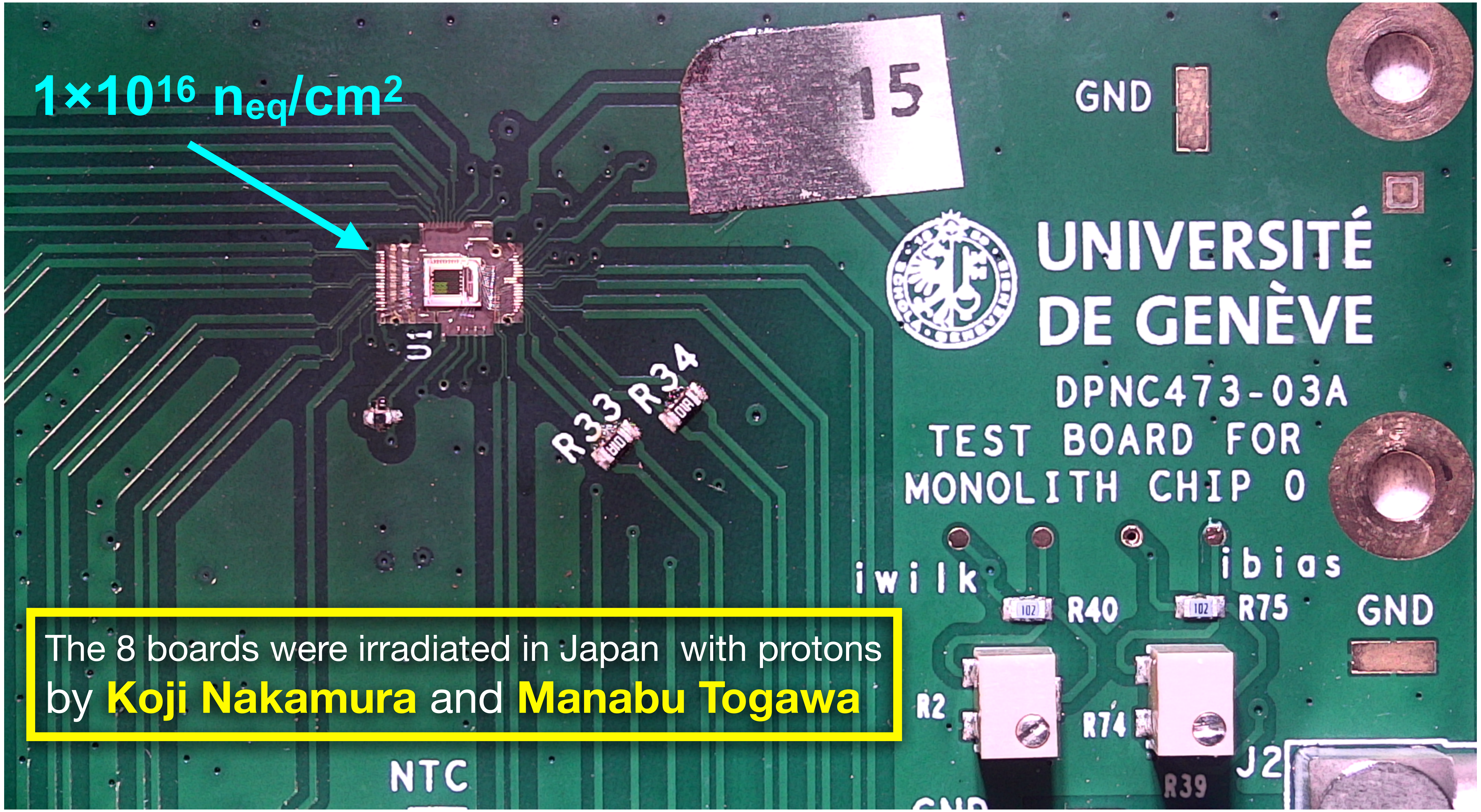
with the MONOLITH prototype2 **without gain**

Total of 40 analog pixels studied

Radiation hardness of SiGe HBTs

Radiation tolerance studies in collaboration with **KEK** and **IHP** colleagues.

8 samples of MONOLITH prototype2 were irradiated with protons in Japan **up to $1\times10^{16}\ n_{eq}/cm^2$**



The 8 boards were irradiated in Japan with protons by **Koji Nakamura** and **Manabu Togawa**

Radiation hardness of SiGe HBTs

Radiation tolerance studies in collaboration with **KEK** and **IHP** colleagues.

8 samples of MONOLITH prototype2 were irradiated with protons in Japan **up to 1×10^{16} n_{eq}/cm^2**

7 out of the 8 irradiated boards had **damaged voltage regulators**: **bypassed** with wire bonds

Three unirradiated boards. (CERN testbeam results already published in JINST 18 (2023) P03047)

Board Name	Fluence [1 MeV n_{eq}/cm^2]
M23	$2 \cdot 10^{13}$
M22	$9 \cdot 10^{13}$
M21	$6 \cdot 10^{14}$
M19	$6 \cdot 10^{14}$
M18	$3 \cdot 10^{15}$
M17	$3 \cdot 10^{15}$
M16	$1 \cdot 10^{16}$
M15	$1 \cdot 10^{16}$
M06	not irradiated – for comparison
M05	not irradiated – for comparison
M07	not irradiated – for comparison

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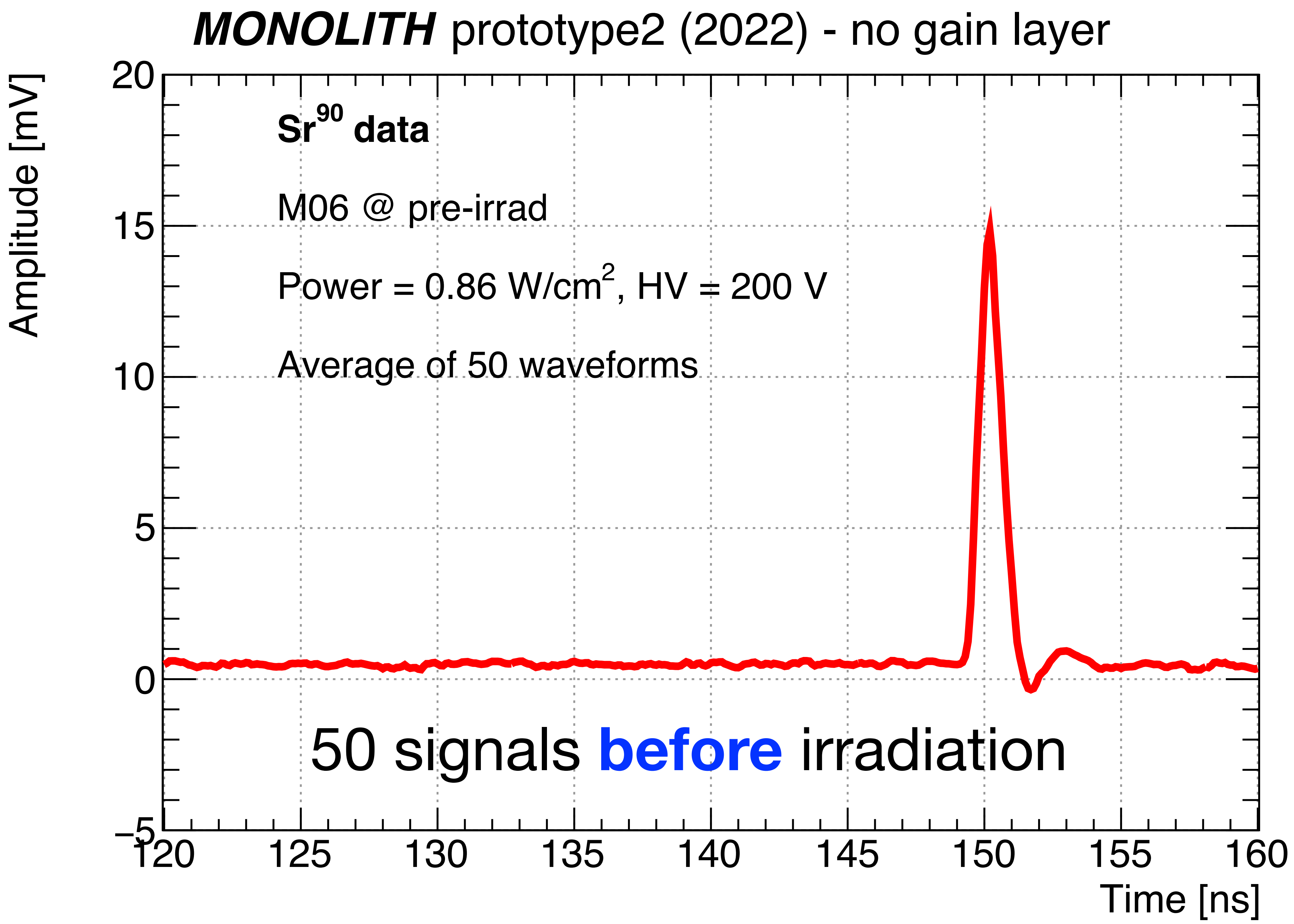
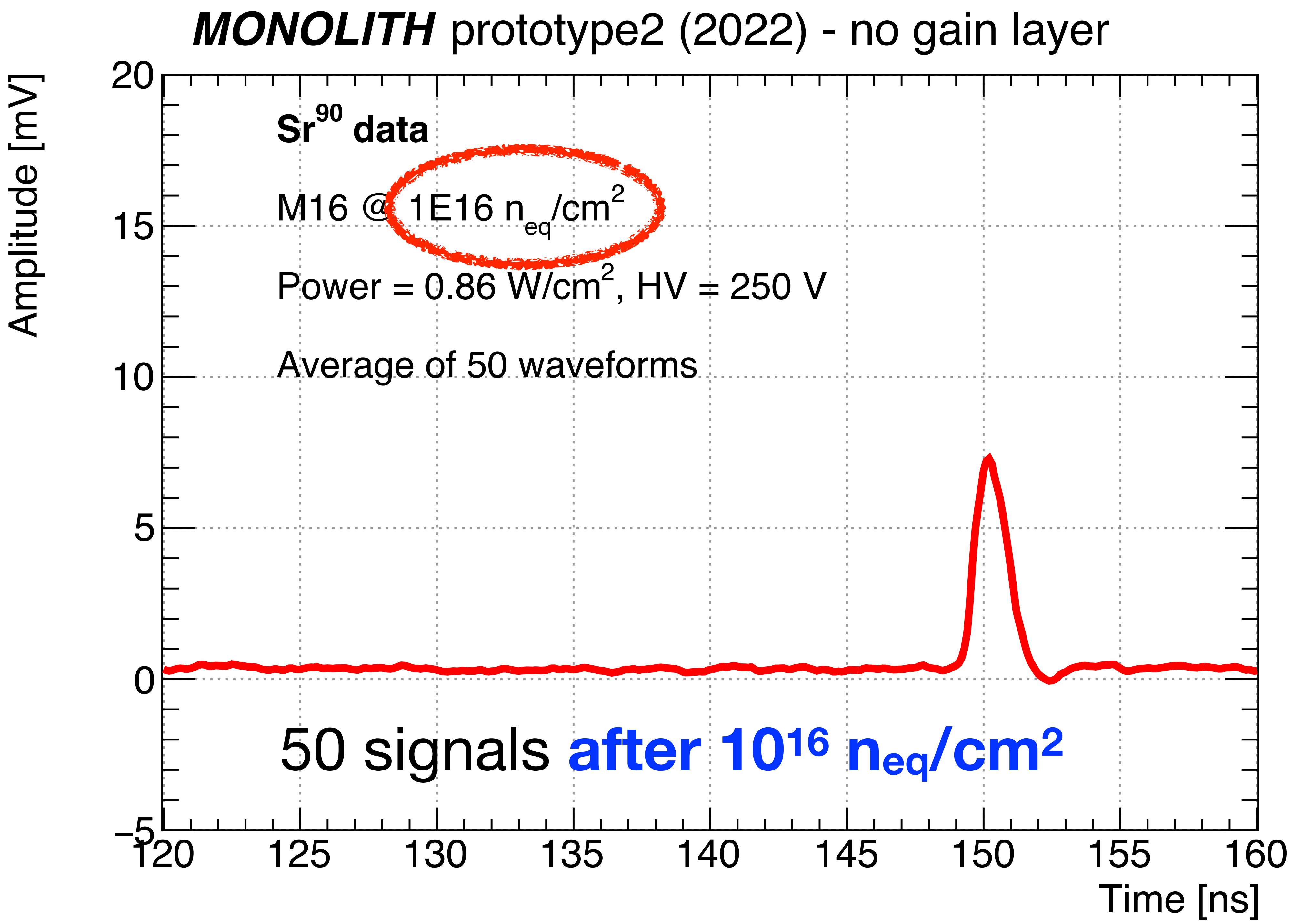
Very good news:
even after 1×10^{16} n_{eq}/cm^2 the ASICs work
although signals are clearly degraded



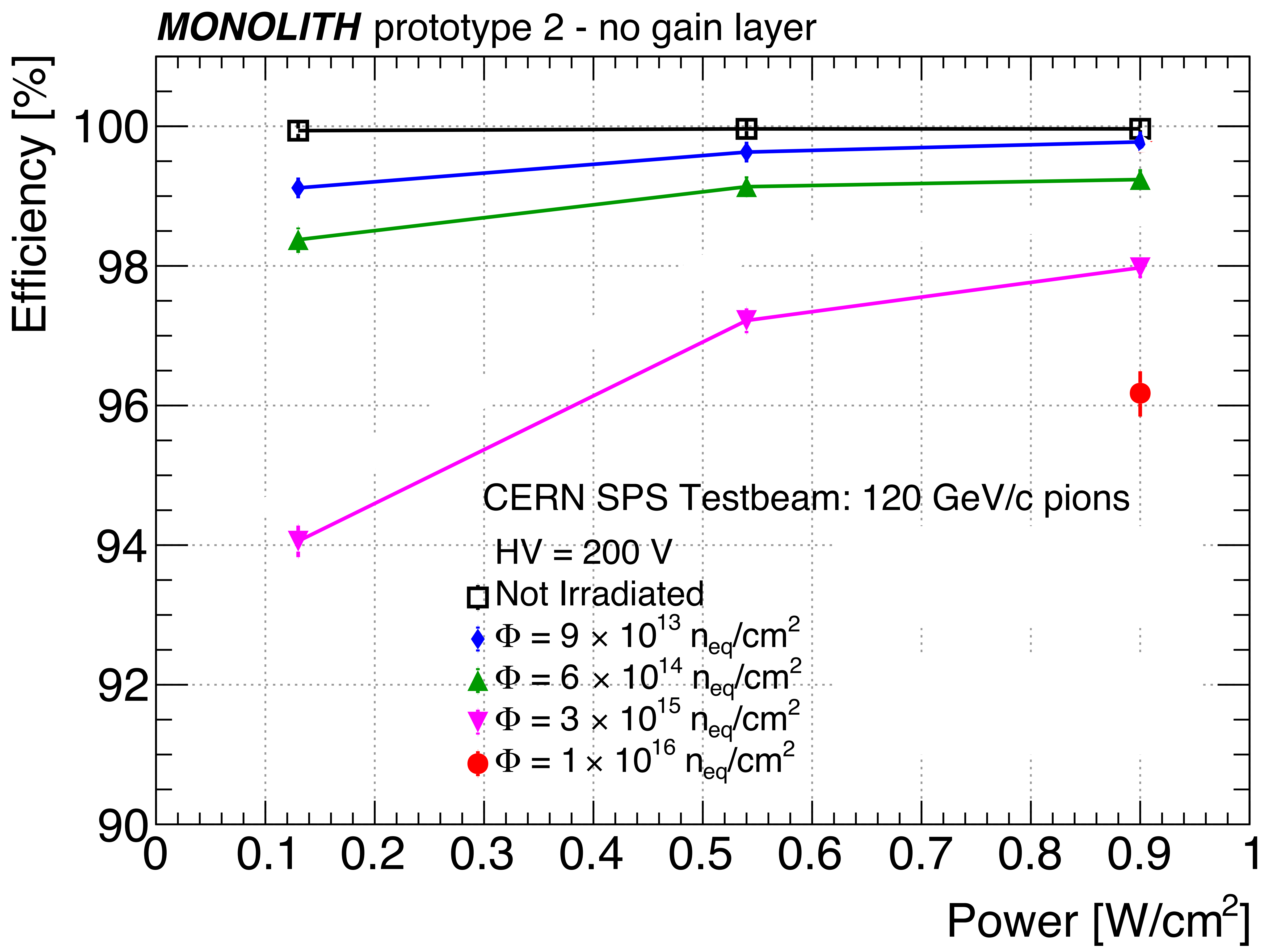
50 signals **before** irradiation



50 signals **after 10^{16} n_{eq}/cm^2**

Efficiency vs. power density

Preliminary

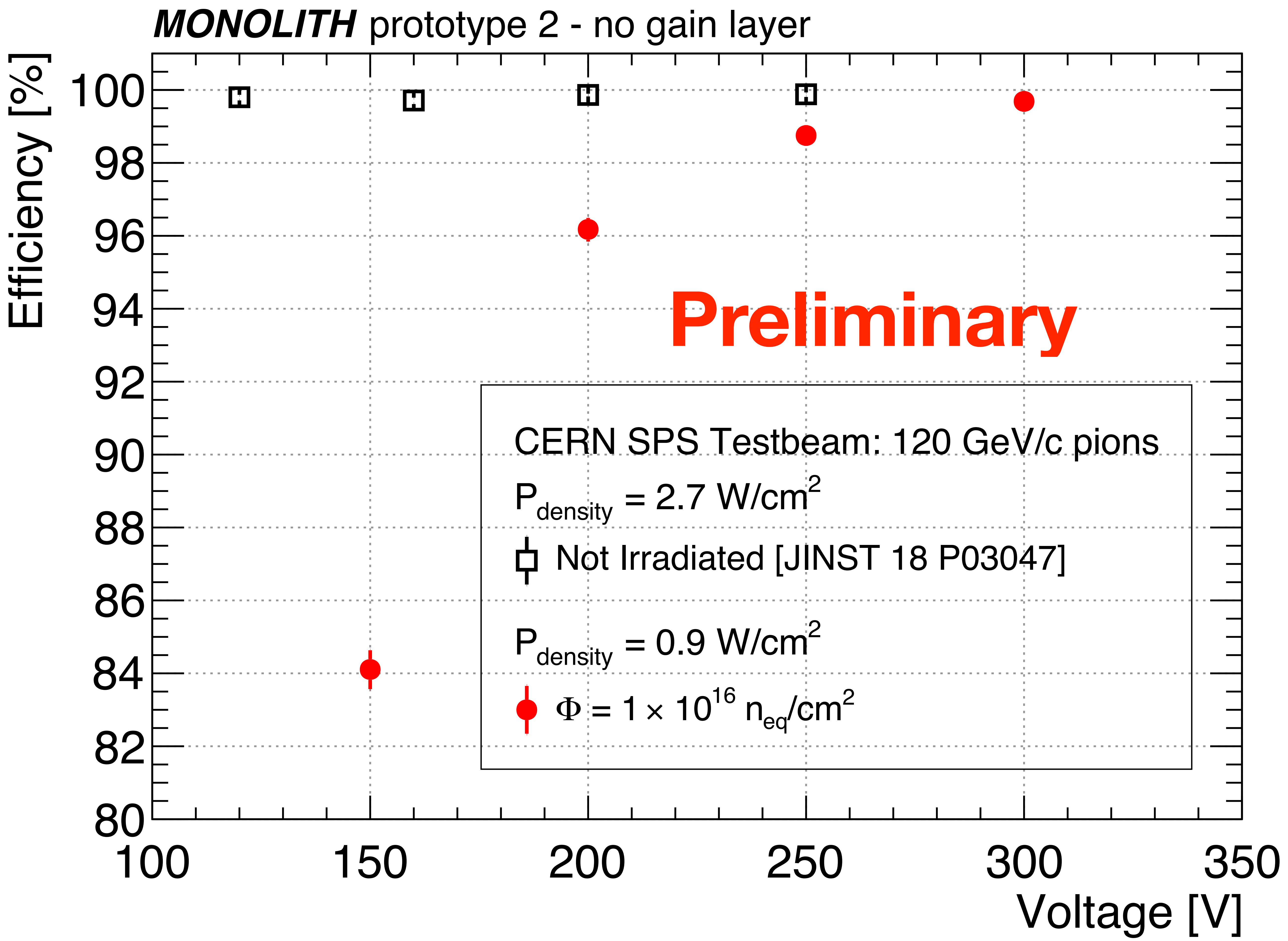


□ Unirradiated:

Efficiency = 99.9% at HV = 120V

● $1x10^{16}$ n_{eq}/cm^2:

Efficiency = 99.6% at HV = 300V
(higher HV still to be exploited)



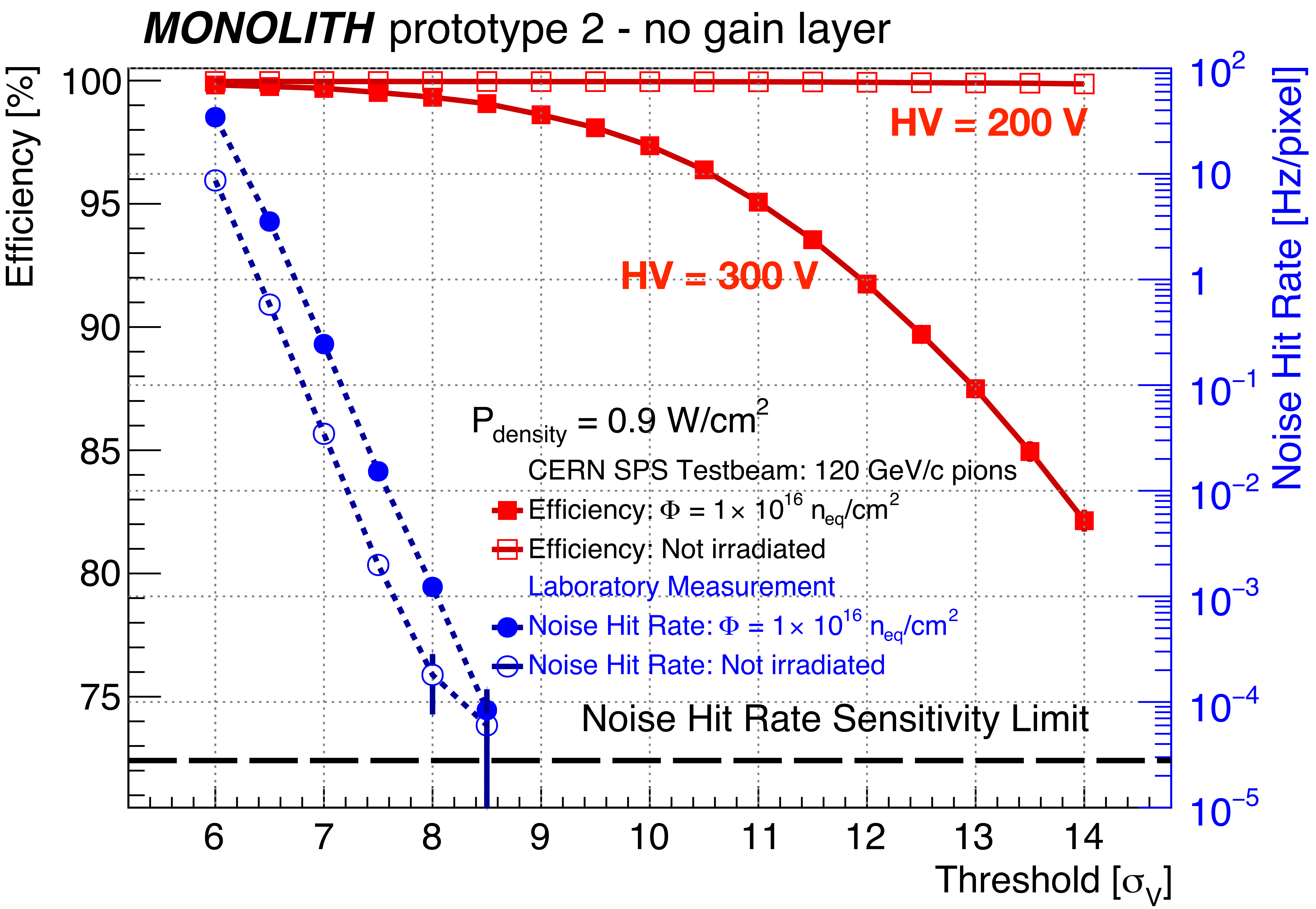
Efficiency and Noise Hit Rate

After 1×10^{16} n_{eq}/cm^2:

Efficiency = 99.6%
with a threshold at 7 σ_V

Noise Hit Rate
increases by a factor of 5

Preliminary



Time resolution vs. power density

Preliminary

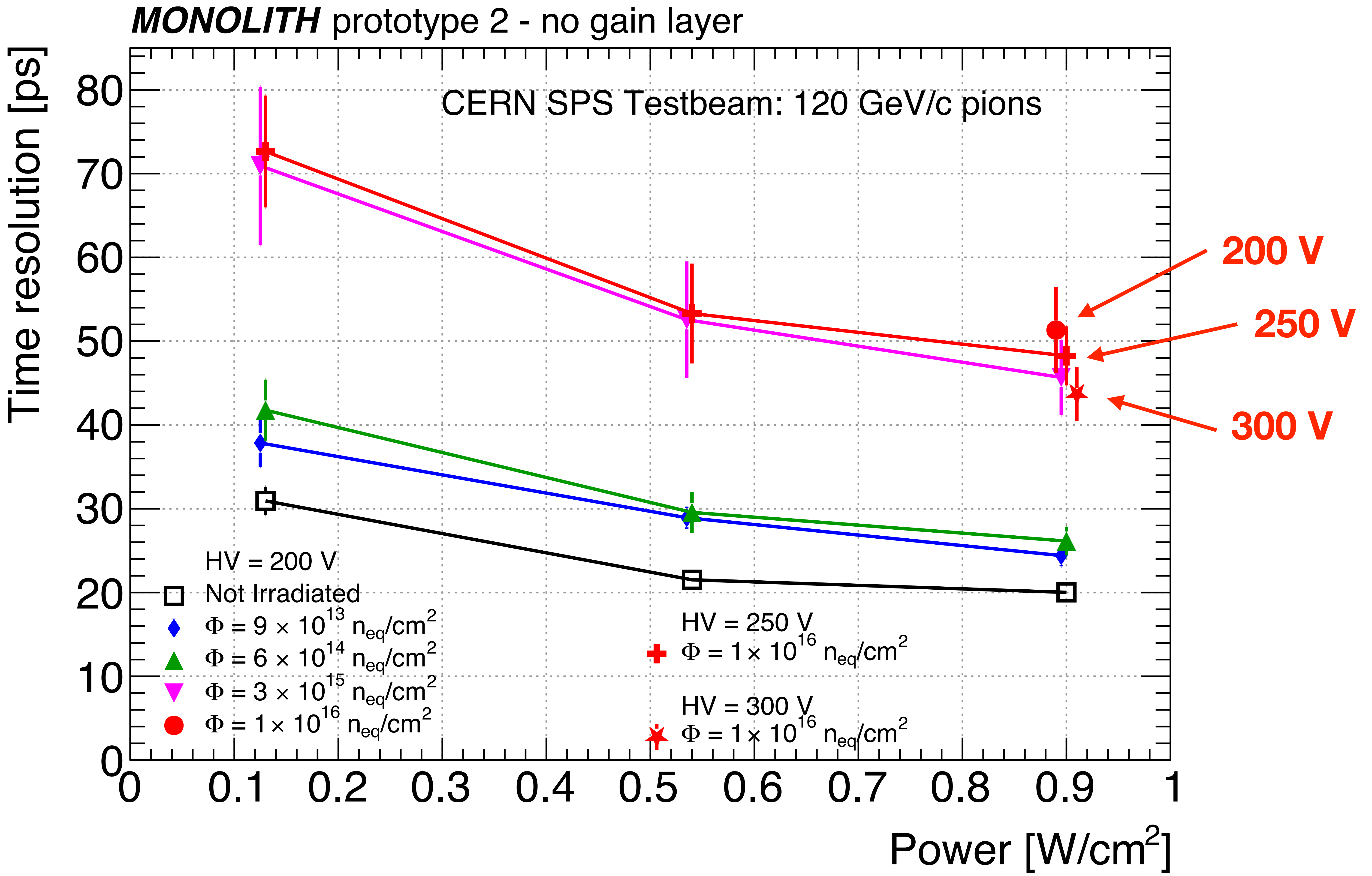
★ 1x10[16] n_{eq}/cm^2:

45 ps at 300 V

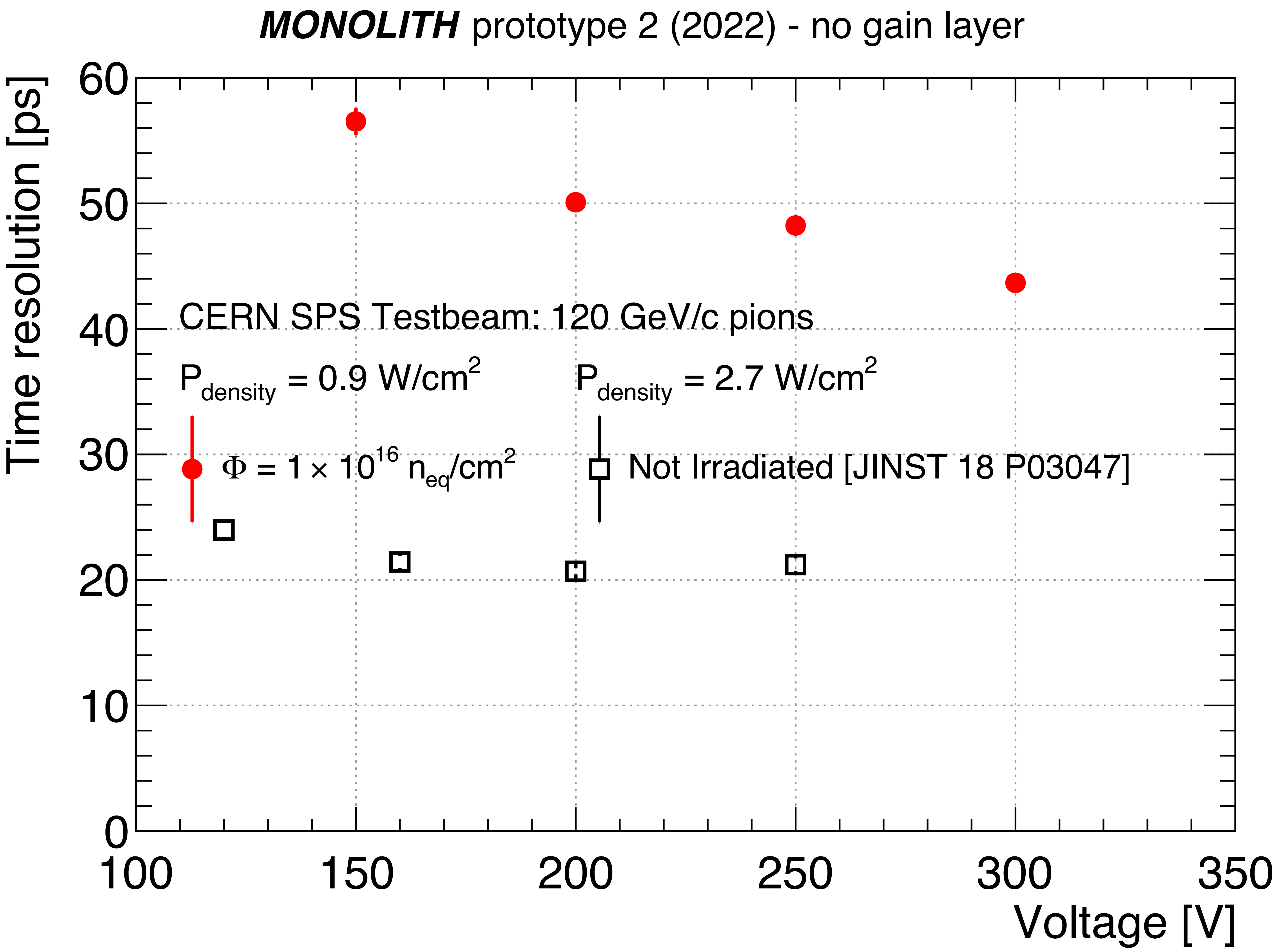
☐ Unirradiated:

20 ps at 200 V

at 0.9 W/cm²

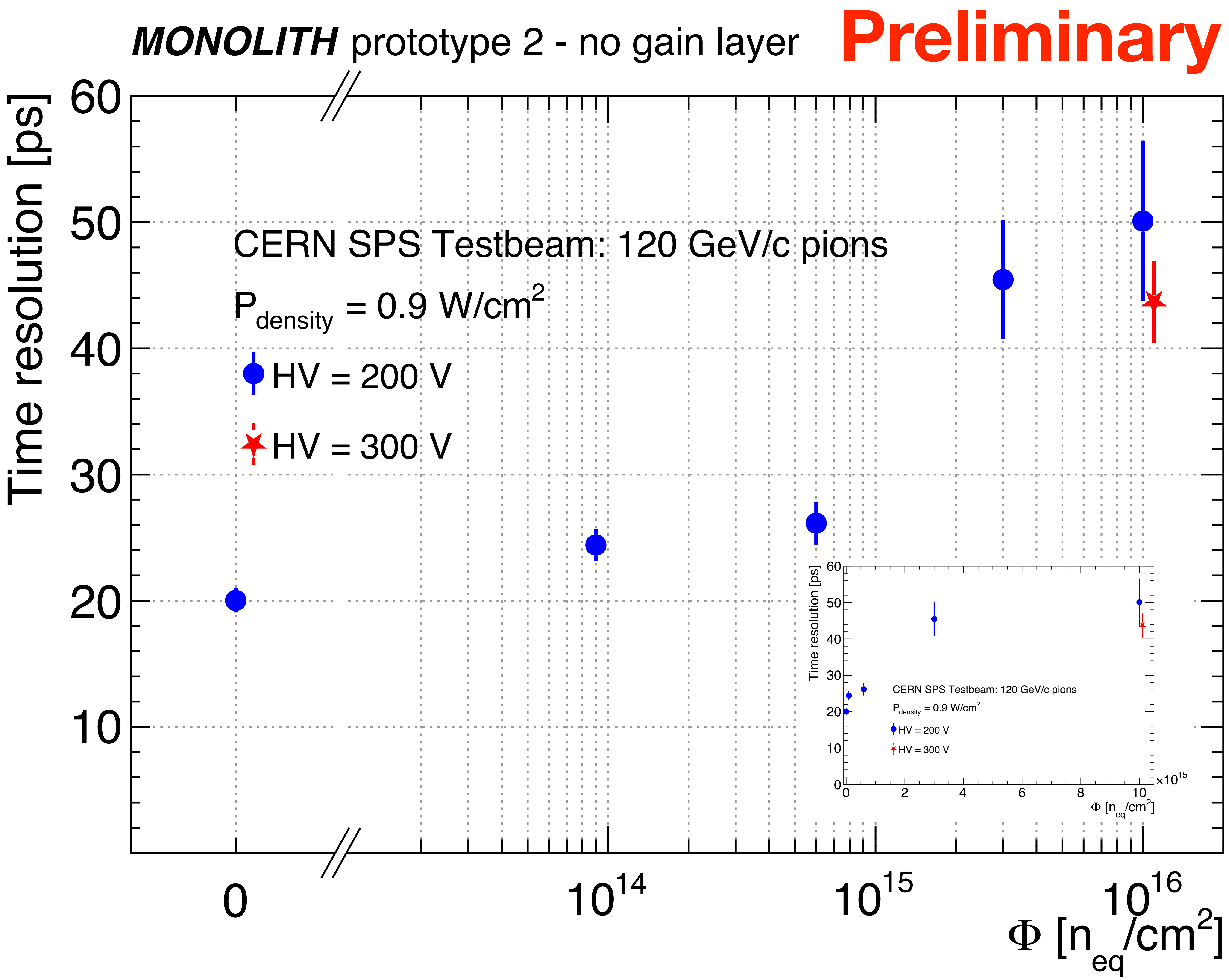


Time resolution vs. sensor bias



Large
plateau vs. HV

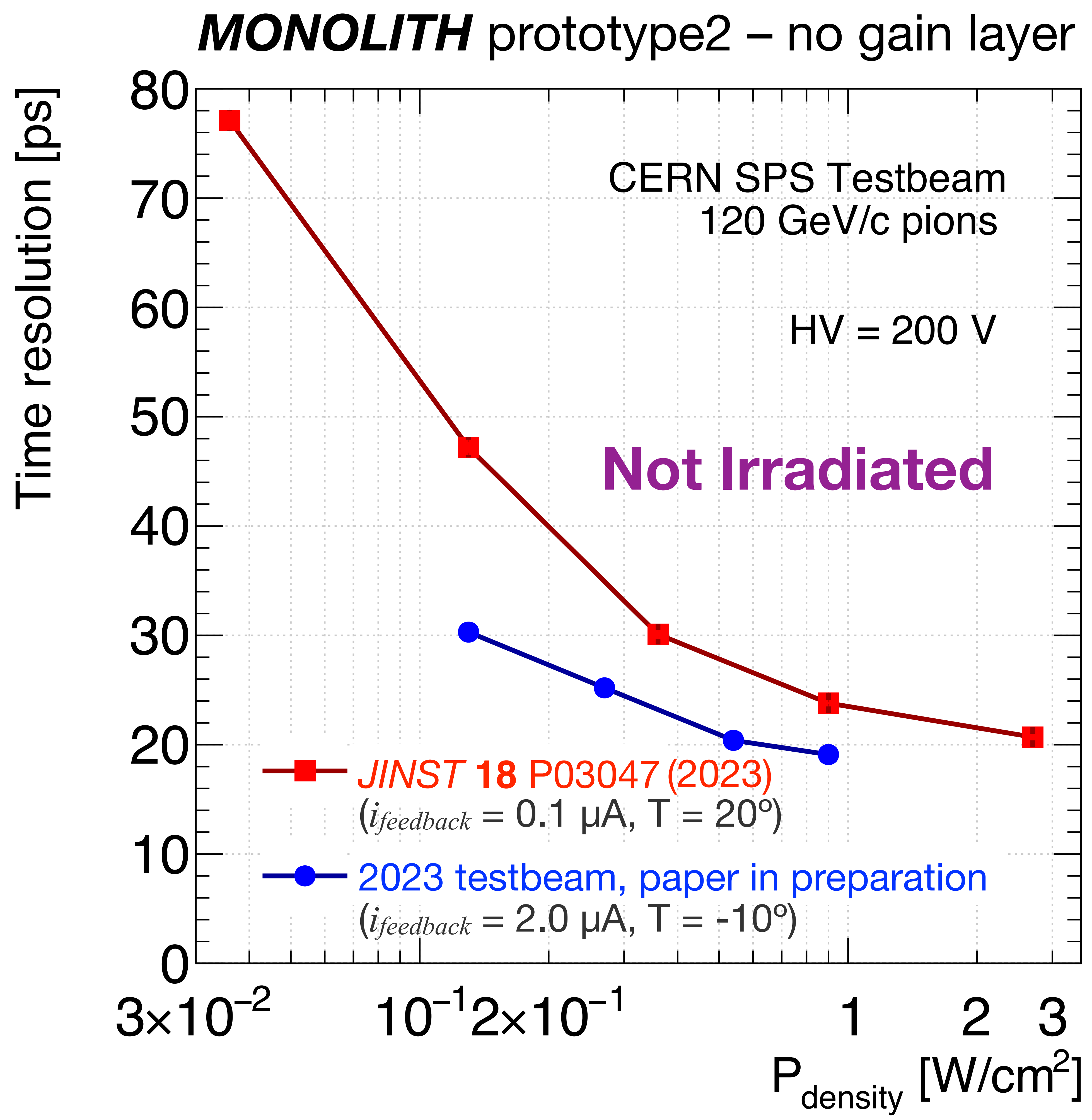
Time resolution vs. proton fluence



New working point

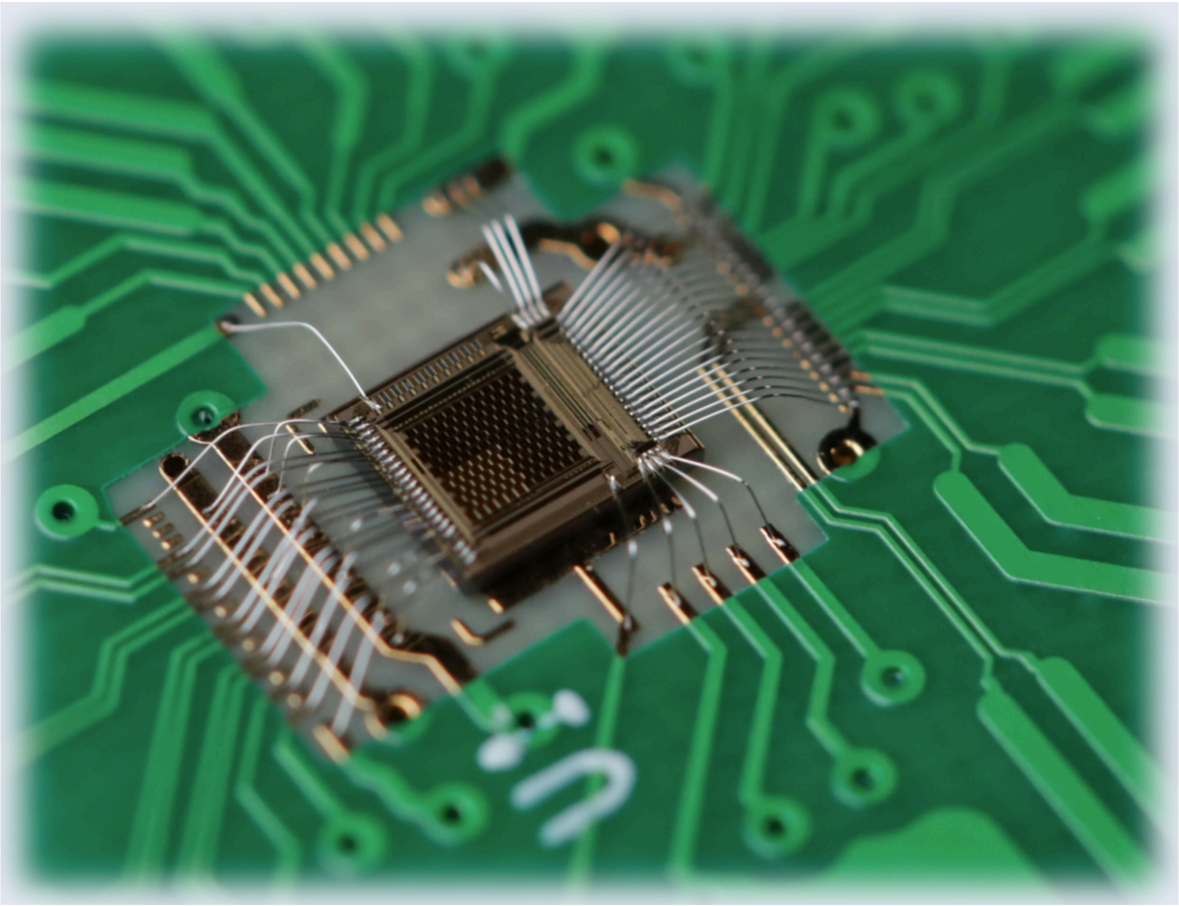
New working point for irradiated boards and **lower temperature**, provide even better time resolutions than old working point :

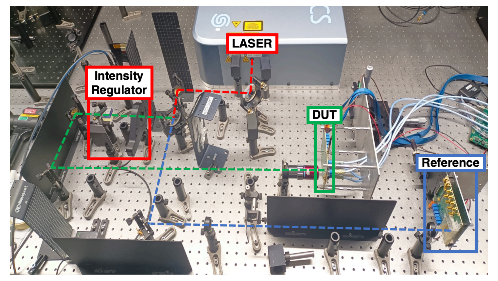
- 30 ps at ~0.13 W/cm²
- 20 ps at ~1 W/cm²



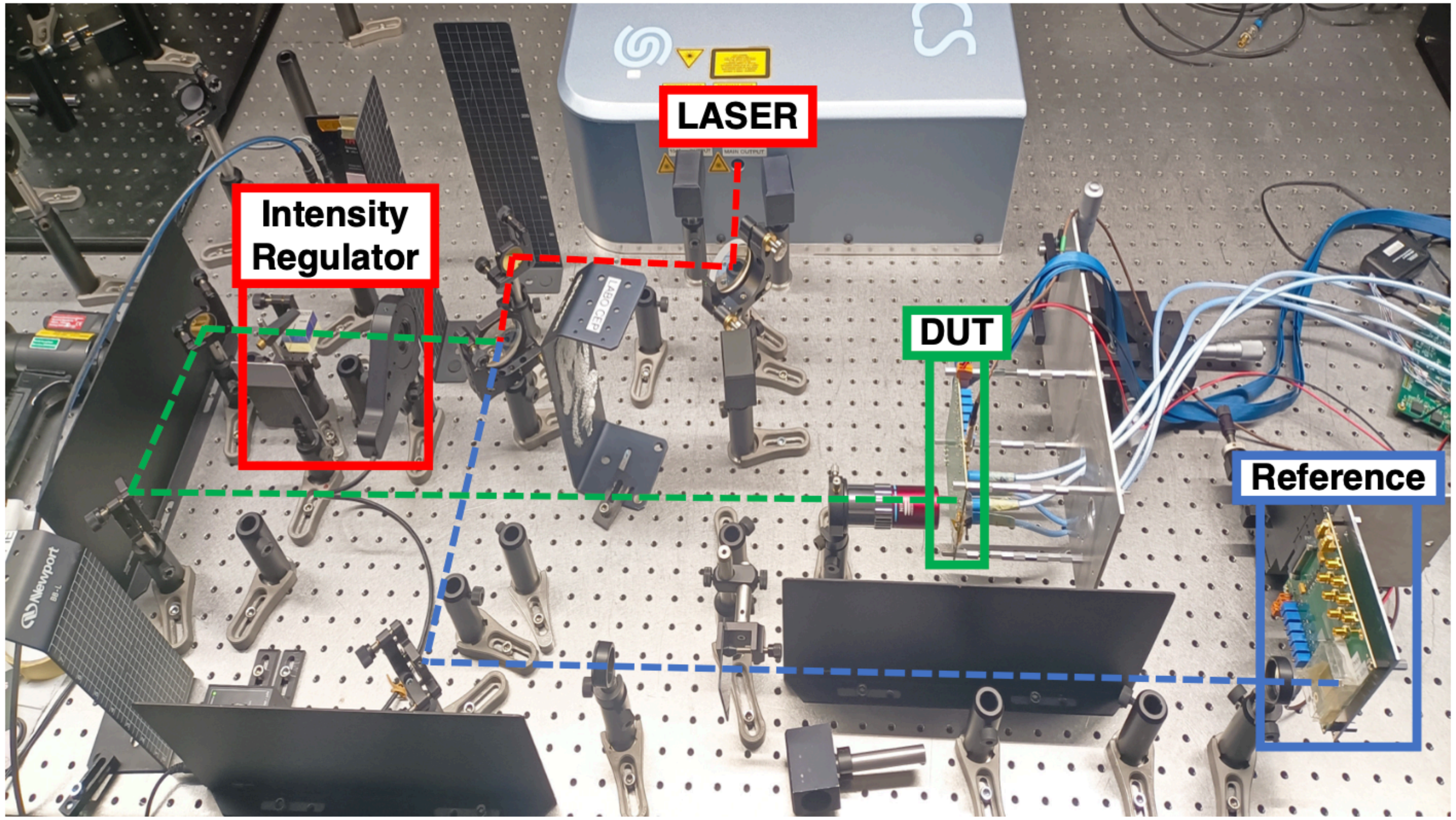
Laser measurements

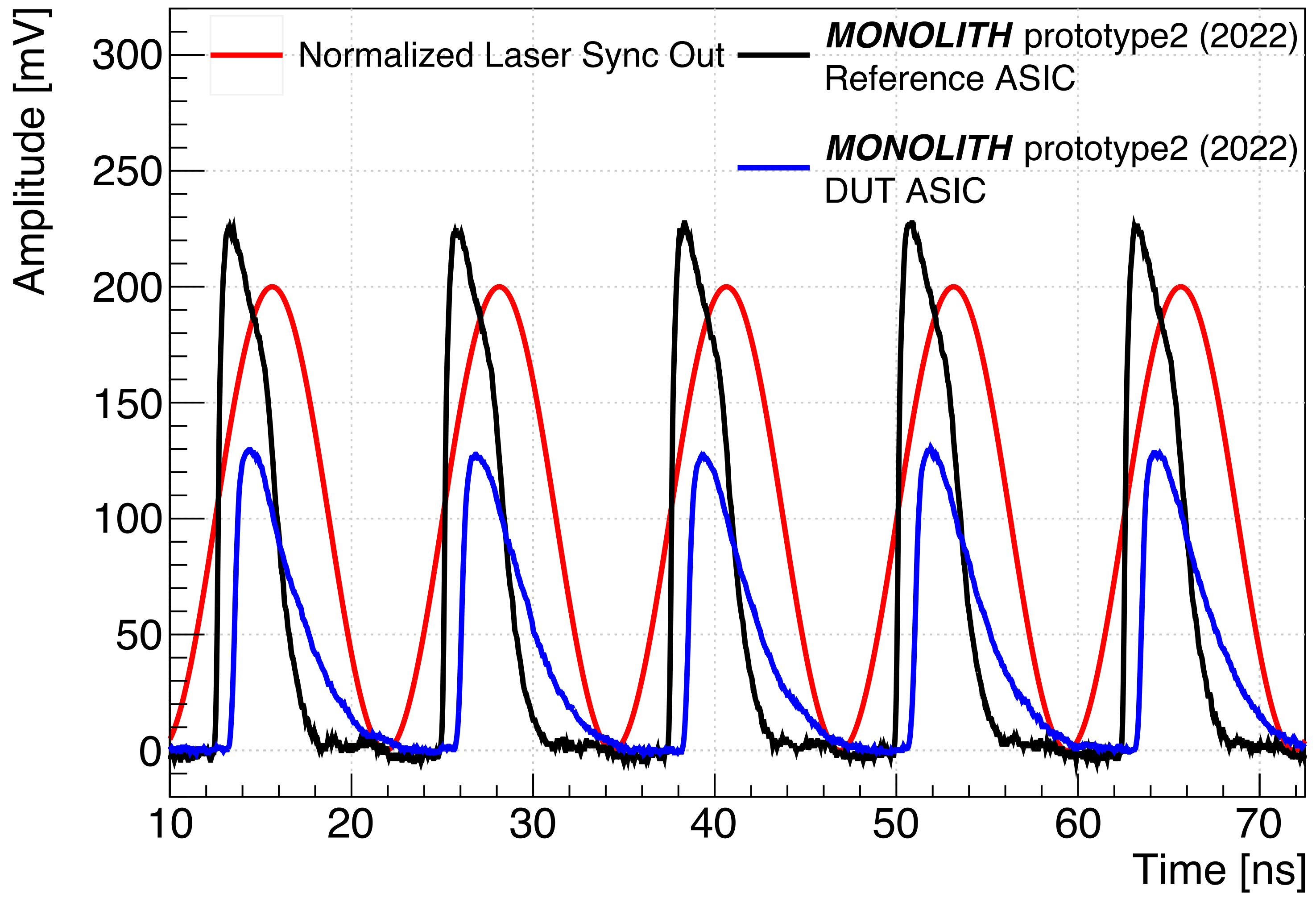
sensor **without gain**





Measurement with a **laser** with a jitter of **100 fs**
(repetition frequency = **80 MHz**)



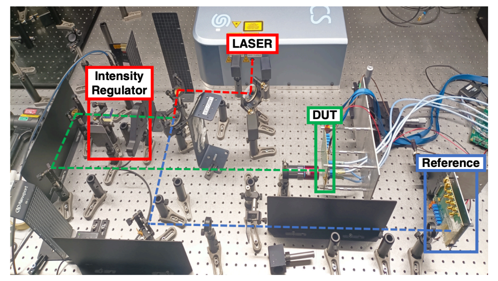


Time coincidence between two of our samples:

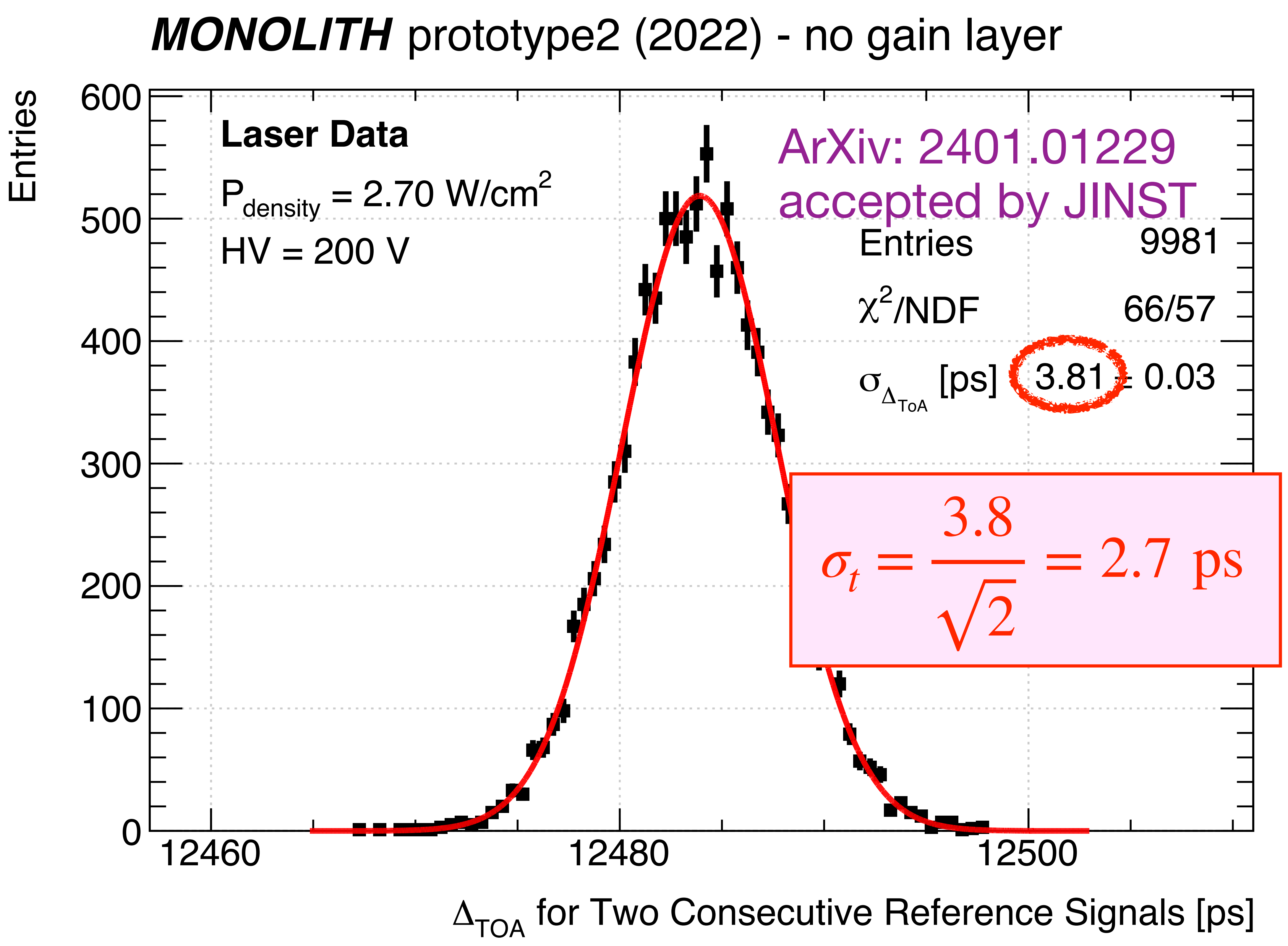
➡ "**Reference**" receiving always large laser pulse producing 17k electrons (σ_t = 2.7 ps)

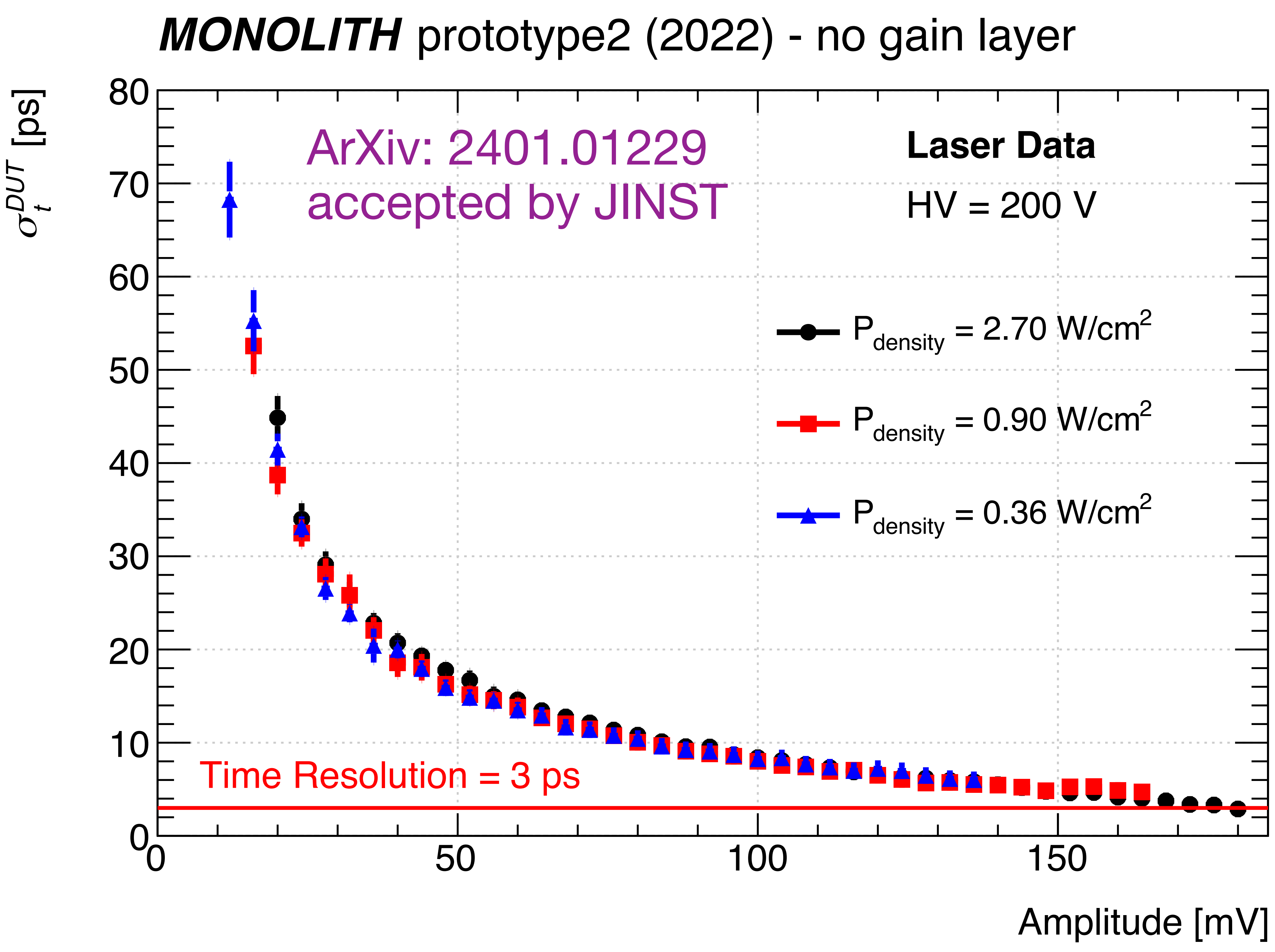
➡ "**DUT**" receiving variable laser power, to study the performance vs. amplitude

prototype2 — no gain layer



Laser Measurement





Our prototype "**Reference**":

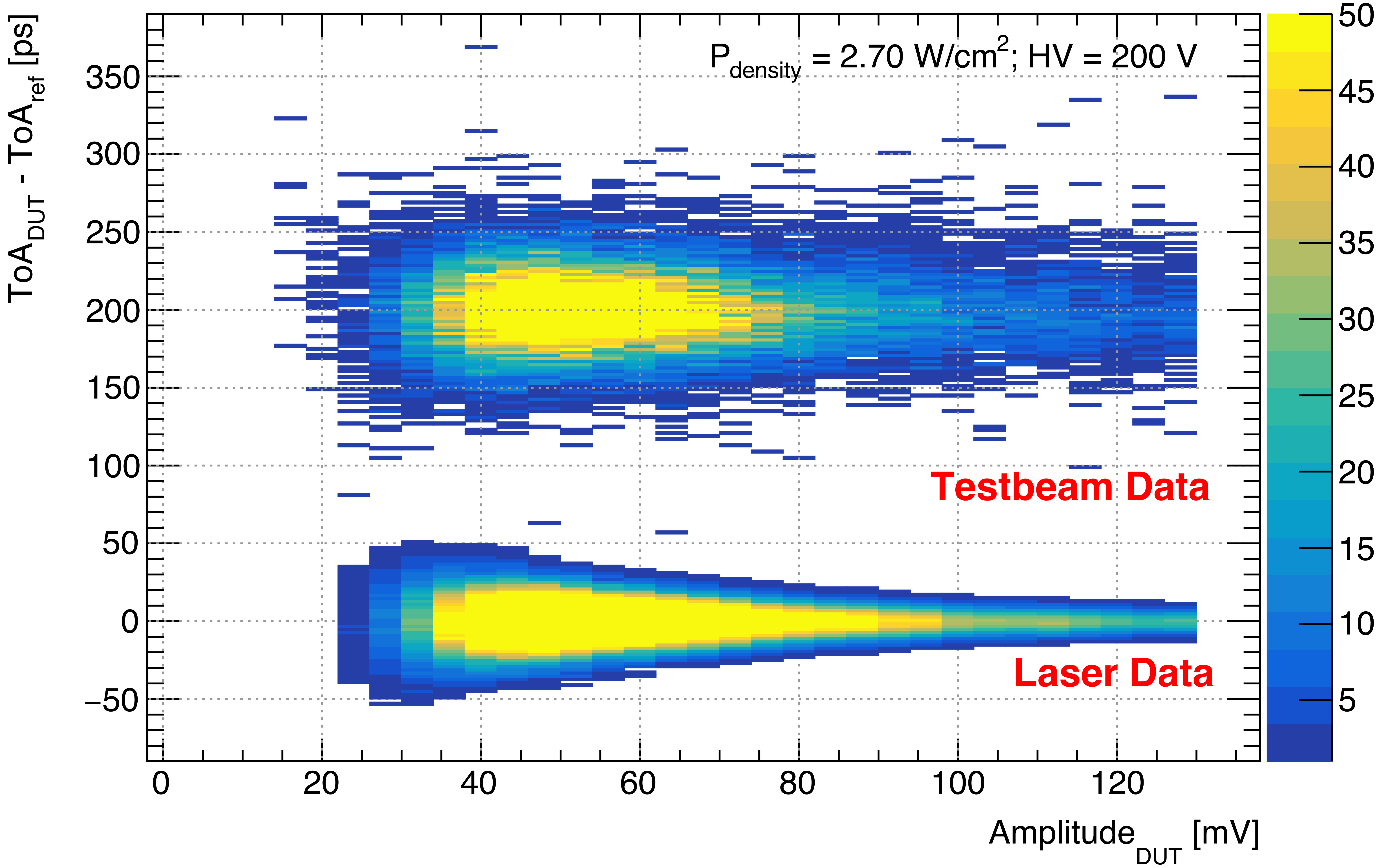
σ_t = 2.7 ps with 17k e^- (5—6 mips)

Our prototype "**DUT**":

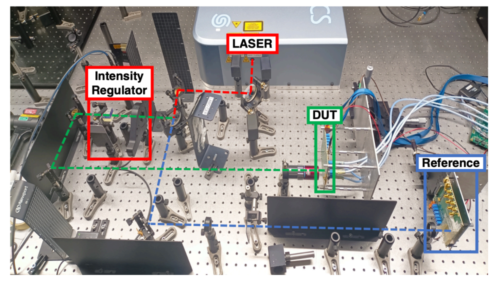
with **max 11k e^-** (≈4 mips)

Laser vs. testbeam data

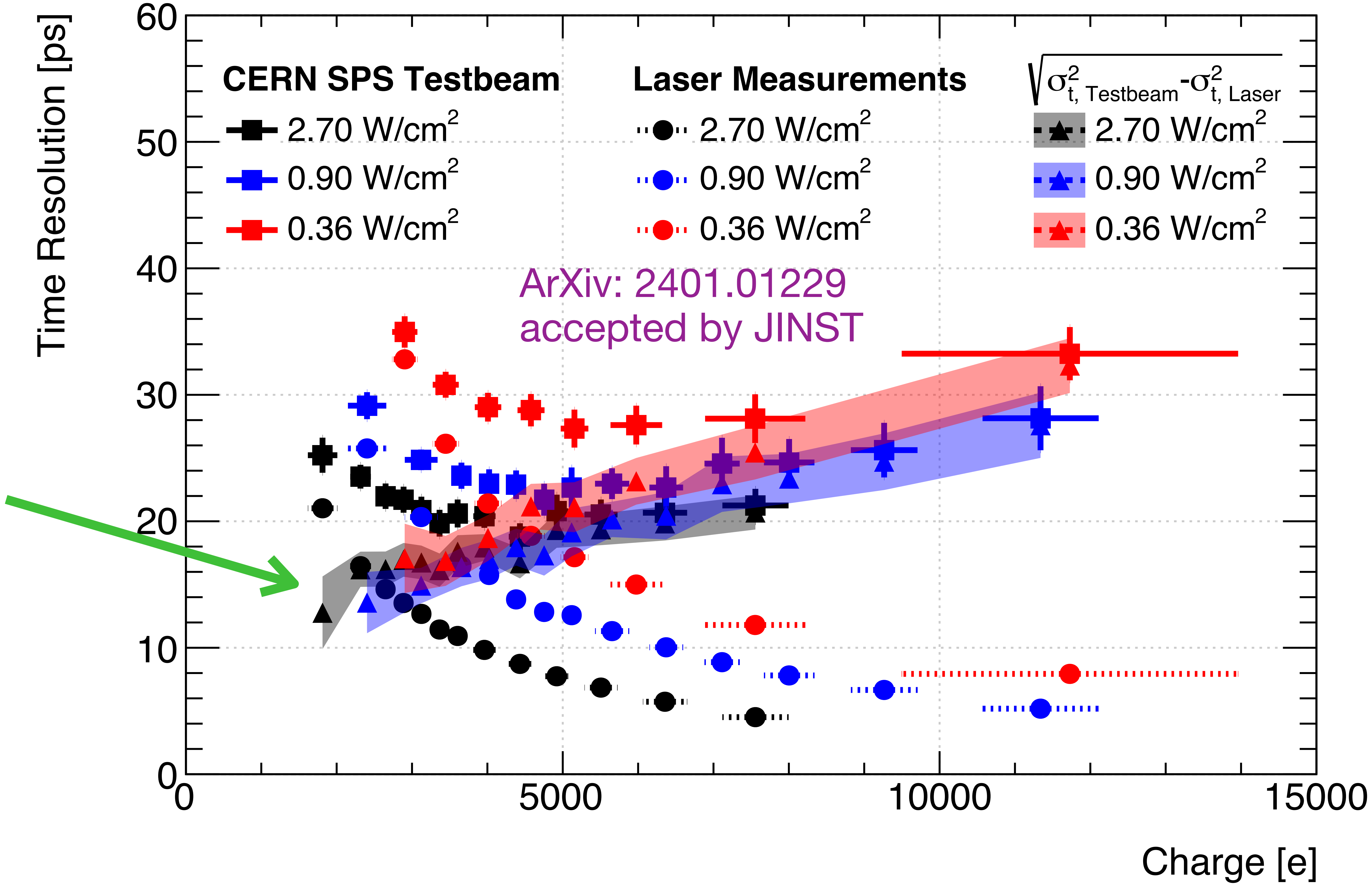
MONOLITH **prototype2 (2022) - no gain layer**



prototype2 — no gain layer



Laser Measurement (preliminary)



The bands estimate the charge-collection (“Landau”) noise

Results with PicoAD prototypes (with gain layer)

MONOLITHIC

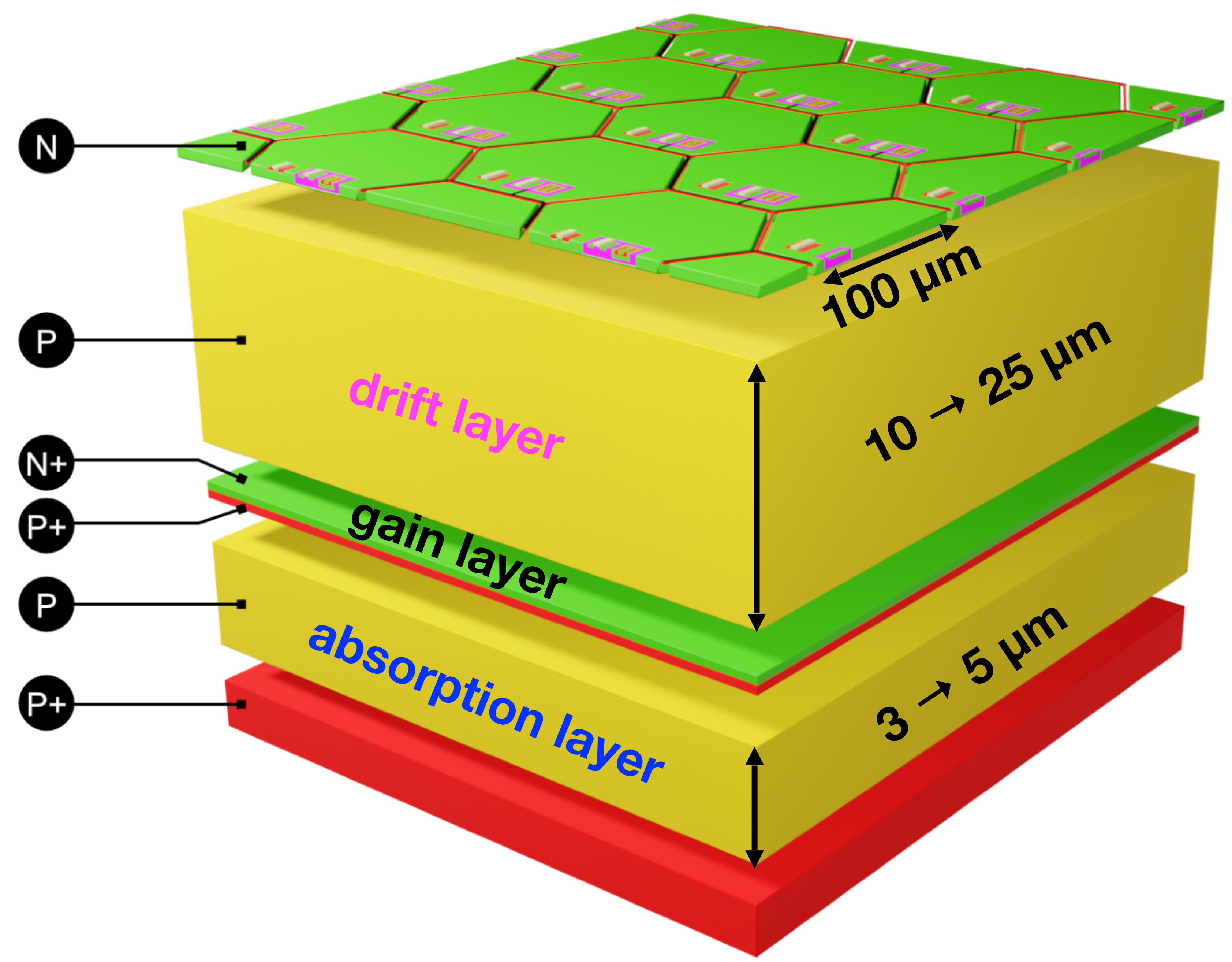
SiGe BiCMOS

PicoAD©:
Picosecond
Avalanche
Detector

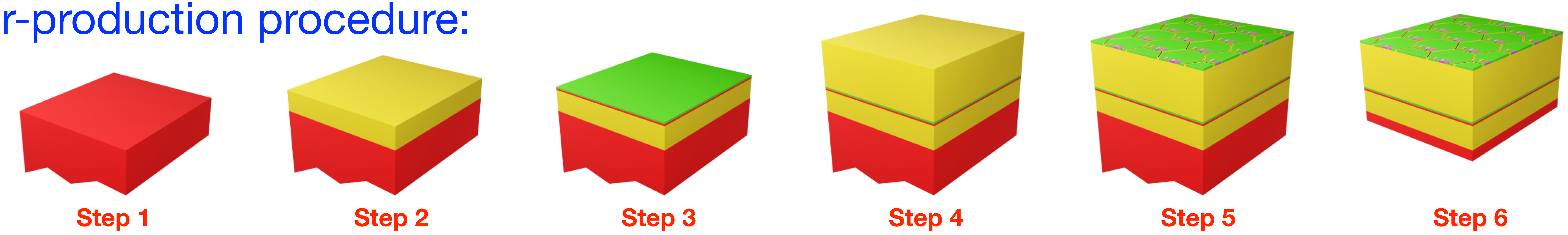
PicoAD:

Multi-Junction Picosecond-Avalanche Detector©
with continuous and deep gain layer:

- De-correlation from implant size/geometry
  ➝ **high pixel granularity and full fill factor**
  (high spatial resolution and efficiency)
- Only small fraction of charge gets amplified
  ➝ **reduced charge-collection (Landau) noise**
  (enhance timing resolution)



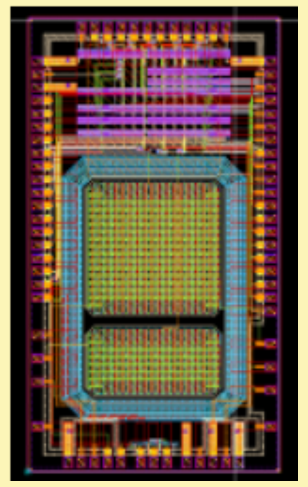
Wafer-production procedure:



Monolithic SiGe BiCMOS for timing

Monolithic prototypes with SiGe BiCMOS (IHP 130nm SG13G2) **without** internal gain layer

2016



200ps

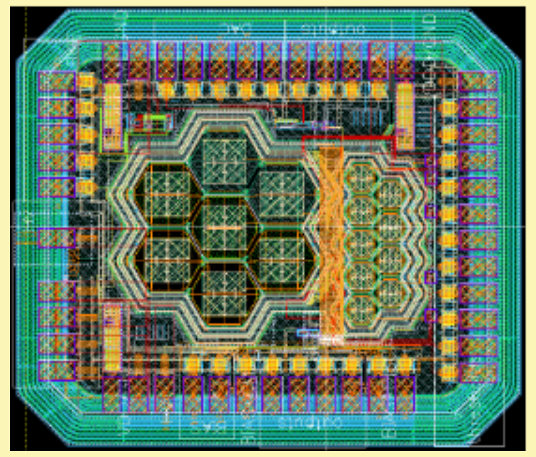
- 1 mm^2 pixel
- Discriminator

2017

110ps

- 30 pixels 500x500μm^2
- 100ps TDC +I/O logic

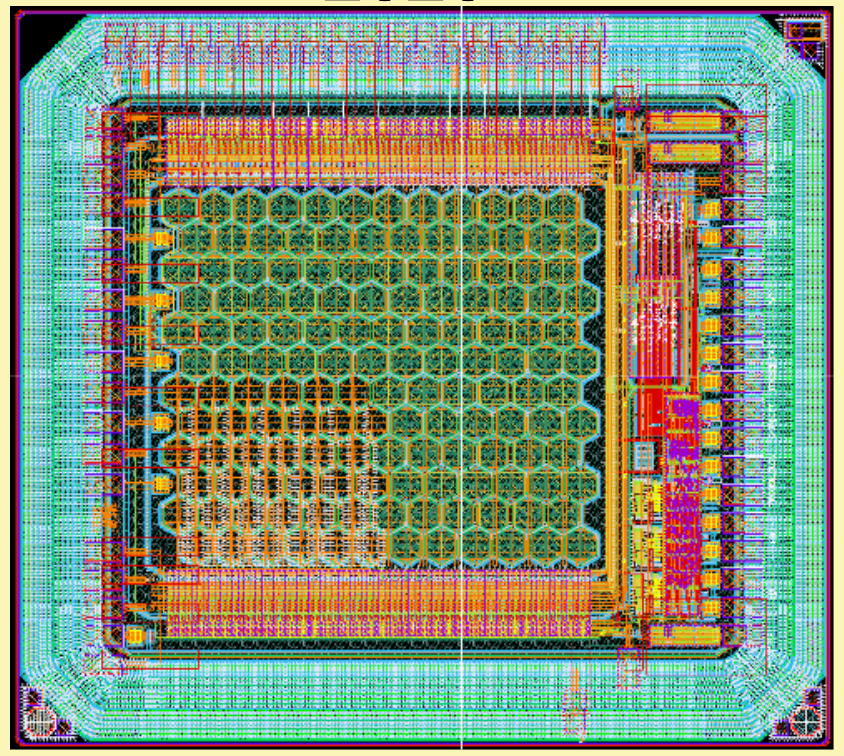
2018



50ps

- Hexagonal pixels 100µm and 200µm pitch
- Discriminator output

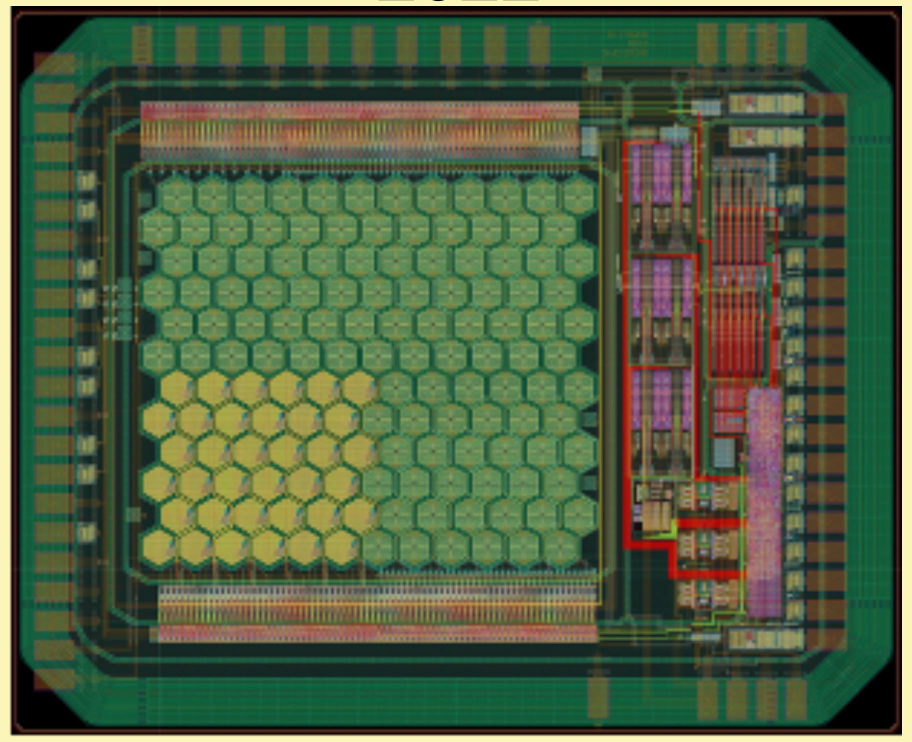
MONOLITH prototype 1
2020



36 ps

- Hexagonal pixels 100µm pitch
- 30ps TDC +I/O logic
- Analog channels

MONOLITH prototype 2
2022



20 ps

- Hexagonal pixels 100µm pitch
- improved electronics
- 50µm epitaxial layer (350Ωcm)

In 2022 : **proof-of-concept**
monolithic prototype
with internal gain layer

(using 2020 masks)

PicoAD
special wafers
produced internally by IHP
(not optimised yet)

PicoAD p.o.c.: Gain with ^{55}Fe source

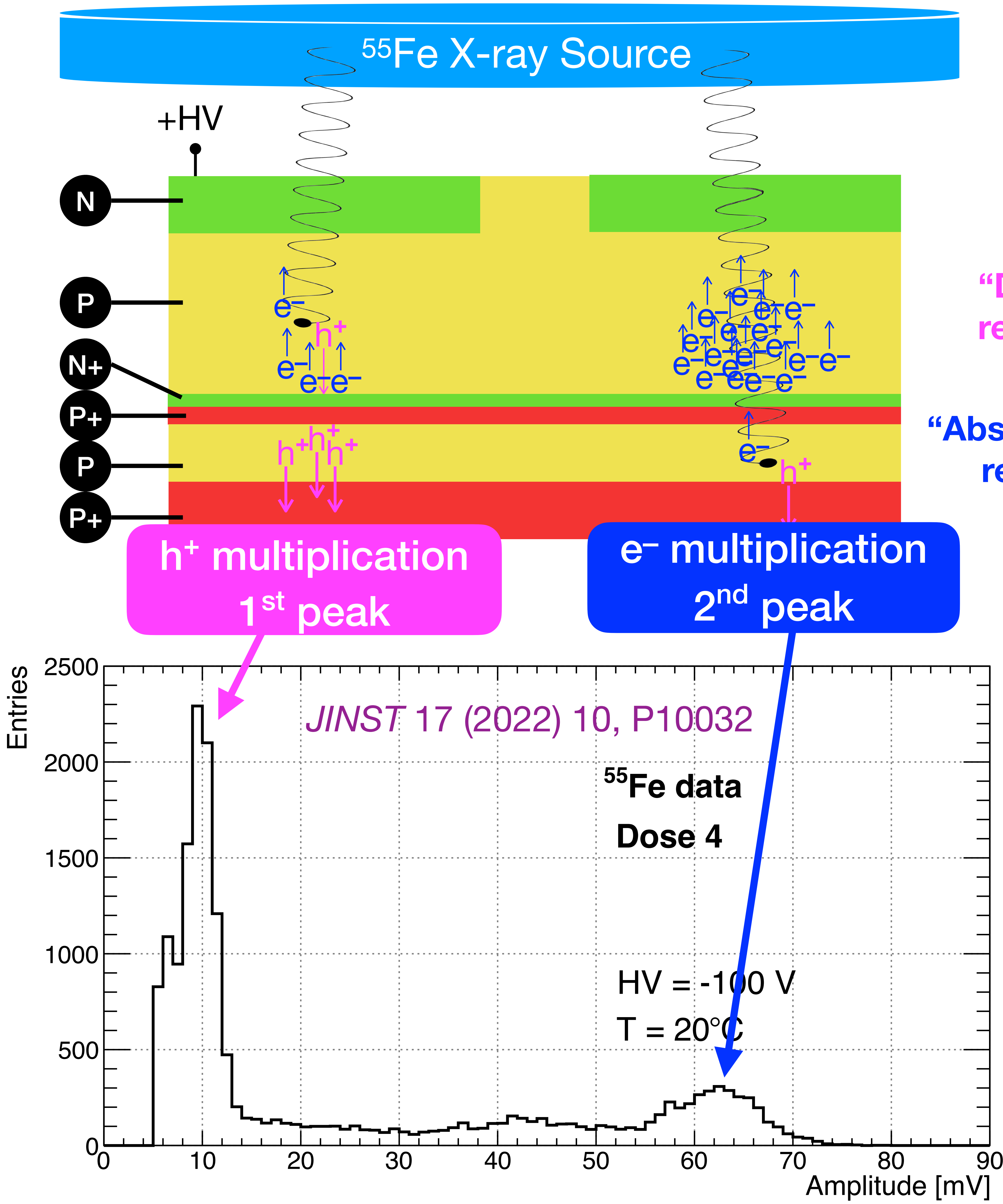
X-rays from ^{55}Fe radioactive source:

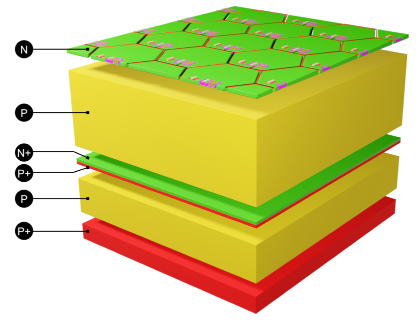
- mainly ~5.9 keV photons
- point-like charge deposition

We found a double-peak spectrum

- photon absorbed in **drift region**
  - ➡ **holes** drift through gain layer & multiplied
  - ➡ **first peak** in the spectrum
- photon absorbed in **absorption region**
  - ➡ **electrons** through gain layer & multiplied
  - ➡ **second peak** in the spectrum

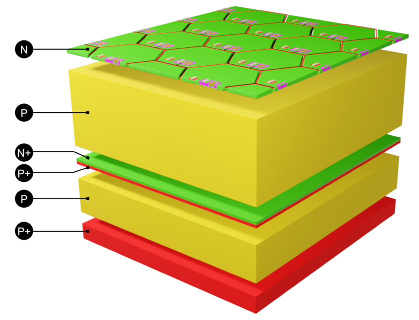
Gain measured: ~20 for ^{55}Fe
(corresponding to ~60 for a m.i.p.)





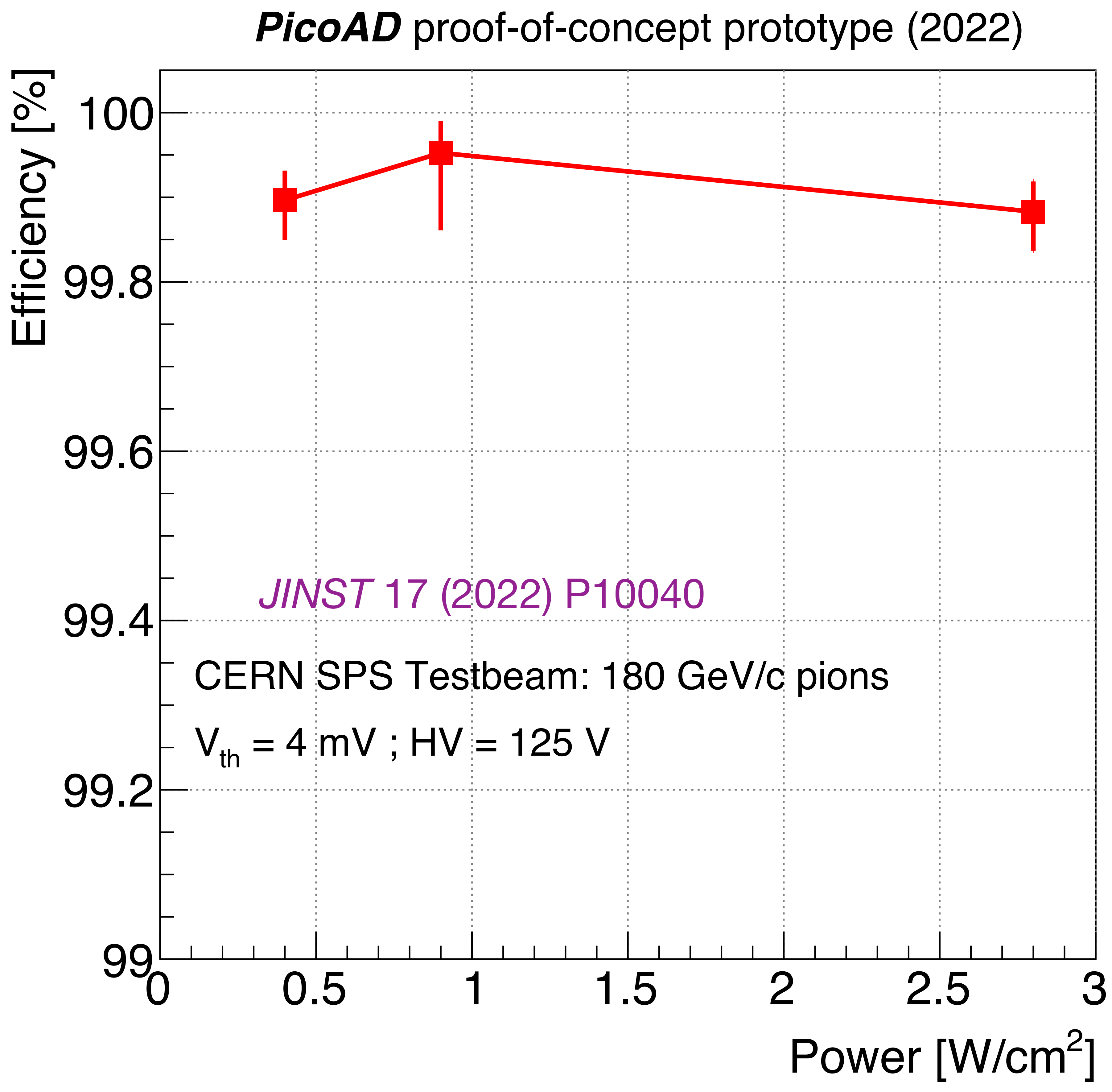
Testbeam PicoAD p.o.c.: Detection Efficiency

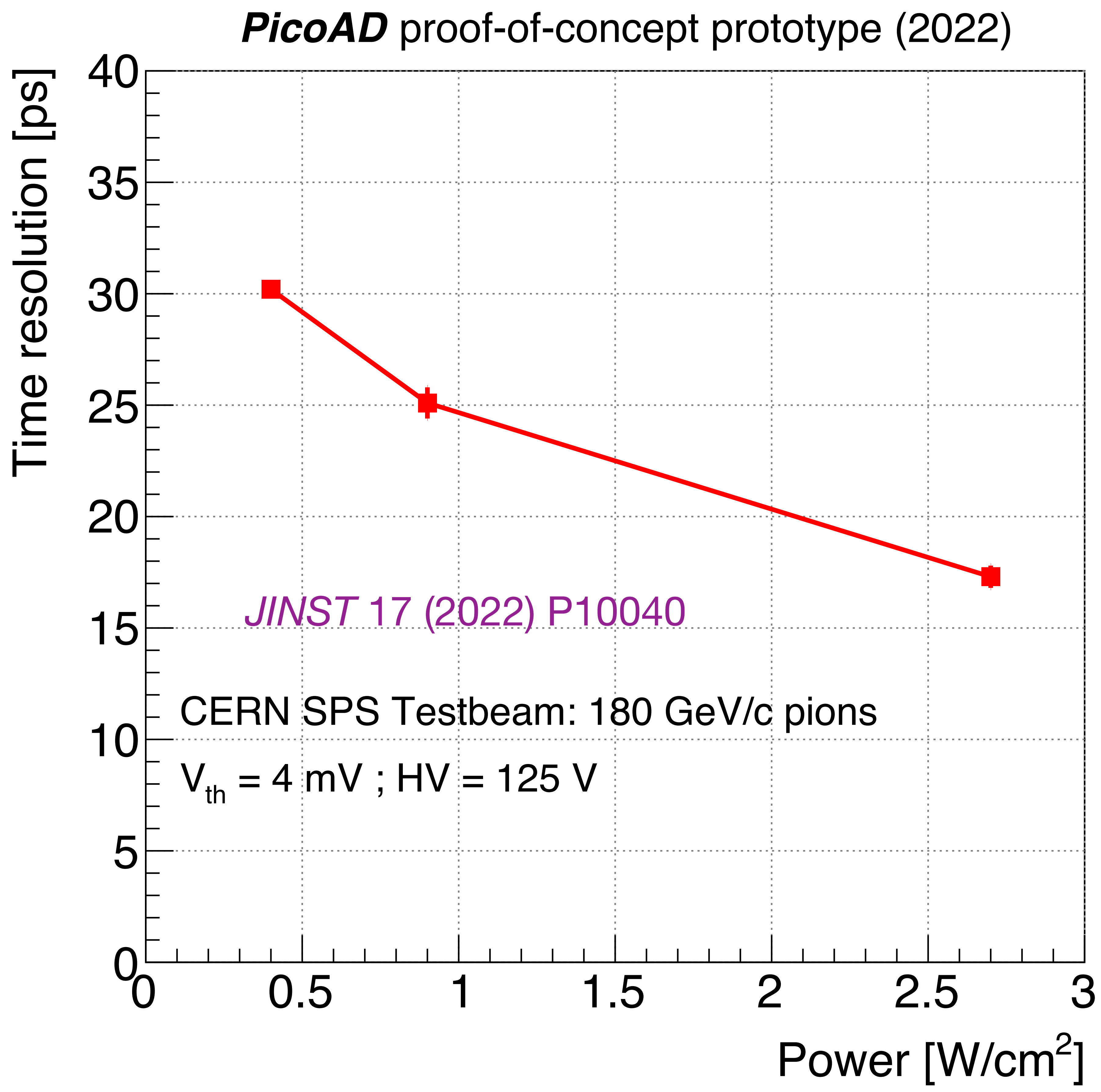
PicoAD



99.9% for all power consumptions

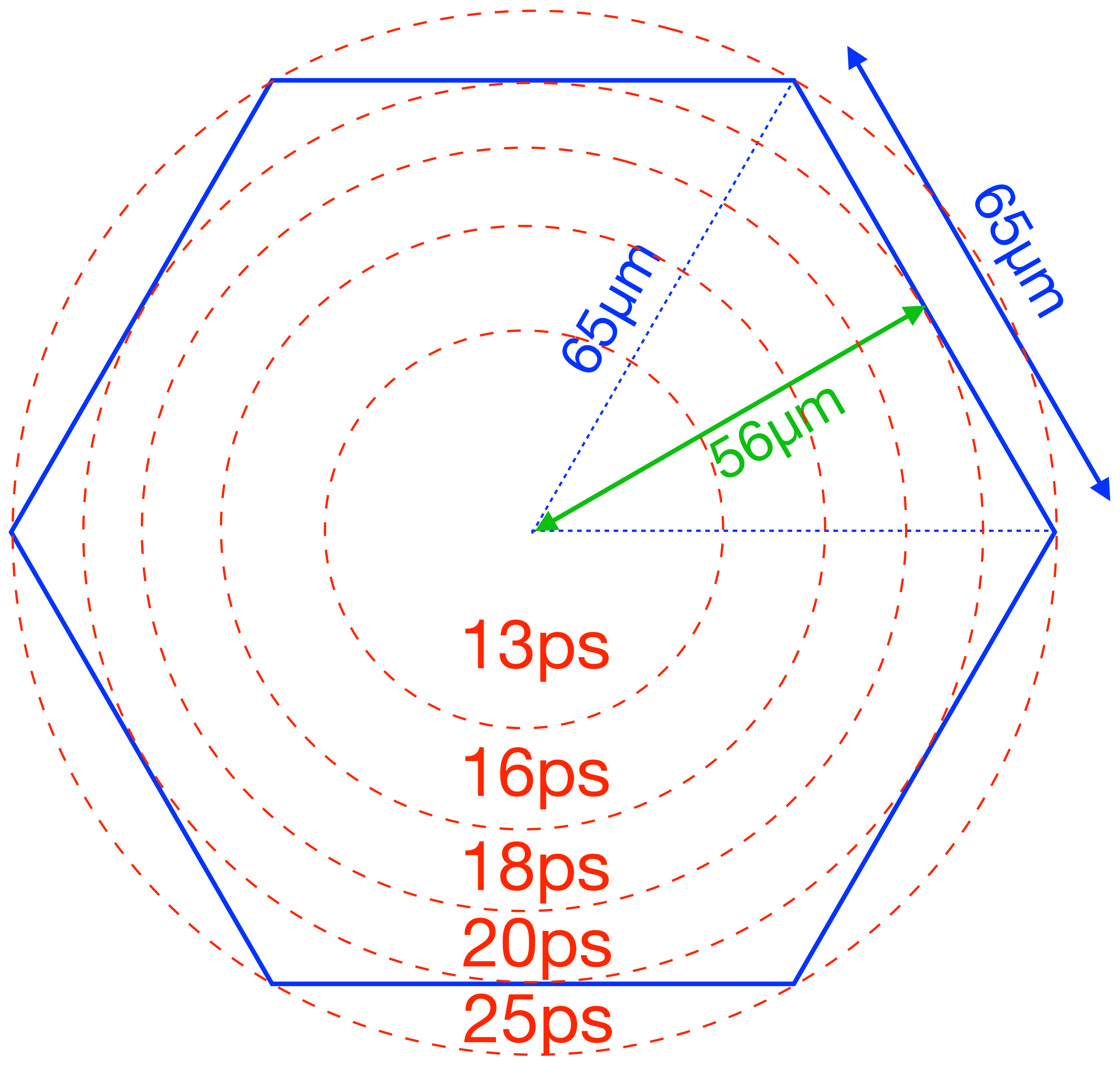
17 ps at 2.7 W/cm²
30 ps at 0.4 W/cm²



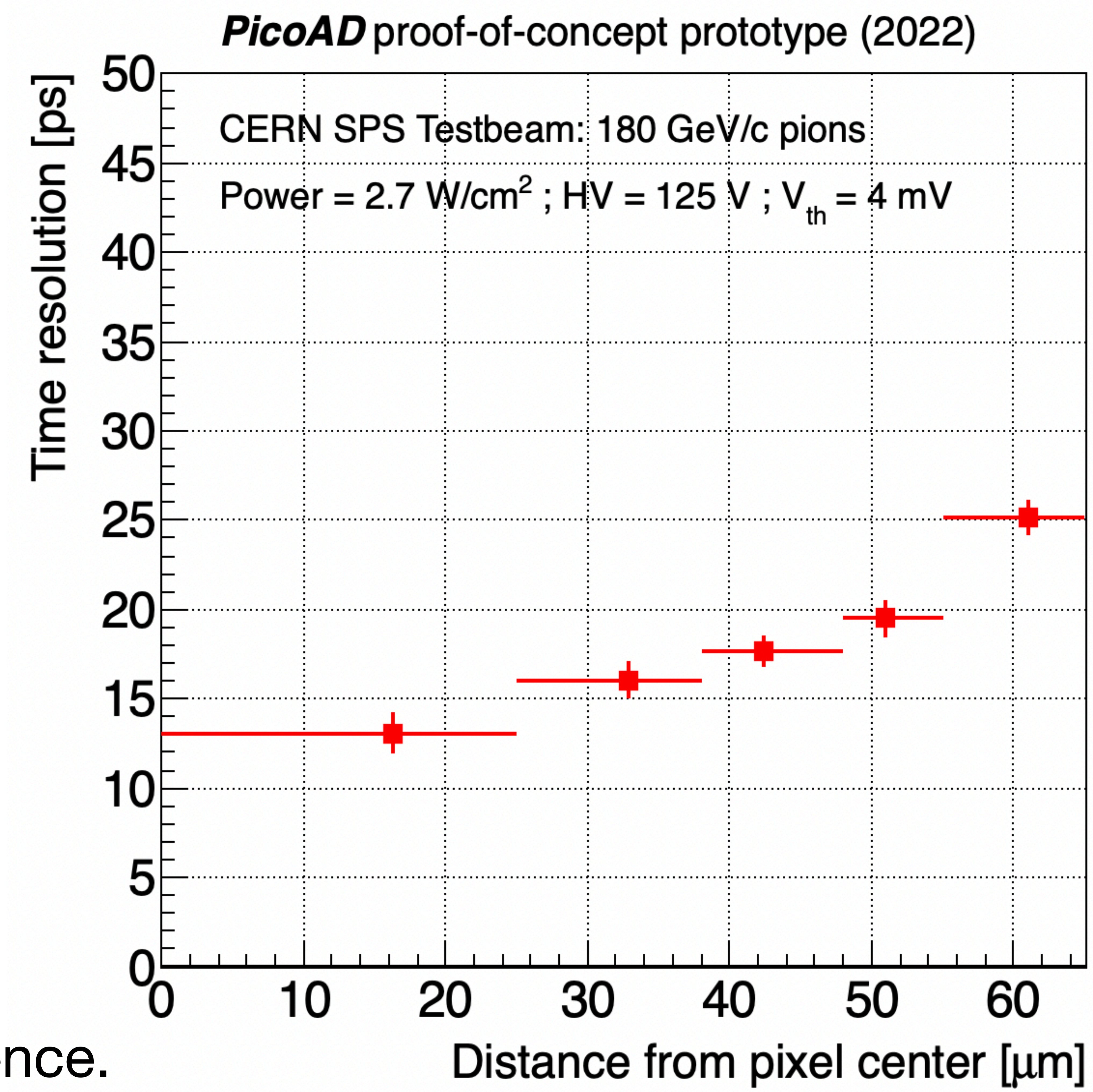


PicoAD

Pixel surface divided in 5 radial areas:



Time resolutions: **13 ps** at the pixel center
25 ps at the pixel edge

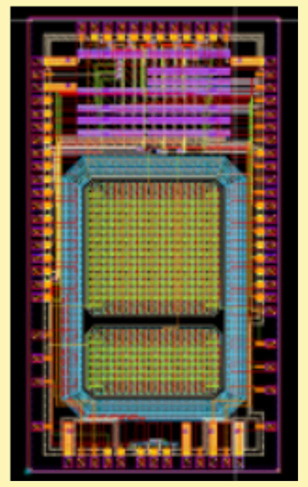


New prototypes devised to improve this dependence.

MONOLITH Project: outlook

Monolithic prototypes with SiGe BiCMOS (without internal gain layer)

2016

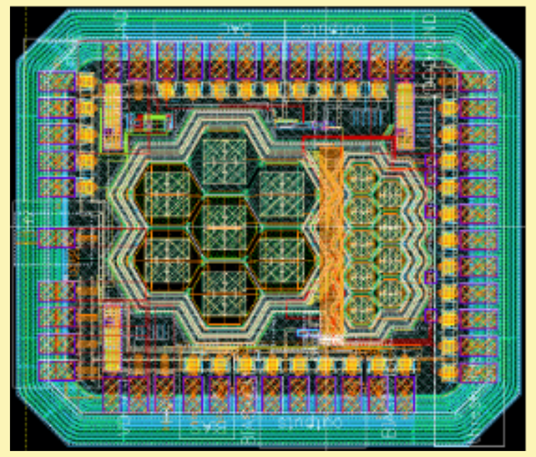


200ps
- 1 mm² pixel
- Discriminator

2017

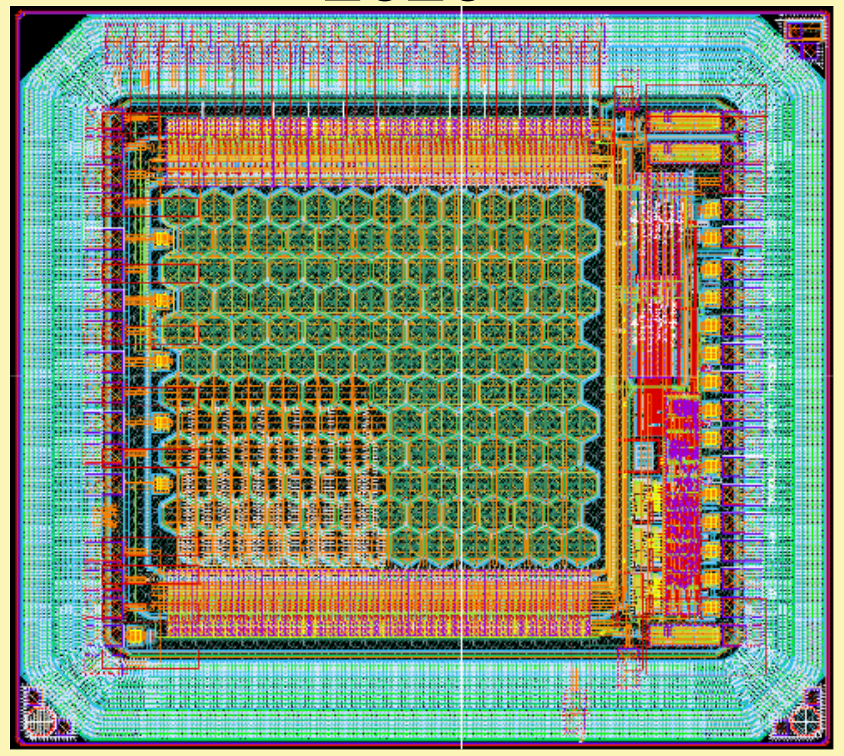
110ps
- 30 pixels 500x500µm²
- 100ps TDC +I/O logic

2018



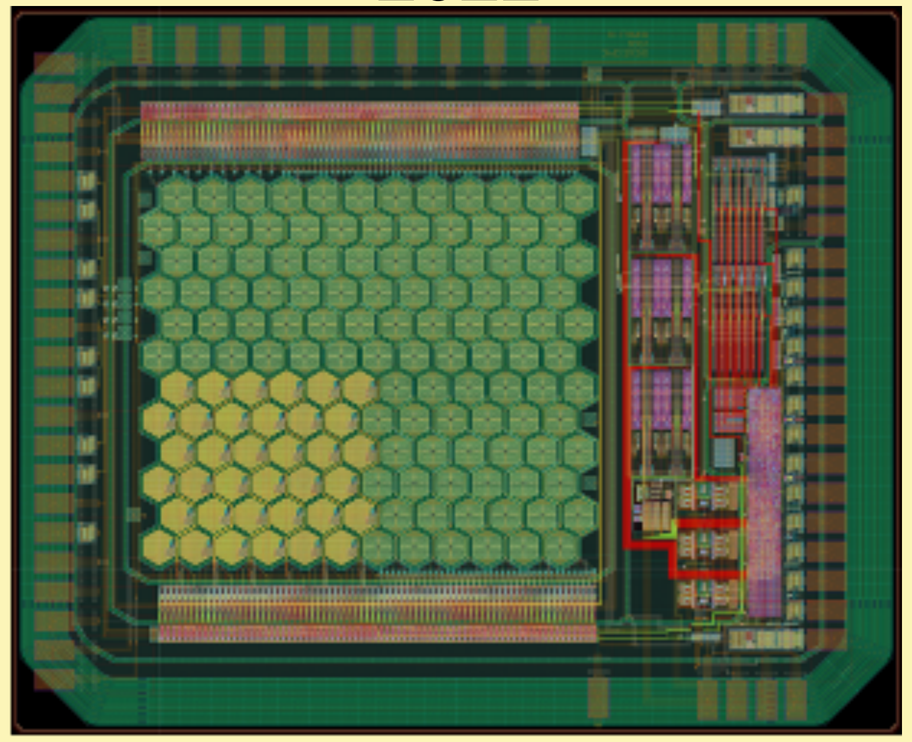
50ps
- Hexagonal pixels 100µm and 200µm pitch
- Discriminator output

MONOLITH prototype 1
2020



36 ps
- Hexagonal … s 100µm pitch
- 30ps TDC … ogic
- Analog cha…

MONOLITH prototype 2
2022



20 ps
- Hexagonal … s 100µm pitch
- improved e… nics
- 50µm epita… yer (350Ωcm)

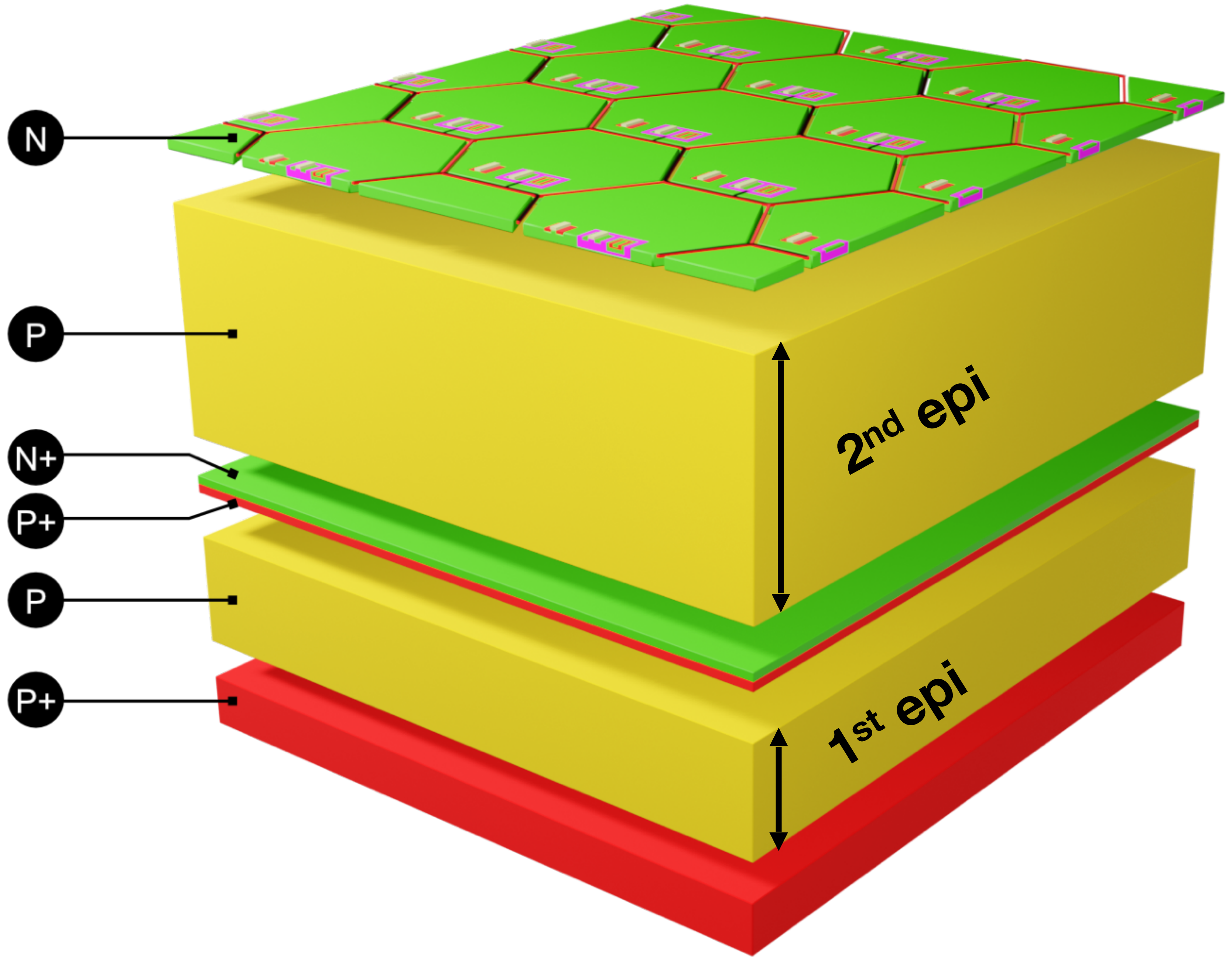
Monolithic prototypes
with internal gain layer:

PicoAD version
(proof-of-concept)
17 ps

PicoAD version
(received: **Jan. 2024**)

2024 PicoAD production

Wafer	1st epi thickness [μm]	2nd epi thickness [μm]	Dose
3	3	15	3
			3.5
			4
4	3	25	3.5a
			3.5b
			4.75
5	3	25	4
			4.5
			5
6	5	15	3
			3.5
			4
7	5	25	4
			4.5
			5

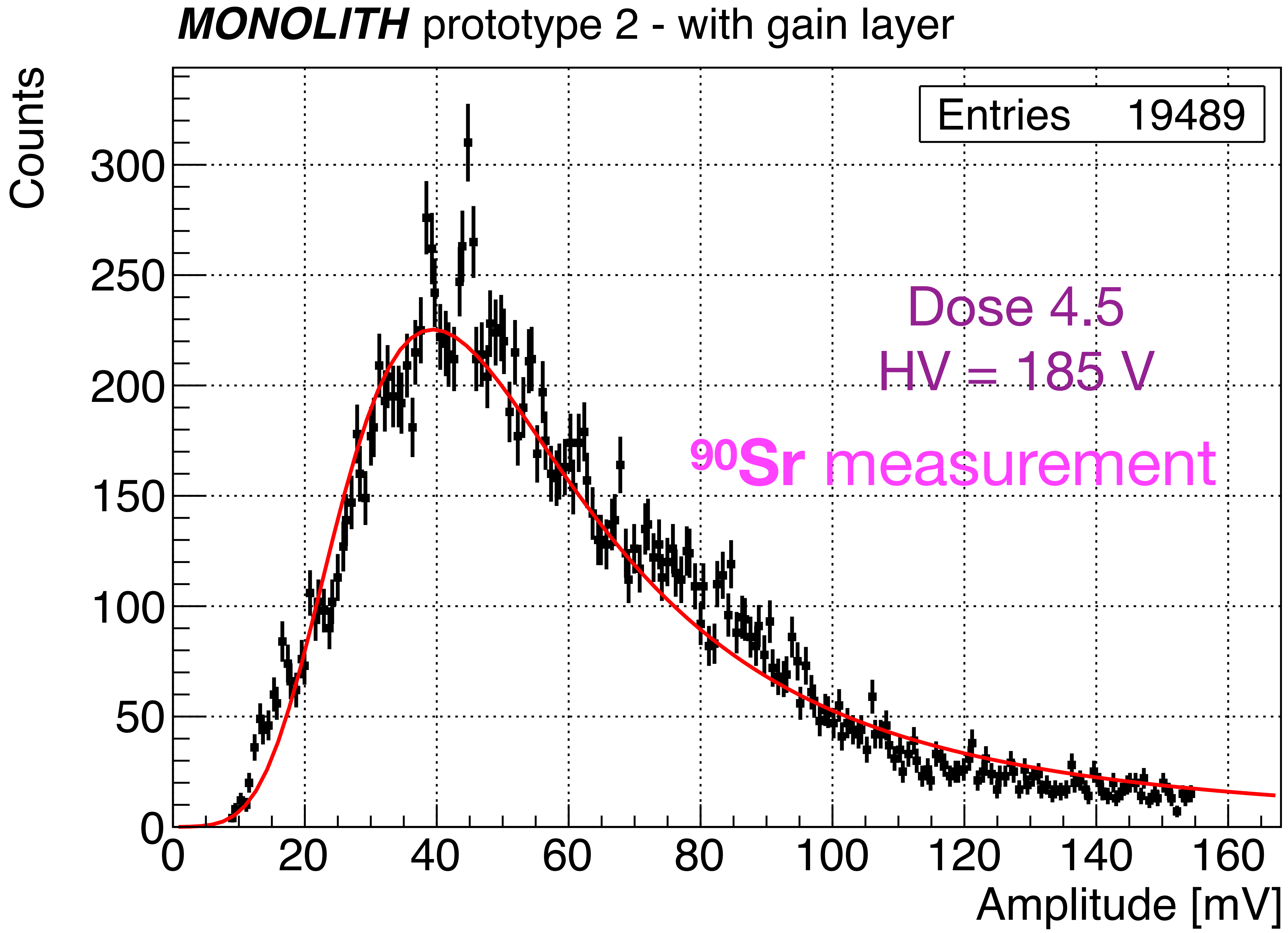


15 different flavours produced;
in 4 geometries

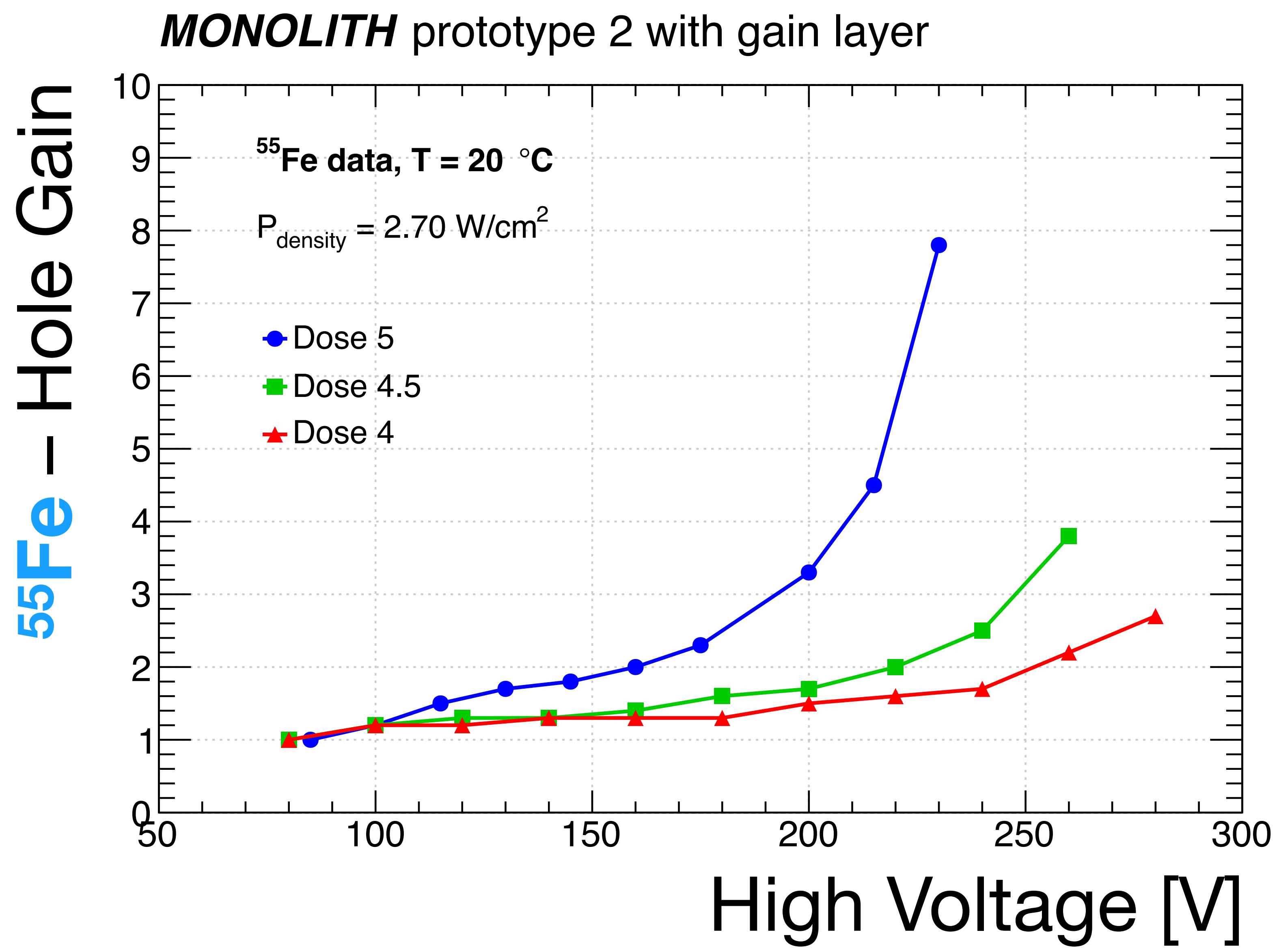
Looked already at 3 flavours (out of 15)

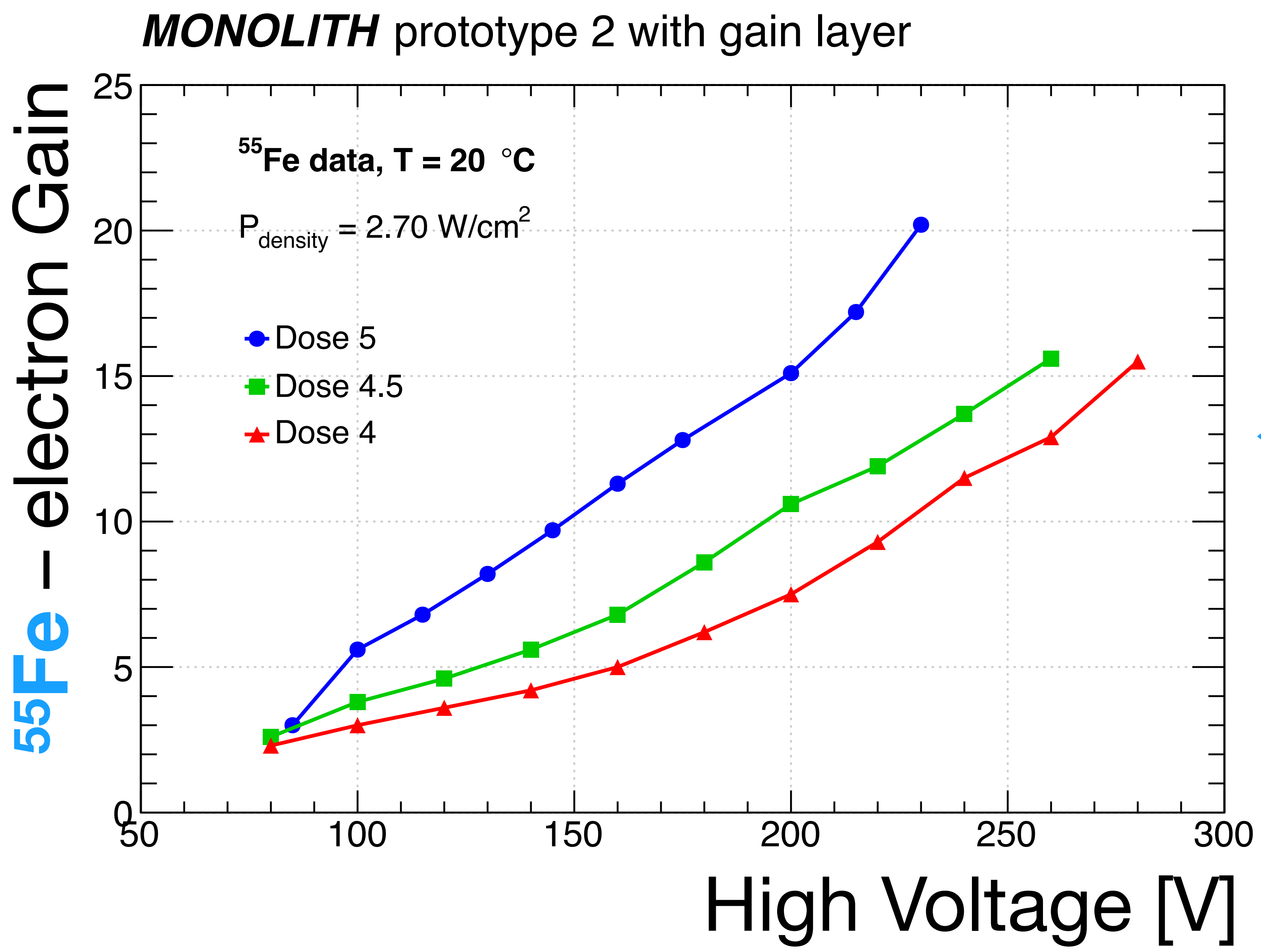
2024 PicoAD production

The detectors work:



2024 PicoAD: ^{55}Fe and ^{90}Sr Measurements

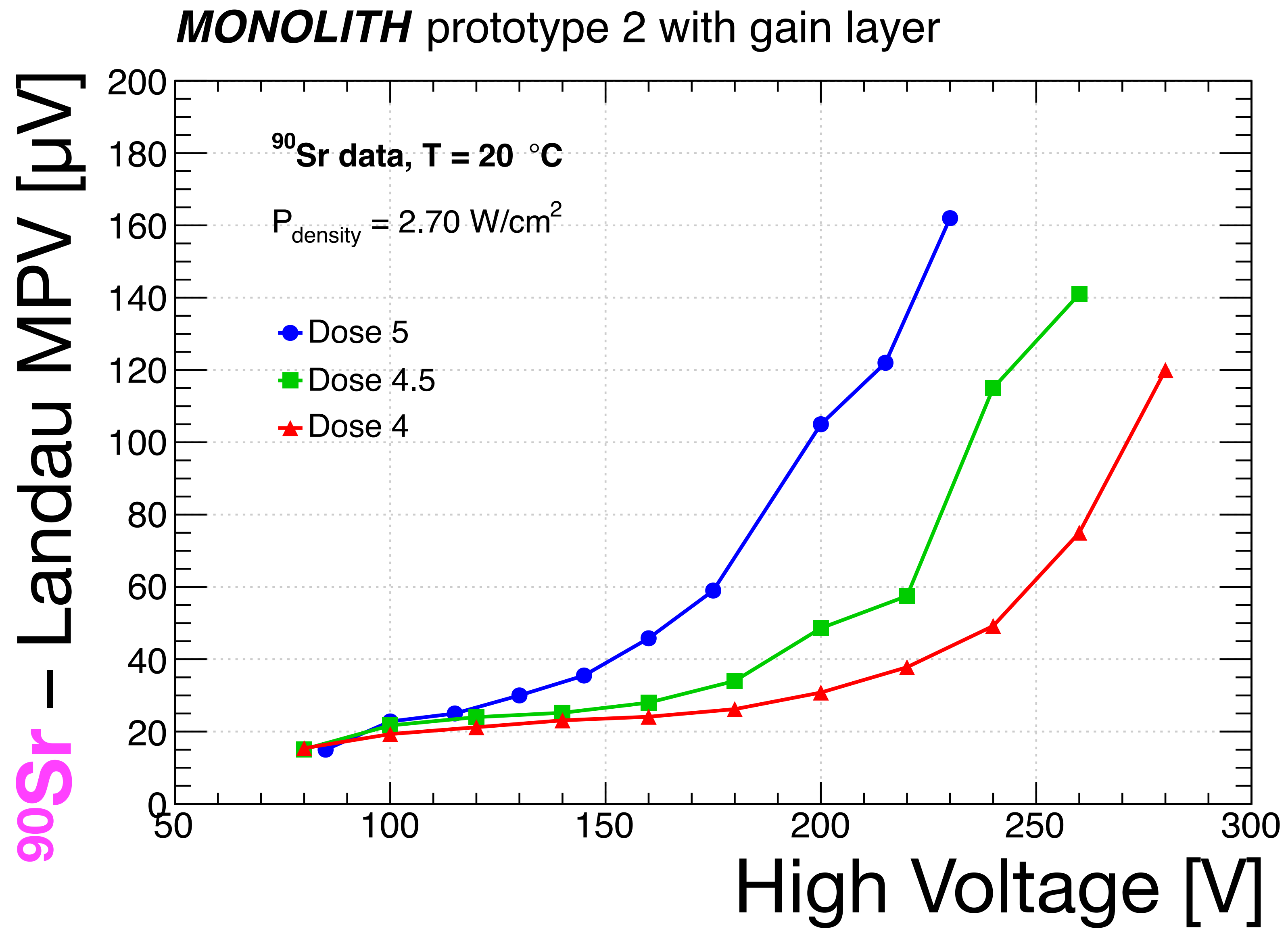


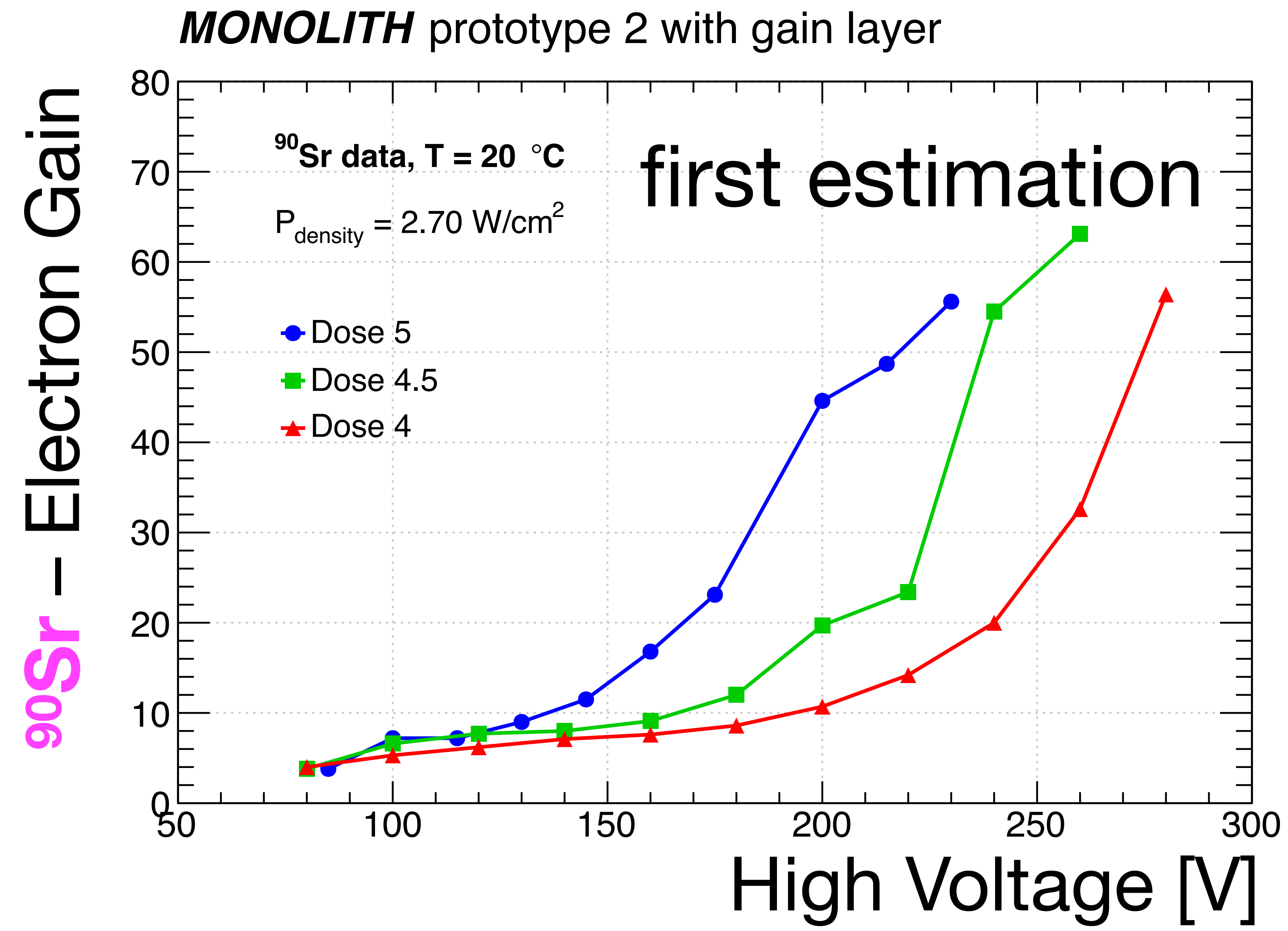


^{55}Fe measurements

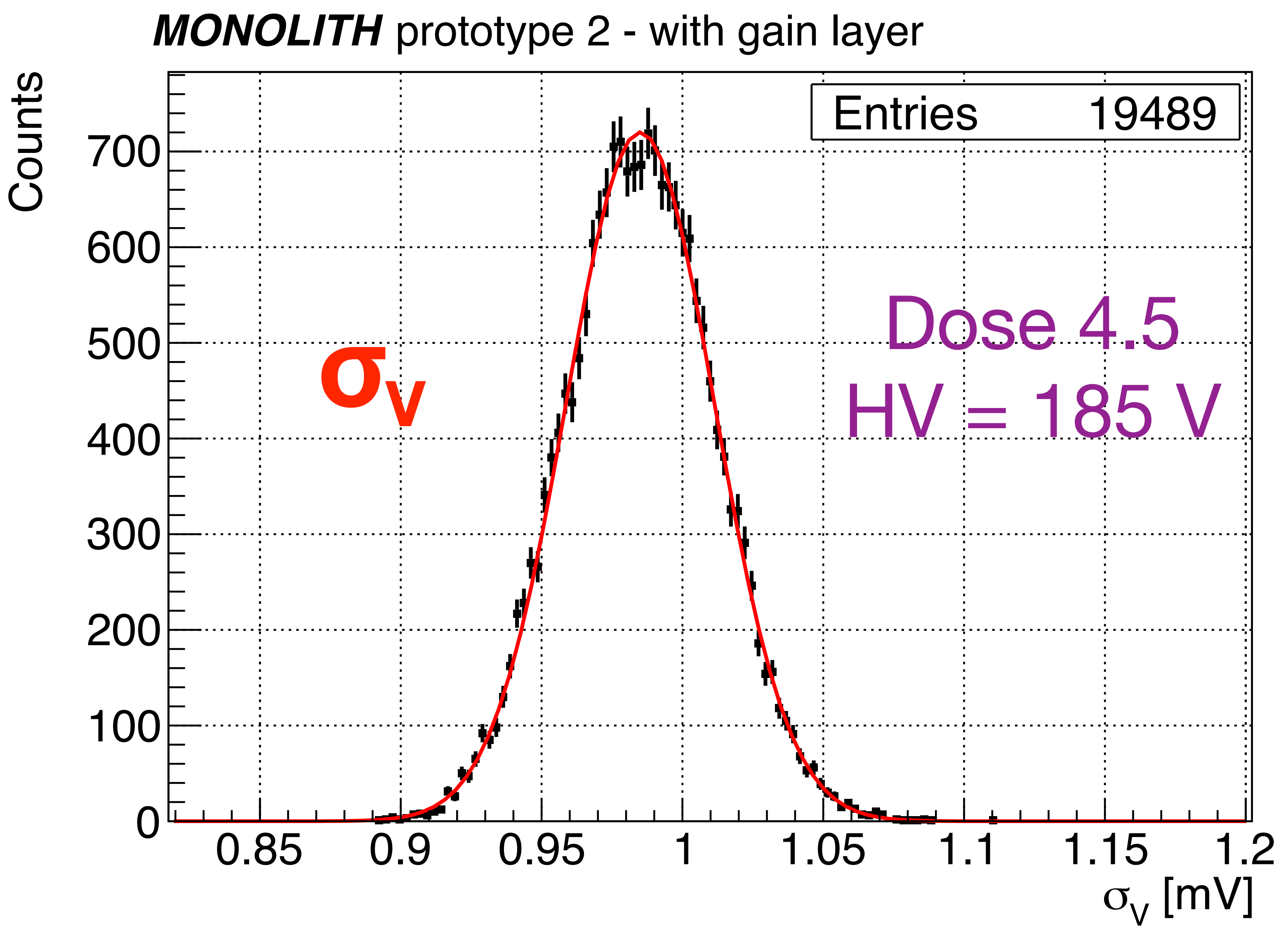
Charge-space effects limit e⁻ gain, see JINST 17 P10032 (2022)

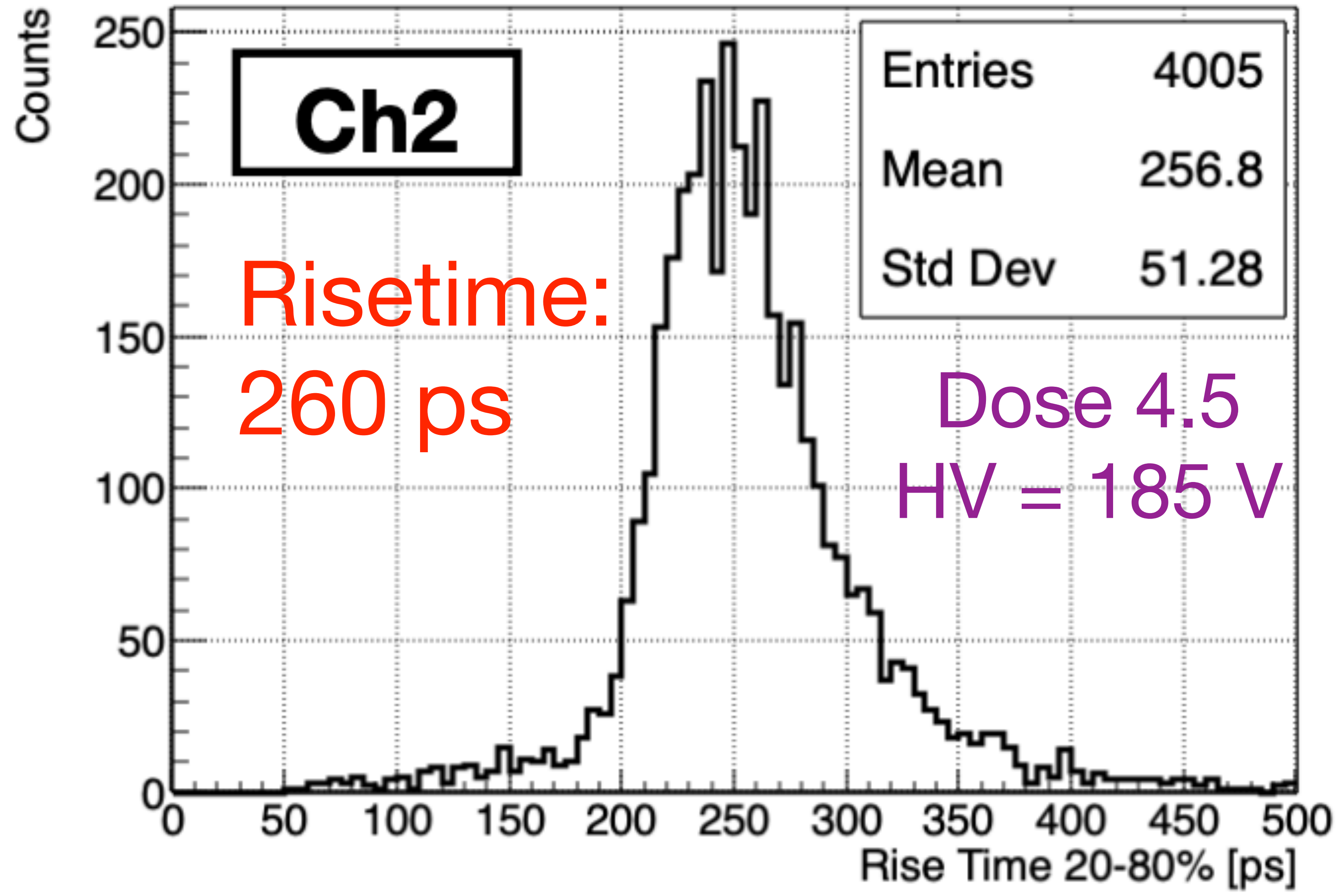
^{90}Sr measurements

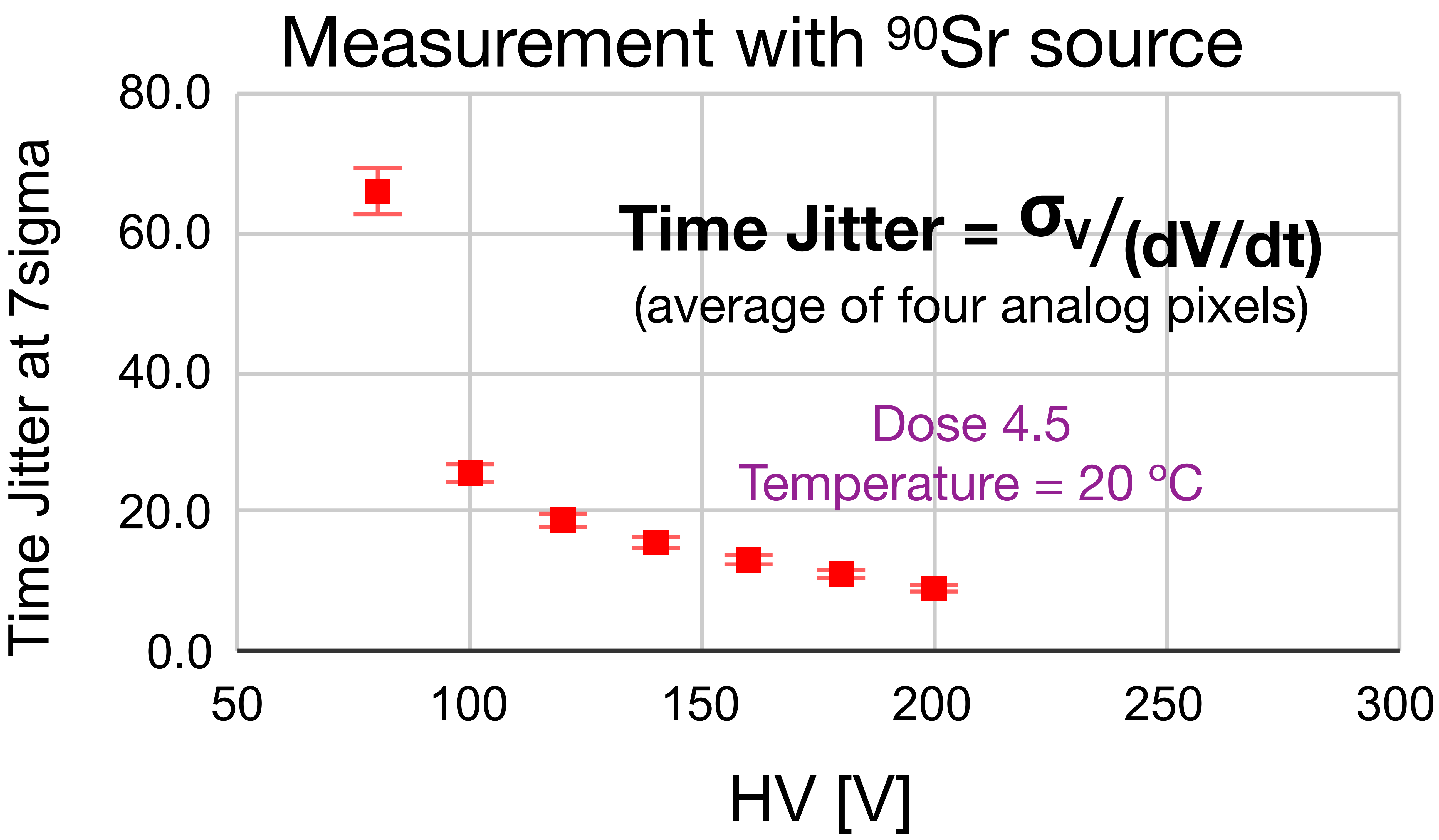




2024 PicoAD: S/N and Time Jitter





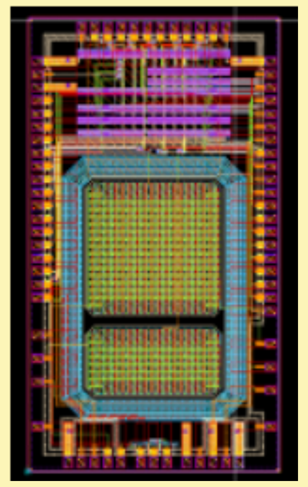


Testbeam at CERN scheduled in May

MONOLITH Project: outlook

Monolithic prototypes with SiGe BiCMOS (without internal gain layer)

2016



200ps
- 1 mm^2 pixel
- Discriminator

2017

110ps
- 30 pixels 500x500µm^2
- 100ps TDC +I/O logic

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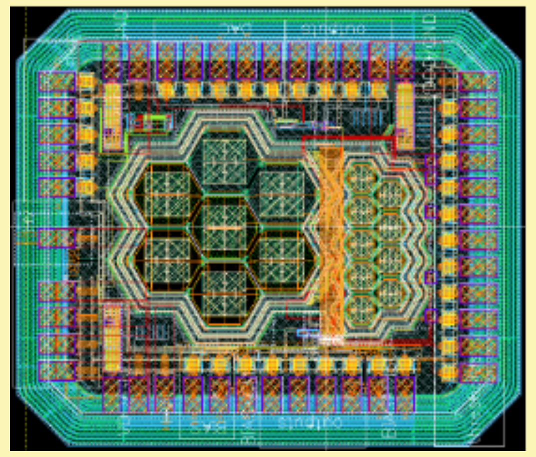
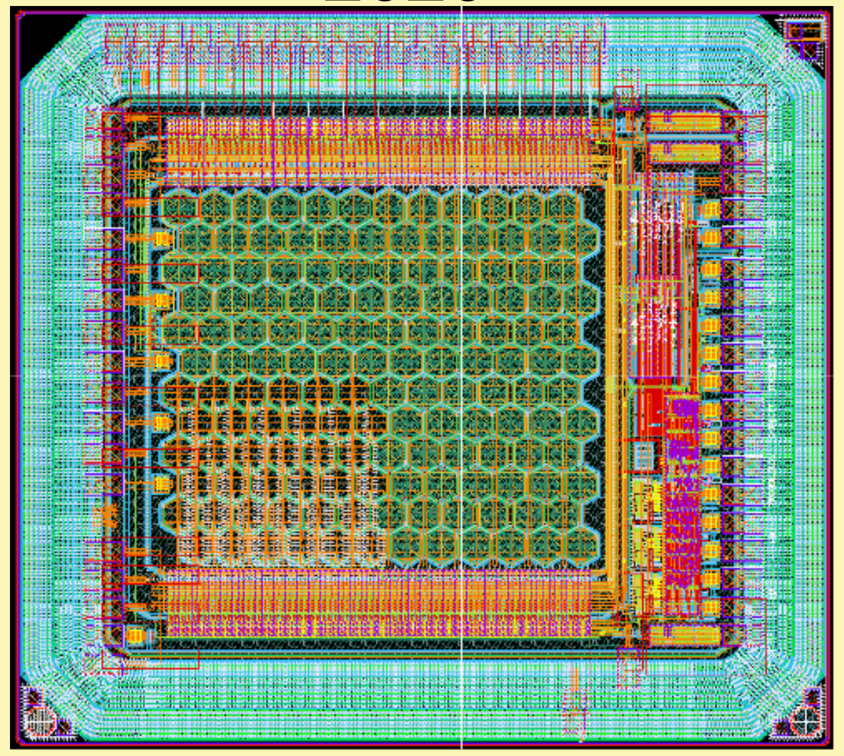


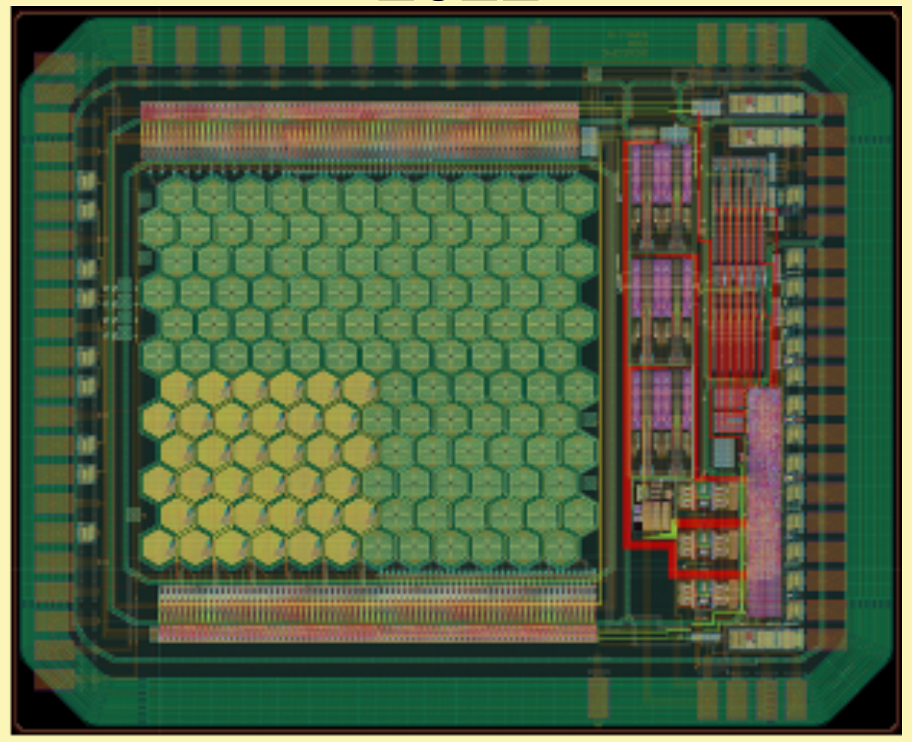
50ps
- Hexagonal pixels 100µm and 200µm pitch
- Discriminator output

MONOLITH prototype 1
2020



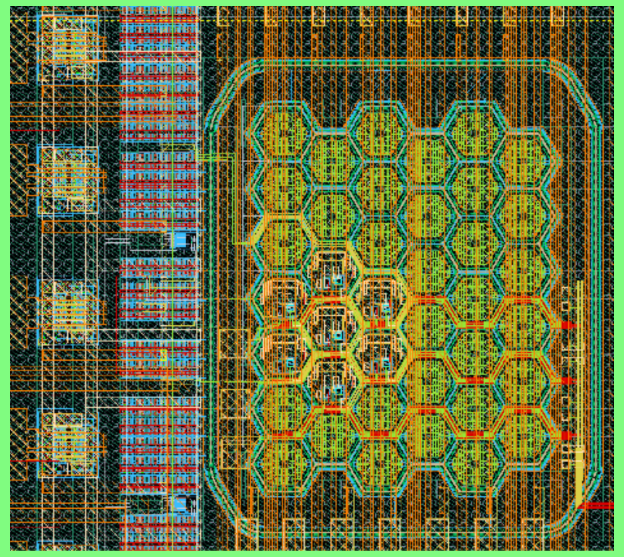
36 ps
- Hexagonal … s 100µm pitch
- 30ps TDC … ogic
- Analog cha…

MONOLITH prototype 2
2022



20 ps
- Hexagonal … s 100µm pitch
- improved e… nics
- 50µm epita… yer (350Ωcm)

MONOLITH prototype 3
2023



- Hexagonal pixels **50µm pitch**
- improved electronics (4 times less power consumption)

Monolithic prototypes
with internal gain layer:

PicoAD version
(proof-of-concept)
17 ps

PicoAD version
(received: **Jan. 2024**)

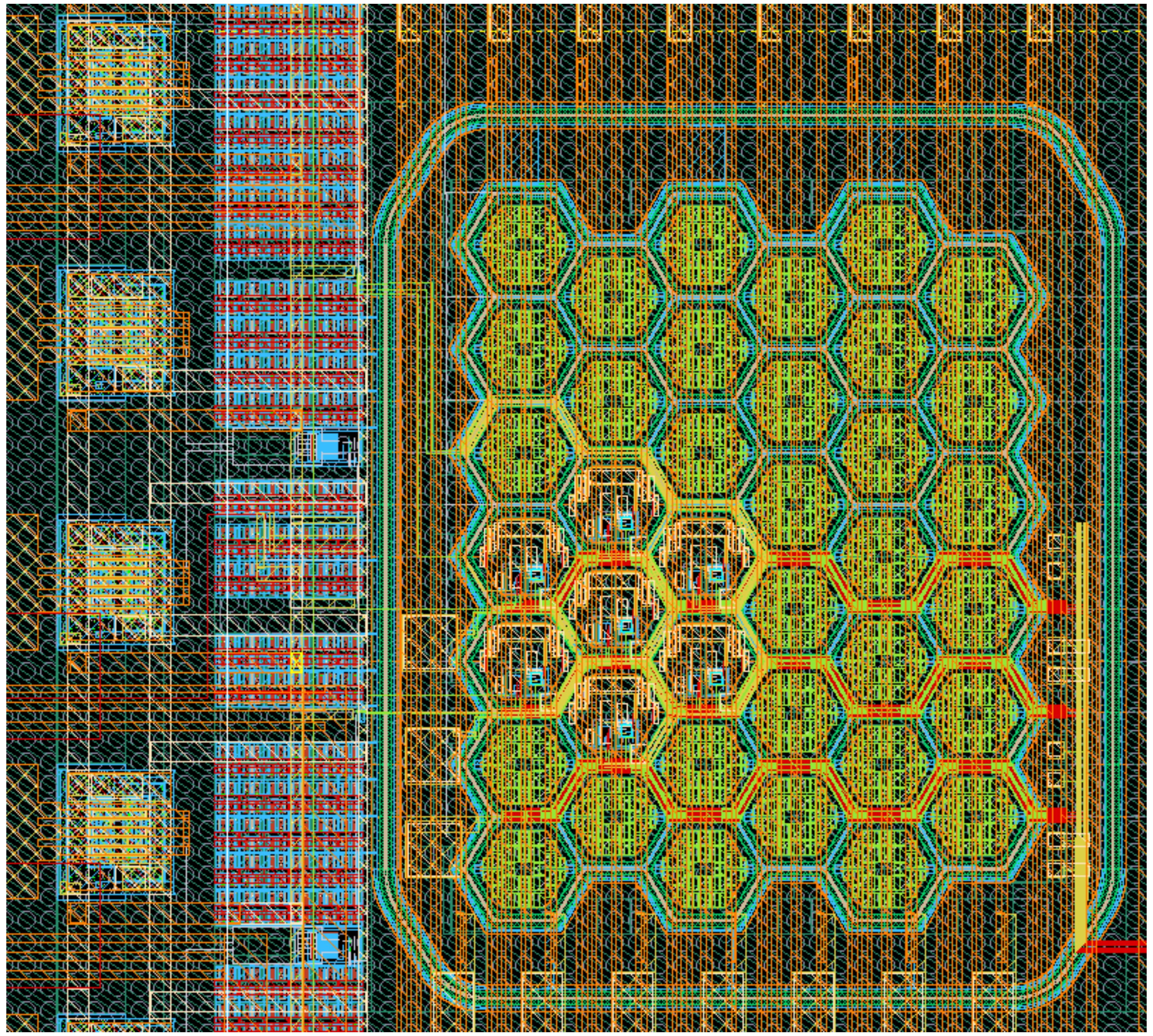
MONOLITH prototype3: 50μm pitch

- New prototype: pixels with **50μm pitch**
  - smaller capacitance

- **improved FE electronics**
  - same timing performance with 4-times less power/channel
  - 3 different configurations:
    - ➡ analog output with FE in pixel
    - ➡ analog output with FE off pixel
    - ➡ discriminated output with FE and discriminator in pixel
  - reduced inter-pixel distance from 10μm to 6μm
    to maintain time resolution at pixel edges

- Back from foundry in June 2023
  - testbeam at CERN SPS late August 2023; analysing data
  - PicoAD version to be submitted in 2024

prototype 3 (2023)

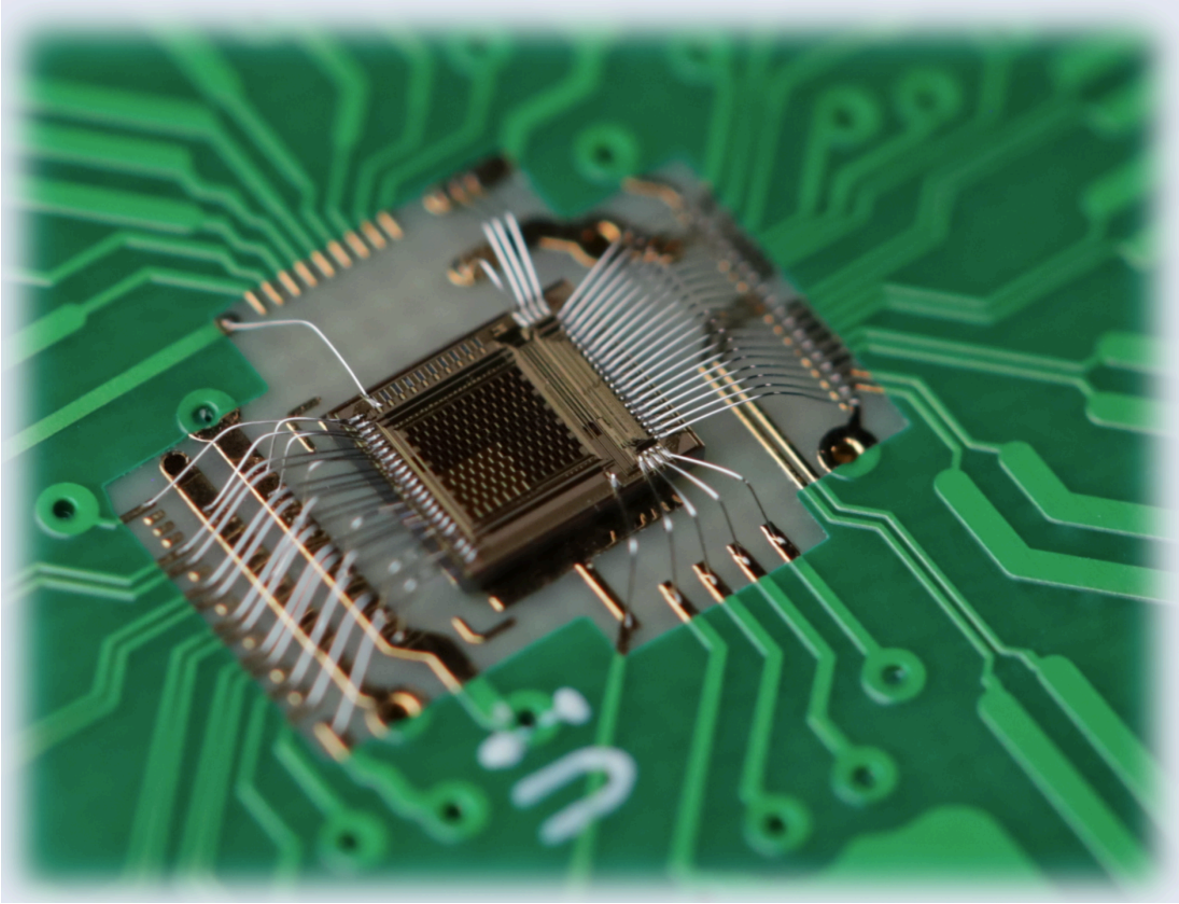


Summary

Our monolithic prototype ASIC **without gain** produced in SiGe BiCMOS provided:

- Not irradiated: **Efficiency = 99.8%** and **time resolution = 20 ps**
- **1×10^{16} n_{eq}/cm^2**: **Efficiency = 99.6%** and **time resolution = 45 ps** (200→300V)

- **Laser** measurement: down to 2.7 ps.

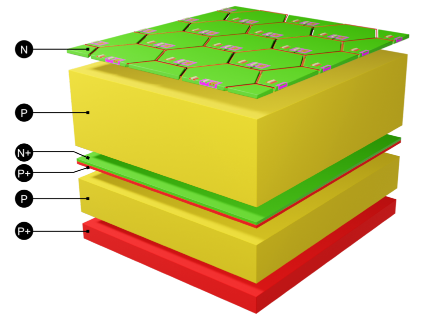


This performance was obtained **without gain layer**

SiGe BiCMOS is a serious candidate for future 4D trackers (and much more)

PicoAD — Summary & Outlook

PicoAD



The PicoAD© sensor works (*JINST* 17 (2022) 10 P10032 ; *JINST* 17 (2022) 17 P10040)

Testbeam of the monolithic proof-of-concept ASIC provided:

- **Efficiency = 99.9 %** including inter-pixel regions
- **Time resolution σ_t = (17.3 ± 0.4) ps**
  13 ps at center and **25 ps** at pixel edge
  (although sensor not yet optimized for timing)

New **PicoAD** prototypes optimised for timing back from foundry in **January 2024.**

The prototypes work.   Lab measurements going on.