ToASt : a 64-channel ASIC for the readout of the Silicon Strip Detectors of the PANDA experiment

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PANDA MVD

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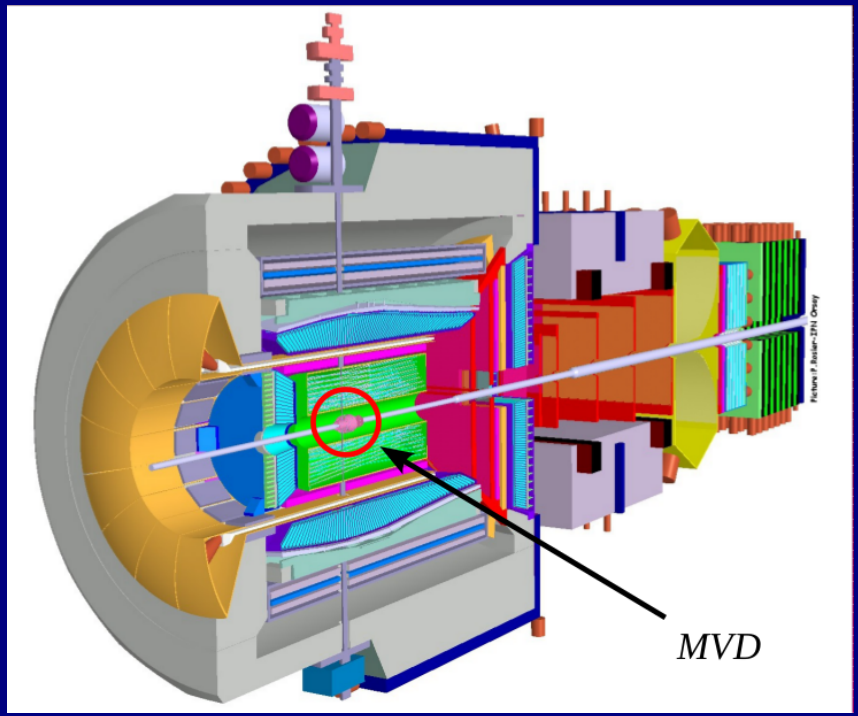
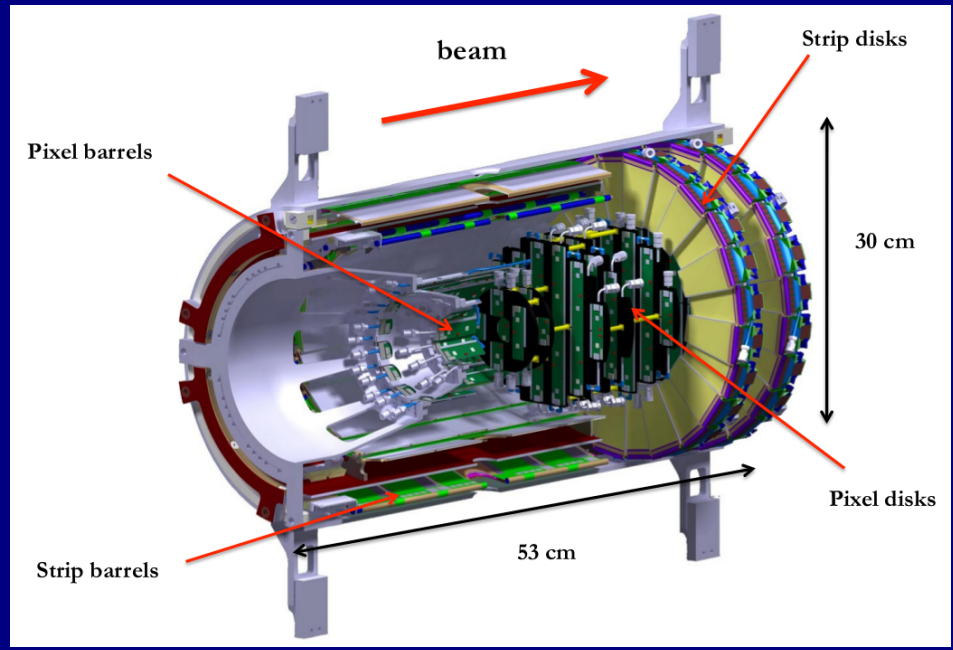
Outline

- The PANDA experiment and its Micro Vertex Detector (MVD)
- Requirements for the readout architecture
- The ToASt project
  - Specifications
  - ToASt architecture
- Test results
- Radiation test results
- Beam test preliminary results
- Conclusions

The PANDA experiment



- Located at the new FAIR facility in Darmstadt
- $\bar{p} - p$ and $\bar{p} - nuclei$ annihilation reactions
- Fixed target (a target pipe intersects the beam pipe) and triggerless experiment

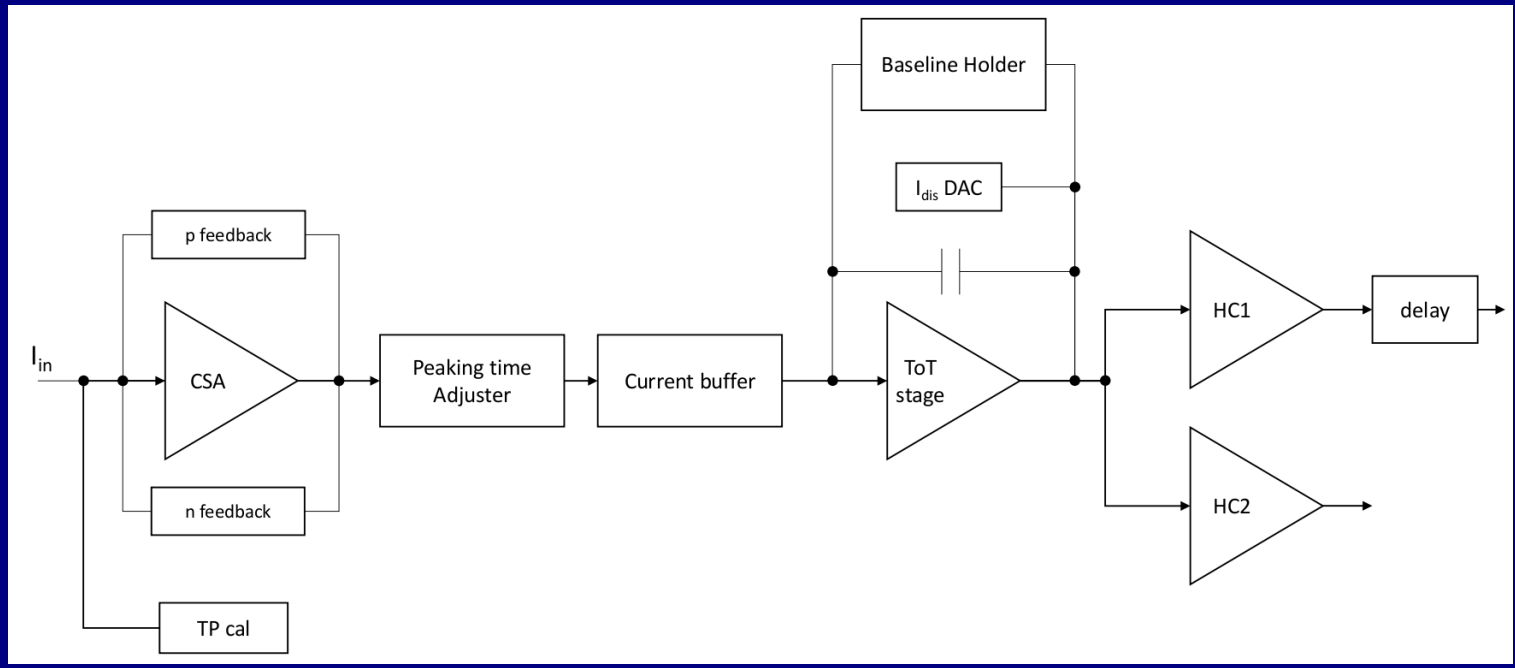


- Barrel region : 2 layers of Silicon Pixel Detectors (SPDs) + 2 of Silicon Strip Detectors
- Forward region : 4 SPDs disks, 2 SPDs + SSDs disks
- Double side SSDs

SSDs readout requirements

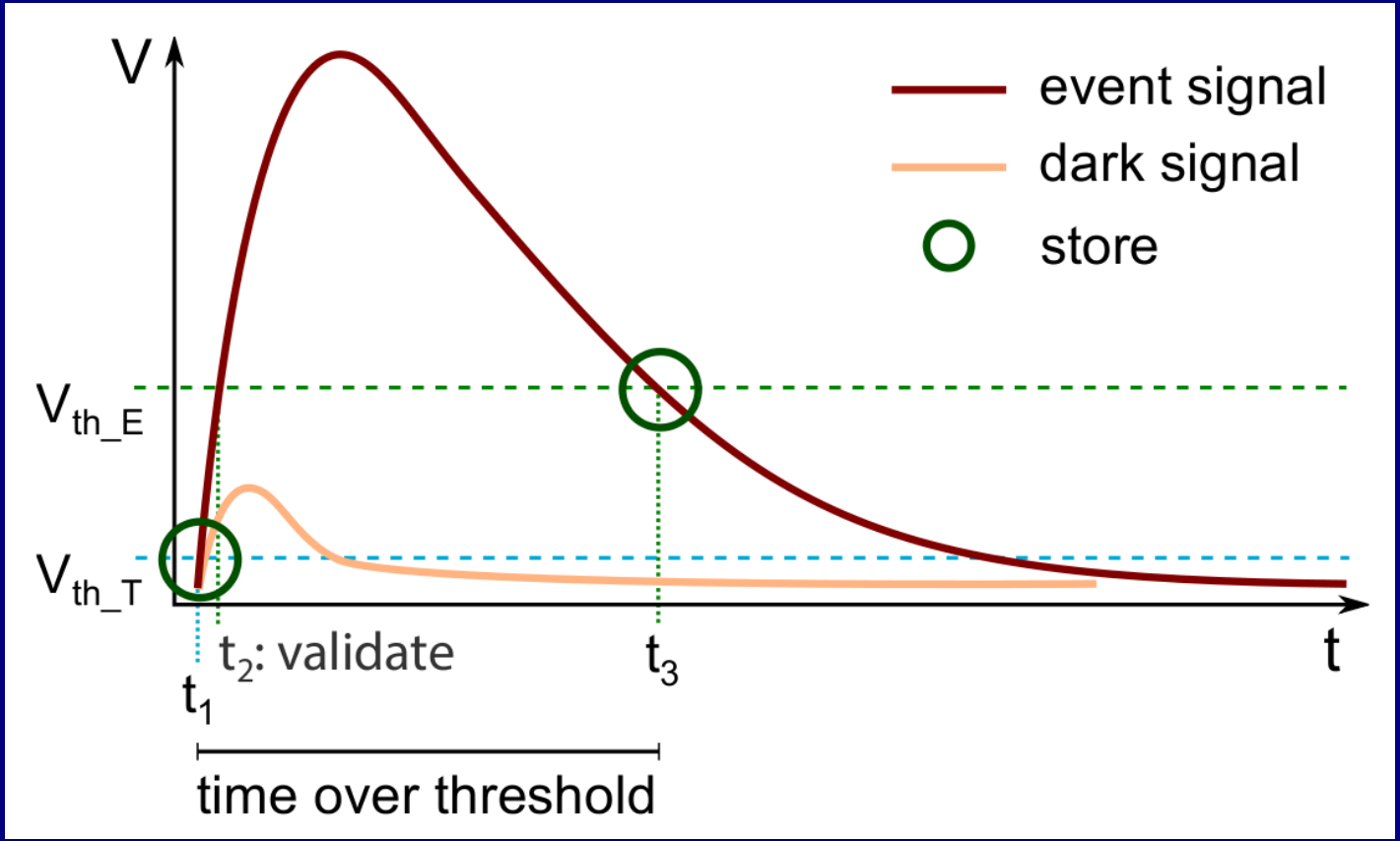
Specification	Min	Max	Unit
Channels per chip	64		
ToA (pk-pk)		6.25	ns
ToA (r.m.s.)		1.8	ns
Charge resolution	8		bits
Input charge	1	40	fC
Input capacitance	2	17	pF
Max rate per strip		40	kHz
Noise		1500	e^-
Preamp peaking time	50	$\geq$ 100	ns
Reference clock		160	MHz
Power consumption		256	mW
Radiation tolerance		20	kGy
Chip dimensions	4.5 $\times$ 3.5		mm^2
Pads position	On two sides only		

ToASt analog channel



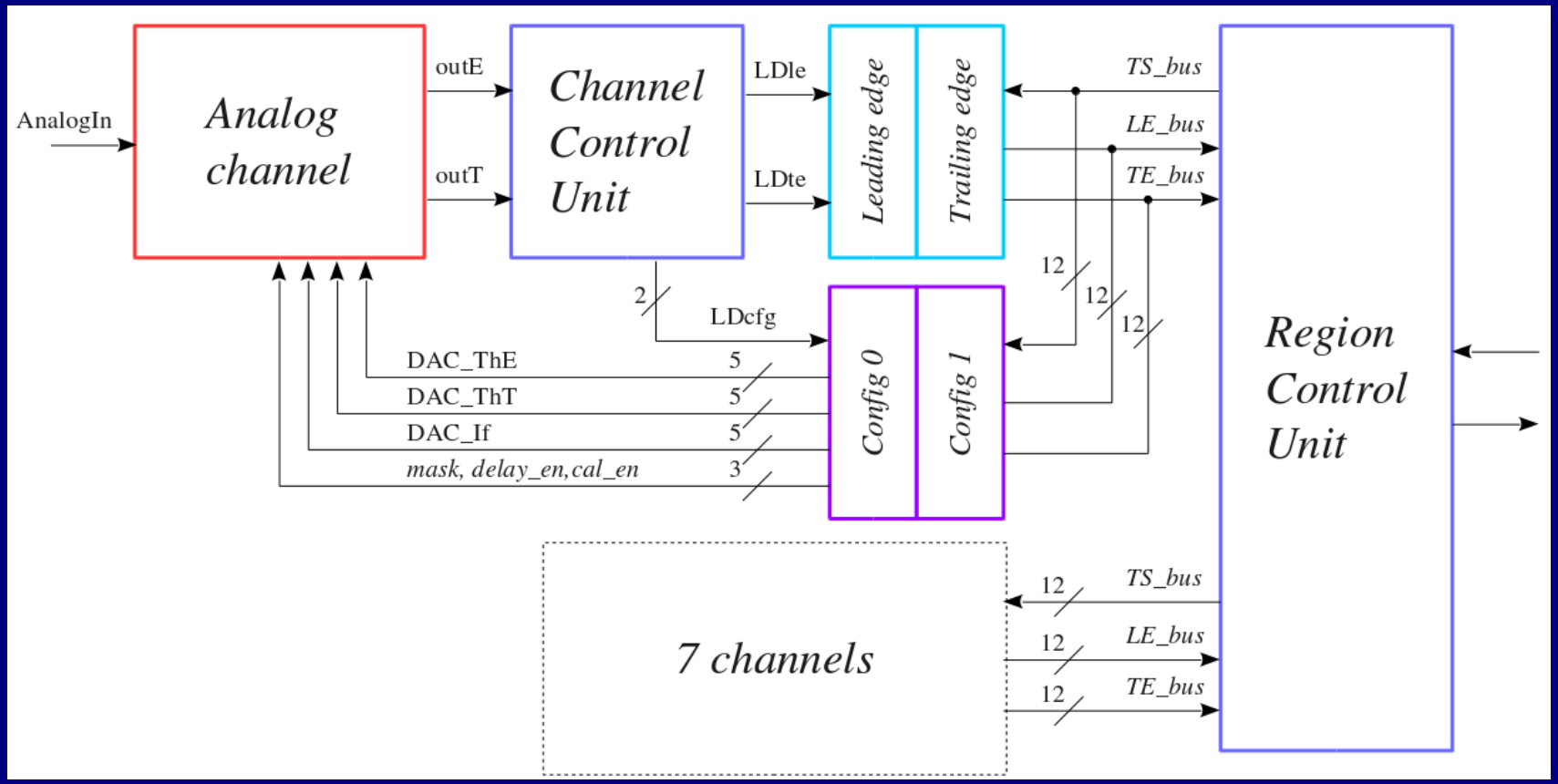
- CSA with selectable input signal polarity, gain ≈ 5 mV/fC
- Shaper with adjustable peaking time
- Current buffer
- Test pulse injection via integrated capacitor
- ToT stage with programmable discharge current
- Low frequency feedback to set baseline
- Two comparators with independent thresholds
- Local DACs for threshold and discharge current fine tuning

Time measurement



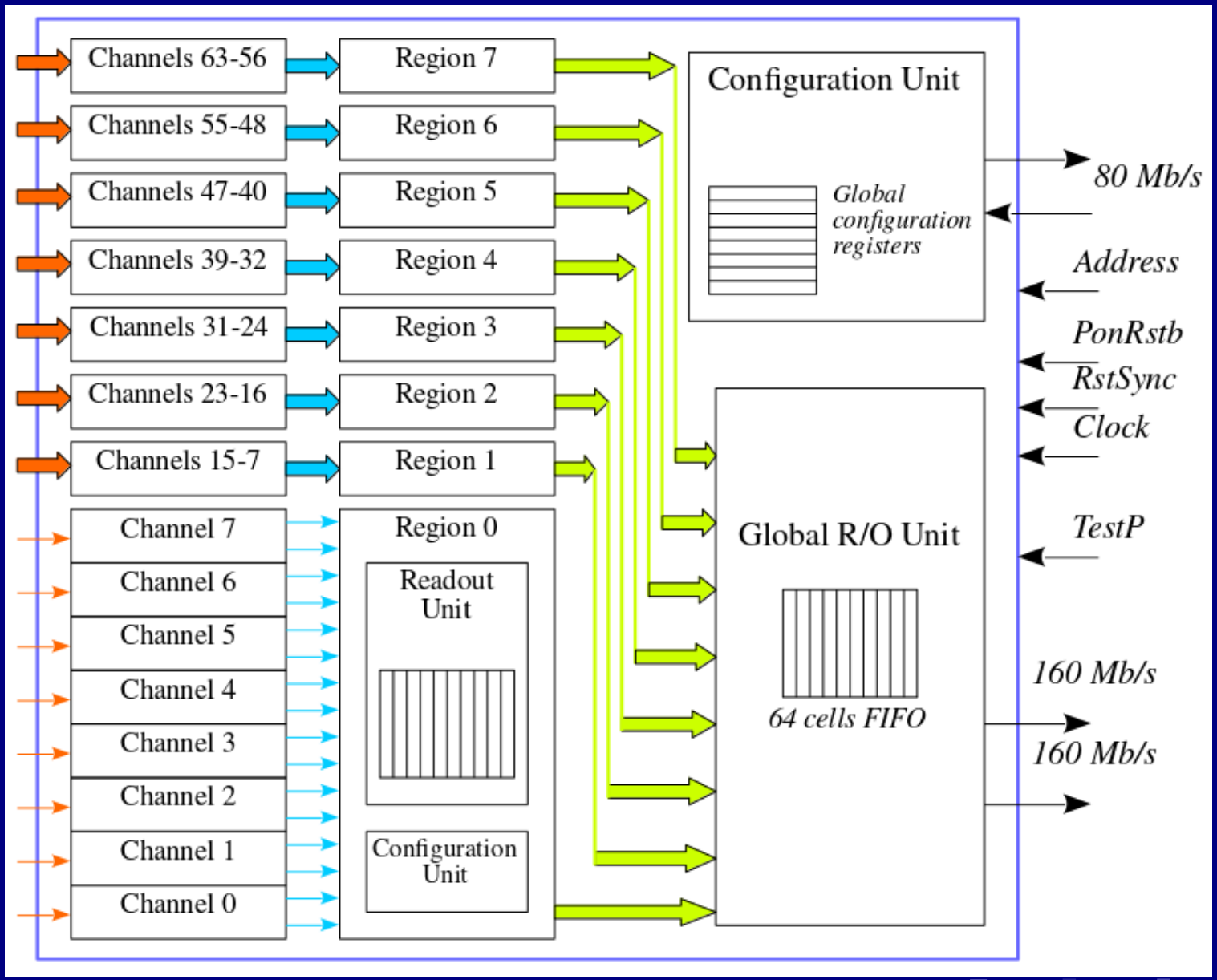
- Two thresholds : V_{thT} and V_{thE}
- Time measurement on V_{thT} to minimize jitter
- Data validated on V_{thE} to minimize noise hits
- ToT = t_3-t_1
- Double threshold validation can be disabled

ToASt channel schematic

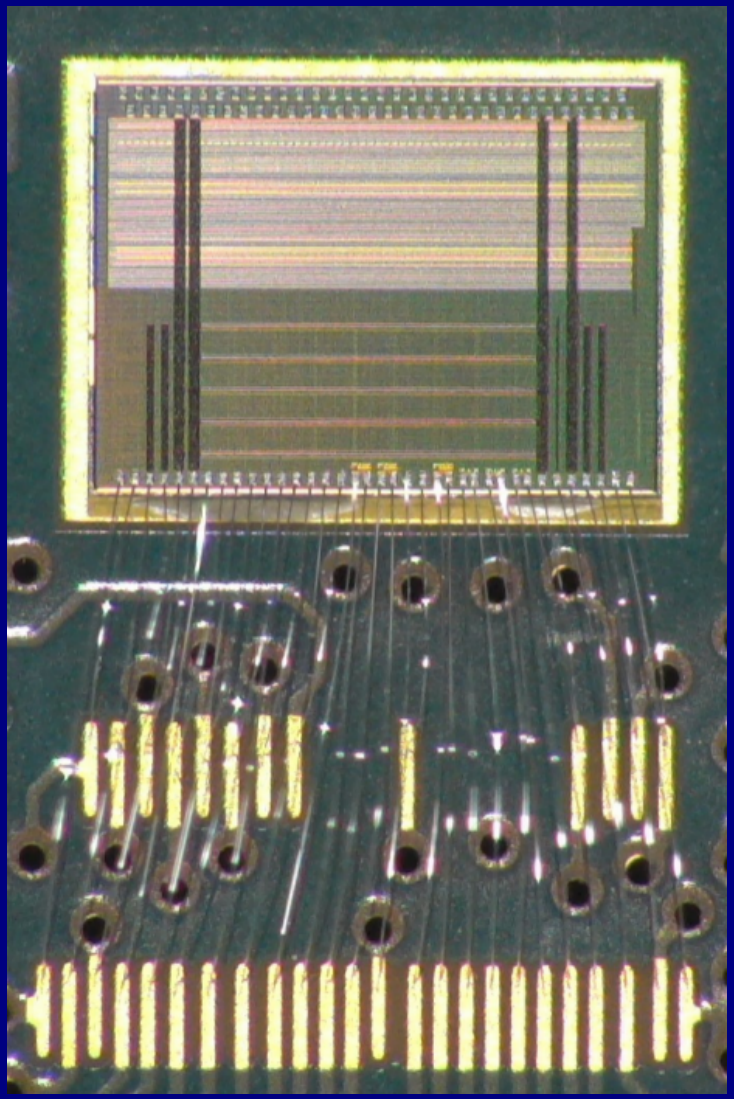


- Common time reference : 12 bits time stamp distributed to all channels
- Time stamp are Gray-encoded
- LE and TE registers latch time stamp at comparator rising/falling edges

ToASt architecture



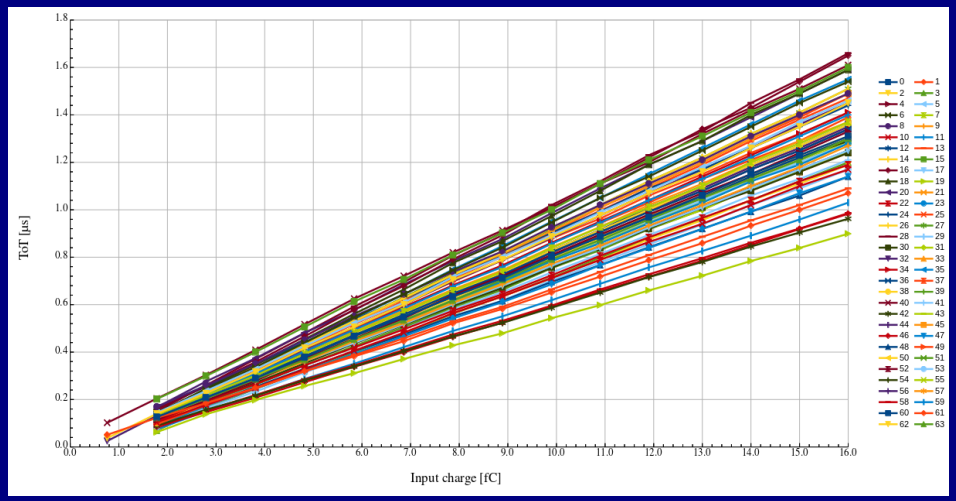
ToASt prototype



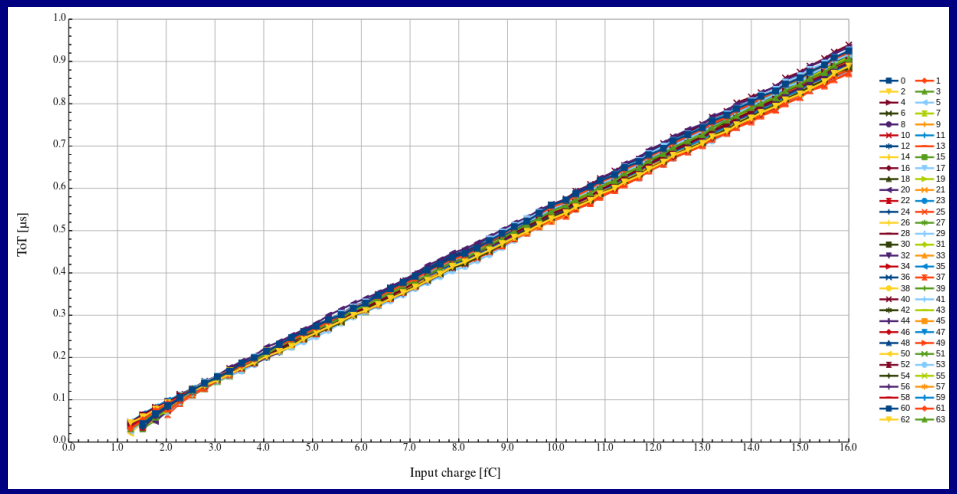
- CMOS UMC 0.11 μm technology
- Digital-on-top design flow
- Die size : 3.24 $\times$ 4.41 mm^2
- Left pads pitch (on two rows) : 63 μm
- Right pads pitch : 90 μm
- Three power domains : analog, digital, digital pads *(all supply voltages at 1.2 V)*
- One external analog reference (V_{BG} = 600 mV)
- SLVS driver/receivers
- TMR protected digital logic

Measurement - transfer function

Before calibration

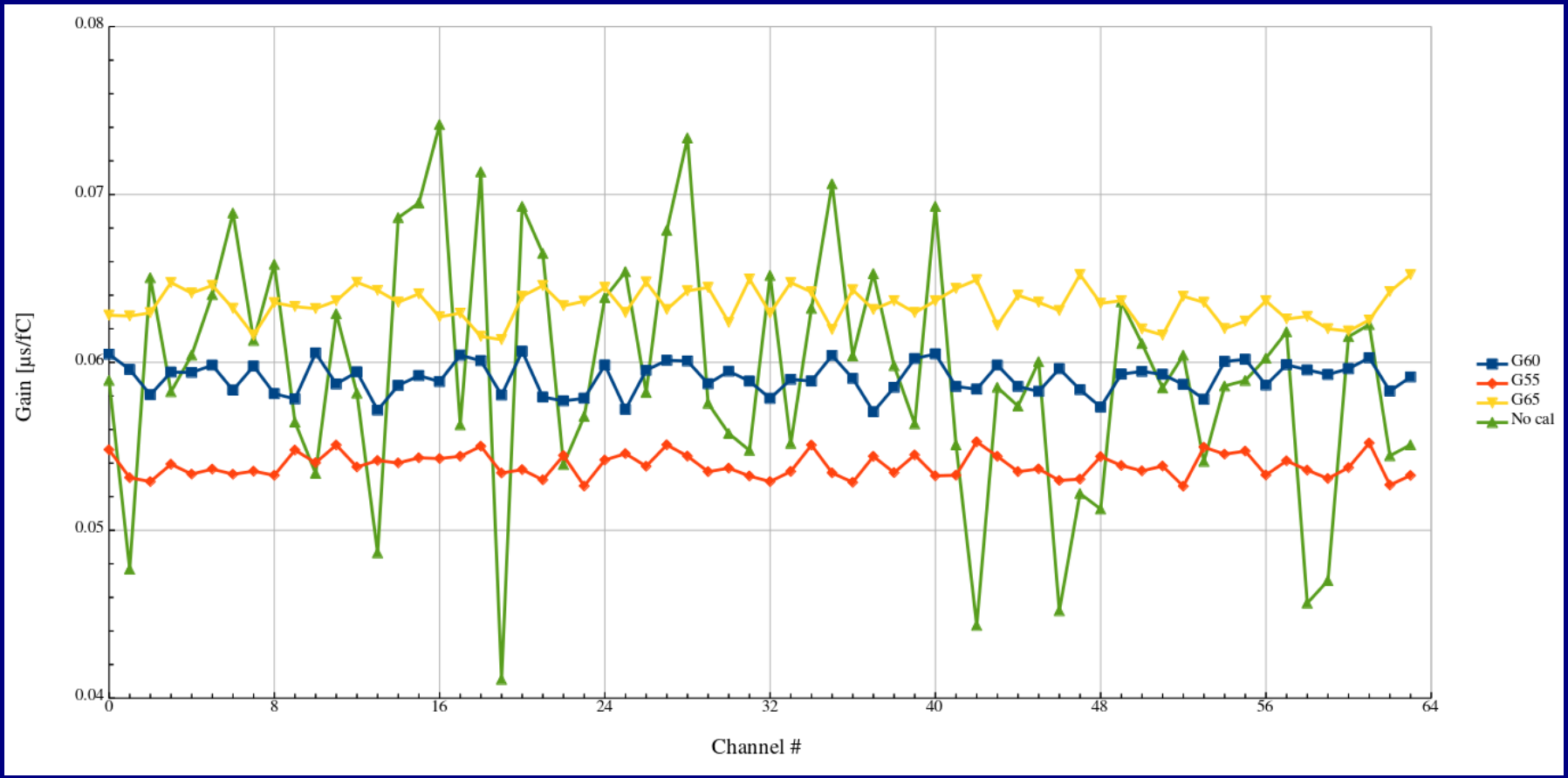


After calibration (gain & offset)



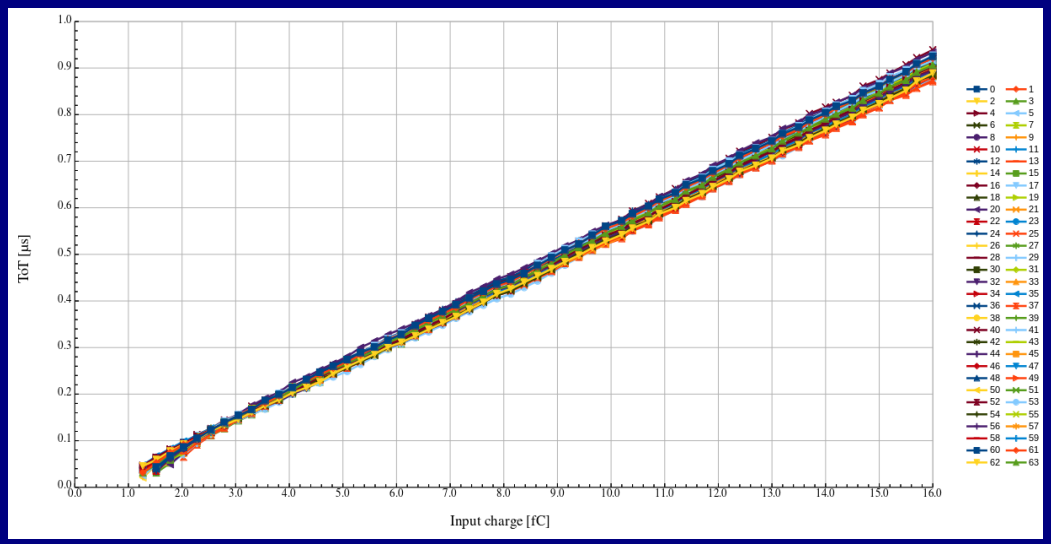
- Fully functional at 160 and 200 MHz
- Fairly large gain spread
  - *Expected : depends on a very small current*
  - Channel level gain calibration implemented - gain spread reduce from 12% to 1.7%
  - Channel level offset calibration implemented - offset spread reduced from 30% to 5.8%
- Power consumption : 180 mW @1.2 V

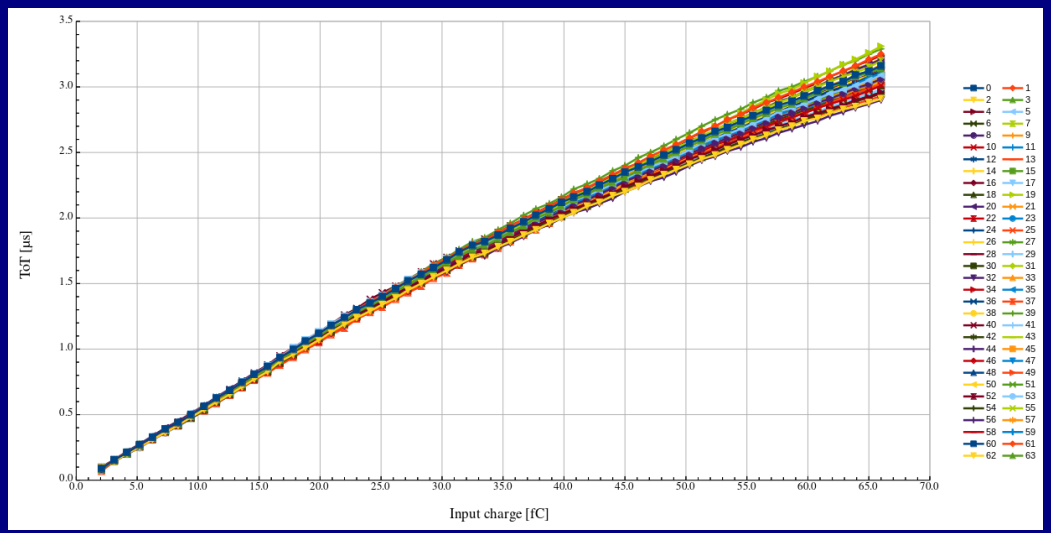
Measurement - gain calibration



- Calibration procedure :
  - For each channel, measure the transfer curve for each channel ToT Ibias DAC value
  - Select a reference gain
  - For each channel, select the DAC value providing the gain closest to the reference

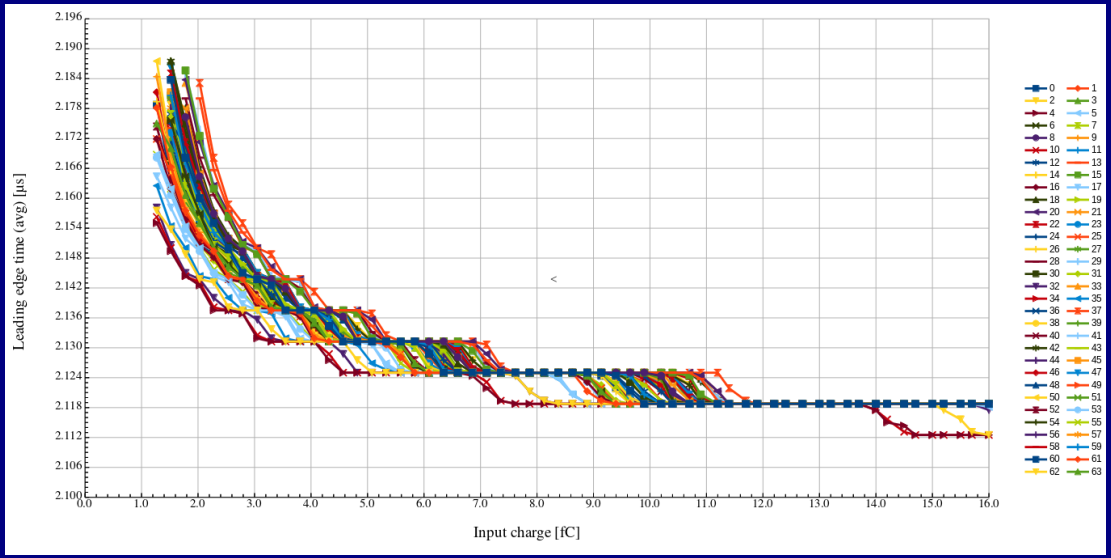
Measurement - test pulse ranges

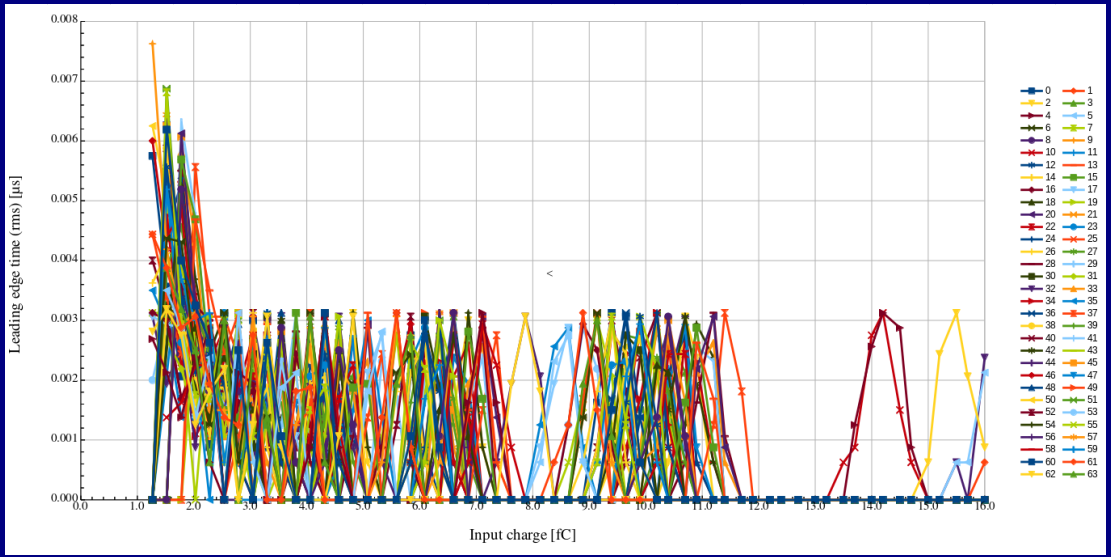




- Test pulse input with internally programmable amplitude via 6+1 bit internal DAC.
- Two test pulse ranges *(the +1 bit)* :
  - Normal range : up to 16 fC, step 0.25 fC
  - Extended range : up to 66 fC, step 1.03 fC
- Non linearity (rms) $<$0.64% in the 2$\div$16 fC range

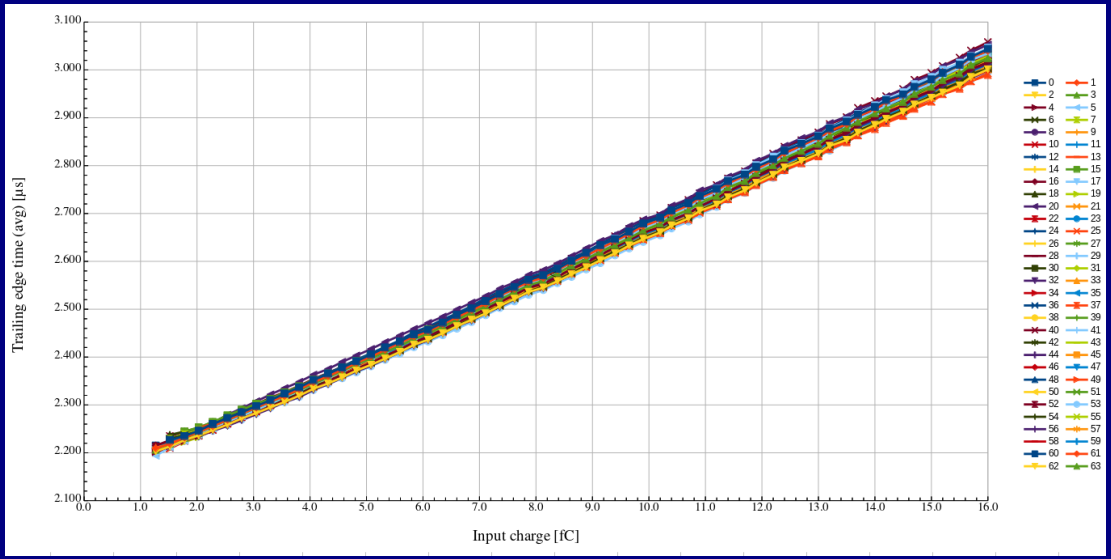
Measurement - leading edge

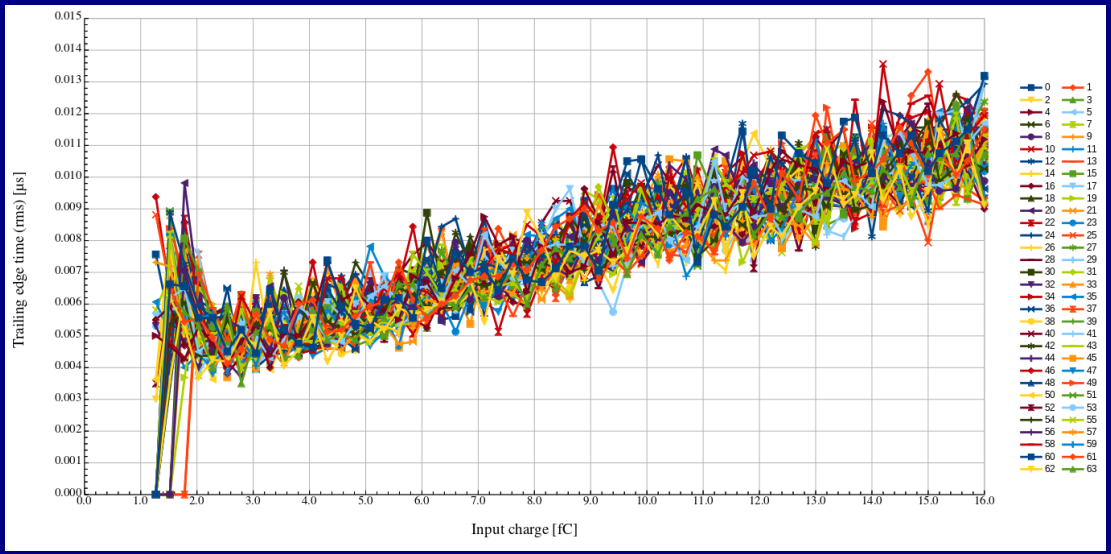




- Test : test pulses synchronous with reset
- Leading egde time
  - Average *(top)*
  - rms *(bottom)*
- Events per channel : 100
- Time bin : 6.25 ns

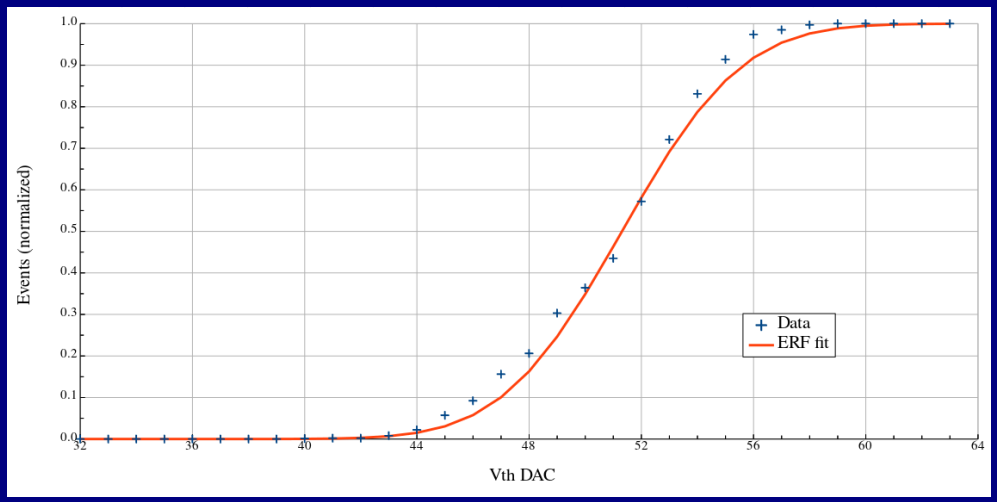
Measurement - trailing edge

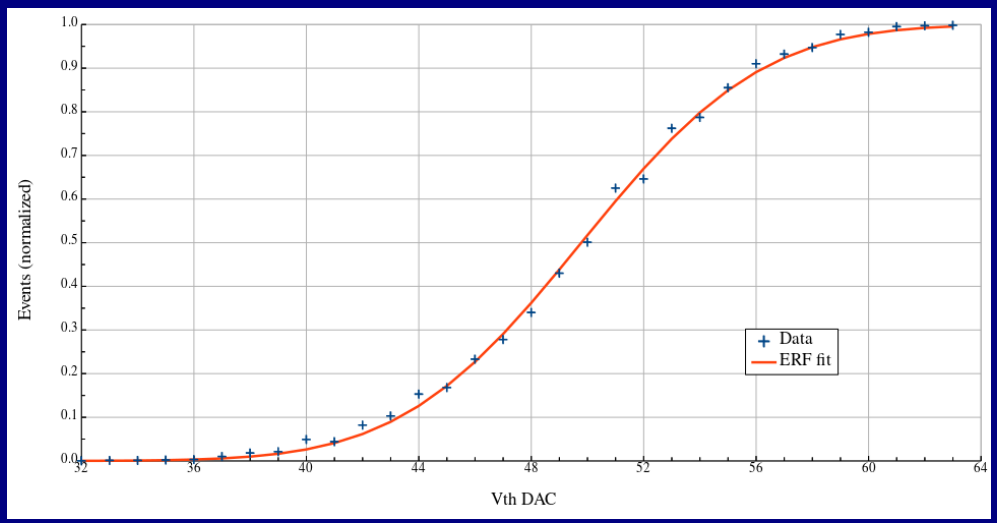




- Test : test pulses synchronous with reset
- Trailing egde time
  - Average *(top)*
  - rms *(bottom)*
- Events per channel : 100
- Time bin : 6.25 ns

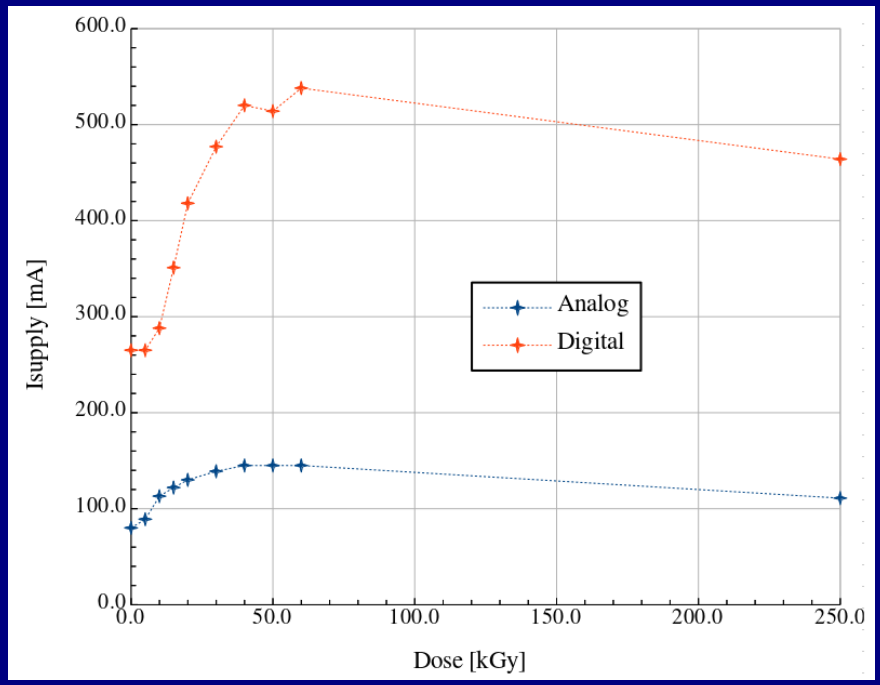
Measurement - noise

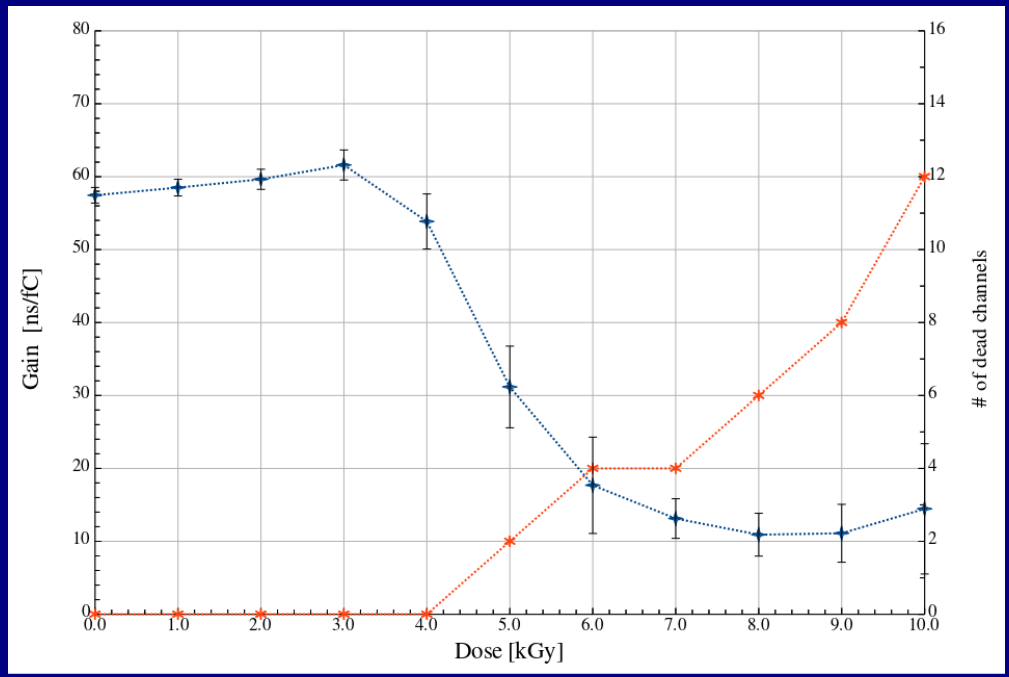




- S-curve obtained with channel threshold scan
  - Test pulse resolution and global threshold resolution too coarse
  - Baseline resolution gives similar results but with fewer points
- Conversion from DAC codes to input charge from simulations
- No input capacitance
- Average noise : 0.034 fC (211 e^-)
- Maximum noise : 0.05 fC (312 e^-)

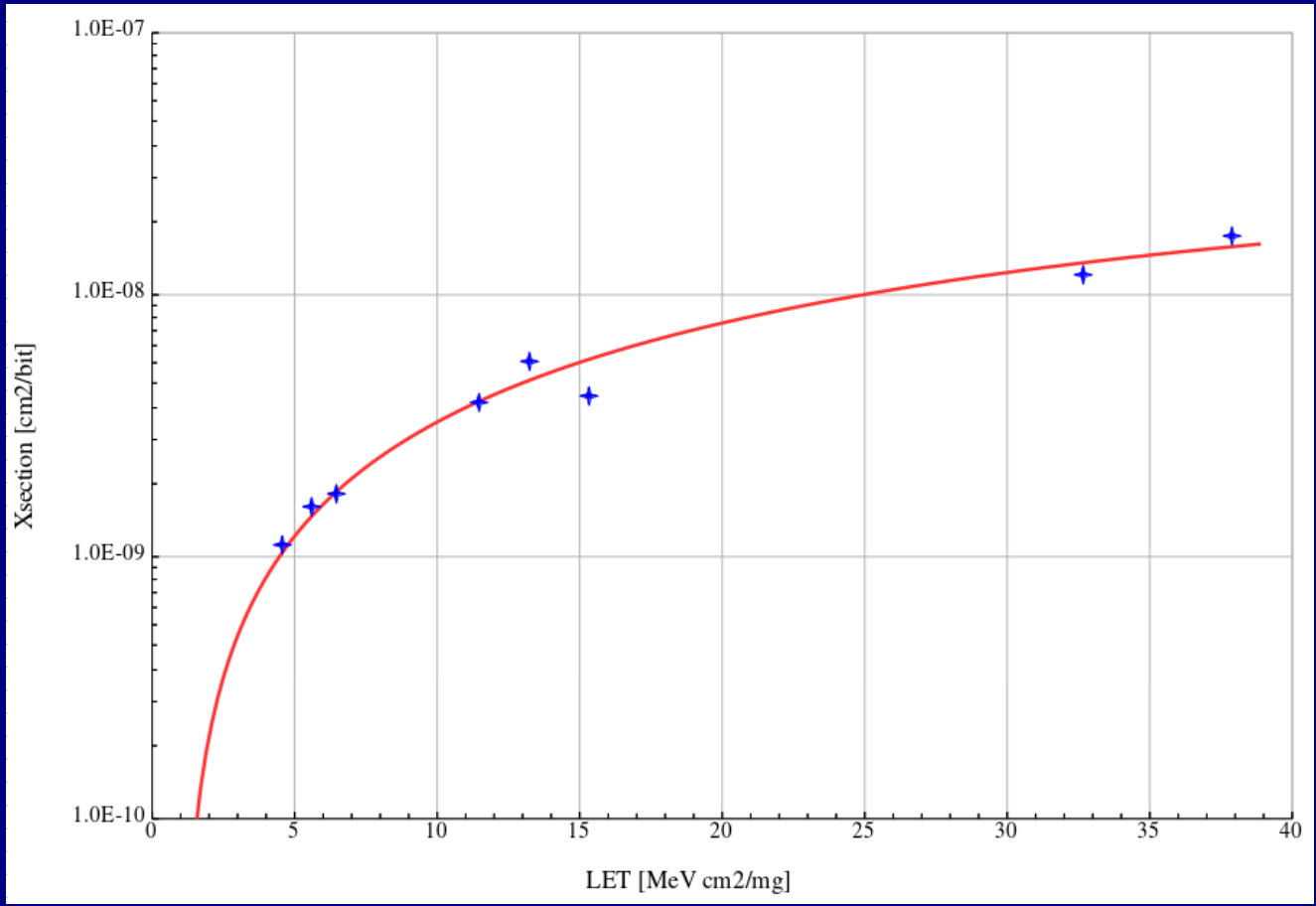
TID test *(@ University of Padova)*





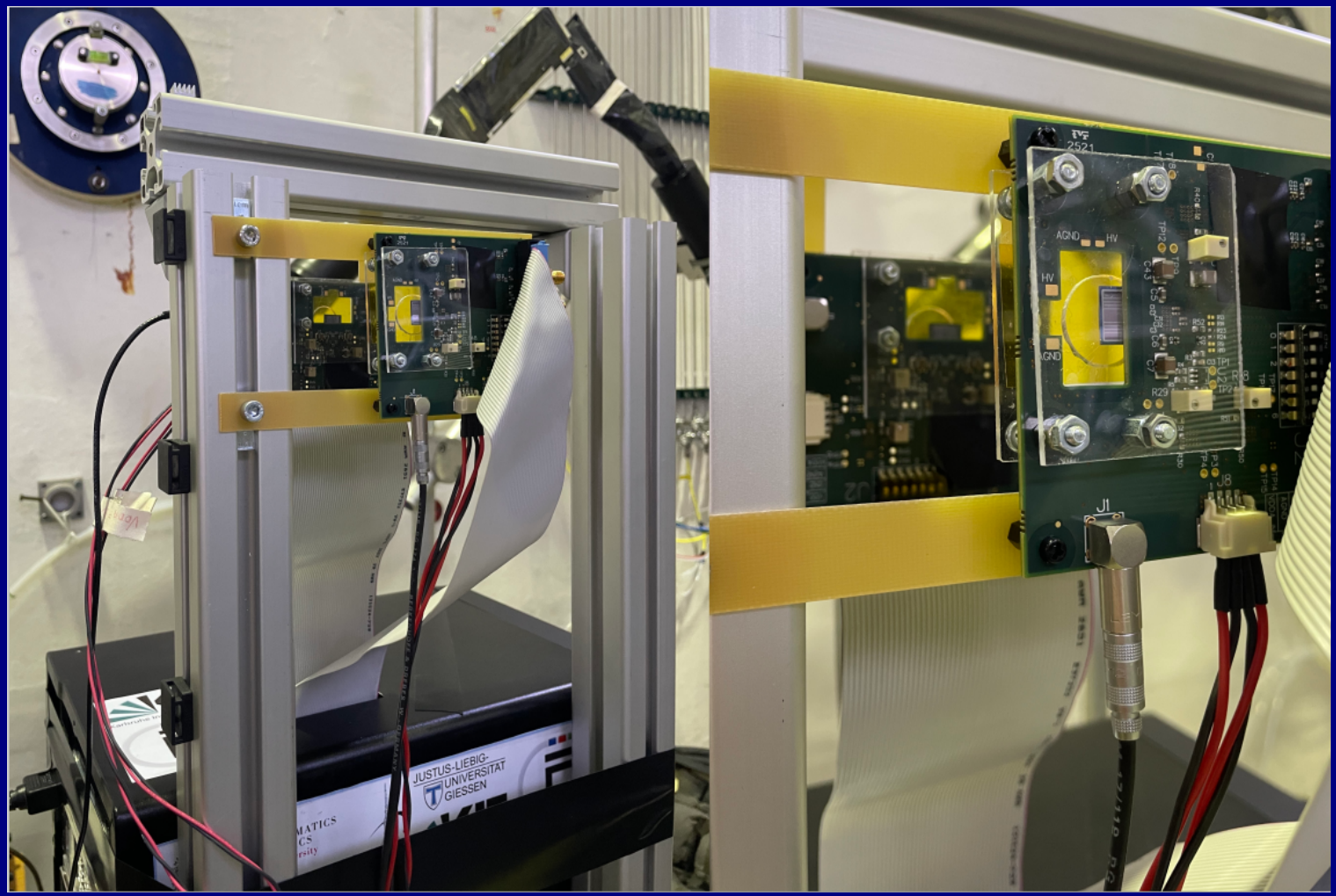
- Digital interface still working after 250 kGy
- Power consumption increase after 10 kGy (expected : leakage current in MOS)
- Gain drop after 4 kGy (unexpected)
- Full recovery after high T annealing
- Problem traced back to leakage current in analog switches
  - Enclosed layout has been adopted for switches in ToASt v2

SEU test *(@ INFN LNL SIRAD facility)*

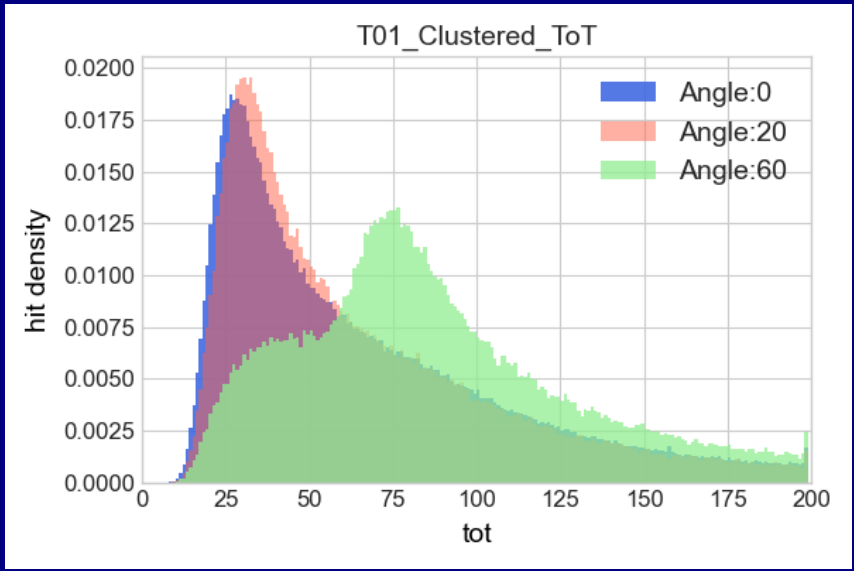


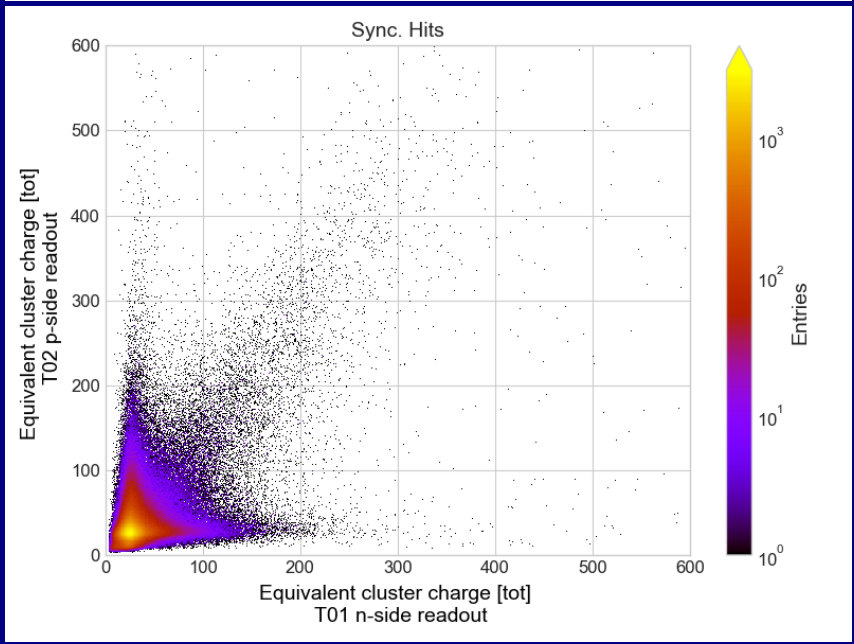
- Ion fluence $\sim 5 \cdot 10^7$ per ion
- Estimated cross section for 200 MeV protons : 3×10^{-15} cm^2
- Hadron flux 5×10^6 hadrons/(cm$^2 \times$s) $\rightarrow 9.3 \times 10^{-2}$ errors/(h chip)
- Only 1$\rightarrow$0 errors observed - triplication error found in the Verilog code

Beam test at COSY - experimental set-up



Beam test at COSY - some preliminary results





- Two test beams at COSY (FZJ Julich) in July and August 2023
- Proton beam, momentun range 2-3 GeV/c, intensity range $10^7 \div 10^8$
- Parasitic beam
- Double-sided strip detector, 285 μm thick, pitch 90 μm
- FPGA-based DAQ from KIT
- Analysis ongoing

Conclusions

- A 64 channels ASIC, named ToASt,has been designed for the readout of the silicon strip detectors of the PANDA MicroVertex Detector
  - Each channel provides particle time of arrival (ToA) and energy deposited informations (via ToT)
  - The particle ToA and ToT and channel address are packed in a 32 bits data word and trasmitted via 1(2) 160 Mb/s serial link(s)
  - A slower (80 MS/s), bidirectional serial link is used for ASIC configuration
- ToASt is designed in a commercial CMOS 0.11 μm technology
  - The control logic has been designed with TMR techniques for SEU protection
- Test results :
  - Lab tests show that the ToASt performances are as expected
  - First ToASt tests with detector in a beam test shows excellent results
  - Radiation tests showed a couple of weakness in the radiation tolerance of the ASIC. The issues has been identified and has been corrected in the next version, which will be submitted in March 2024.

Spare slides

ToASt main characteristics

- 64 input channels
- Time of Arrival (ToA) and Time over Threshold (ToT) measurements
- Master clock frequency : 160 MHz
- Region : groups of 8 channels with local FIFO
- Second level FIFO buffering for the 8 regions
- Two output serial links at 160 Mb/s
- Serial configuration protocol at 80 Mb/s
- Full SEU protection via Triple Modular Redundancy
- CMOS 0.11 μm technology

Output data format

- Data output in 32 bits words over 160 Mb/s serial links
- It can be configured to use 1 or 2 links
- Frame : rollover time for the time stamp counter, i.e. 25.6 μs at 160 MHz
- Data within a frame are packed within a frame header and a frame trailer
- Frame header contains chip id and frame number
- Frame trailers contains the number of valid samples and CRC

Packet type	Header *2 bits*	Data *30 bits*
Data	11	Region[2:0] Channel[2:0] Le[11:0] Te[11:0]
Header	10	10 ChipId[6:0] Reserved[12:0] FrameN[7:0]
Trailer	01	01 DataCnt[11:0] CRC[15:0]
Sync	00	00 1100 1100 1100 1100 1100 1100 1111

Radiation tolerance

- Total Ionizing Dose : no special techniques have been adopted to increase the TID tolerance of ToASt. However, other studies [1] show that the technology is sufficiently radiation tolerant for the PANDA MVD application
- Single Event Effects : the digital logic has been protected via Triple Modular Redundancy using the TMRG tool [2]
  - Only channel and region registers are left non-triplicated to save power
  - Clock and reset nets are triplicated
  - Synchronous reset net
  - Minimum distance between triplicated DFF set to 20 μm

[1] E.Riceputi et al., "Total ionizing dose effects on CMOS devices in a 110 nm technology", IEEE PRIME 2017 proceedings

[2] S.Kulis, "Single Event Effects mitigation with TMRG tool", TWEPP 2016 proceedings

Test for Single Event Upset tolerance

- Test at the SIRAD facility at LNL
  - May 23^{th}-24^{th} 2022
  - Beam time : 48 hours

Ion	Angle	Energy $[MeV]$	LET $[MeV \cdot cm^2/mg]$	Fluence $[ions/cm^2]$
O	0°	95.4	4.57	$6.31 \cdot 10^7$
F	0°	110.7	5.60	$1.01 \cdot 10^8$
F	30°	110.7	6.47	$3.03 \cdot 10^7$
Si	0°	141.6	11.47	$6.80 \cdot 10^7$
Si	30°	141.6	13.24	$4.11 \cdot 10^7$
Cl	0°	162.7	15.33	$4.99 \cdot 10^7$
Br	0°	218.9	32.67	$4.39 \cdot 10^7$
Ag	0°	247.0	37.89	$1.52 \cdot 10^7$

Aim : estimate the SEU rate at LHC from ions cross section

(reference : M.Huhtinen and F.Faccio, Computational method to estimate Single Event Upset rates in an accelerator environment, NIM A 450 (2000) pp 155-172)

Simulation results - event loss probability

Chip n.	Input events	Output events	Lost events	N. of frames	Link occupancy Tx0	Link occupancy Tx1
0	208	205	3	29	4.82%	3.84%
1	135	133	2	30	3.69%	3.02%
2	192	190	2	29	4.75%	3.70%
3	169	163	6	30	4.18%	3.40%
4	164	161	3	30	4.27%	3.30%
5	149	142	7	30	3.81%	3.25%
6	140	132	8	30	3.70%	3.03%
7	102	100	2	29	3.27%	2.57%
8	179	178	1	30	4.78%	3.15%
9	162	159	3	30	4.37%	3.14%
10	207	196	11	30	5.01%	3.40%
11	166	165	1	29	4.60%	2.95%
Single driver						
10	207	196	11	30	6.83%	0%
11	166	165	1	29	6.01%	0%

- HDL simulations with data from PANDA physics simulations
- Barrel case (similar results with the forward case)
- Lost events : 2.5%
- Event loss due to FE dead time