ToASt : a 64-channel ASIC for the readout of the Silicon Strip Detectors of the PANDA experiment


PANDA MVD

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The PANDA experiment and its Micro Vertex Detector (MVD)

Requirements for the readout architecture

The ToASSt project
  - Specifications
  - ToASSt architecture

Test results

Radiation test results

Beam test preliminary results

Conclusions
The PANDA experiment

- Located at the new FAIR facility in Darmstadt
- \(\bar{p} - p\) and \(\bar{p} - nuclei\) annihilation reactions
- Fixed target (a target pipe intersects the beam pipe) and triggerless experiment

- Barrel region: 2 layers of Silicon Pixel Detectors (SPDs) + 2 of Silicon Strip Detectors
- Forward region: 4 SPDs disks, 2 SPDs + SSDs disks
- Double side SSDs
## SSDs readout requirements

<table>
<thead>
<tr>
<th>Specification</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels per chip</td>
<td>64</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ToA (pk-pk)</td>
<td></td>
<td>6.25</td>
<td>ns</td>
</tr>
<tr>
<td>ToA (r.m.s.)</td>
<td>1.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Charge resolution</td>
<td>8</td>
<td></td>
<td>bits</td>
</tr>
<tr>
<td>Input charge</td>
<td>1</td>
<td>40</td>
<td>fC</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>2</td>
<td>17</td>
<td>pF</td>
</tr>
<tr>
<td>Max rate per strip</td>
<td>40</td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>Noise</td>
<td></td>
<td>1500</td>
<td>e⁻</td>
</tr>
<tr>
<td>Preamp peaking time</td>
<td>50</td>
<td>≥ 100</td>
<td>ns</td>
</tr>
<tr>
<td>Reference clock</td>
<td>160</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>256</td>
<td></td>
<td>mW</td>
</tr>
<tr>
<td>Radiation tolerance</td>
<td>20</td>
<td></td>
<td>kGy</td>
</tr>
<tr>
<td>Chip dimensions</td>
<td>4.5</td>
<td>3.5</td>
<td>mm²</td>
</tr>
<tr>
<td>Pads position</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G. Mazza (PANDA MVD Group)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
ToASSt analog channel

- CSA with selectable input signal polarity, gain $\approx 5 \text{ mV/fC}$
- Shaper with adjustable peaking time
- Current buffer
- Test pulse injection via integrated capacitor

- ToT stage with programmable discharge current
- Low frequency feedback to set baseline
- Two comparators with independent thresholds
- Local DACs for threshold and discharge current fine tuning
Two thresholds: \( V_{thT} \) and \( V_{thE} \)

- Time measurement on \( V_{thT} \) to minimize jitter
- Data validated on \( V_{thE} \) to minimize noise hits

\[ \text{ToT} = t_3 - t_1 \]

Double threshold validation can be disabled
Common time reference: 12 bits time stamp distributed to all channels
Time stamp are Gray-encoded
LE and TE registers latch time stamp at comparator rising/falling edges
ToAS$t architecture

Channels 63-56 → Region 7
Channels 55-48 → Region 6
Channels 47-40 → Region 5
Channels 39-32 → Region 4
Channels 31-24 → Region 3
Channels 23-16 → Region 2
Channels 15-7 → Region 1
Channel 7
Channel 6
Channel 5
Channel 4
Channel 3
Channel 2
Channel 1
Channel 0

Configuration Unit

Global configuration registers

Global R/O Unit

64 cells FIFO

80 Mb/s
Address
PonRstb
RstSync
Clock
TestP

160 Mb/s
160 Mb/s
ToASt prototype

- CMOS UMC 0.11 \( \mu \text{m} \) technology
- Digital-on-top design flow
- Die size: \( 3.24 \times 4.41 \, \text{mm}^2 \)
- Left pads pitch (on two rows): 63 \( \mu \text{m} \)
- Right pads pitch: 90 \( \mu \text{m} \)
- Three power domains: analog, digital, digital pads \((\text{all supply voltages at } 1.2 \, \text{V})\)
- One external analog reference \((V_{BG} = 600 \, \text{mV})\)
- SLVS driver/receivers
- TMR protected digital logic
Measurement - transfer function

- Fully functional at 160 and 200 MHz
- Fairly large gain spread
  - *Expected: depends on a very small current*
  - Channel level gain calibration implemented - gain spread reduce from 12% to 1.7%
  - Channel level offset calibration implemented - offset spread reduced from 30% to 5.8%
- Power consumption: 180 mW @1.2 V
Calibration procedure:
- For each channel, measure the transfer curve for each channel ToT Ibias DAC value
- Select a reference gain
- For each channel, select the DAC value providing the gain closest to the reference
Measurement - test pulse ranges

- Test pulse input with internally programmable amplitude via 6+1 bit internal DAC.

- Two test pulse ranges (*the +1 bit*):
  - Normal range : up to 16 fC, step 0.25 fC
  - Extended range : up to 66 fC, step 1.03 fC

- Non linearity (rms) <0.64% in the 2÷16 fC range
Measurement - leading edge

- Test: test pulses synchronous with reset
- Leading edge time
  - Average (top)
  - rms (bottom)
- Events per channel: 100
- Time bin: 6.25 ns
Measurement - trailing edge

- Test: test pulses synchronous with reset
- Trailing edge time
  - Average (top)
  - rms (bottom)
- Events per channel: 100
- Time bin: 6.25 ns
Measurement - noise

- S-curve obtained with channel threshold scan
- Test pulse resolution and global threshold resolution too coarse
- Baseline resolution gives similar results but with fewer points
- Conversion from DAC codes to input charge from simulations
- No input capacitance
- Average noise : 0.034 fC (211 e\(^-\))
- Maximum noise : 0.05 fC (312 e\(^-\))
Digital interface still working after 250 kGy
- Power consumption increase after 10 kGy (expected: leakage current in MOS)
- Gain drop after 4 kGy (unexpected)
- Full recovery after high T annealing
- Problem traced back to leakage current in analog switches
  - Enclosed layout has been adopted for switches in ToASSt v2
Ion fluence $\sim 5 \cdot 10^7$ per ion

Estimated cross section for 200 MeV protons: $3 \times 10^{-15}$ cm$^2$

Hadron flux $5 \times 10^6$ hadrons/(cm$^2 \times $s) $\rightarrow 9.3 \times 10^{-2}$ errors/(h chip)

Only 1$\rightarrow$0 errors observed - triplication error found in the Verilog code
Beam test at COSY - experimental set-up
Beam test at COSY - some preliminary results

- Two test beams at COSY (FZJ Julich) in July and August 2023
- Proton beam, momentum range 2-3 GeV/c, intensity range $10^7 \div 10^8$
- Parasitic beam
- Double-sided strip detector, 285 $\mu$m thick, pitch 90 $\mu$m
- FPGA-based DAQ from KIT
- Analysis ongoing
Conclusions

- A 64 channels ASIC, named ToASlSt, has been designed for the readout of the silicon strip detectors of the PANDA MicroVertex Detector.
  - Each channel provides particle time of arrival (ToA) and energy deposited informations (via ToT).
  - The particle ToA and ToT and channel address are packed in a 32 bits data word and transmitted via 1(2) 160 Mb/s serial link(s).
  - A slower (80 MS/s), bidirectional serial link is used for ASIC configuration.
- ToASlSt is designed in a commercial CMOS 0.11 µm technology.
  - The control logic has been designed with TMR techniques for SEU protection.
- Test results:
  - Lab tests show that the ToASlSt performances are as expected.
  - First ToASlSt tests with detector in a beam test shows excellent results.
  - Radiation tests showed a couple of weakness in the radiation tolerance of the ASIC. The issues has been identified and has been corrected in the next version, which will be submitted in March 2024.
Spare slides
ToASt main characteristics

- 64 input channels
- Time of Arrival (ToA) and Time over Threshold (ToT) measurements
- Master clock frequency : 160 MHz
- Region : groups of 8 channels with local FIFO
- Second level FIFO buffering for the 8 regions
- Two output serial links at 160 Mb/s
- Serial configuration protocol at 80 Mb/s
- Full SEU protection via Triple Modular Redundancy
- CMOS 0.11 µm technology
Output data format

- Data output in 32 bits words over 160 Mb/s serial links
- It can be configured to use 1 or 2 links
- Frame: rollover time for the time stamp counter, i.e. 25.6 $\mu$s at 160 MHz
- Data within a frame are packed within a frame header and a frame trailer
- Frame header contains chip id and frame number
- Frame trailers contains the number of valid samples and CRC

<table>
<thead>
<tr>
<th>Packet type</th>
<th>Header</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2 bits</td>
<td>30 bits</td>
</tr>
<tr>
<td>Data Trailer</td>
<td>10</td>
<td>10 ChipId[6:0] Reserved[12:0] FrameN[7:0]</td>
</tr>
<tr>
<td>Sync</td>
<td>01</td>
<td>01 DataCnt[11:0] CRC[15:0]</td>
</tr>
<tr>
<td></td>
<td>00</td>
<td>00 1100 1100 1100 1100 1100 1100 1111</td>
</tr>
</tbody>
</table>
Radiation tolerance

- Total Ionizing Dose: no special techniques have been adopted to increase the TID tolerance of ToASt. However, other studies [1] show that the technology is sufficiently radiation tolerant for the PANDA MVD application.

- Single Event Effects: the digital logic has been protected via Triple Modular Redundancy using the TMRG tool [2]
  - Only channel and region registers are left non-triplicated to save power
  - Clock and reset nets are triplicated
  - Synchronous reset net
  - Minimum distance between triplicated DFF set to 20 $\mu$m

[1] E. Riceputi et al., "Total ionizing dose effects on CMOS devices in a 110 nm technology", IEEE PRIME 2017 proceedings

Test for Single Event Upset tolerance

- Test at the SIRAD facility at LNL
  - May 23\textsuperscript{th}-24\textsuperscript{th} 2022
  - Beam time: 48 hours

<table>
<thead>
<tr>
<th>Ion</th>
<th>Angle</th>
<th>Energy [MeV]</th>
<th>LET [MeV \cdot cm^{2}/mg]</th>
<th>Fluence [ions/cm^{2}]</th>
</tr>
</thead>
<tbody>
<tr>
<td>O</td>
<td>0°</td>
<td>95.4</td>
<td>4.57</td>
<td>6.31 \cdot 10^{7}</td>
</tr>
<tr>
<td>F</td>
<td>0°</td>
<td>110.7</td>
<td>5.60</td>
<td>1.01 \cdot 10^{8}</td>
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<tr>
<td>F</td>
<td>30°</td>
<td>110.7</td>
<td>6.47</td>
<td>3.03 \cdot 10^{7}</td>
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<tr>
<td>Si</td>
<td>0°</td>
<td>141.6</td>
<td>11.47</td>
<td>6.80 \cdot 10^{7}</td>
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<td>Si</td>
<td>30°</td>
<td>141.6</td>
<td>13.24</td>
<td>4.11 \cdot 10^{7}</td>
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<tr>
<td>Cl</td>
<td>0°</td>
<td>162.7</td>
<td>15.33</td>
<td>4.99 \cdot 10^{7}</td>
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<tr>
<td>Br</td>
<td>0°</td>
<td>218.9</td>
<td>32.67</td>
<td>4.39 \cdot 10^{7}</td>
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<tr>
<td>Ag</td>
<td>0°</td>
<td>247.0</td>
<td>37.89</td>
<td>1.52 \cdot 10^{7}</td>
</tr>
</tbody>
</table>

Aim: estimate the SEU rate at LHC from ions cross section

## Simulation results - event loss probability

<table>
<thead>
<tr>
<th>Chip n.</th>
<th>Input events</th>
<th>Output events</th>
<th>Lost events</th>
<th>N. of frames</th>
<th>Link occupancy Tx0</th>
<th>Link occupancy Tx1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>208</td>
<td>205</td>
<td>3</td>
<td>29</td>
<td>4.82%</td>
<td>3.84%</td>
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<tr>
<td>1</td>
<td>135</td>
<td>133</td>
<td>2</td>
<td>30</td>
<td>3.69%</td>
<td>3.02%</td>
</tr>
<tr>
<td>2</td>
<td>192</td>
<td>190</td>
<td>2</td>
<td>29</td>
<td>4.75%</td>
<td>3.70%</td>
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<tr>
<td>3</td>
<td>169</td>
<td>163</td>
<td>6</td>
<td>30</td>
<td>4.18%</td>
<td>3.40%</td>
</tr>
<tr>
<td>4</td>
<td>164</td>
<td>161</td>
<td>3</td>
<td>30</td>
<td>4.27%</td>
<td>3.30%</td>
</tr>
<tr>
<td>5</td>
<td>149</td>
<td>142</td>
<td>7</td>
<td>30</td>
<td>3.81%</td>
<td>3.25%</td>
</tr>
<tr>
<td>6</td>
<td>140</td>
<td>132</td>
<td>8</td>
<td>30</td>
<td>3.70%</td>
<td>3.03%</td>
</tr>
<tr>
<td>7</td>
<td>102</td>
<td>100</td>
<td>2</td>
<td>29</td>
<td>3.27%</td>
<td>2.57%</td>
</tr>
<tr>
<td>8</td>
<td>179</td>
<td>178</td>
<td>1</td>
<td>30</td>
<td>4.78%</td>
<td>3.15%</td>
</tr>
<tr>
<td>9</td>
<td>162</td>
<td>159</td>
<td>3</td>
<td>30</td>
<td>4.37%</td>
<td>3.14%</td>
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<tr>
<td>10</td>
<td>207</td>
<td>196</td>
<td>11</td>
<td>30</td>
<td>5.01%</td>
<td>3.40%</td>
</tr>
<tr>
<td>11</td>
<td>166</td>
<td>165</td>
<td>1</td>
<td>29</td>
<td>4.60%</td>
<td>2.95%</td>
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</tbody>
</table>

### Single driver

<table>
<thead>
<tr>
<th></th>
<th>Input events</th>
<th>Output events</th>
<th>Lost events</th>
<th>N. of frames</th>
<th>Link occupancy Tx0</th>
<th>Link occupancy Tx1</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>207</td>
<td>196</td>
<td>11</td>
<td>30</td>
<td>6.83%</td>
<td>0%</td>
</tr>
<tr>
<td>11</td>
<td>166</td>
<td>165</td>
<td>1</td>
<td>29</td>
<td>6.01%</td>
<td>0%</td>
</tr>
</tbody>
</table>

- HDL simulations with data from PANDA physics simulations
- Barrel case (similar results with the forward case)
- Lost events : 2.5%
- Event loss due to FE dead time