

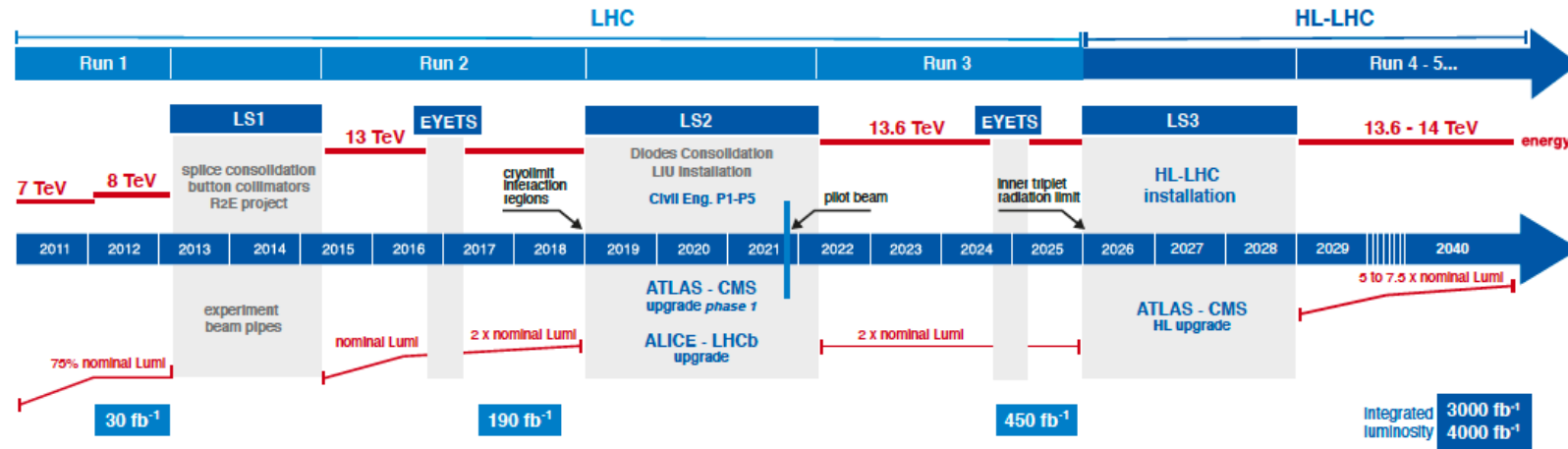
STATUS OF THE UPGRADE OF THE CMS INNER TRACKER FOR THE HL-LHC

E.Migliore

Università di Torino/INFN

on behalf of the CMS Tracker Group

HL-LHC and Inner Tracker timeline



[LHC/HL-LHC plan Feb 2022](#)

Jul 2017: TDR “The phase-2 upgrade of the CMS Tracker”
[CERN-LHCC-2017-009](#)

Definition of requirements

Oct 2023: Inner Tracker Engineering Design Review
 => transition to the construction phase

Final decisions on:

- **Inner Tracker system:** layout of the detector and services
- **Inner Tracker building blocks** (e.g. modules):
 - technology and specs of the sensors
 - finalization of the readout chip (CROC)

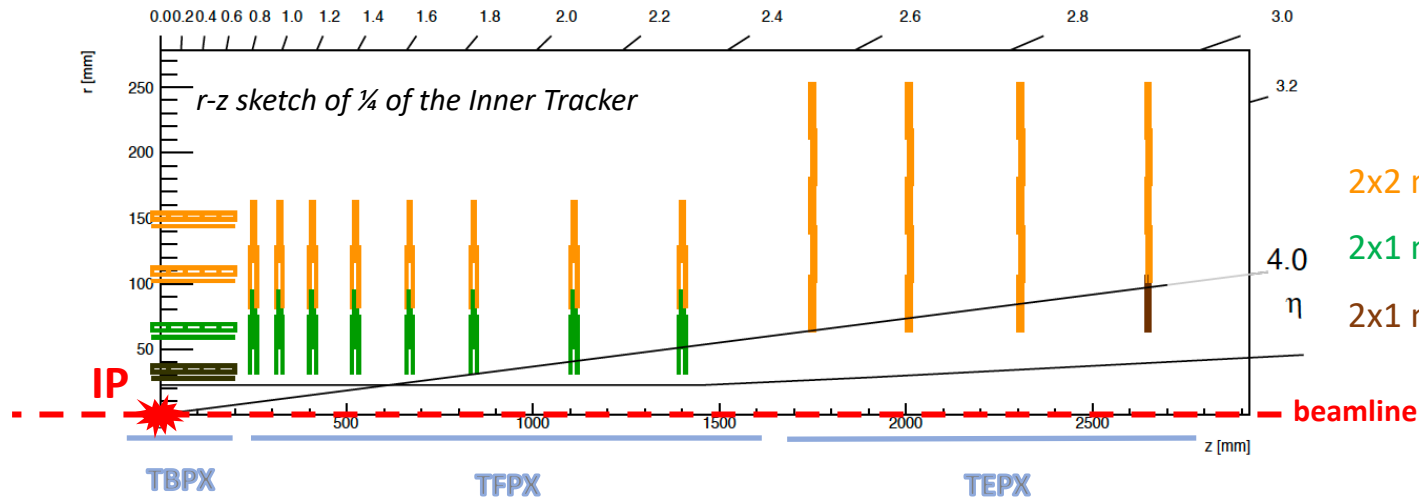
2028: start of installation at LHC P5

Status of the production

Requirements for the Inner Tracker at HL-LHC

- **High granularity** for efficient pattern recognition at high pileup and two-track separation in dense jets environment: 2×10^{-3} occupancy at pileup 200
- **Extended coverage** up to $|\eta|=4$ for efficient identification of b-jets and VBF jets, and extended pileup mitigation
- **Radiation hardness** up to 1.2 Grad TID and 2.3×10^{16} n_{eq}/cm^2 hadron fluence after 3000 fb^{-1} at the innermost radius ($r \simeq 3 \text{ cm}$) - If underperforming, replacing it partially at half HL-LHC lifetime
- **Large data rates:** readout compatible with 750 kHz L1A rate and increased L1 latency of $12.5 \mu\text{s}$
=> hybrid pixels modules (e.g. sensor bump-bonded to readout chip)
- **Low mass** despite the high heat dissipation (50 kW) due to high granularity (2G pixels) and high leakage current in irradiated sensors
=> lightweight mechanical structures, 2-phase CO_2 cooling, serial powering

Layout

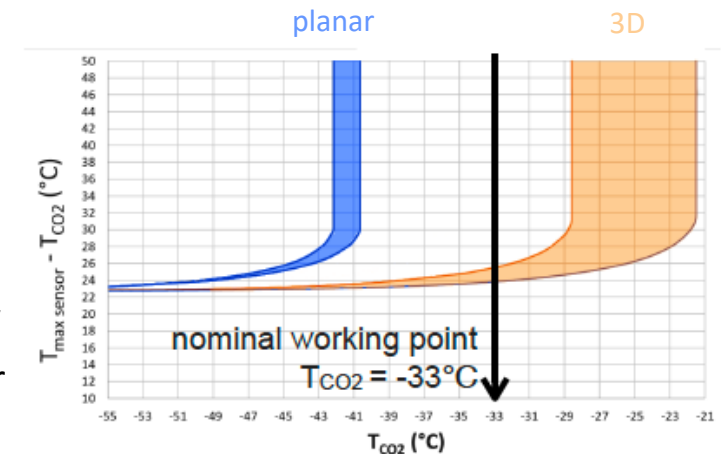


- 2x2 modules ("quad" planar sensors)
- 2x1 modules ("double" planar sensors)
- 2x1 modules ("1+1" 3D sensors)

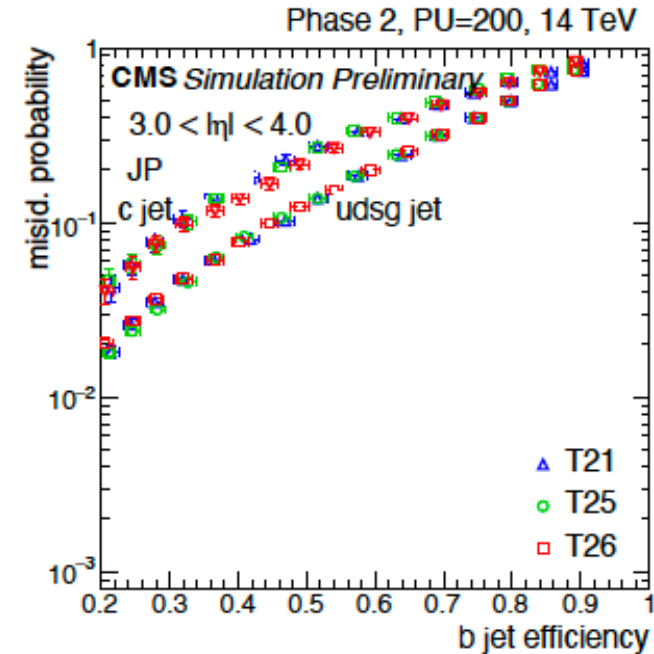
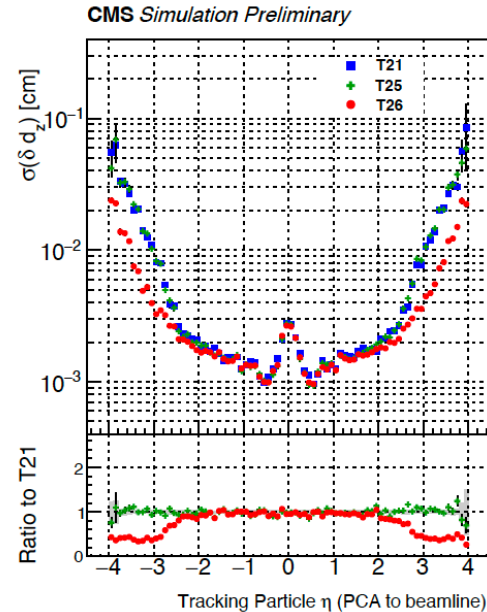
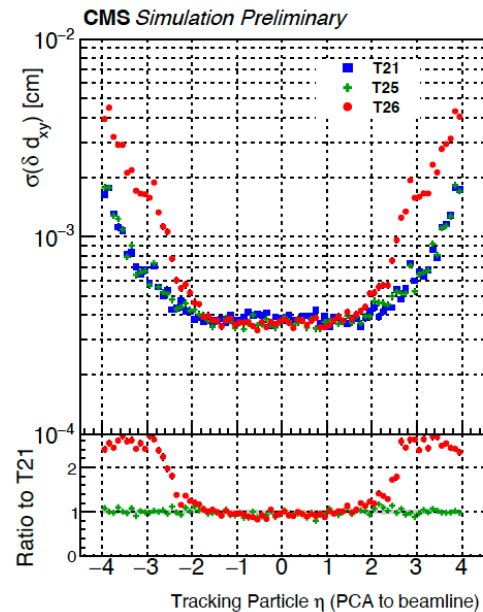
3 sub-systems: TBPX (barrel), TFPX (forward), TEPX (endcap)

3892 hybrid pixel modules with 2 or 4 readout chips

- Two key decisions on the layout taken in 2022:
 - 3D sensors in TBPX layer1
reason: efficient charge collection in irradiated ($1.5 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$) 3D sensors (already) at $V_{\text{bias}}=140 \text{ V}$ (x1/4 planar) => up to 10 °C margin wrt thermal runaway
 - $100 \times 25 \text{ } \mu\text{m}^2$ pixel cells everywhere: validated using full simulation of the detector



Validation of the layout



T21: 100x25 μm^2 planar everywhere (as in TDR)

T25: 100x25 μm^2 3D in TBPX layer1 and 100x25 μm^2 planar elsewhere

T26: 100x25 μm^2 3D in TBPX layer1 and 100x25 μm^2 planar in TBPX layer2-3-4, 50x50 μm^2 planar in TFPX and TEPX

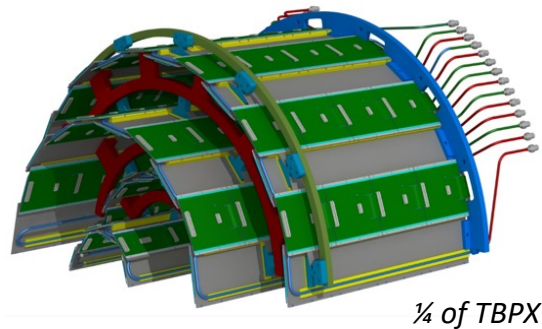
[CERN-CMS-DP-2022-071](https://cds.cern.ch/record/2811071/files/CERN-CMS-DP-2022-071)

Validation using both low-level (track impact parameters d_{xy} and d_z) and high-level observables (e.g. b-tagging ROC)

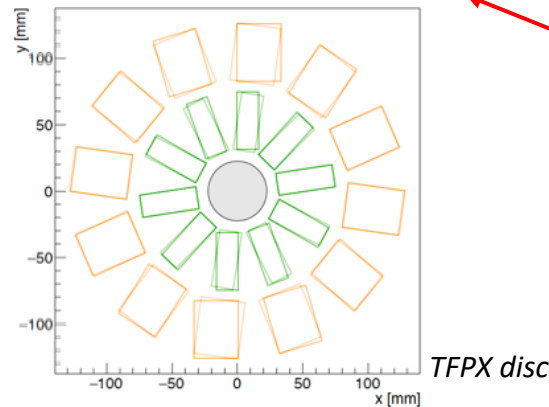
- wide φ -acceptance of TBPX layer1 guarantees charge sharing => no degradation in d_{xy} resolution between 3D and planar sensors
- the difference on d_{xy} and d_z resolution for the layout (**T26**) with square pixels in TFPX and TEPX does not translate into a difference in b-tagging performance at large η (while increasing the complexity/risks of the production)

Mechanics

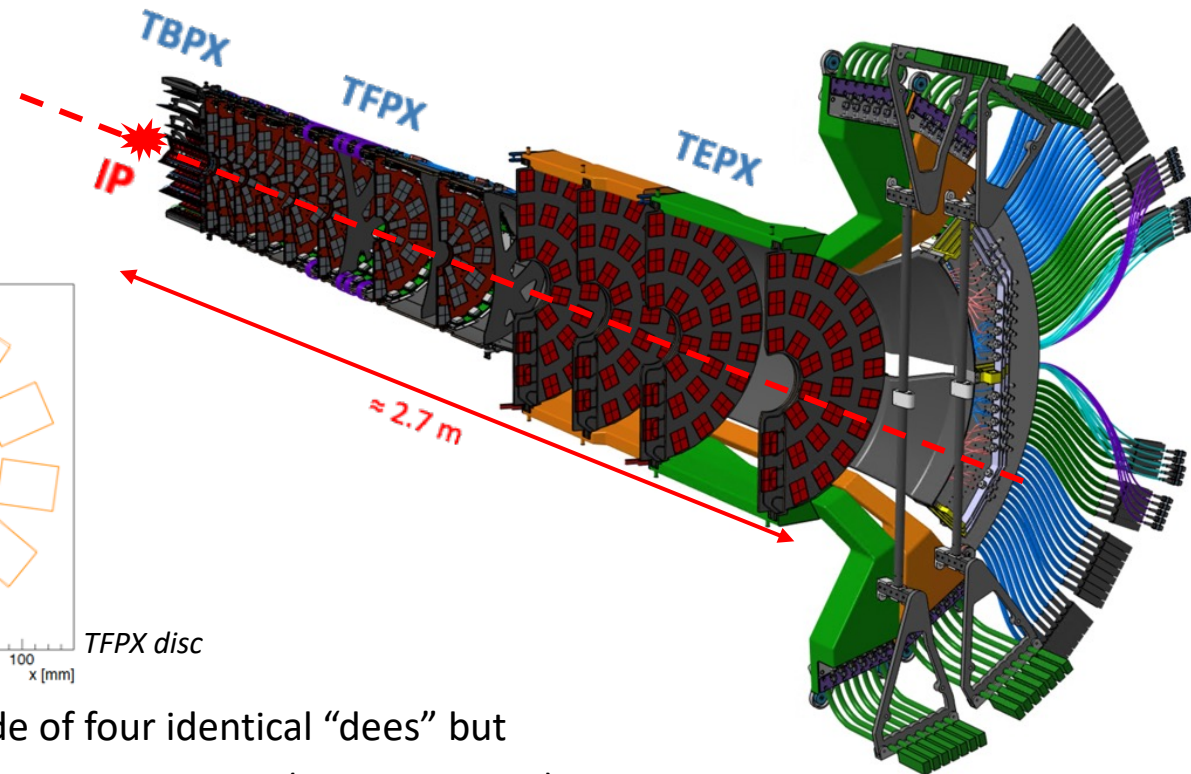
- No mechanical connections between Inner Tracker and the beampipe => possibility to extract the detector in extended technical stops for maintenance and replacement of the innermost layer and ring
- Inner Tracker divided into quadrants made of modular components designed to preserve hermeticity (but no clashes)



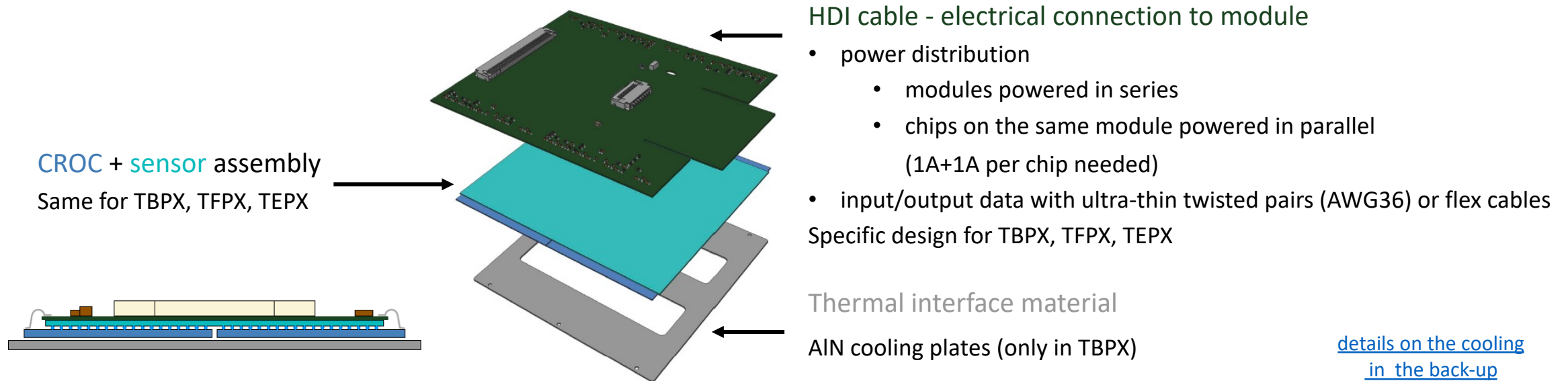
TBPX: split layers staggered to avoid projective cracks at $z=0$



TFPX and TEPX discs made of four identical “dees” but modules on TFPX discs non φ -symmetric (yaw geometry)



Modules



Ingredients for the production:

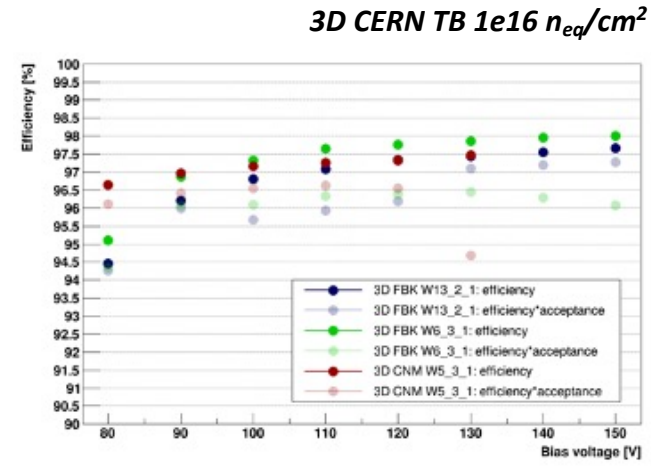
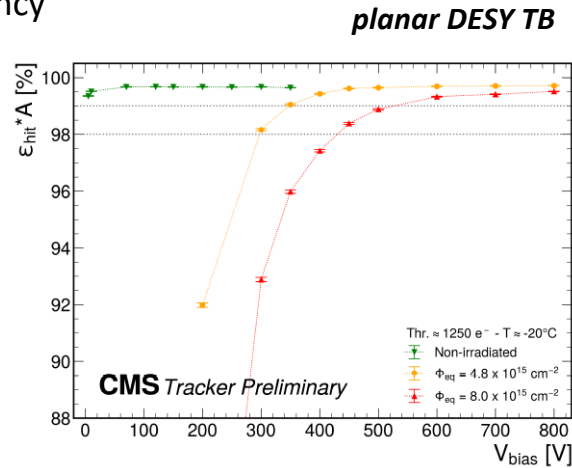
- Design of all the 6 HDI types completed
- Hybridization (=production of the CROC+sensor assembly from CROC and sensor wafers) made at companies
NB: it is one of the hotspots in the construction of the detector
- In-house production of the modules distributed among three consortia
 - TBPX (installed 756+spares): manual assembly using jigs and templates + wire bonding
 - TFPX (installed 1728+spares): assembly using jigs and templates on parts pre-positioned by a gantry + wire bonding
 - TEPX (installed 1408+spares): full assembly using a robotic arm + wire bonding

Assembly accuracy between **10-20 μm**

Silicon sensors

- Technology and design validated in beam tests before and after irradiation

- sensor efficiency



masked† pixels $\lesssim 1\%$

†masked if occupancy larger than

10^{-4} (DESY TB) or 2×10^{-5} (CERN TB)

$\epsilon_{hit} * A \geq 96\%$ (3D normal incidence)

$\geq 98\%-99\%$ (planar)

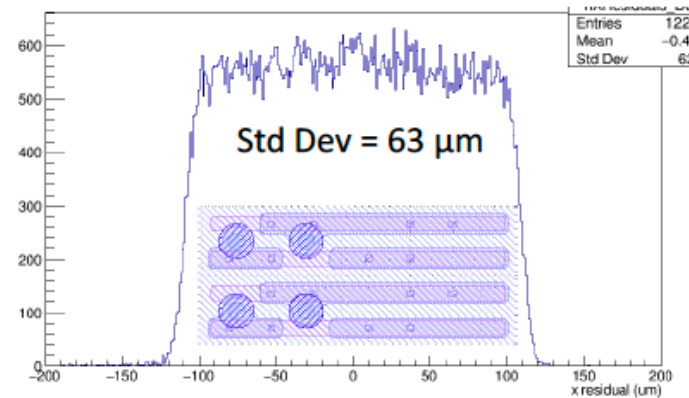
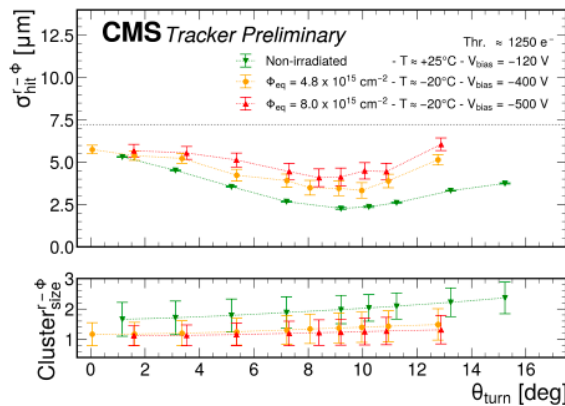
ϵ_{hit} = fraction of matched tracks on DUT

A = fraction of unmasked pixels

- single-hit resolution for standard pixels ($100 \times 25 \mu\text{m}^2$) and elongated pixels ($225 \times 25 \mu\text{m}^2$) in the interchip region

resolution below pitch/ $\sqrt{12}$

minimum at $\tan^{-1}(25\mu\text{m}/150\mu\text{m})$



Silicon sensors

- Specs frozen since 2022

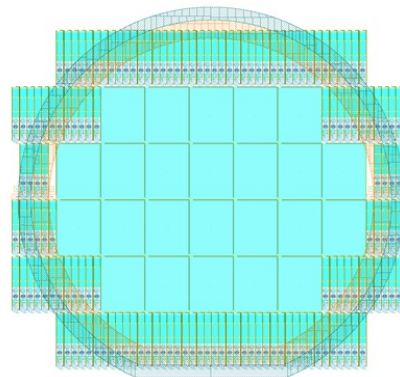
3D sensors	planar sensors
150 μm active thickness + 100 μm support	150 μm active thickness and no support
cell geometry: 1E central	cell geometry: bitten n-type implant
no elongated pixels, 175 μm periphery	elongated pixels in the interchip region, 450 μm periphery
temporary metal for wafer-level IV qualification	no bias dot (IV only from guard ring or test structures)
$V_{\text{dep}} < 10 \text{ V}$, $V_{\text{bd}} > V_{\text{dep}} + 35 \text{ V}$ (fresh) $V_{\text{bd}} > 200 \text{ V}$ (irrad)	$V_{\text{bd}} > 350 \text{ V}$ (fresh) $V_{\text{bd}} > 600 \text{ V}$ (irrad)
hit efficiency: > 96% (normal incidence)	hit efficiency: > 99%

- Production in progress

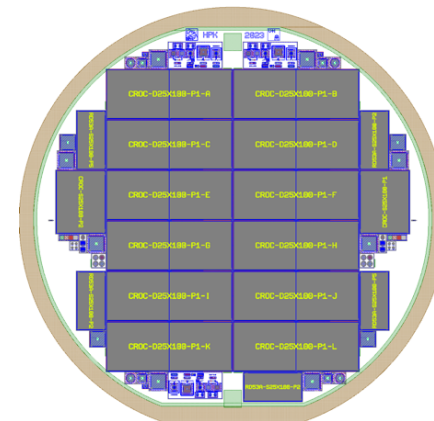
- 3D sensors from FBK
 - ≈ 320 single sensors by mid 2025
- planar sensors from HPK
 - ≈ 2000 double + 4000 quad sensors by mid-end 2025

- All production lines on 6" wafers
 - => same useful area/wafer

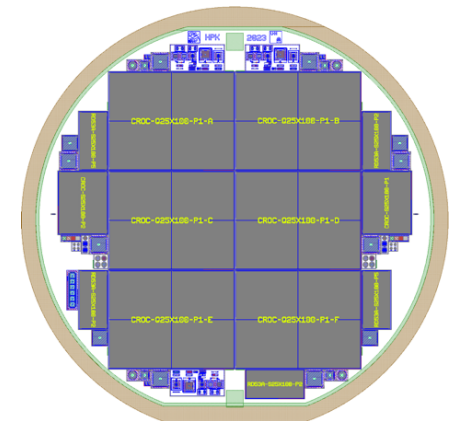
24 single 3D sensors/wafer



12 double planar sensors/wafer



6 quad planar sensors/wafer



CROC readout chip

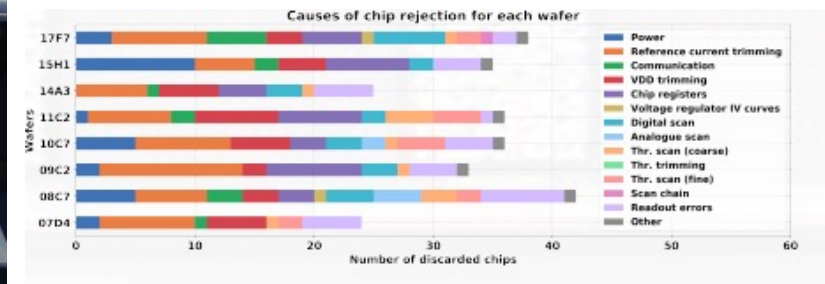
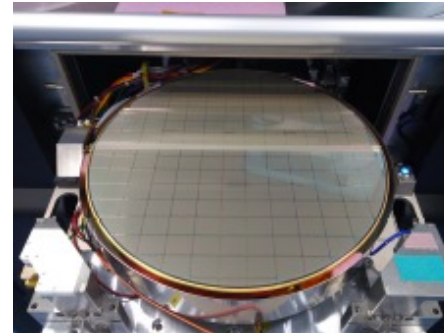
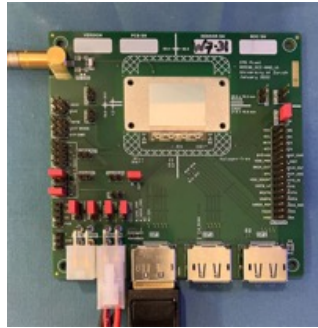
- 432 x 336 cells (50x50 μm^2 bonding pad reticle) made in CMOS 65 nm technology
- Key parameters for operating in hostile radiation environment
 - mitigating degraded electronics
 - radiation tolerance up to **0.5 Grad** and robustness to SEU up to 100 Hz
 - mitigating degraded sensors
 - in-time threshold of **1000 e** to detect low signals from heavily irradiated sensors
 - analog FE with adjustable feedback for leakage current compensation up to **10 nA/ch**
- Key parameters impacting physics performance
 - limiting the material budget
 - small power consumption **1 W/cm²**
 - supporting **serial powering**
 - 4 differential serial inputs (0.32 Gbps/lane) for **merging data** from other CROCs on the same module
 - readout with 4 digital electrical links per chip (1.28 Gbps per link)
 - exploiting the full physics reach
 - 6-to-4 bit dual slope ToT mapping for charge compression (fine granularity for charge sharing, coarse granularity for heavily ionizing particles)



NB: limited radiation tolerance of readout opto-electronics => $r \geq 16$ cm

CROC readout chip

All functionalities of the CROCv1 extensively characterized



- single chip-sensor assemblies used for bench tests and beam tests
 - ENC: 80 e (fresh) / 150 e (after 0.5 Grad)
 - threshold dispersion: 50 e (fresh) / 80 e (after 0.5 Grad)
 - analog and digital efficiency vs. hit rate (emulated with X-rays)
- bare chip in wafer level test (138 chip/wafer, 8 min/chip)
 - power consumption
 - tuning of the thresholds of each pixel (5 bit trimming)
 - calibration of internal ADC and DAC
 - calibration of T sensors

Yield for 1932 CROCv1 chips measured to be > 70%

CROCv2 version (engineering run) submitted in Oct 2023 with the first 16 wafers received in Jan 2024

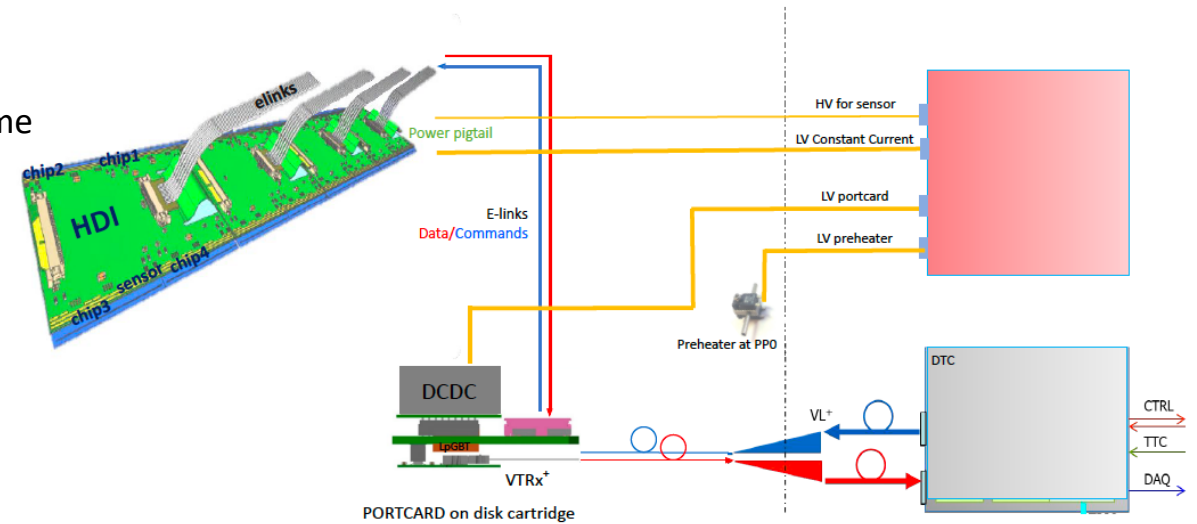
System aspects

Powering scheme

- **500 serial power chains** (from 5 to 11 modules)
- Cu (Cu-cladded Al) **cables** outside (inside) the detector volume
- **260 PS Module** with 2 PS Units each
 - LV: 1 current source for the modules (8A)
 - HV: 2 voltage source for the modules (800V)
 - LV: 2 voltage sources for opto-boards and pre-heaters

Data flow

- **≈7k AC coupled e-links** from CROC to IpGBT
1.28 Gbps u/s (160 Mbps d/s) per link
- **680 opto-boards** (“portcard”) hosting 3 IpGBT
- portcard to **Data Trigger and Control** board (DTC) on Apollo platform
10.24 Gbps u/s (2.56 Gbps d/s) per IpGBT
- **36 DTC** to DAQ
400 Gbps per DTC

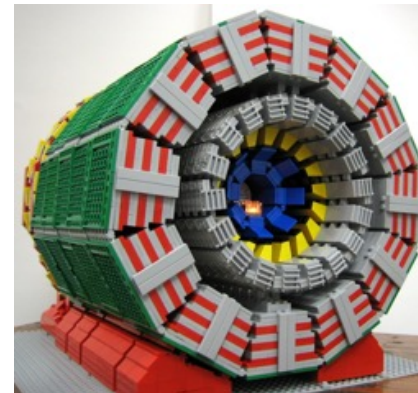


Rule

DO NOT CROSS readout lane or sensor bias among modules in different serial power chains

Summary

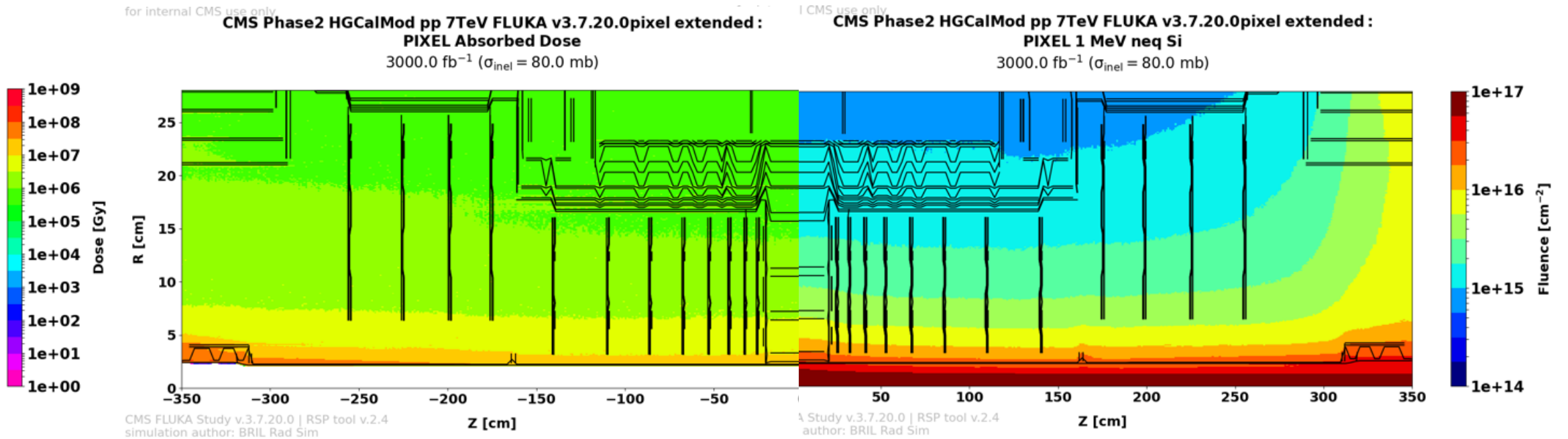
- The Inner Tracker of the CMS experiment has been completely redesigned for HL-LHC. It represents a shift of paradigm compared to the current pixel detector
 - instrumented surface: $\approx 2 \text{ m}^2 \Rightarrow \approx 5 \text{ m}^2$
 - number of pixels: $\approx 125 \text{ M} \Rightarrow \approx 2 \text{ G}$
- All components of the modules validated, production of the modules starting in 2024
- Challenging years ahead for going from building blocks to the final detector



[Courtesy of CMS/UniMaryland/LEGO](#)

EXTRA SLIDES

Radiation environment at 3000 fb⁻¹



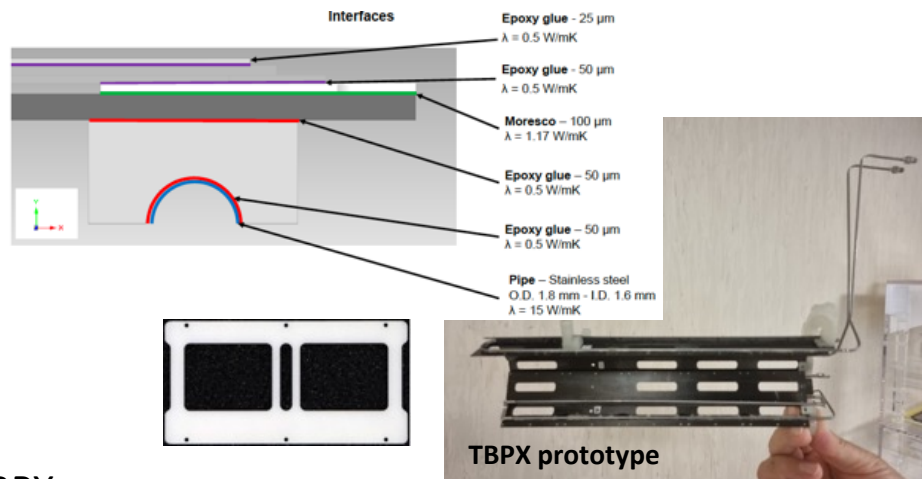
Radiation requirements

	RUN 4 (800 fb ⁻¹)		RUN 5 (1300 fb ⁻¹)		RUN 4+5 (2100 fb ⁻¹)		RUN 4+5+6 (3000 fb ⁻¹)		Not in Chamonix 2022 (4000 fb ⁻¹) For reference only	
	1E16 1 MeV neq	Grad	1E16 1 MeV neq	Grad	1E16 1 MeV neq	Grad	1E16 1 MeV neq	Grad	1E16 1 MeV neq	Grad
TBPX L1	0.69	0.36	1.12	0.58	1.81	0.93	2.58	1.34	3.44	1.78
TBPX L2	0.18	0.11	0.29	0.17	0.48	0.28	0.68	0.40	0.98	0.54
TFPX R1	0.46	0.31	0.75	0.49	1.22	0.79	1.74	1.13	2.32	1.5
TFPX R2	0.21	0.14	0.35	0.23	0.57	0.37	0.82	0.53	1.09	0.71

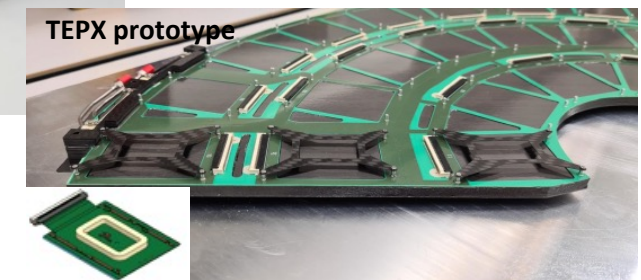
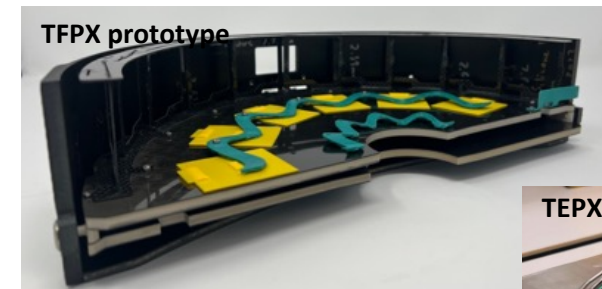
In red: max lifetime of modules before exceeding 1 Grad (max TID at which CROC has been tested)

Cooling

- Based on 2-phase CO₂
- CFD-based optimization of operating parameters (e.g. VQ) to limit T_{CO2} under the module (max -33 °C)
- Specific solutions to optimize heat removal for TBPX, TFPX and TEPX

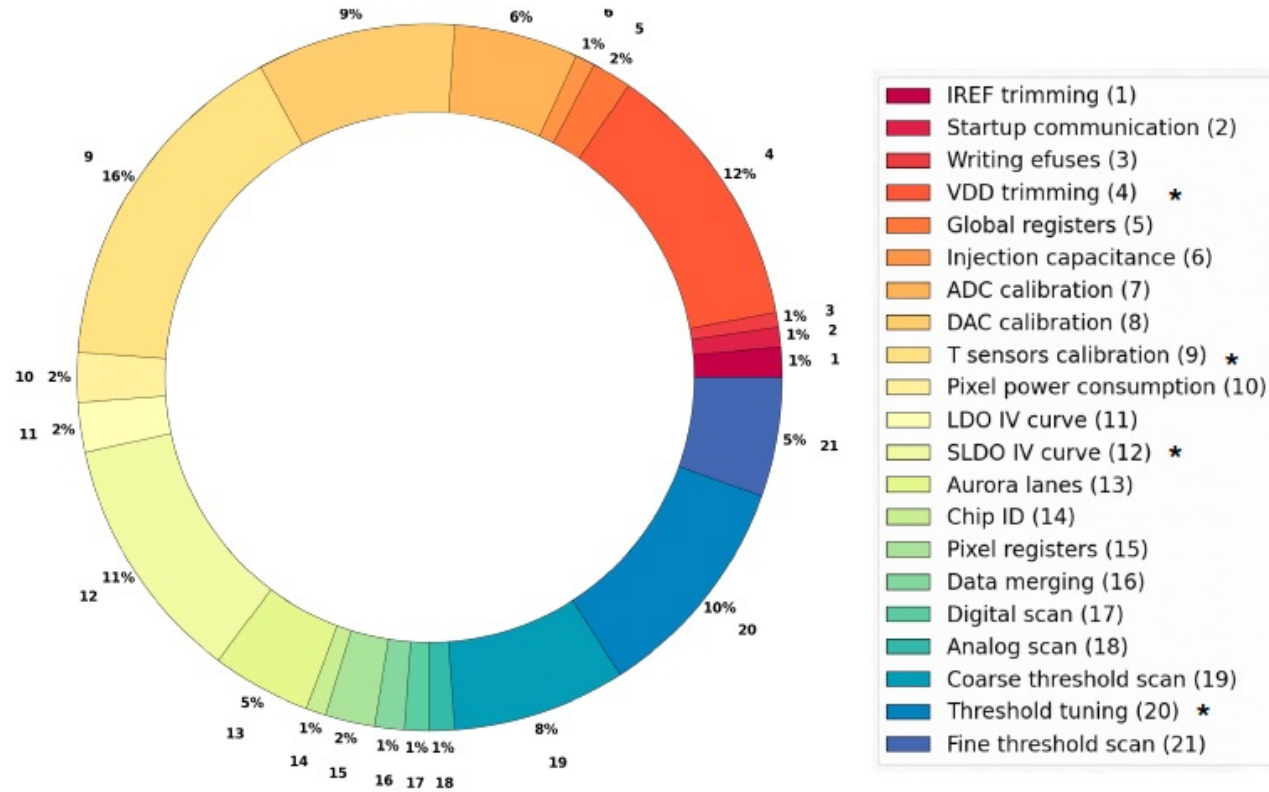


- TBPX
 - ultra-small stainless-steel pipes (ID: 1.6 mm, OD: 1.8 mm) embedded in the ladders (carbon foam)
 - thermal contact achieved with AlN cooling plates and diamond-doped glue and thermal grease (specs following an extensive R&D)



- TFPX and TEPX
 - Titanium pipes embedded in the dees
 - TFPX: ID: 2.6 mm, OD: 3.3 mm
 - TEPX: ID: 2.1 mm, OD: 2.3 mm
 - thermal contact achieved with CF springs (TFPX) or CF clampers “spiders” + Airex frame (TEPX)

Breakdown of the CROCV1 WLT execution time (as at TWEPP 2022)



- Tuning of pixel thresholds: 10%+8%
- Calibration of T sensors: 16%
- IV curve in ShuntLDO: 11%
- Calibration of ADC+DAC: 9%+6%