The Evolution of ArduSiPM technology : A Compact, Versatile, and Cost-effective Detector Platform for Radiation and Photon Flux Measurements

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(5)Sapienza University



**2023 IEEE** Nuclear Science Symposium, Medical Imaging Conference, and Room Temperature Semiconductor Detector Conference

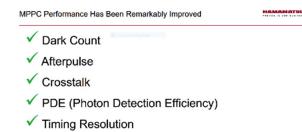
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# ArduSiPM Technology

In electronics, finding technologies with decade-long growth potential is like seeking a beacon in the dark. With ever-present obsolescence risks, when a path shows promise, why not pursue it determinedly?

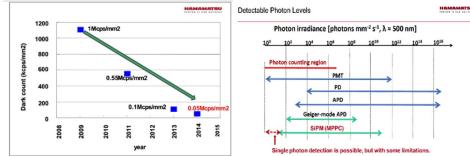


## In the last years we have seen a fast increasing and positive trend of SiPMs performances



✓ Larger Area (with Assembly Technology)

#### **Dark Counts reduction**



An even greater increase is that shown by the features and peripherals available in system-on-chip (SoC)



• In early 2000s Soc featured cheaper and smaller mobile phones

• In 2001, it was the release of the iPod that was based on the twin-core ARM SoC

The emergence of IoT further boost the evolution of SoC

#### SoC integrate more and more functions into a single chip!

- general-purpose microcontroller unit (MCU)
- numerous high-performance peripherals (amplifiers, ADCs, DACs, counters)
- non-volatile memory
- Network interfaces



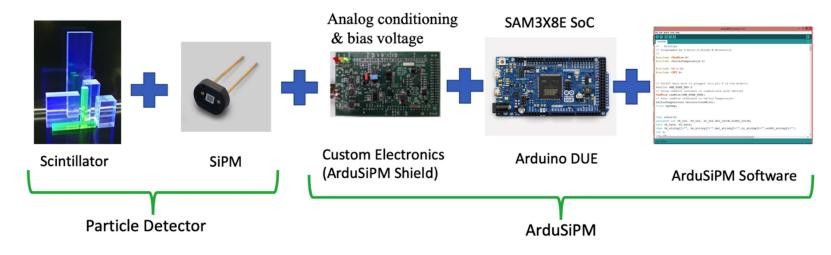
In 2014 we have created and published a new kind of detector using the new generation of **SiPM** and System on Chip (**SoC**).

V. Bocci, G. Chiodi, F. Iacoangeli, M. Nuccetelli and L. Recchia, "The ArduSiPM a compact trasportable Software/Hardware Data Acquisition system for SiPM detector," 2014 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2014, pp. 1-5, doi: 10.1109/NSSMIC.2014.7431252.



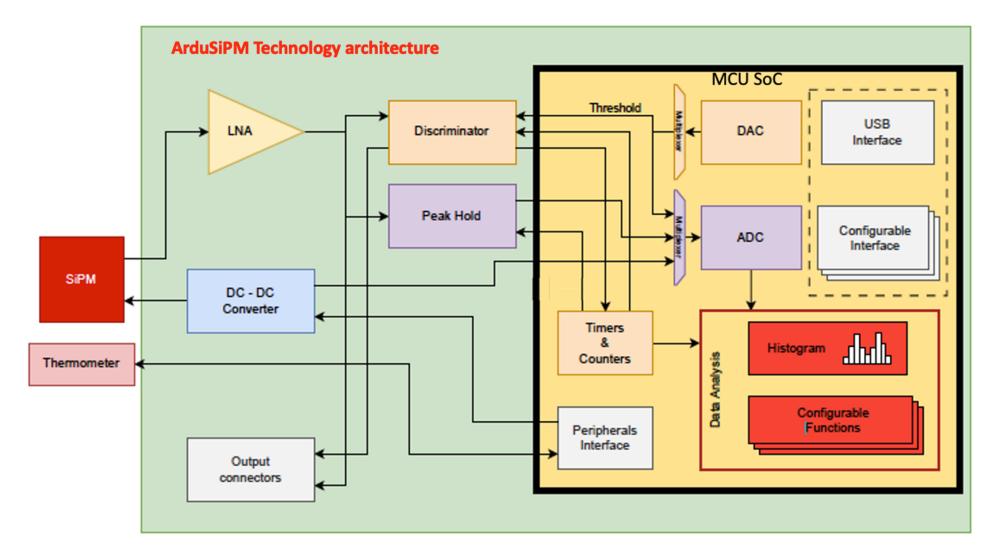
The ArduSiPM technology joins the innovation of the system on a chip (SoC) and the simultaneous improvement of Silicon photomultiplier detectors in a new generation of all-in-one scintillation detectors conceived from INFN Roma in 2014.

The basic idea is to minimize the use of COTS components (typically fast analog) and develop a large part of the peripherals inside the SoC, thus obtaining compact electronics without using ASICs and an external data acquisition system.



# Block diagram of the ArduSiPM technology

The guiding principle is that all non-strictly analog functions, such as ADC, DAC, counters, and edge computing data transmission, are entrusted to the SOC.



### The ArduSiPM architecture can scale with SoC Growth



2014



- 32-bit ARM <sup>®</sup> Cortex<sup>®</sup>-M3 RISC
- 84 MHZ
- 12 bits 1 Msamples/s ADC
- SRAM 64 + 32 Kbytes
- Flash 2 x 256 Kbytes





## SAMV71

- 32-bit ARM<sup>®</sup> Cortex<sup>®</sup>-M7 RISC
- 300 MHZ
- 12 bits 2 Msamples/s ADC analog offset compensation
- 12 bits DAC with 0 offset.
- Multi port SRAM 384 Kbytes
- Flash 2048 Kbytes
- Cache 16/16 Kbytes
- Two Analog Front-End Controllers (AFEC), allowing dual sample-andhold at up to 1.7 Msps. Offset and gain error correction feature.

- Better time resolution.
- More memory –> RT histogram



<b>SAM V7x</b>	512–2048 KB/
Arm® Cortex®-M7, 300 MHz	256–384 KB
<b>SAM E7x</b>	512–2048 KB/
Arm Cortex-M7, 300 MHz	256–384 KB
<b>SAM S7x</b>	512–2048 KB/
Arm Cortex-M7, 300 MHz	256–384 KB
SAM E5x	256–1024 KB/
Arm Cortex-M4F, 120 MHz	128–256 KB
SAM D5x	256–1024 KB/
Arm Cortex-M4F, 120 MHz	128–256 KB
<b>SAM G</b>	256–512 KB/
Arm Cortex-M4F, 120 MHz	64–176 KB
SAM 4	128–2048 KB/
Arm Cortex-M4F, 48-120 MHz	32–160 KB
<b>SAM D</b>	8–256 KB/
Arm Cortex-M0+, 48 MHz	2–32 KB
<b>SAM C</b>	32–256 KB/
Arm Cortex-M0+, 48-64 Mhz	4–32 KB
SAM L21/L22	32–256 KB/
Arm Cortex-M0+, 32-48 MHz	4–40 KB
SAM L10/L11	16-64 KB/
Arm Cortex M-23, 32 MHz	4-16 KB
	Arm® Cortex®-M7, 300 MHz SAM E7x Arm Cortex-M7, 300 MHz SAM S7x Arm Cortex-M7, 300 MHz SAM E5x Arm Cortex-M4F, 120 MHz SAM D5x Arm Cortex-M4F, 120 MHz SAM G Arm Cortex-M4F, 120 MHz SAM 4 Arm Cortex-M4F, 48-120 MHz SAM D Arm Cortex-M0+, 48 MHz SAM C Arm Cortex-M0+, 48 MHz SAM L21/L22 Arm Cortex-M0+, 32-48 MHz SAM L10/L11

# SAM3X8E

#### M3A... 1 / 1459 | — 93% + | 🕄 🚸

Atmel

#### SAM3X / SAM3A Series

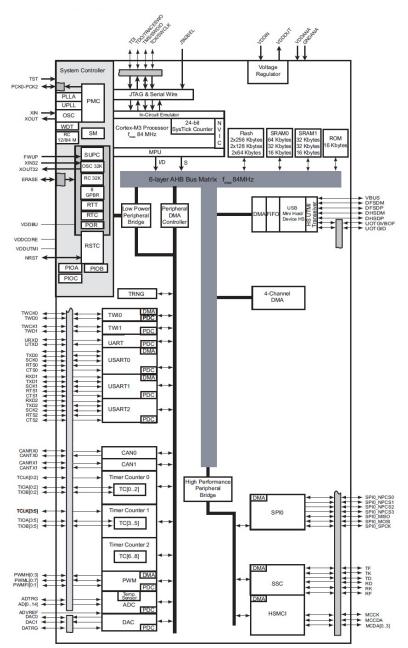
Atmel | SMART ARM-based MCU

#### DATASHEET

#### Description

The Atmel<sup>®</sup> | SMART SAM3X/A series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM<sup>®</sup> Cortex<sup>®</sup>-M3 RISC processor. It operates at a maximum speed of 84 MHz and features up to 512 Kbytes of Flash and up to 100 Kbytes of SRAM. The peripheral set includes a High Speed USB Host and Device port with embedded transceiver, an Ethernet MAC, 2 CANs, a High Speed MCI for SDIO/SD/MMC, an External Bus Interface with NAND Flash Controller (NFC), 5 UARTs, 2 TWIs, 4 SPIs, as well as a PWM timer, three 3-channel general-purpose 32-bit timers, a low-power RTC, a low-power RTT, 256-bit General Purpose Backup Registers, a 12-bit ADC and a 12-bit DAC.

The SAM3X/A devices have three software-selectable low-power modes: Sleep, Wait and Backup. In Sleep mode, the processor is stopped while all other functions can be kept running. In Wait mode, all clocks and functions are stopped but some peripherals can be configured to wake up the system based on predefined conditions. In Backup mode, only the RTC, RTT, and wake-up logic are running.



# SAMV71

VDDIO -

VDDPLL -

VDDCORE -

📜 Purchase Options



#### Features

#### Core

- Arm<sup>\*</sup> Cortex<sup>\*</sup>-M7 running at up to 300 MHz
- 16 Kbytes of I-Cache and 16 Kbytes of D-Cache with Error Code Correction (ECC)
- Single-precision and double-precision HW Floating Point Unit (FPU)
- Memory Protection Unit (MPU) with 16 zones
- DSP Instructions, Thumb\*-2 Instruction Set
- Embedded Trace Module (ETM) with instruction trace stream, including Trace Port Interface Unit (TPIU)

#### Memories

- · Up to 2048 Kbytes embedded Flash with unique identifier and user signature for user-defined data Up to 384 Kbytes embedded Multi-port SRAM
- Tightly Coupled Memory (TCM)
- 16 Kbytes ROM with embedded Bootloader routines (UART0, USB) and IAP routines
- · 16-bit Static Memory Controller (SMC) with support for SRAM, PSRAM, LCD module, NOR and NAND Flash with on-the-fly scrambling

#### System

· Embedded voltage regulator for single-supply operation



#### SAMV71Q21RT 🕸

**Radiation Tolerant Cortex M7 MCU** 

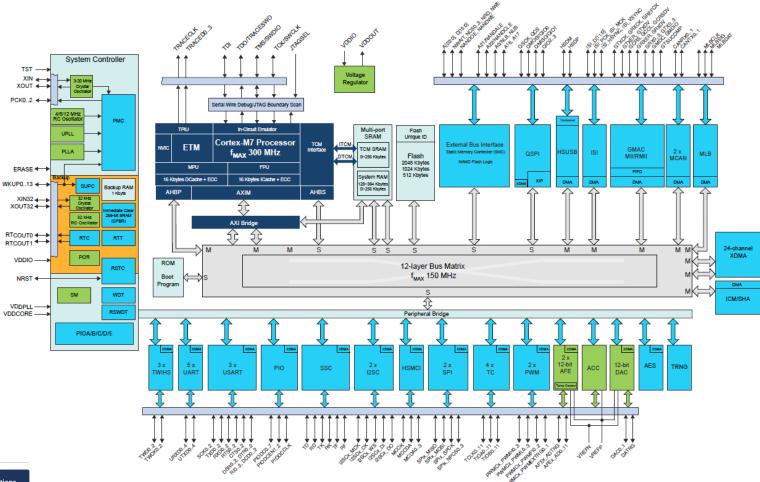
Status: In Production.

Documentation

SAMV71Q21RT Radiation-Tolerant 32-bit Arm® Cortex®-M7 Microcontroller: PDF



The SAMV71Q21RT is the radiation tolerant version of the popular Microchip SAMV71Q21 based on the high-performance 32-bit ARM Cortex-M7 processor with a Double Precision Floating Point Unit (FPU). These devices operate at up to 300MHz and feature up to 2048 Kbytes of Flash, and up to 384 Kbytes of multi-port SRAM which is configurable Instruction and Data Tightly Couple Memories to leverage the advanced DSP capabilities of the core.



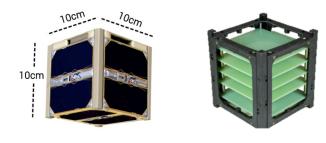


Cosmo ArduSiPM (GEN2)

ArduSIPM analog + SAMV71

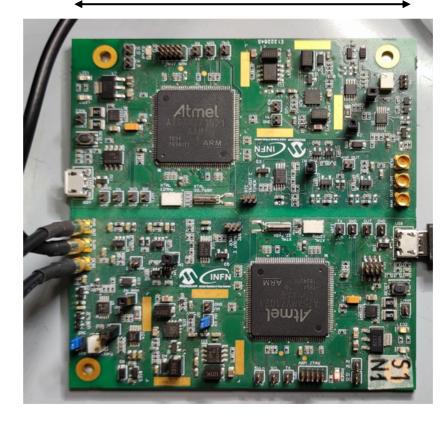
Collaboration Agreement ref. TTD 19RM1 020

INFN-Microchip Technology



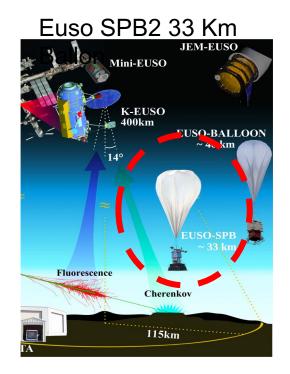
- 0.1 CubeSat Unit occupancy
- 2 channels
- Weigh 42 grams
- Low Power consumption <1Wh</li>
- Rad-tolerant version of MCU availability on market

9.6 cm



### Cubesat LEO or MEO





### Some measuraments with GEN2 (Cosmo ArduSiPM)

(see also Poster Session N-01-173) Threshold Scan Plot 1 Phe Pulsed light (centered about 10 Phe) Maximum CosmoArduSiPM time resolution: 2 Phe ADC histogram LED TDC\_CLK= CPU\_CLK/2 = 150 MHz 6.6 ns 120000 3 Phe 100 us 100000 4 Phe 80000 Simulated ADC peaks from Threshold scan data - Threshold scan with low LED pul T123199371 T123199371 60000 Threshold scan 123199371-123184371=15000 CLK 40000 and its derivative The GEN2 can measure time with a 20000 (comparable precision of 6.6 ns. Furthermore, it to ADC spectra). 100 200 300 400 500 can be synchronized with a ADC\_code universal reference, such as the PPS output from a GPS system or Dark noise + pulsed light >2 phe an atomic clock. Photons spectra ADC histogram LED ADC histogram LED Cosmo ArduSiPM vs 12 bits Le Croy Scope 250000 1 Phe ADC Histo 200000 2 Phe 150000 100000 3 Phe 50000 80 ADC value 100 ADC code 125 100 ADC code 125 150 175 200 ADC spectra the integral show to Log scale be equivalent to the scan plot Lin scale Credits to the graduating students, Simone Mariottini and Lorenza Masi

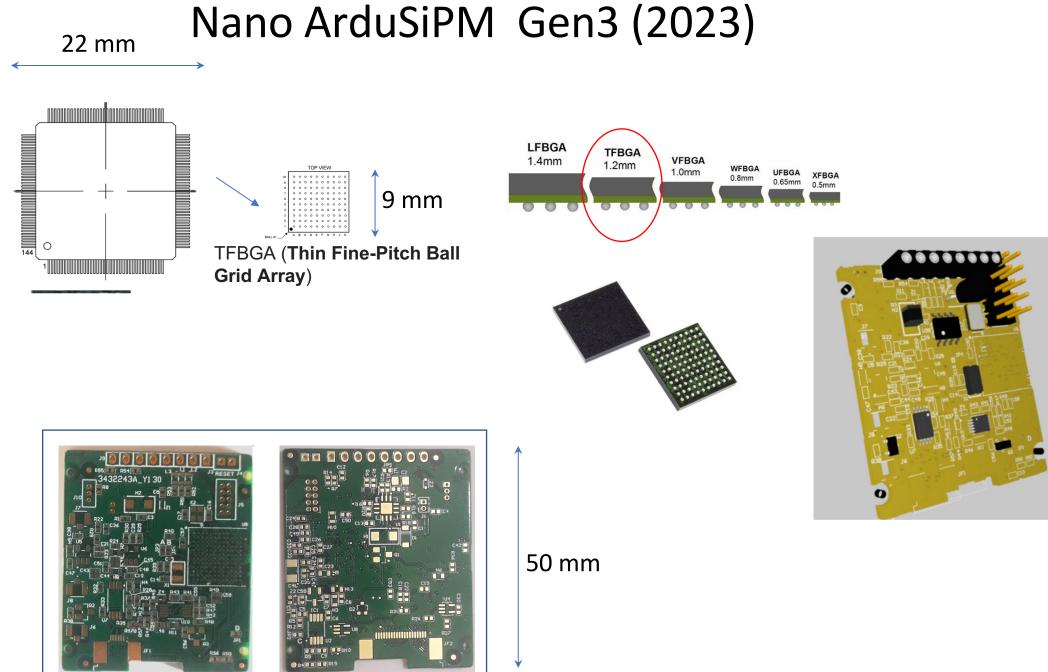
> 125 kil 2 5 (205 1 d) = 51= 0.00 mV 0X= 11 52= 11.0 mV 1/0X= 04

## Next STEP picosatellite

5 cm 1 U Picosatellite Camera Module Magnetorquer Module Scintillator INFN TECHTRANSFER stituto Nazionale di Fisica Nucl MICROCHIP te i Vieran Nano ArduSiPM Picosatellite OBC Photons sensibility to **On Board Computer** GPS Module Visible or IR

#### Valerio Bocci INFN Roma Vancouver 2023 NSS-MIC-RTSD

Earth TX/RX Module



## ArduSiPM Technology Evolution

(Strong Performance Boost and Remarkable Density Enhancements with Lighter Channel Weight)

Reduction in Size and Weight of the Individual Channel"

**1 channel** ArduSiPM (TT 2014)



<sup>2</sup> x 100 mm x 50 mm

### GEN2

**1 channel** Half Cosmo ArduSiPM (2021)

**1 channel** Nano ArduSiPM (2023)

**2 channel** LITE SPLD (2026)



GEN3



 $2 \text{ cm}^2/\text{ch}$ 

3 g/ch

25 cm<sup>2</sup> 10 g/ch

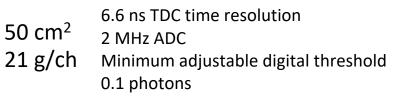
GEN4



50 mm x 50 mm

20 mm x 20 mm

2 plane x 55 cm²23 ns TDC time resolution<br/>1 MHz ADC<br/>Minimum adjustable digital threshold 3 photons



### The detectors obtained are compact and lightweight and can be used in various fields.

Application have been identified, leaving the use open within the HEP community

Scintillation particle detector Application in cubesats or picosatellites. LEO orbit. Monitoring of radiation in picosatellites and in constellations of picosatellites (Space Weather).



We've developed photon flux measurements for bioluminescence, leading to portable instruments for fieldwork in collaboration with Analytical Chemistry Department at the University of Bologna and CNR IMM.

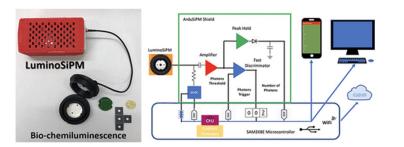




Figure S1. (A) The three components of LuminoSiPM dark box. (B) The assembly of sample holder in the dark box. (C) Mechanical protrusions and complementary alignment holes guarantee light tightness. (D) The box closed and ready for measurement.

In particle physics, these devices are perfect for triggering in test beams. They can excel in experiments with distributed detector systems. In our all-in-one detector, SiPMs connect directly to the electronics, eliminating the need for long analog cables. In this scenario, multichannel chips don't offer an apparent advantage over our digital-only wiring setup.

## Mocris particle detector Instrumentation

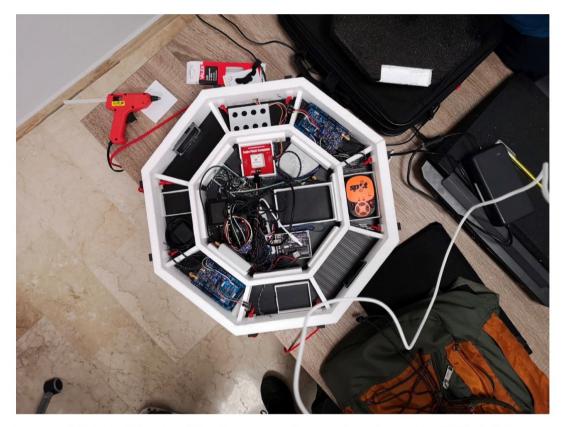


Figura 2.6. Foto del carico del pallone aerostatico per l'esperimento MoCRiS, si distinguno i due ArduSiPM e M5Stack.



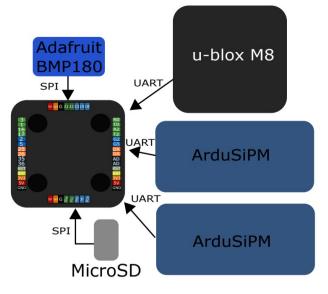
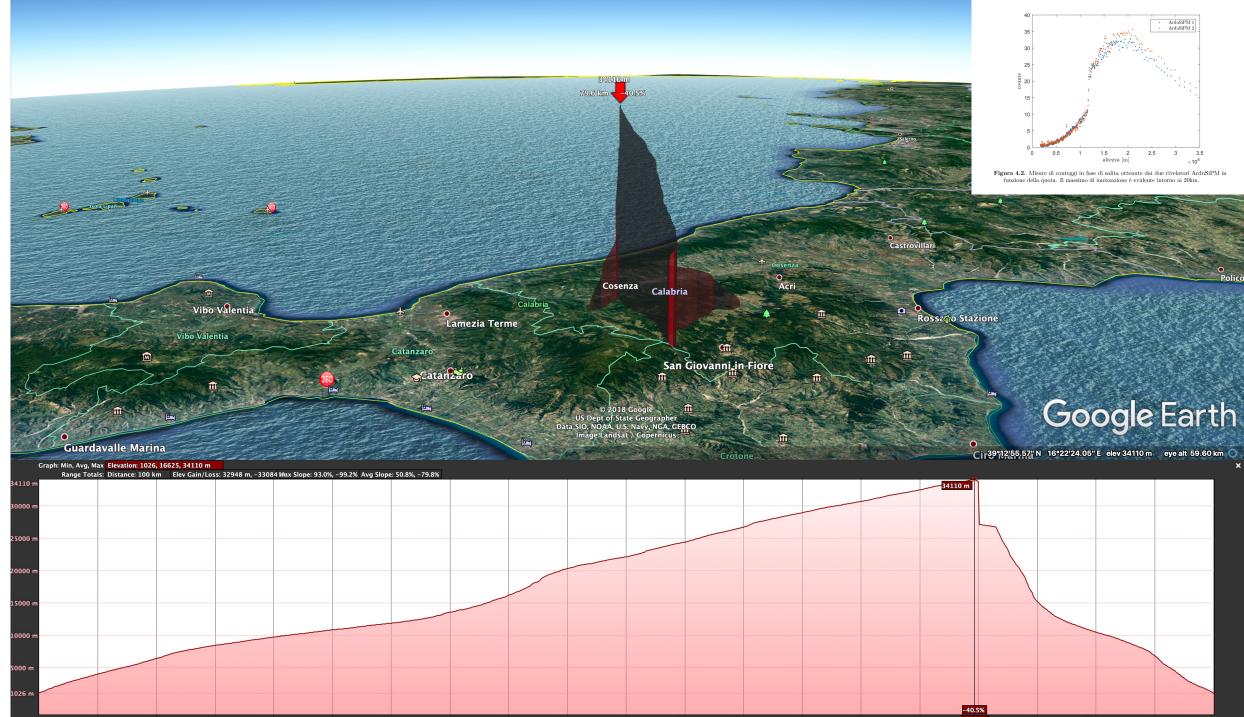


Figura 2.5. Diagramma a blocchi dell'apparato elettronico per la misura del flusso di raggi cosmici dell'esperimento MoCRiS. Sono riportati i tipi di protocolli seriali utilizzati per comunicare da ciascun elemento del sistema.

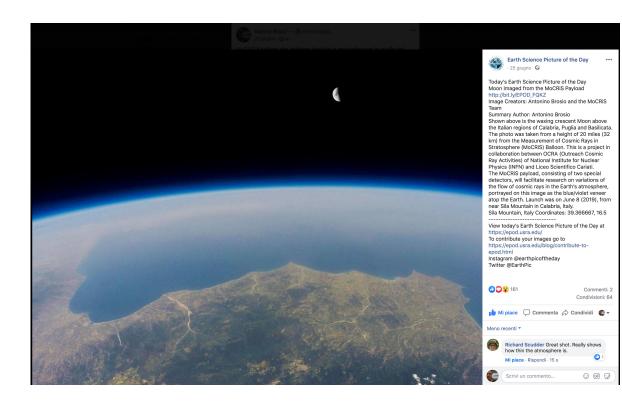


Հիա 10 կաս 15 կաս 20 կաս 25 կաս 20 կաս 25 կաս 40 կաս 45 կաս 50 կաս 55 կաս 56 կաս 55 կաս 70 կաս 70 կաս 95 կաս 95 կաս 00 կաս 05 կաս 10



#### Moon Imaged from the MoCRiS Payload

June 25, 2019





#### Image Creators: Antonino Brosio and the MoCRiS Team Summary Author: Antonino Brosio

Shown above is the waxing crescent Moon above the Italian regions of Calabria, Puglia and Basilicata. The photo was taken from a height of 20 miles (32 km) from the Measurement of Cosmic Rays in Stratosphere (MoCRiS) Balloon. This is a project in collaboration between OCRA (Outreach Cosmic Ray Activities) of National Institute for Nuclear Physics (INFN) and Liceo Scientifico Cariati.

The MoCRiS payload, consisting of two special detectors, will facilitate research on variations of the flow of cosmic rays in the Earth's atmosphere, portrayed on this image as the blue/violet veneer atop the Earth. Launch was on June 8 (2019), from near Sila Mountain in Calabria, Italy.

Sila Mountain, Italy Coordinates: 39.366667, 16.5

- Related Links High Altitude Balloon Flight Over Mt. Olympus, Greece
- 💽 Student Links How to detect cosmic rays **Composition of Earth's Atmosphere**
- Earth Observatory **Probing the Electric Space Around Earth**

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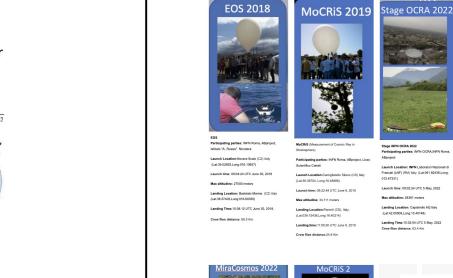


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## Testing of the electronics and communication system using stratospheric Light Balloon (Total weight < 4 Kg)



**On-field** experience in synergy with schools in OCRA INFN (Outreach Cosmic ray Activity) https://sites.google.com/view/particledetectors/loom-platform











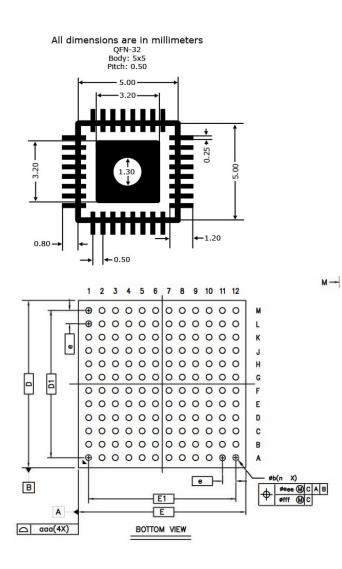
oject	HOOTIGE LOED
ole, Opera (MI) 18) Sep. 2022	Participating parties: INFN Roma, ABProject Space, Liceo Scientifico Cariati, Dipartimento di Fisica UNICAL, ADA Project Laboratory, ArpaCa Lab. Fisico E. Majorana, Catanzaro, OCRA Collaboration
	Launch Location: Stadio Comunale di Paola (CS) Italy (39'22'24'N 16'1'40'E)
(CR) Italy (10.13041)	Launch time: 09:00:00 UTC June 14, 2023
Sep, 2022	Max altitudine: 33.205 meters
	Landing Location: Acri (CS), Italy, (Lat: 39,4679 (Long: 16,4917)



Crow flies distance: 46 K

**GEN2** Detector on Balloon LoRa Link  $LOS = \sqrt{2R_eh + h^2}$ ~500 km 20 km

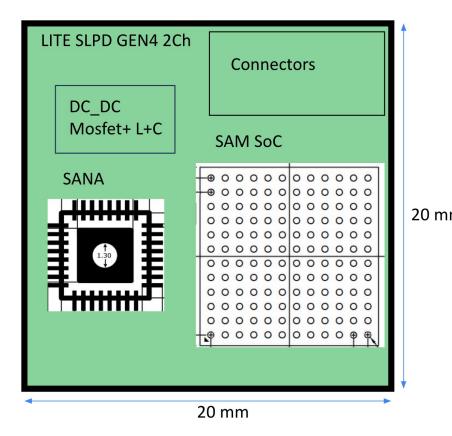
Employing stratospheric balloons to conduct altitude-based detector tests and to evaluate LoRa transmitters for data transmission from LEO orbit to Earth.



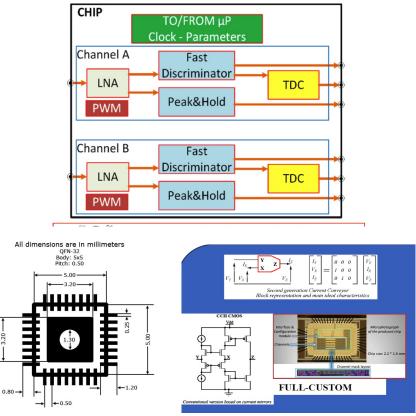
		Symbol	Common Dimensions		
			MIN.	NOM.	MAX
Package :				TFBGA	( ) ( ) ( ) ( ) ( ) ( ) ( ) ( ) ( ) ( )
Data Maria	X	E	10.000		
Body Size:	Y	D			
Ball Pitch :		•	0.800		
Total Thickness :		A			1.20

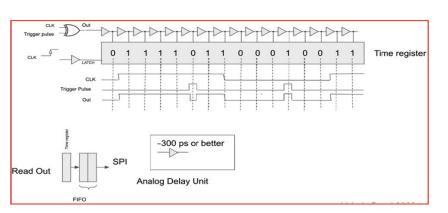
### The Upcoming 4th Generation: LITE-SPLD Project (Lightweight Integrated Technology for Space Luminescence and Particle Detection)





## LITE-SPLD Project: The Chip





(under CSN5 INFN)

The idea is to start from an already developed 'Front-End for MPPC' chip project devolped in INFN Tor Vergata, which includes all the GEN2 analog features and is optimized in terms of size and number of channels. The initial chip was intended for TOF applications and will need to be modified (significantly), while still maintaining the chosen technology for economic convenience and design familiarity.

Front-End chip for MPPC in standard 0.35 um CMOS technology: Low input impedance to reduce the reset time as much as possible All signals and thresholds are processed in the current domain using fast current comparators and a modified version of the second generation Current Conveyors (CCII) based on current mirror as building blocks for the amplifiers.

One of the notable innovations introduced by this chip is the inclusion of a segmented Time-to-Digital Converter (TDC). This advanced TDC design is segmented, meaning it is divided into smaller sections, each capable of performing time-to-digital conversions independently. This segmentation enables the chip to achieve a temporal resolution that is significantly finer than the duration of a single clock cycle used by the system. Essentially, it can precisely measure time intervals that are a fraction of the clock period, leading to enhanced timing accuracy in digital signals.

## Conclusions on the ArduSiPM Technology

- Introduced in 2015 by INFN's tech transfer, the first version of ArduSiPM is still purchasable online through an INFN non-exclusive license from RobotDomestici and CShark. Popular in labs and among global students, it's won numerous awards, especially in outreach and with makers.
- Thanks to the rapid advancement and adoption of MCU SOC technology in sectors like IoT, automotive, and space, ArduSiPM has experienced significant development and growth.
  - Since the first ArduSiPM was introduced at NSS MIC in Seattle 2014, we have developed two additional generations: "Cosmo ArduSiPM GEN2 " and "Nano ArduSiPM GEN3".
- We will soon have third-generation nano ArduSiPM prototypes. In the near future, we plan to send the Gen2/Gen3 versions into space on board of Cubesat e Picosatellite.
- The Second and Third generation, continuously updated in firmware, will be available to select users and experiments through scientific collaboration for particle detection, luminescence, and other potential applications.
- A Fourth generation is in the works, featuring 2 channels in 10 Euro Cent size. This can also be utilized in HEP experiments due to its minimal occupancy per channel and the lack of necessity to transmit analog signals over long distances.

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