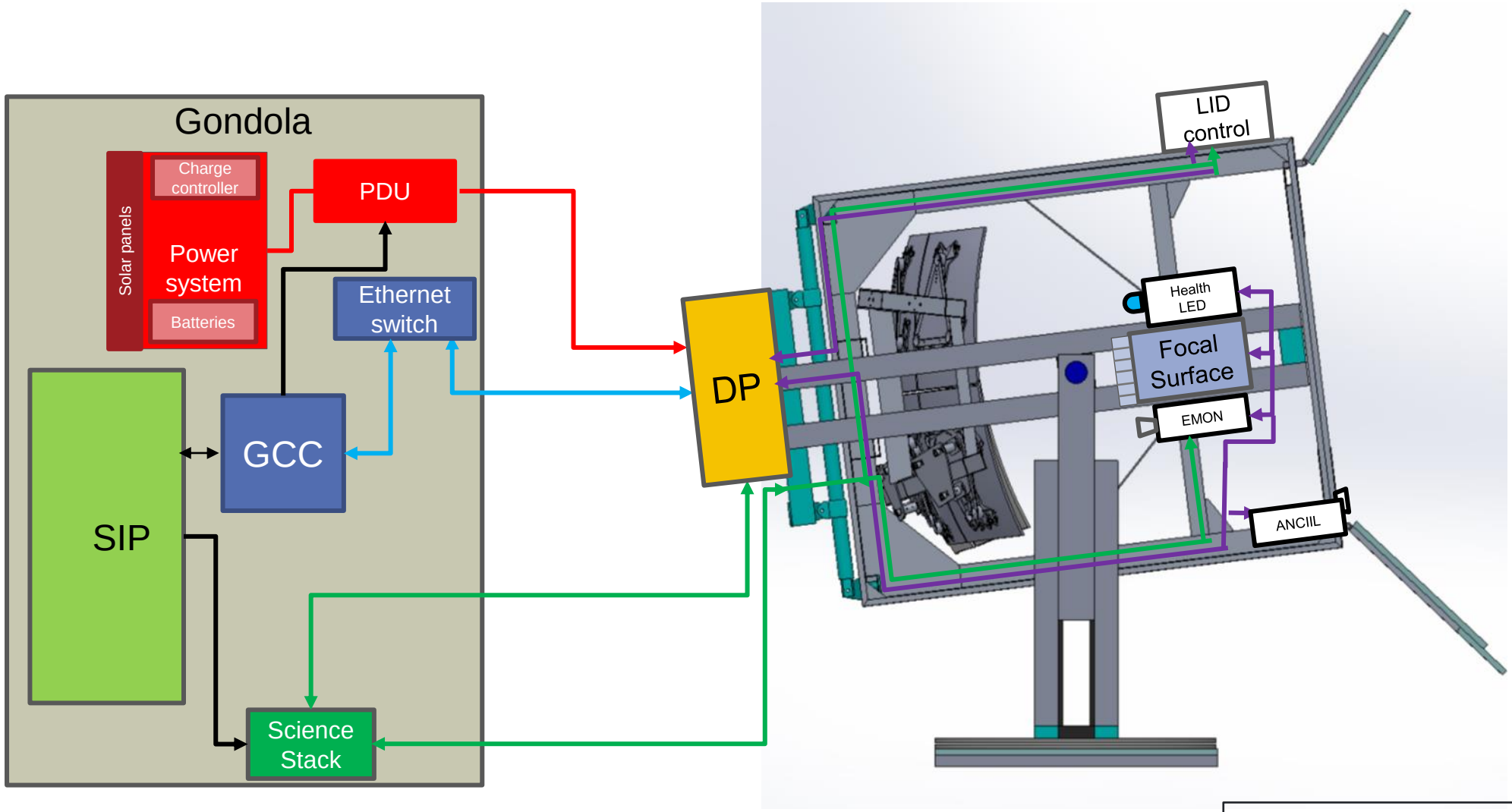
PBR
Wanaka NZ
2027

TELESCOPE CONTROL & DAQ SYSTEM OVERVIEW

GIUSEPPE OSTERIA (INFN NAPOLI)

TELESCOPE MAIN INTERFACES



TELESCOPE MAIN SUB-SYSTEMS

Focal surface

- **Fluorescence Camera**
  - **Optics**
    - 4 x FC PDMs → 36 Elementary Cells (EC) with 4 MAPMTs each → 144 MAPMTs
    - Field Flatners and BG-3
  - **Electronics**
    - ASIC board (144 units), Cockcroft-Walton board (144 units)
    - Zynq boards (4 units)
    - Cross boards (12 units)
    - HV generator (4 units) + switches (4 units)
    - DC-DC converters (4 units)
  - **Trigger**
    - (Firmware on the Zynq board)
  - **Mechanics**
    - PDM mechanical structure, Cooling system, EMC shielding
- **Cherenkov Camera**
  - **Optics**
    - 4 x CC PDMs → 32 Elementary Cell (EC) with 1 SiPM array each
  - **Electronics**
    - ASIC boards (4 units?)
    - FPGA boards (4 units)
    - Synchronization system (1 unit)
    - Bias voltages generators (? units)
    - DC-DC converters (? Units)
  - **Trigger**
    - (Firmware on the FPGA board)
  - **Mechanics**
    - CC mechanical structure, Cooling/heating system, EMC shielding

TELESCOPE MAIN SUB-SYSTEMS

Data Processor

- **Electronics**
  - CPU (2 units, Hot and Cold)
  - Trg&Sync Boards (2 units)
  - GPS receivers (2 units, four antennas)
  - HK board
  - Ethernet switches (4 units)
  - Solid State Power Controller (2 units)
- **Mechanics**
  - DP box1 (Eurocard chassis)
  - DP box2 (Power & Ethernet box) (Eurocard chassis)
  - DP box3 (Power & Ethernet box) (Eurocard chassis)

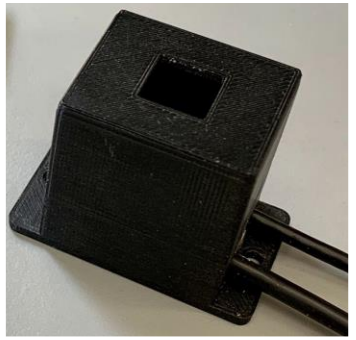
Ancillary devices

- Health LED (2 units)
- EMON (2 units)
- LID Controller ?
- Tilt system?

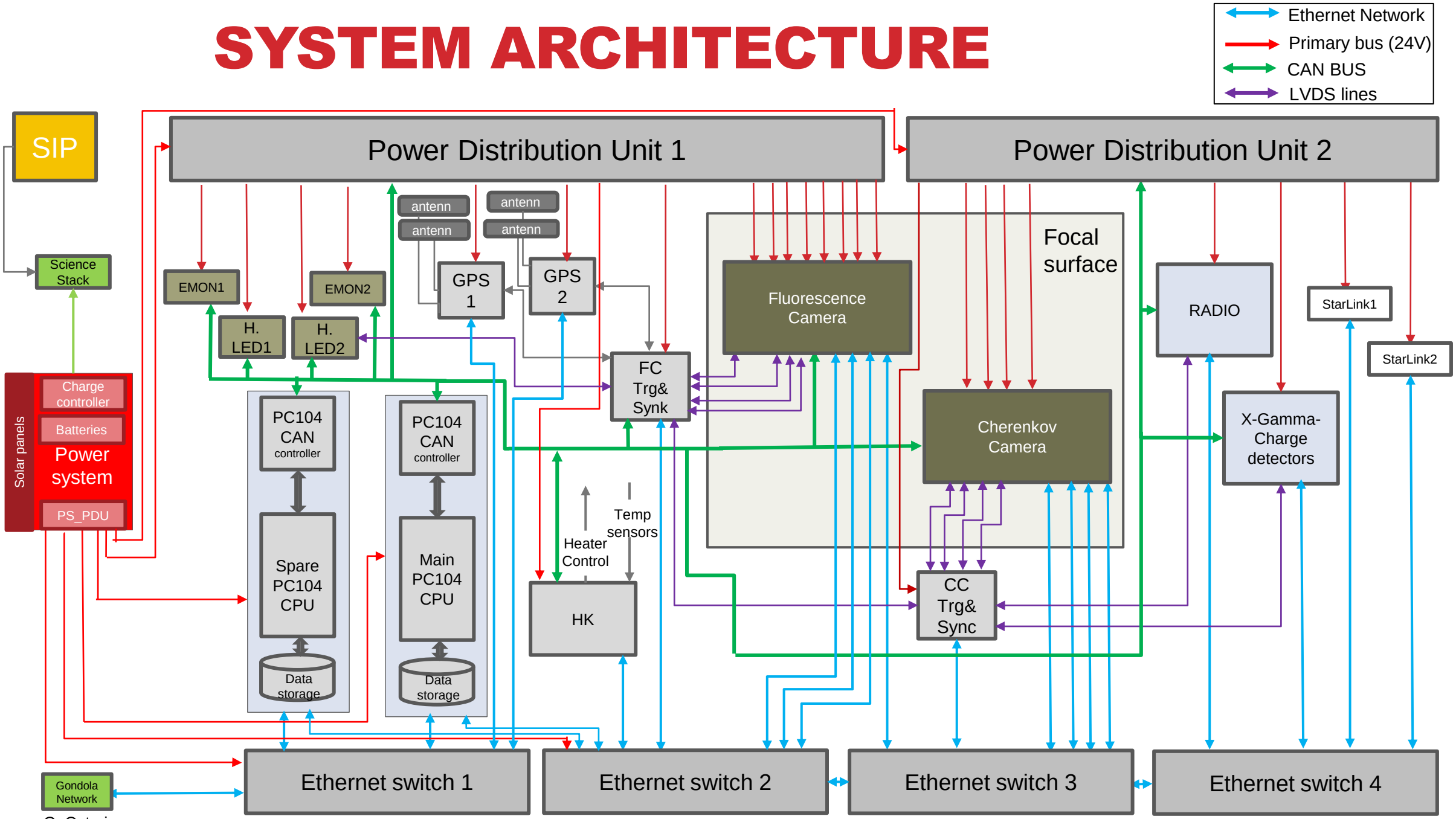
External Detectors

- RADIO
- X-Gamma detectors

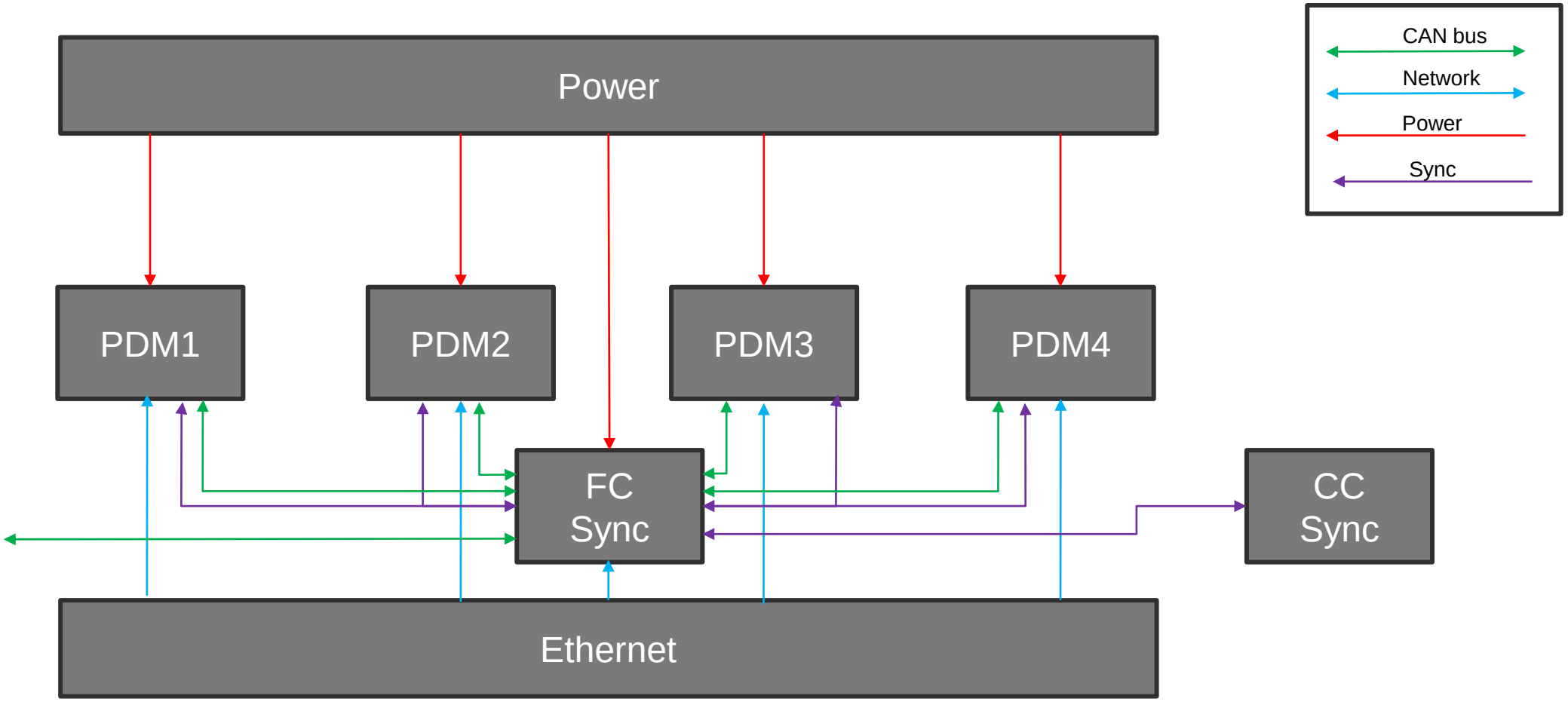
Harness (Cables, connectors, hatch panels) (a lot of…)



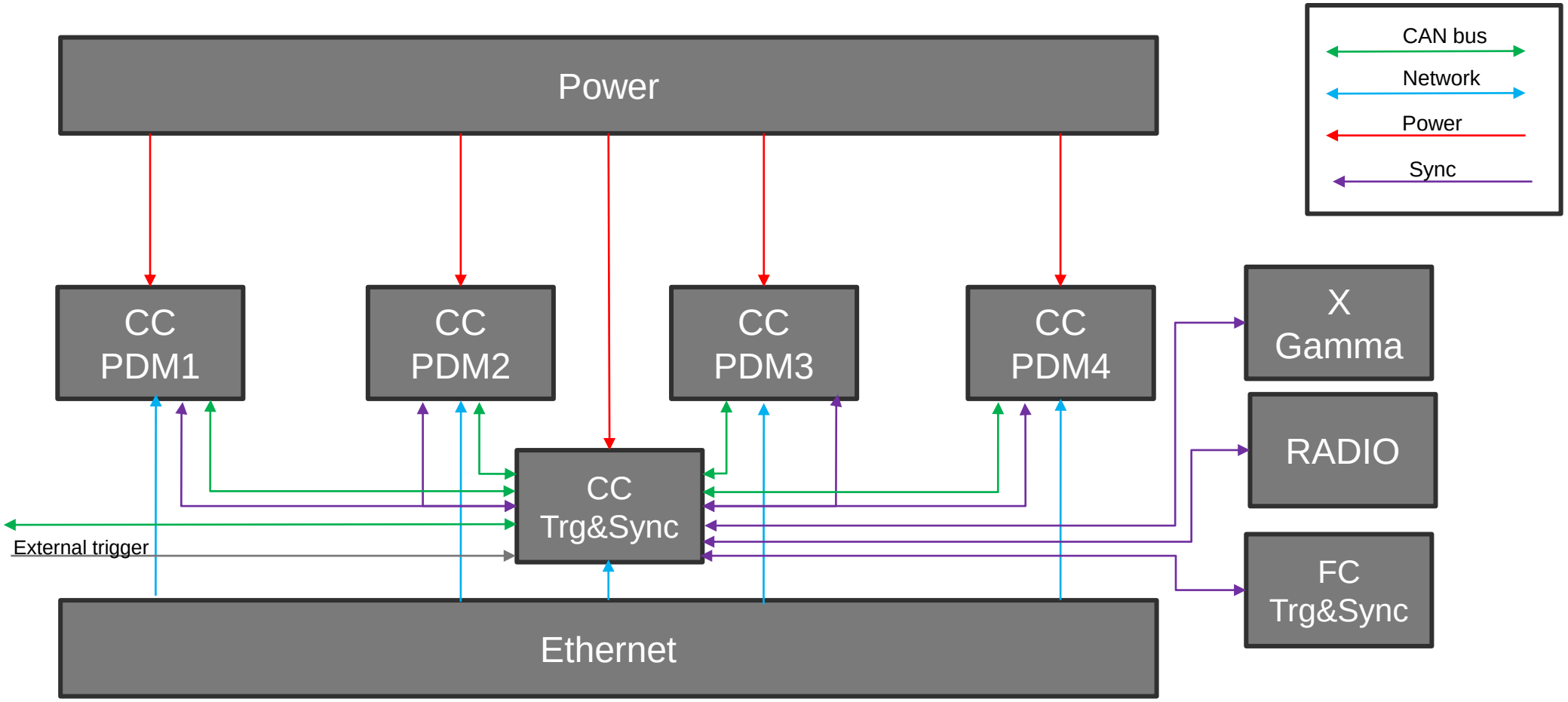
SYSTEM ARCHITECTURE



FC CAMERA

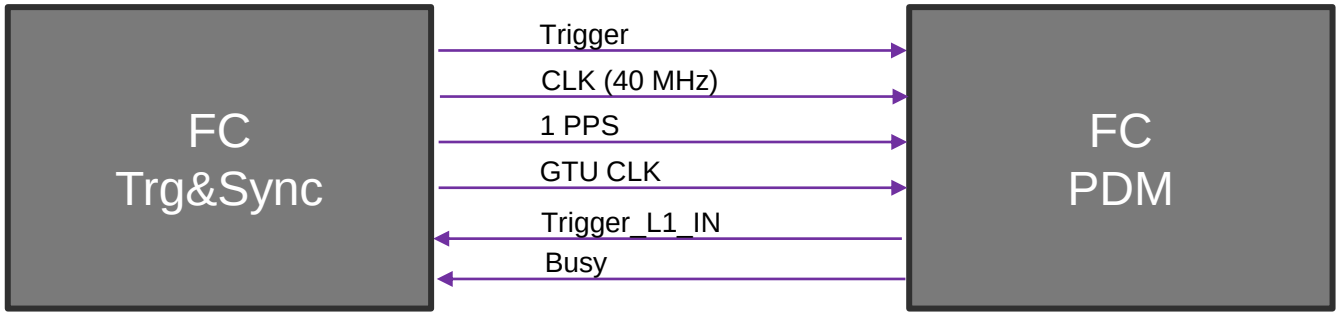

Power
PDM1
PDM2
PDM3
PDM4
FC
Sync
CC
Sync
Ethernet
CAN bus
Network
Power
Sync

CC CAMERA


CAN bus
Network
Power
Sync
Power
CC PDM1
CC PDM2
CC PDM3
CC PDM4
X Gamma
RADIO
FC Trg&Sync
CC Trg&Sync
External trigger
Ethernet

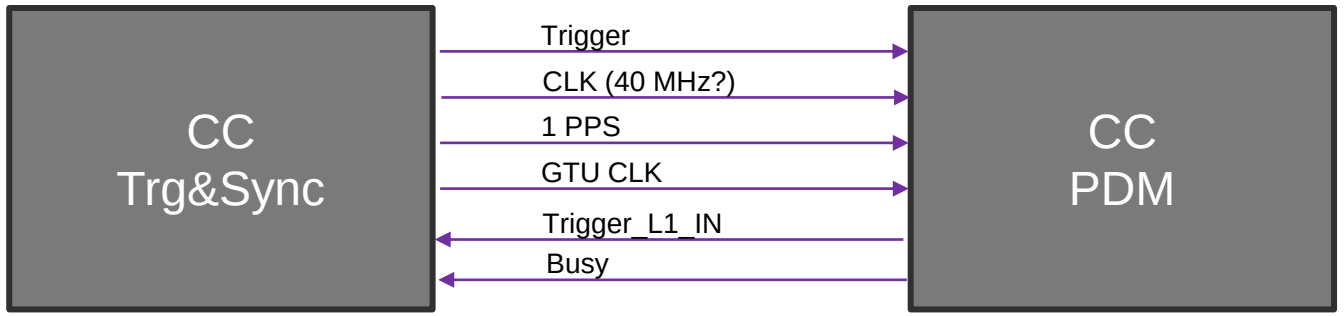
SYNCRHONIZATION SIGNALS: FC

LVDS opto isolated (on the CC_Trg&Sync side)



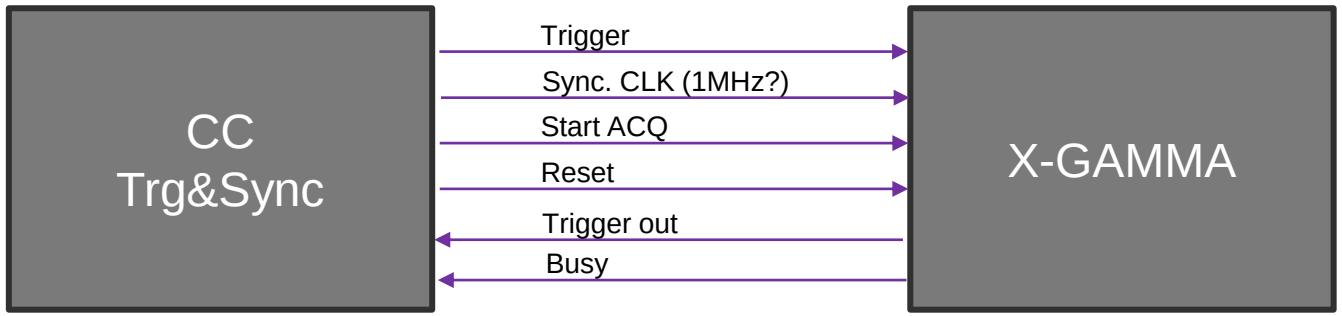
SYNCRHONIZATION SIGNALS: CC

LVDS opto isolated (on the CC_Trg&Sync side)



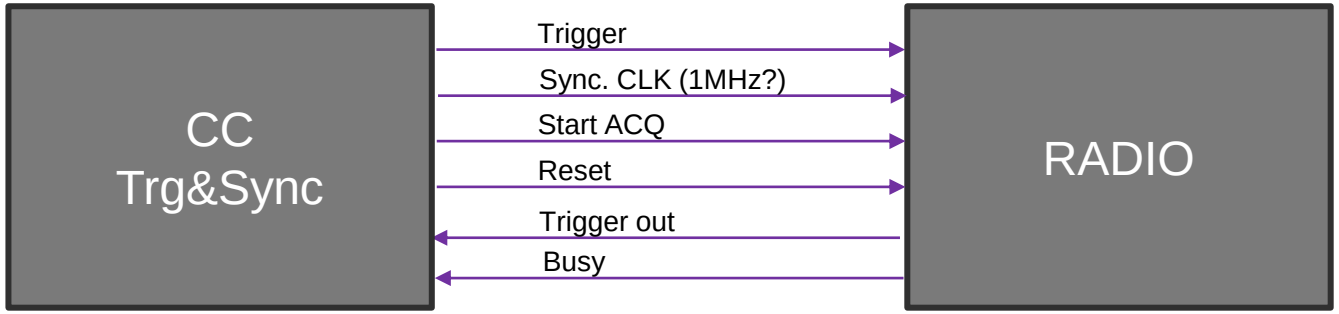
SYNCRHONIZATION SIGNALS: X-GAMMA

LVDS opto isolated (on the CC_Trg&Sync side)



SYNCRHONIZATION SIGNALS: RADIO

LVDS opto isolated (on the CC_Trg&Sync side)



TIMING & SYNC SIGNALS

CC and RADIO synchronized data acquisition

- **Trigger signal maximum delay ≈ 130 ns → memory buffer to store data on RADIO Board**
- **Trigger counter on RADIO board (counter Input = CLK_Trigger, counter reset = CLK_Reset)**
- **Time counter on RADIO board (counter Input = CLK_Sync, counter reset = CLK_Reset)**
  - Second time counter (counter Input = 100 MHz local clock, counter reset = CLK_Sync)
  - Event time stamp obtained by combining data from the two time counters
- **Start acquisition: on command and on waiting for CLK_Start_ACQ**
- **Busy signal asserted by Radio board after receiving a CLK_Trigger signal and maintained until the end of event processing**

DAQ TIMING

Power ON :

- **Internal integrity check**
- **Reset all the internal counters**
- **Busy signal is asserted**
- **Acquires and transmits on CAN BUS slow control parameters**
- **Wait for a Configure System commands sequence from CPU**
  - Configure parameters
- **Wait for a Start ACQ command from CPU**

DAQ TIMING

Start Acquisition:

- **Busy signal is de-asserted**
- **Wait for a trigger**

DAQ TIMING

When a trigger occurs:

- **Busy signal is asserted**
- **Scientific data are produced (ADC conversion, data transfer, etc)**
- **Scientific data are packed and stored in a FIFO memory**
  - FIFO depth > n events
  - (FIFO control lines move the Busy status)
- **As soon as the system is ready to receive a new trigger, Busy is de-asserted**
- **Wait for a new trigger**
- **A Finite State Machine starts to unpack and transfer data to the CPU**
  - Data ready to be transferred to the CPU («push» logic?)

DAQ TIMING

Stop Acquisition:

- **Busy signal is asserted**
- **Complete the unpack and transfer data to the CPU procedure**
- **Wait for a new command from the CPU**