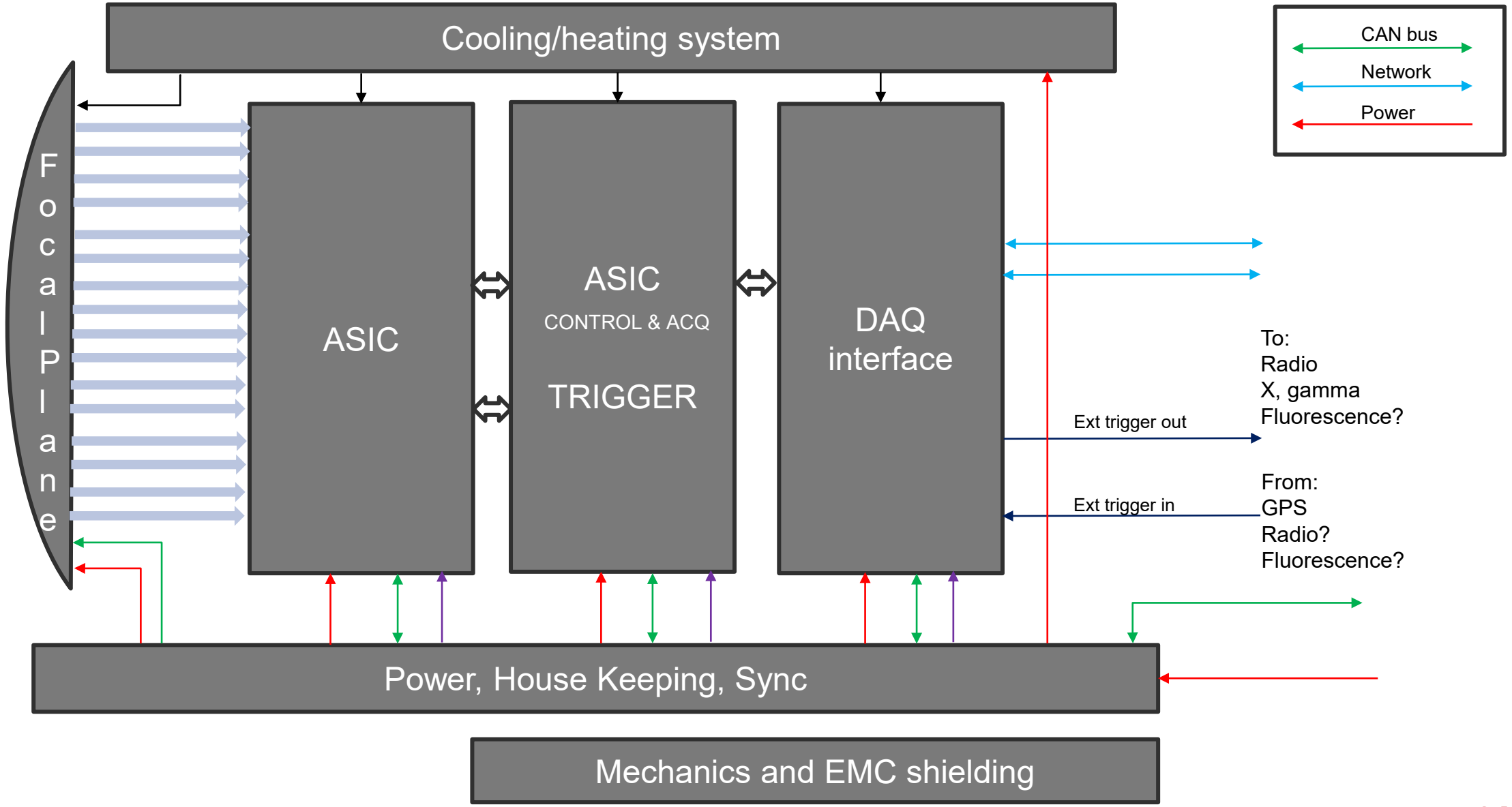
PBR
Wanaka NZ
2027

CHERENKOV CAMERA: AN OVERVIEW

GIUSEPPE OSTERIA (INFN NAPOLI)

CHERENKOV CAMERA: BLOCK DIAGRAM



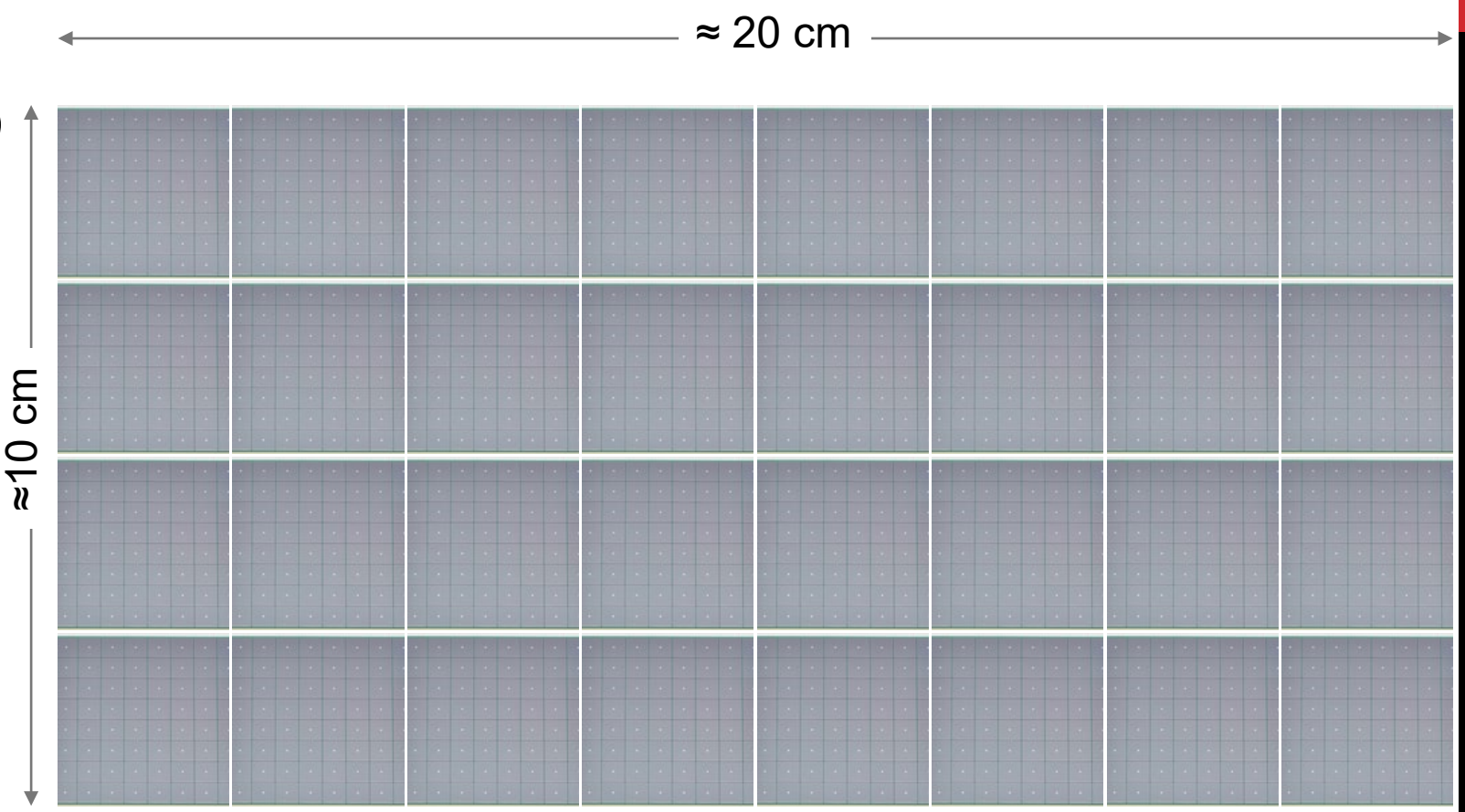
CC FOCAL PLANE

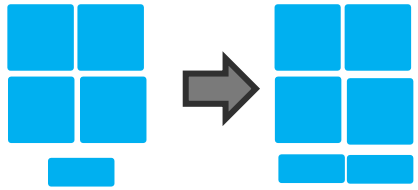
Requirements: (from simulations)

- **Pixel size: 3 x 3 mm²**
- **Pixel FoV: 0.2°**
- **Total FoV: 12° x 6° ****

Implementation:

- **SiPM arrays:**
  - 8 x 8 channels
    - 4 x 8 = 32 SiPM arrays
    - 2048 pixels
  - 4 x 4 channels
    - 8 x 16 = 96 SiPM arrays





** Why not 24° x 6°

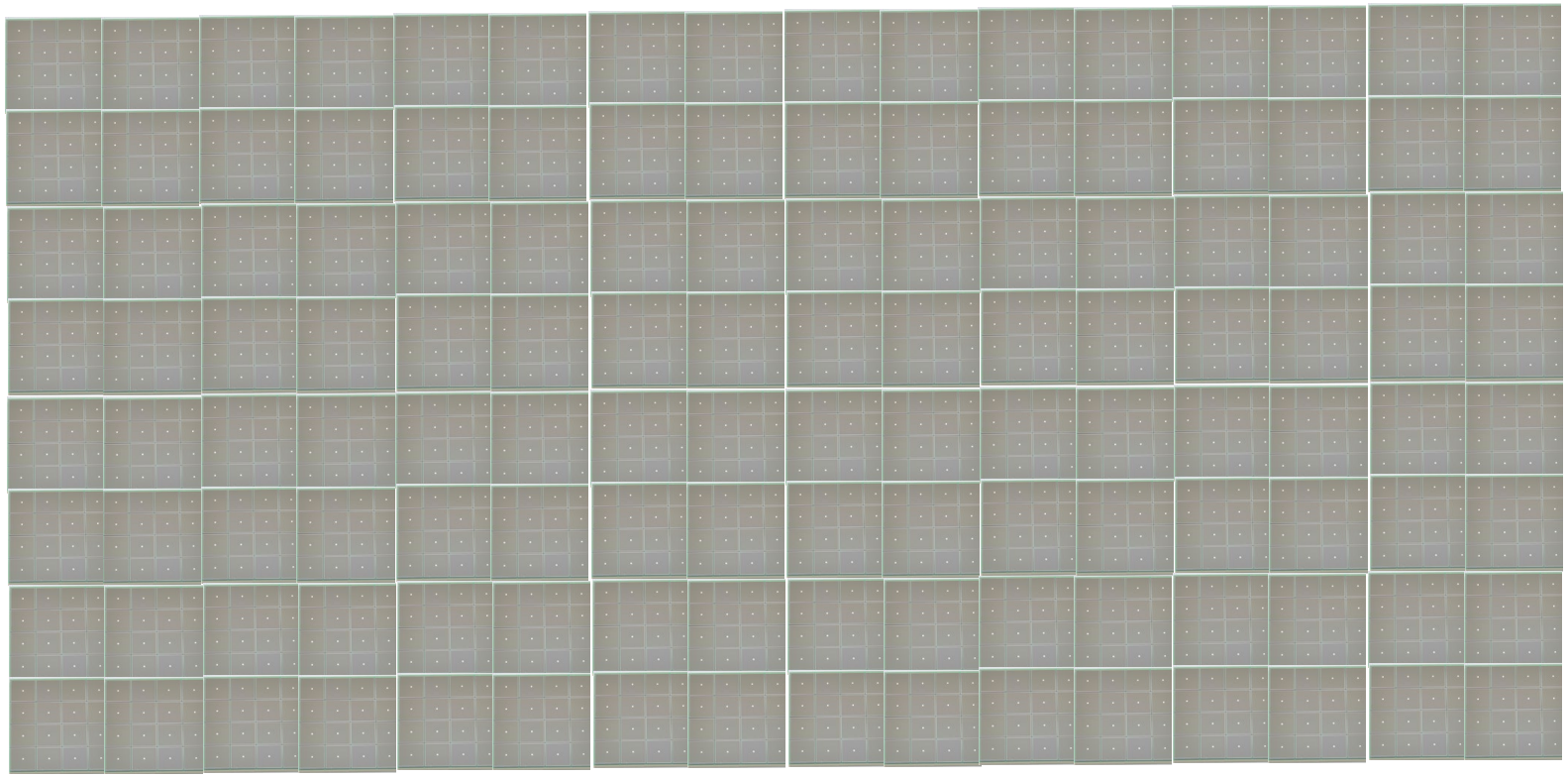
CC FOCAL PLANE

Requirements

- **Pixel size: 3 x 3 mm²**
- **Pixel FoV: 0.2°**
- **Total FoV: 12° x 6°**

Implementation:

- **SiPM arrays:**
  - 8 x 8 channels
    - 4 x 8 = 32 SiPM arrays
  - 4 x 4 channels
    - 8 x 16 = 96 SiPM arrays
    - 2048 channels



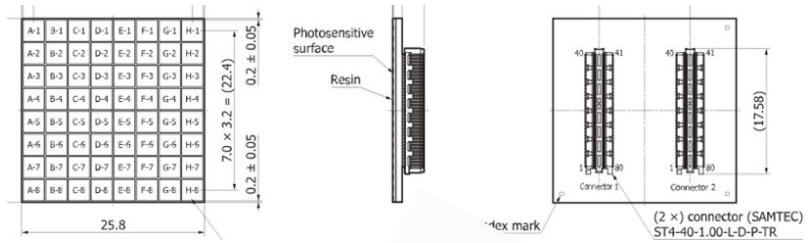
The choice should be guided by:

- Geometry of the resulting focal surface (the best approximation to the theoretical one)
- Fill factor or effective area
- Quality of the SiPM arrays (PDE, AP, CT, DCR, etc)
- Cost and delivery time of the SiPM arrays
- Complexity of the focal plane mechanics design
- Others…

CC FOCAL PLANE: GEOMETRY

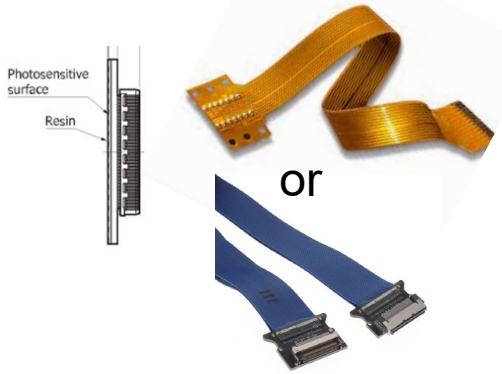
The PBR approach (study in progress)

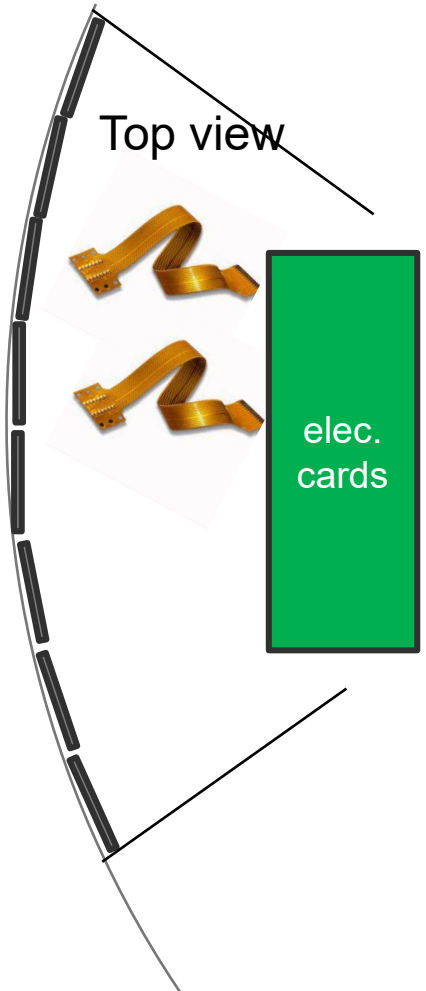
SiPM arrays: 8 x 8 channels (or 4 x 4 channels)
Pixel: 3 x 3 mm^2
Size of the elementary cell (EC): 2.5 x 2.5 cm^2 (or 1.3 x 1.3 cm^2)
1 arrays mounted on a flat PCB

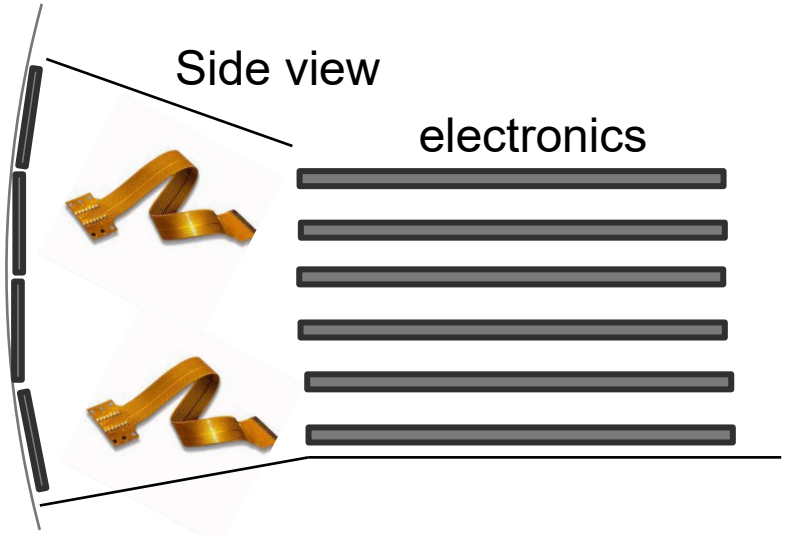


SiPM array mounted on PCB connected to the electronics through rigid flex connection

- Good geometry (better by using the 4x4 channels)
- Electronics cards far from sensors (separate cooling/heating systems for electronics and focal plane)
- EMC shielding: easy for the electronics cards







Problems:

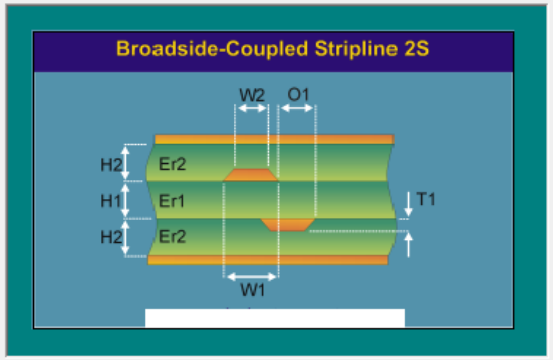
- Signal integrity?
- Cross talk?

Could the micro coaxial bundles (i.e. Samtec) be an alternative to a rigid-flex connection?

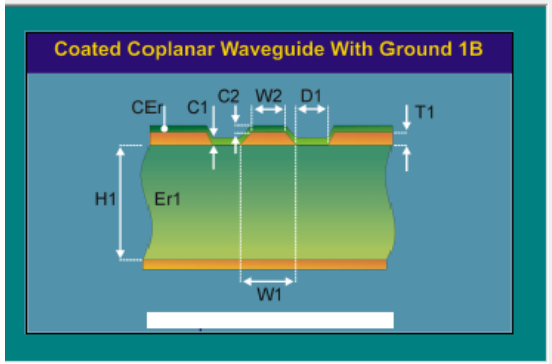
38 AWG 50 Ω coax or
36 AWG 50 Ω high-temp coax

CC FOCAL PLANE: GEOMETRY

Rigid-flex connection under study



				Tolerance	Minimum	Maximum	
Substrate 1 Height	H1	50,0000	+/-	0,0000	50,0000	50,0000	Calculate
Substrate 1 Dielectric	Er1	3,5000	+/-	0,0000	3,5000	3,5000	Calculate
Substrate 2 Height	H2	1000,0001	+/-	0,0000	1000,0001	1000,0001	Calculate
Substrate 2 Dielectric	Er2	3,5000	+/-	0,0000	3,5000	3,5000	Calculate
Lower Trace Width	W1	120,0000	+/-	0,0000	120,0000	120,0000	
Upper Trace Width	W2	110,0000	+/-	0,0000	110,0000	110,0000	Calculate
Trace Offset	O1	0,0000	+/-	0,0000	0,0000	0,0000	Calculate
Trace Thickness	T1	18,0000	+/-	0,0000	18,0000	18,0000	Calculate
Differential Impedance	Zdiff	50,60			50,60	50,60	Calculate



				Tolerance	Minimum	Maximum	
Substrate 1 Height	H1	1000,0001	+/-	0,0000	1000,0001	1000,0001	Calculate
Substrate 1 Dielectric	Er1	3,5000	+/-	0,0000	3,5000	3,5000	Calculate
Lower Trace Width	W1	300,0000	+/-	0,0000	300,0000	300,0000	
Upper Trace Width	W2	300,0000	+/-	0,0000	300,0000	300,0000	Calculate
Ground Strip Separation	D1	100,0000	+/-	0,0000	100,0000	100,0000	Calculate
Trace Thickness	T1	35,0000	+/-	0,0000	35,0000	35,0000	Calculate
Coating Above Substrate	C1	40,0000	+/-	0,0000	40,0000	40,0000	
Coating Above Trace	C2	40,0000	+/-	0,0000	40,0000	40,0000	
Coating Dielectric	CEr	3,5000	+/-	0,0000	3,5000	3,5000	
Impedance	Zo	52,42			52,42	52,42	Calculate

CC FOCAL PLANE: GEOMETRY

A possible PBR approach (TBD)

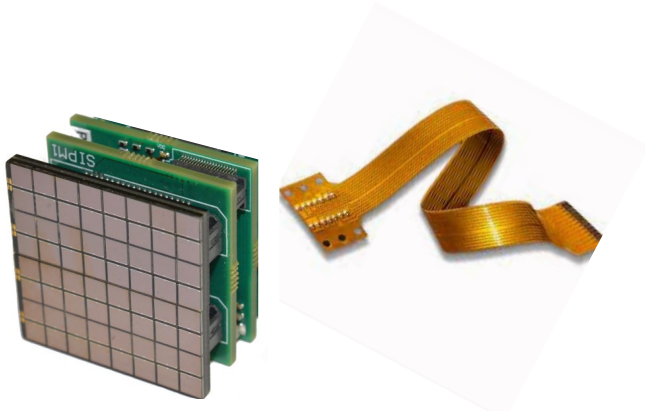
SiPM arrays: 8 x 8 channels
Pixel: 3 x 3 mm^2
Size of the elementary cell (EC): 2.5 x 2.5 cm^2
1 arrays mounted on a flat PCB

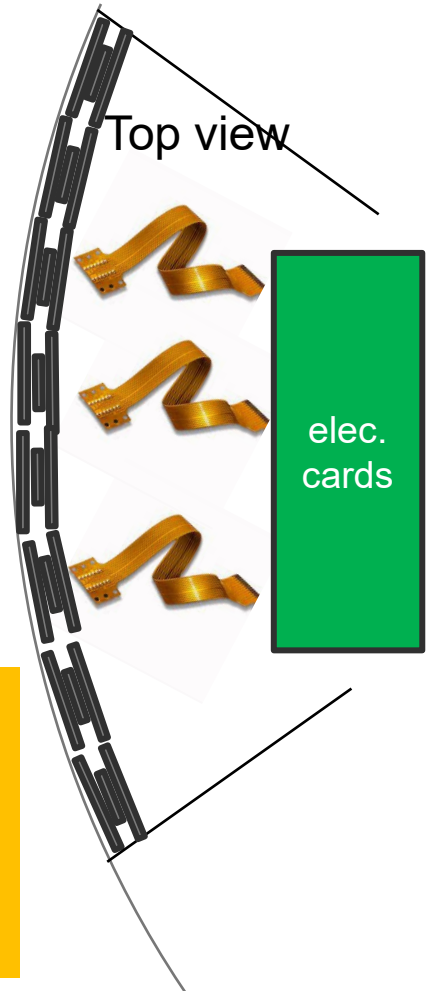
SiPM array mounted on PCB connected to a second PCB containing only the ASIC
the second PCB is connected to the electronics through a rigid-flex connection

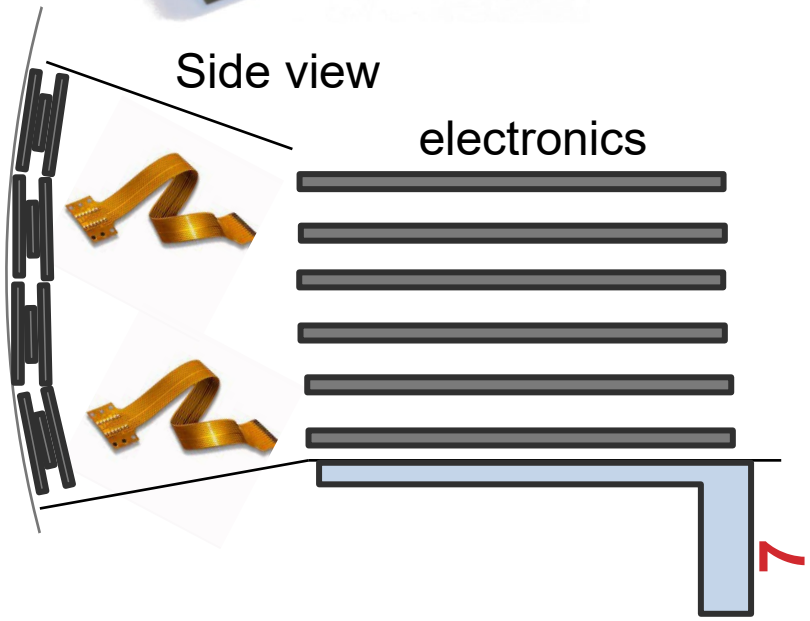
- Good (enough) geometry
- Signal integrity, No cross-talk
- Electronics cards (FPGA) far from sensors (easy cooling and EMC shielding systems)
-

Problems:

- Electronics (ASIC) close to the sensors
- → complex cooling/heating system for the focal plane
- EMC shielding of the focal plane complex







CC FOCAL PLANE: SENSORS

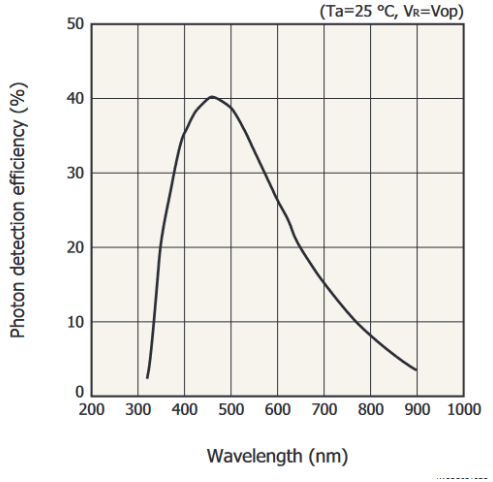
Hamamatsu S13361-3050 series

- S13361-3050-NE-04 (4x4ch), pixels 3mm^2
- S13361-3050-NE-08 (8x8ch), pixels 3mm^2

Absolute maximum ratings

Parameter	Symbol	S13361-3050NE-04	S13361-3050AE-04	S13361-3050NE-08	S13361-3050AE-08	Unit
Operating temperature*2	Topr	-20 to +60				°C
Storage temperature*2	Tstg	-20 to +80				°C
Soldering temperature*3	Tsol	240 (twice)	-	240 (twice)	-	°C

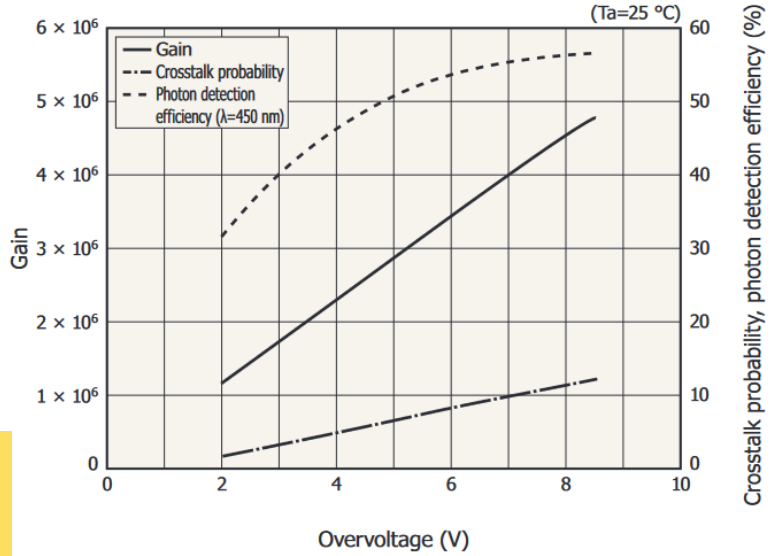
Photon detection efficiency vs. wavelength (typical example)



Electrical and optical characteristics (Typ. Ta=25 °C, Vover=3 V, unless otherwise noted)

Parameter		Symbol	Value	Unit
Spectral response range		λ	320 to 900	nm
Peak sensitivity wavelength		λp	450	nm
Photon detection efficiency (λ=λp)*4		PDE	40	%
Dark count*5	Typ.	CD	0.5	Mcps
	Max.		1.5	
Terminal capacitance		Ct	320	pF
Gain		M	1.7×10^6	-
Breakdown voltage		VBR	53 ± 5	V
Recommended operating voltage		Vop	VBR + 3	V
Vop variation between channels in one product	Typ.	-	0.1	V
	Max.		0.3	
Temperature coefficient of recommended operating voltage		ΔTVop	54	mV/°C

Overvoltage specifications of gain, crosstalk probability, photon detection efficiency



S13361-3050-NE-08
- Cost: (100 pce) 450/p €
- Delivery time: 5 months

CC FOCAL PLANE: SENSORS

FBK

NUV-HD-LowCT: (8 x 8 ch) pixels 3x3 mm^2

NUV-HD-MT

- DCR: 50 kHz/mm2
- AP: 5%
- CT: 5%-20%

- Cost: (100 pce) > 1000/pc €
- Delivery time: not before of November

Possible agreement to fund the production of the arrays needed for PBR (discussion in progress with GSSI)

CC FOCAL PLANE: TEMPERATURE SENSORS & BIAS VOLTAGES

One (at least) temperature sensor must be placed close to each SiPM array

- The measured temperature value shall be stored as scientific data for each event
- The temperature sensors shall be connected to the bias voltage system

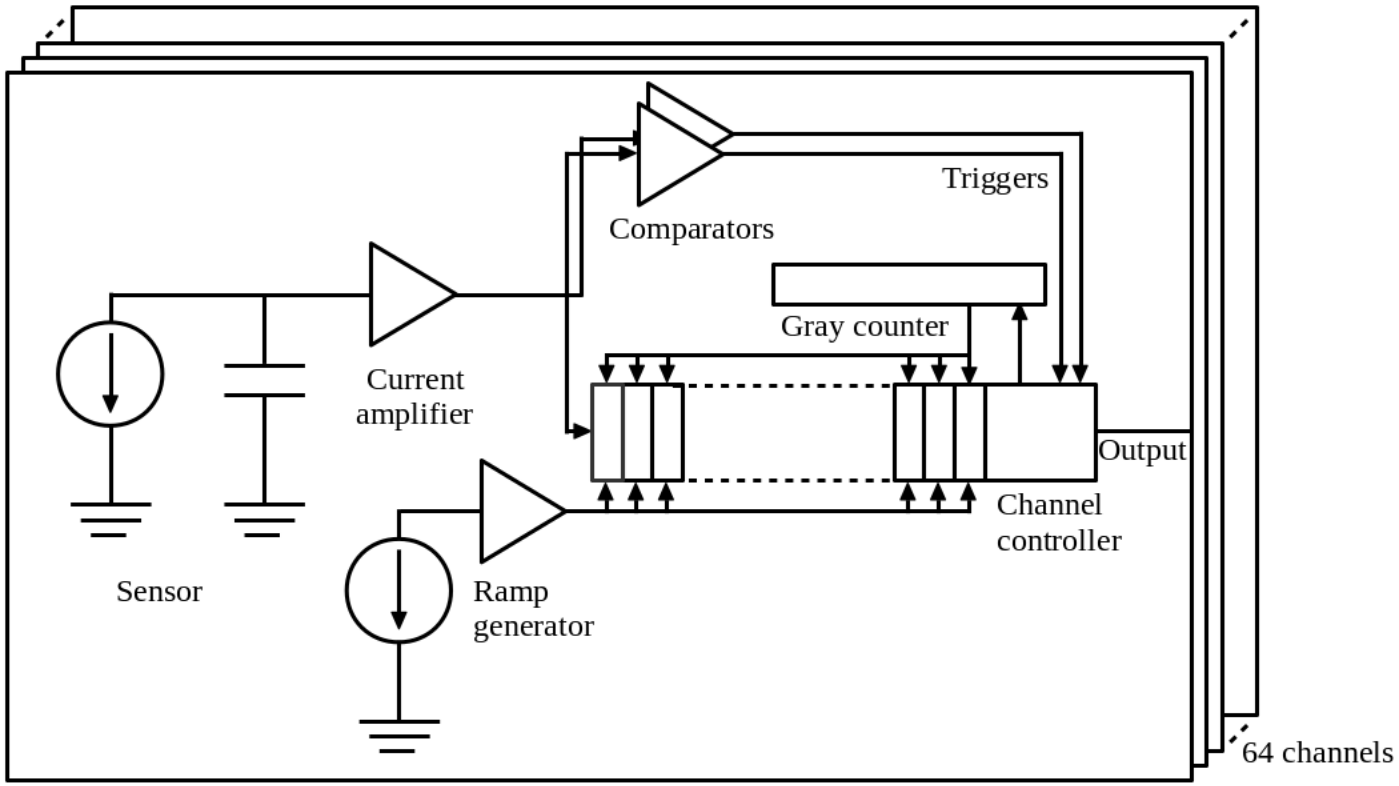
The Bias voltage distribution system shall provide one (at least) bias voltage for each SiPM array

- The bias voltage of each SiPM array shall be adjusted based on the value read by the temperature sensor
- The measured bias voltages shall be stored as scientific data for each event

The Bias Voltage system shall be hosted on the ASIC FPGA board

CC ASICS

MIZAR



- 64-channel ASIC implemented in a commercial 65 nm CMOS technology.
- High level of configurability
- Segmentation:
  - 32 cells
  - 64 cells
  - 256 cells
- Resolution:
  - 8 - 12 bits
- Trigger:
  - Internally generated
  - Externally provided
- Mode:
  - Sparse
  - Imaging

See talk by Mario

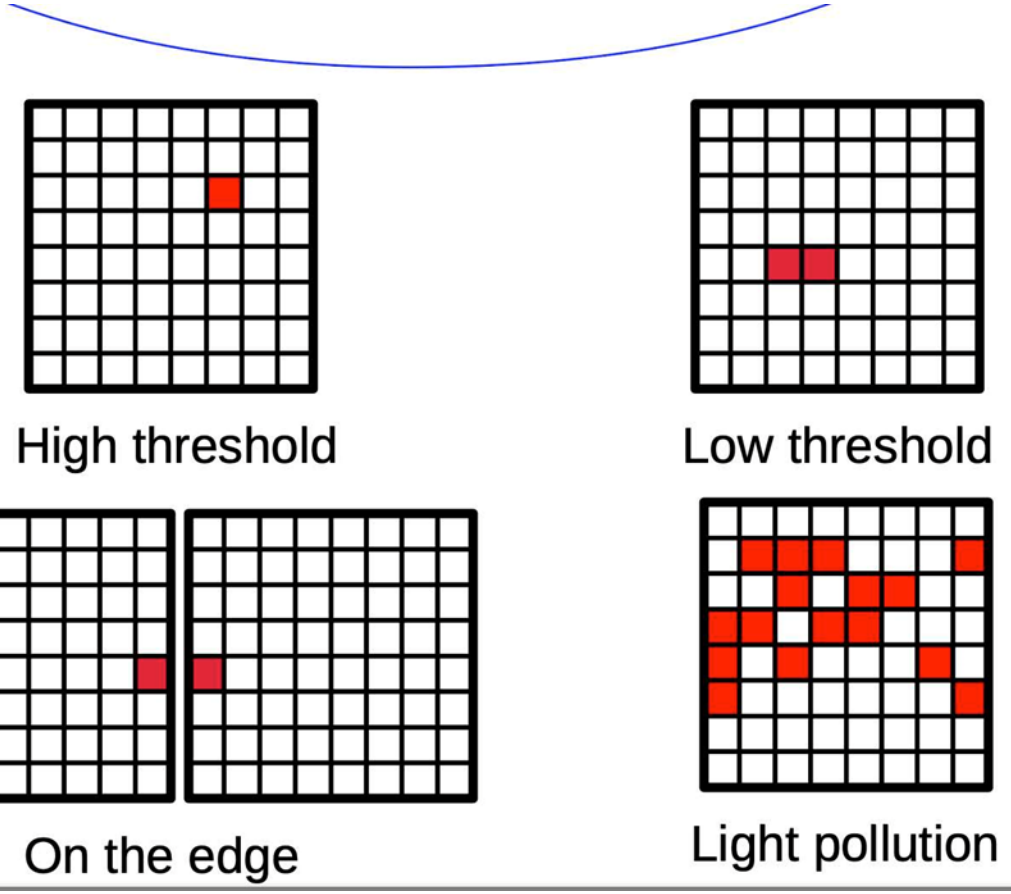
CC TRIGGER (MIZAR)

MIZAR ASIC:

internal logic to provide hitmaps

Three modes:

- **TIME WINDOW**
- **THRESHOLD DRIVEN**
- **FPGA REQUEST**



What about the bifocal events?

See talk by Stefan

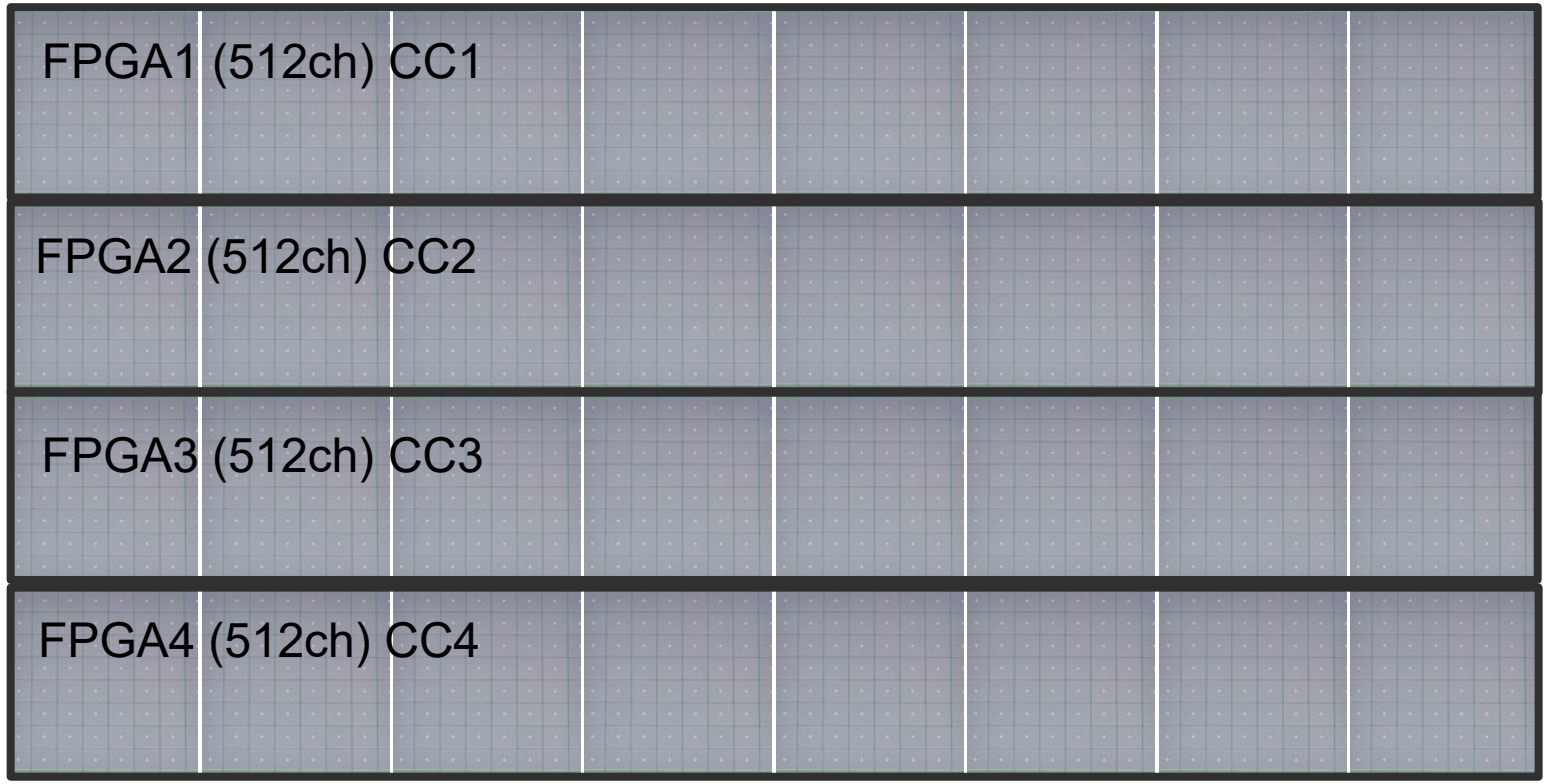
CC FPGA (MIZAR ASIC)

1 (big) FPGA could control up to 8 MIZAR ASIC

The four segments of the CC need to be synchronized by a master board

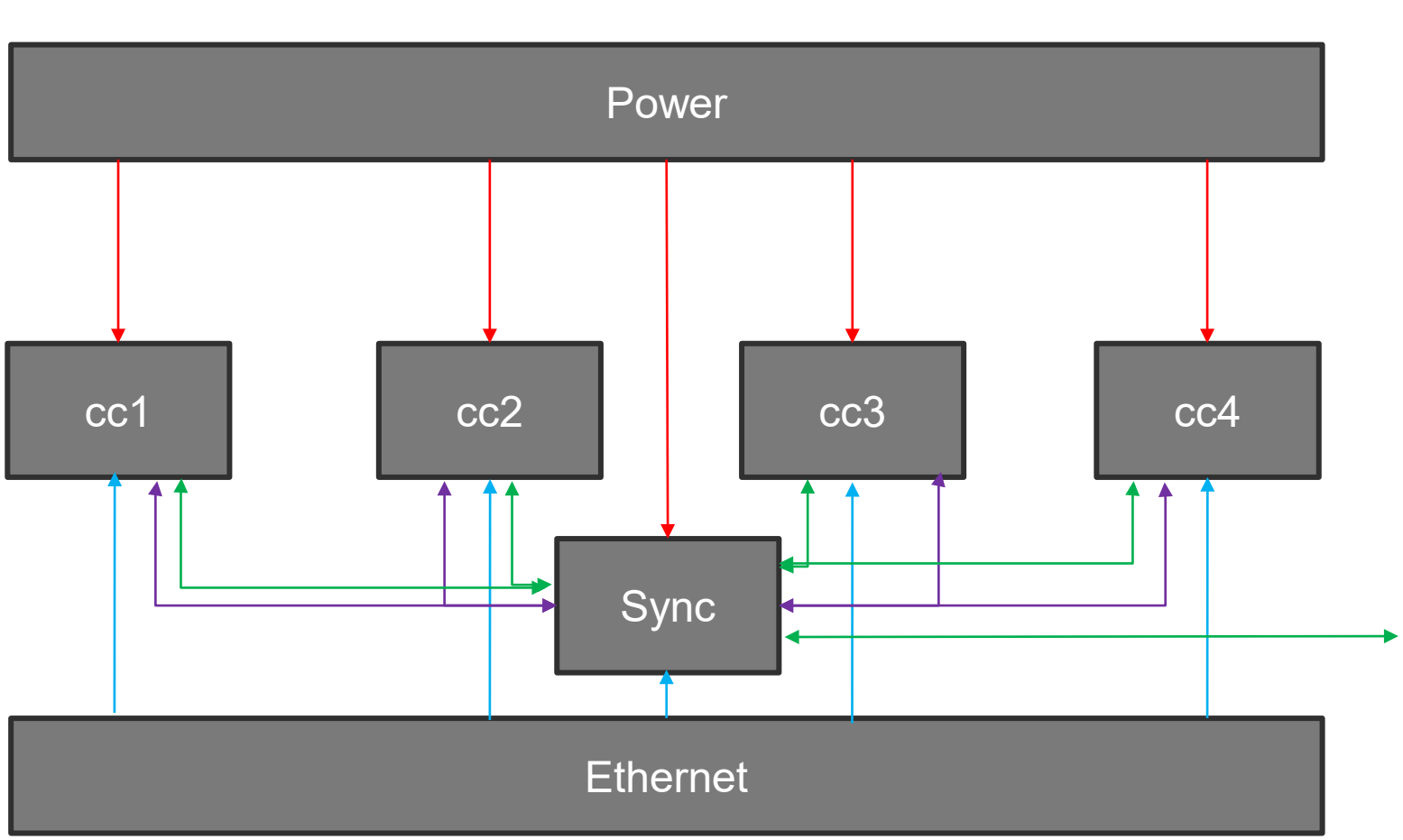
The master board manages and distributes:

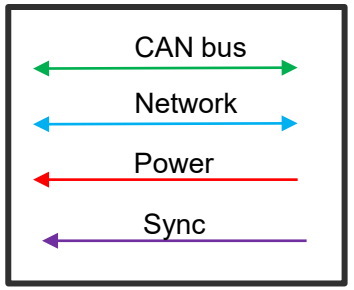
- **synchronization signals,**
- **Local and global trigger signals**
- **1 PPS signals from GPS**
- **Reset signals**
- **Vetos and Busy signals needed to define the live and dead time of the full camera (or of each segment in case they are acquired independently (TBD)**



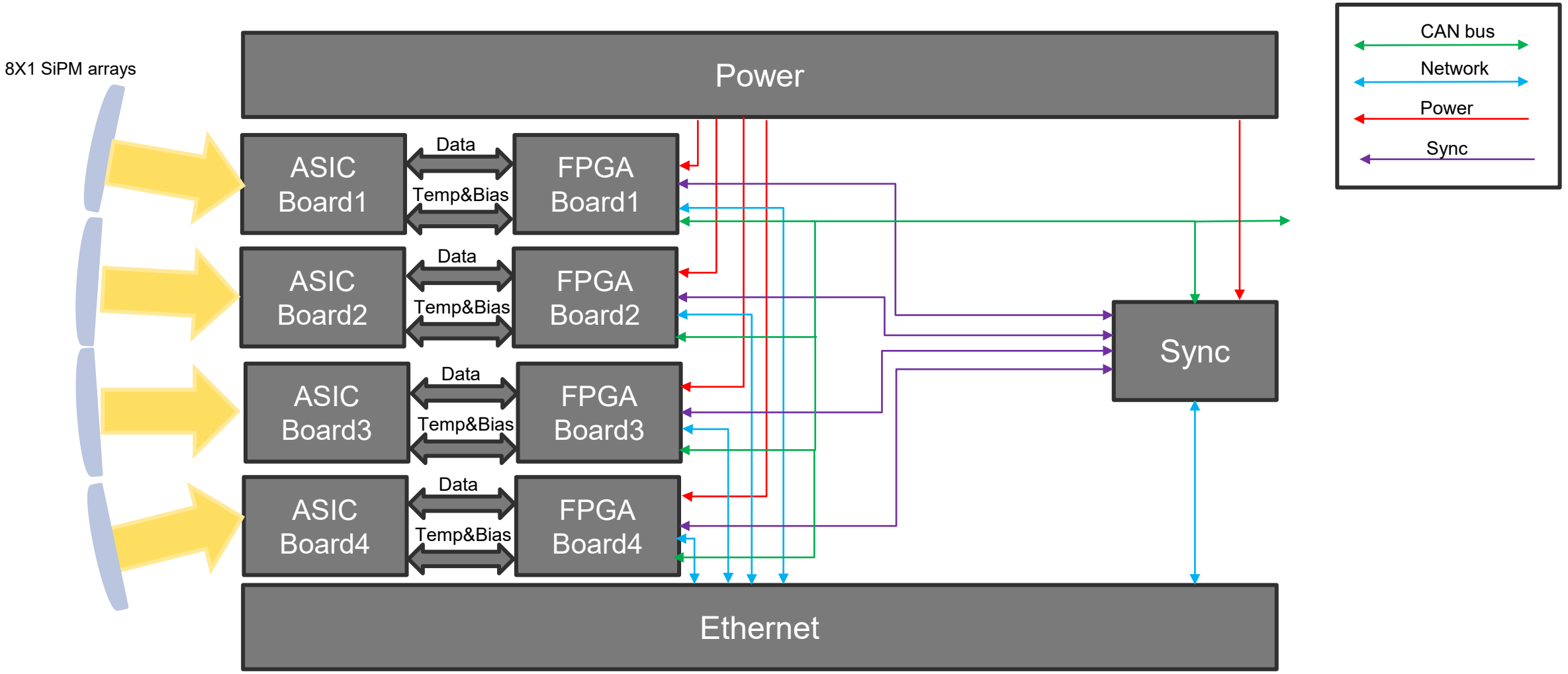
The master board could also perform the function of interface with the DAQ system (TBD)

CC CAMERA


Power
cc1
cc2
cc3
cc4
Sync
Ethernet


CAN bus
Network
Power
Sync

CC CAMERA


8X1 SiPM arrays
Power
ASIC Board1
Data
Temp&Bias
FPGA Board1
ASIC Board2
Data
Temp&Bias
FPGA Board2
ASIC Board3
Data
Temp&Bias
FPGA Board3
ASIC Board4
Data
Temp&Bias
FPGA Board4
Sync
Ethernet
CAN bus
Network
Power
Sync

STATUS (SUMMARY)

SIPM arrays procurement

- Hamamatsu S13361-3050 family selected as the baseline (TBC)
  - 100 pcs available by the end of May 2024 if ordered by Jan 2024
    - Cost for 100 pcs (S13361-3050-AE-08) is 450€ each
  - A few arrays have already been ordered and will be available by the end of January 2024 for prototype study.
- FBK NUV-HD-LowCT: (8 x 8 ch) pixels 3x3 mm^2
  - 100 pcs available by the end of November 2024 if ordered now
    - Cost for 100 pcs > 1000€ each

ASIC procurement

- MIZAR ASIC: order for a foundry run on February 2024 just placed
  - 150 pcs available for PBR by the end of May
- Other ASICs: available in a few months (or less) from the order

FPGA procurement

- Very preliminary study on the availability of the FPGA part numbers we are interested to
  - Most of the part numbers are available in stock
  - Longer delivery time for «industrial» or «automotive» versions of the same part numbers

SiPM arrays signals connection to ASICs

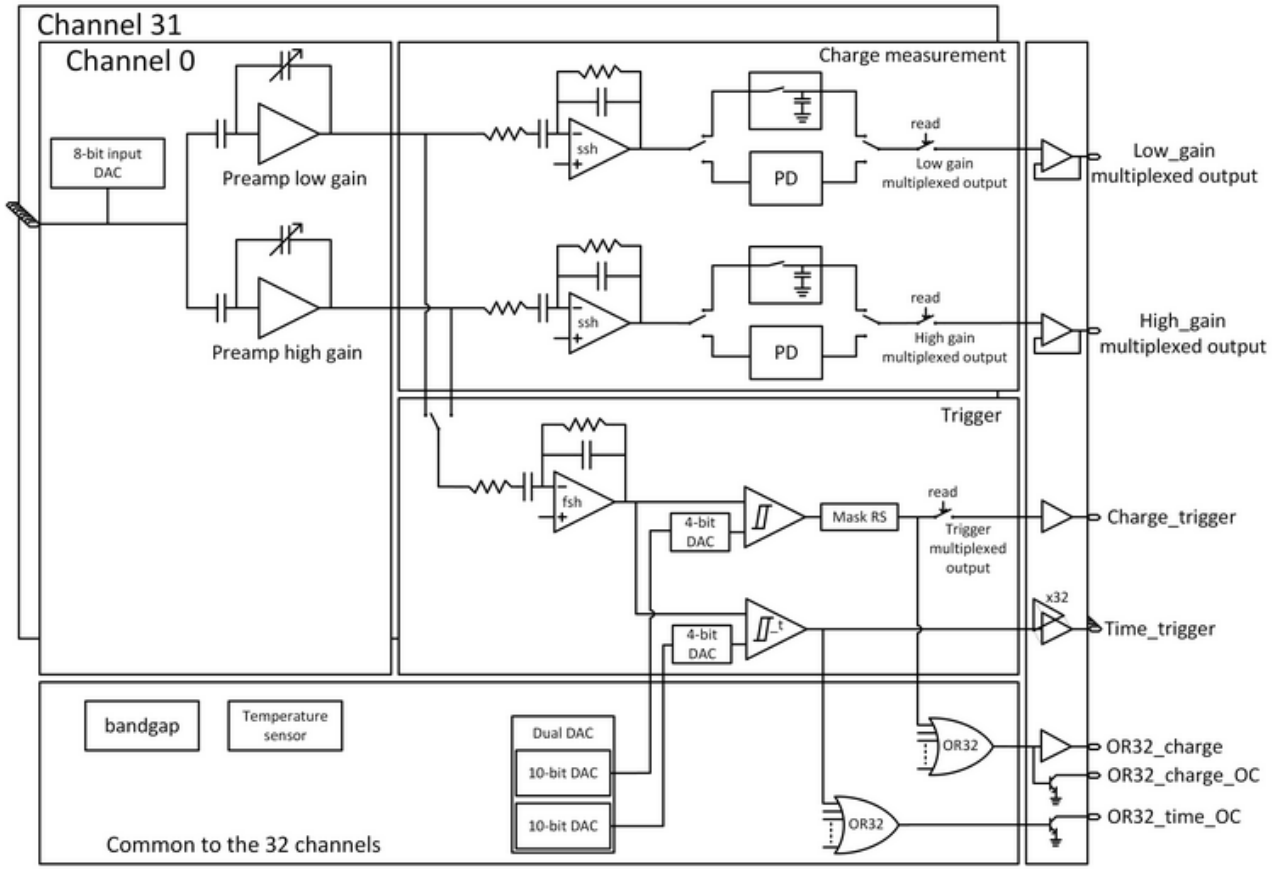
- Design of Rigid-flex PCBs with connectors for Hamamatsu S13361-3050-AE-04/08 in progress, order for several different prototypes already placed. First prototypes will be delivered by the end of 2023.

SPARE

CC ASICS

Alternative to MIZAR:

Citiroc 1A (or Radioroc*)



- 32-channel ASIC
  - 64 ch readout needs 2 ASICs
- Peak sensing mode
- 2 separate thresholds
- High and low gain output
- Need external ADCs
- Trigger algorithms only topological

*Radioroc is an evolution of the Citiroc 1A, same architecture, but with 64 channels and faster discriminators

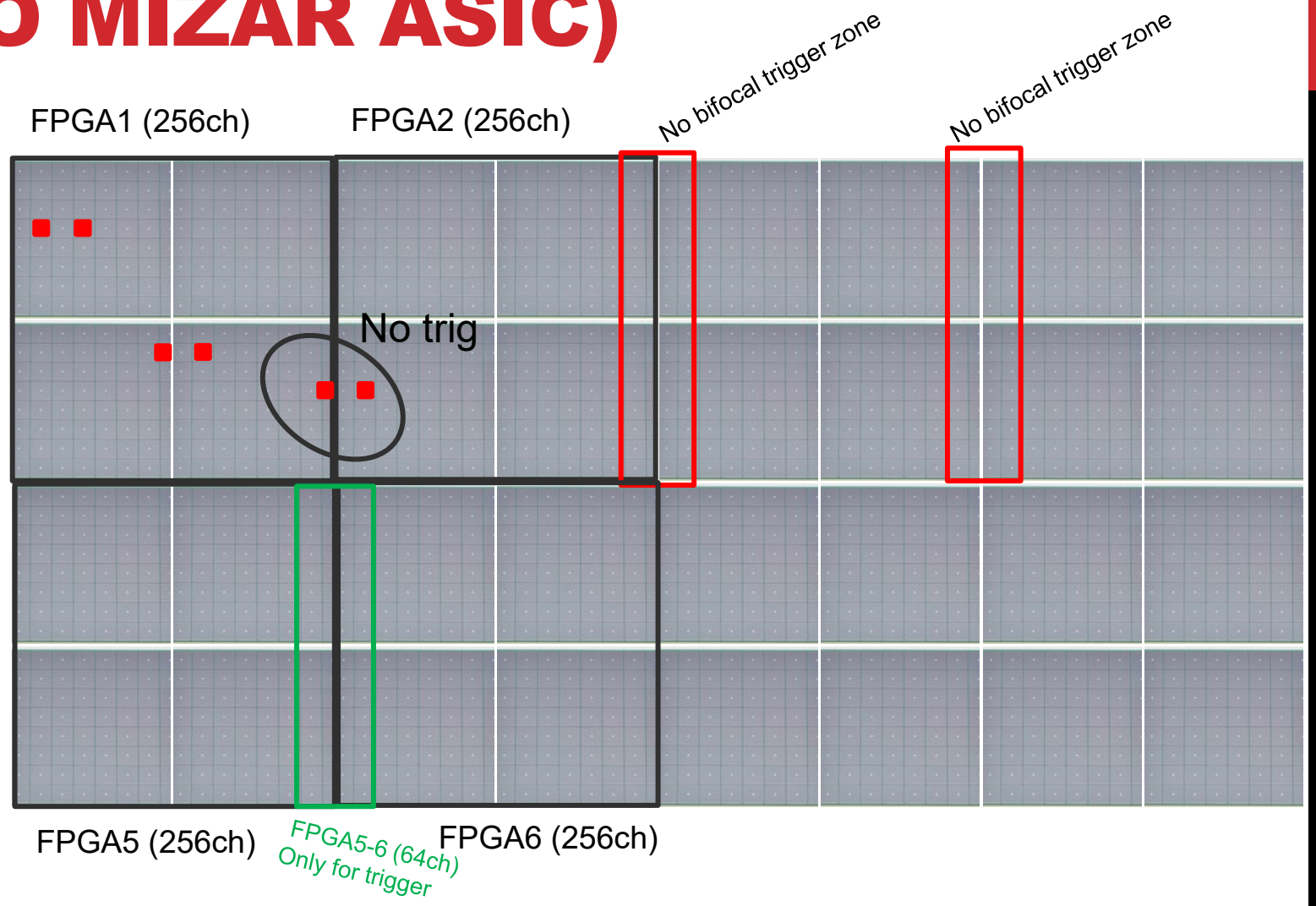
CC TRIGGER (NO MIZAR ASIC)

No hitmaps. ASIC outputs (one per pixel) must be used to generate the trigger. No event buffer, first level trigger decision very fast.

The trigger must be based on bifocal patterns.

The trigger efficiency of the full camera depends on how many ASICs are connected to the FPGA.

In this simplified scheme, the trigger is not working on about the 20% of the array's surface.



FPGA for trigger could be different from the one used to control and acquire the ASIC

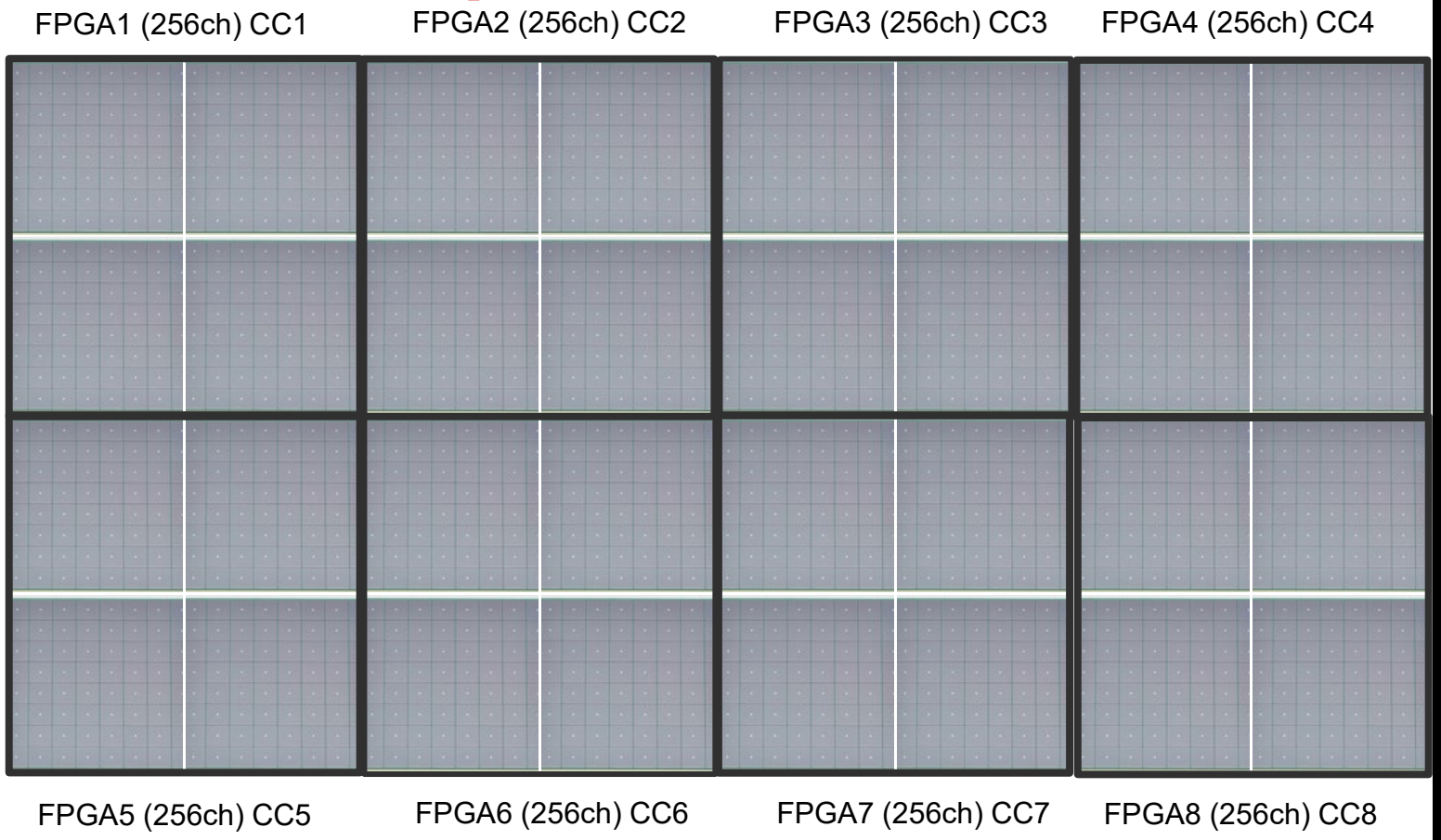
CC FPGA (NO MIZAR ASIC)

1 FPGA (Artix 7 family with 400 I/O pins) could control up to 4 ASICs

The eight segments of the CC need to be synchronized and acquired by a master board

The master board manages:

- **synchronization signals**
- **Local and global trigger signals**
- **1 PPS signal from GPS**
- **Reset signals**
- **Vetos and Busy signals needed to define the live and dead time of the full camera (or of each segment in case they are acquired independently (TBD)**



CC CAMERA NO MIZAR ASIC)