ALCOR FE & FAKE FE UPDATES

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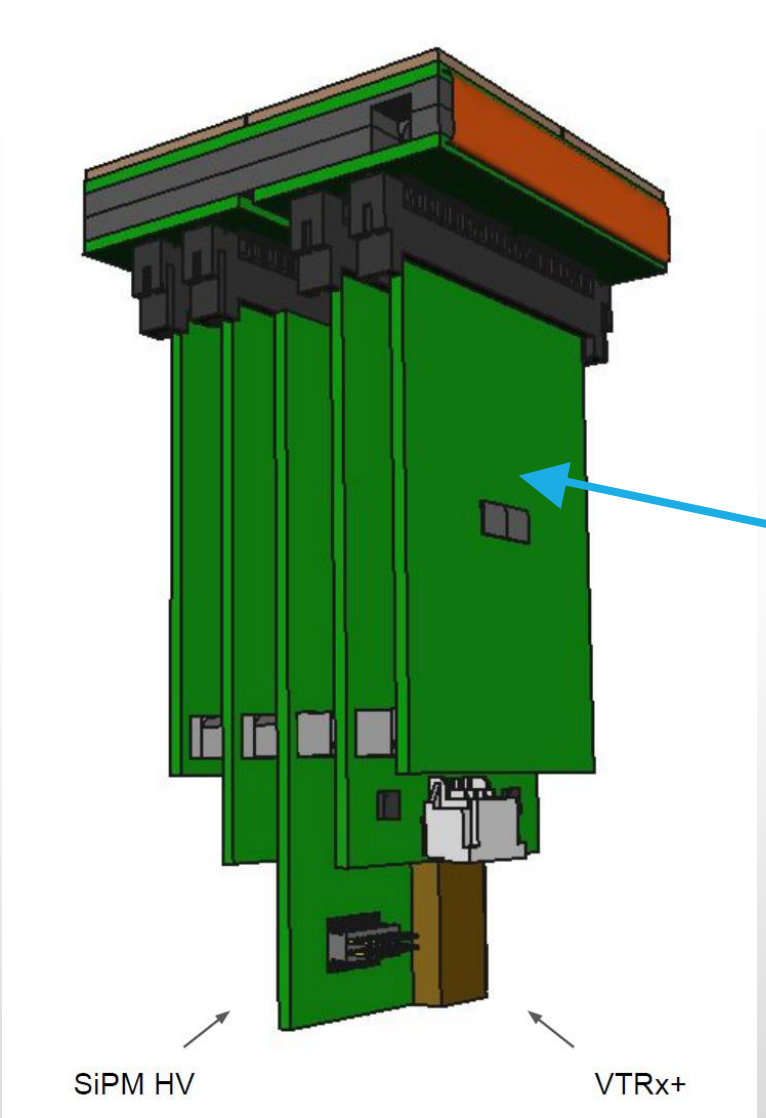
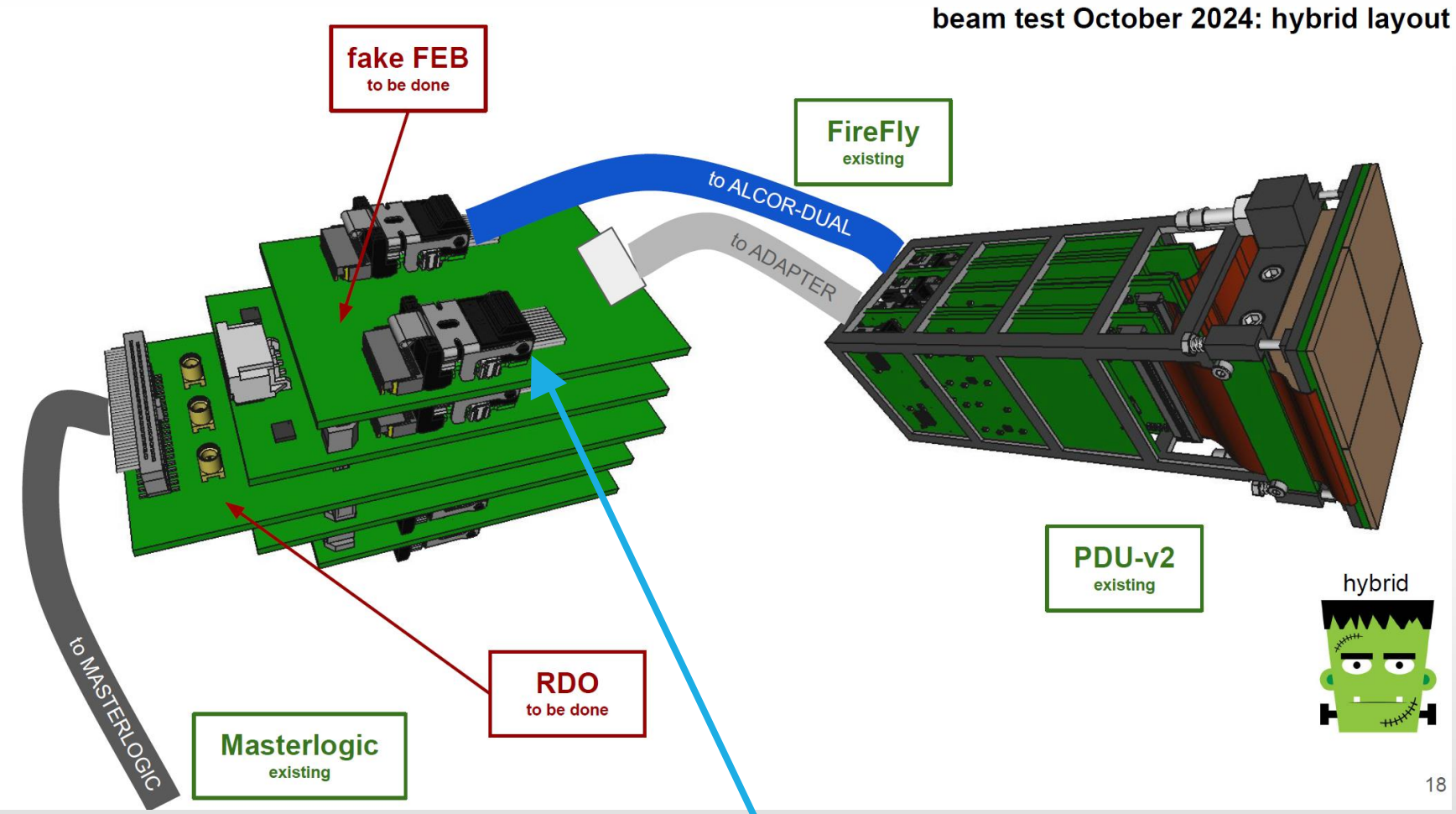
ALCOR 64 FE board



1 ALCOR 64 each FE board

Roberto's presentation
dRICH meeting May 2023

ALCOR 32 fake FE board



2x ALCOR32 each fake FE board

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ALCOR 64 digital signal count

- CLKin
- CLKout
- TP/SH
- 4x SPI signals (SDI, SDO, SCLK, SS)
- Reset
- 8x data links

- 16 signals, 32 pins
- Signals must be kept differential to minimize noise induction

ALCOR 32 digital signal count

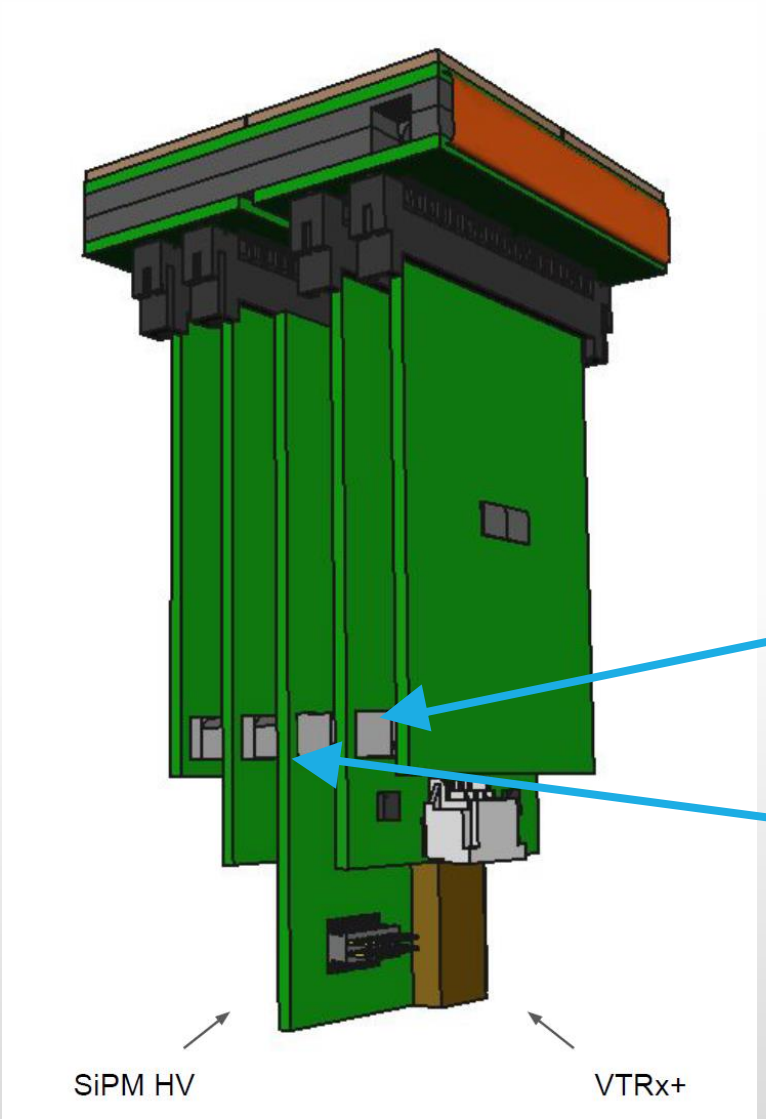
- CLKin
- CLKout
- TP/SH
- 4x SPI signals (SDI, SDO, SCLK, SS)
- Reset
- 4x data links

- 12 signals, 24 pins => 48 pins for 2x ALCOR32
- Pin count reduction is required to make it compatible with RO board pinout

Fake FE board pinout (digital)

- CLKout not used for serial data alignment. FPGA tests required (Davide F.)
- Reset and SPI enable (SS) single ended from FPGA. CMOS/LVDS translators on fake FE. The board won't be passive!
- TP, CLKin, SDI and SCLK splitted on board (single signal from FPGA). Active buffers required!
- SDO left as they are
- Total pin count for 2x ALCOR32: 32 pins like one ALCOR64 chip

ALCOR 64 FE board



ALCOR64 digital signals: 16 signals

2x ALCOR64 digital signals: 32 signals

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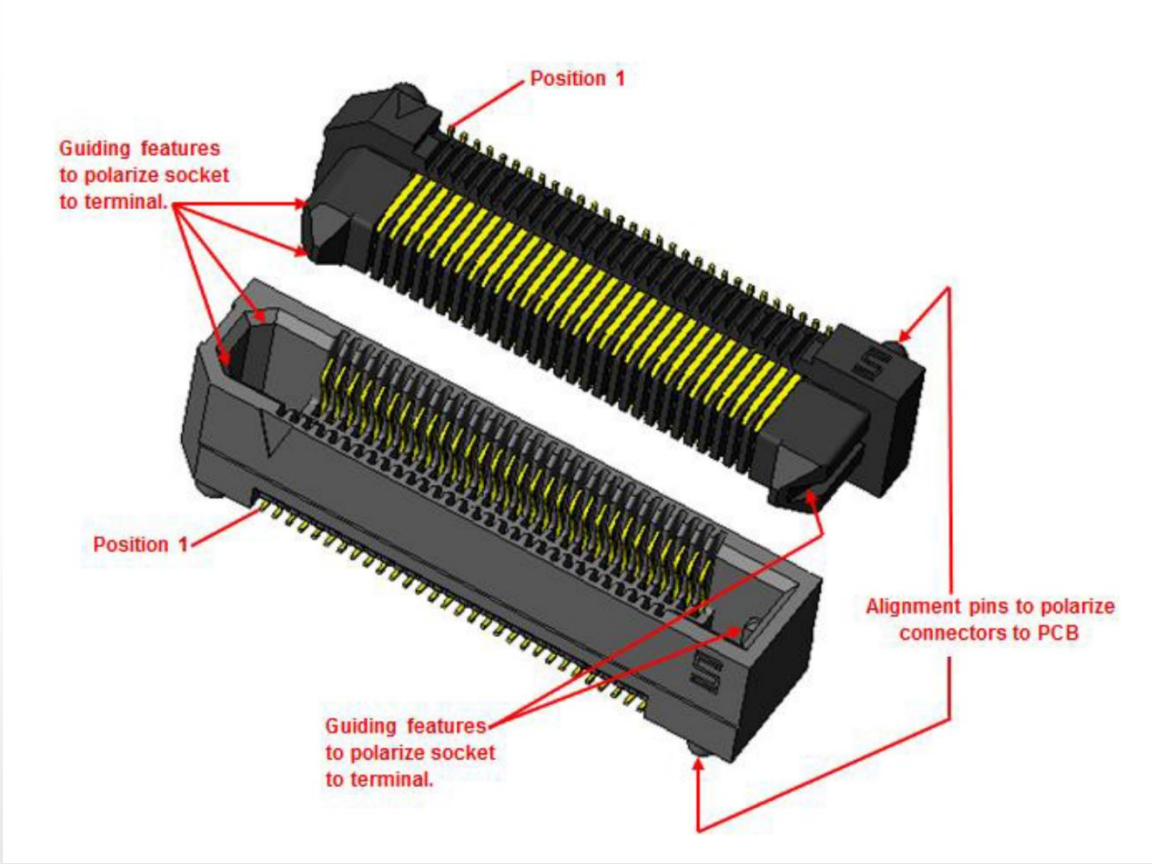
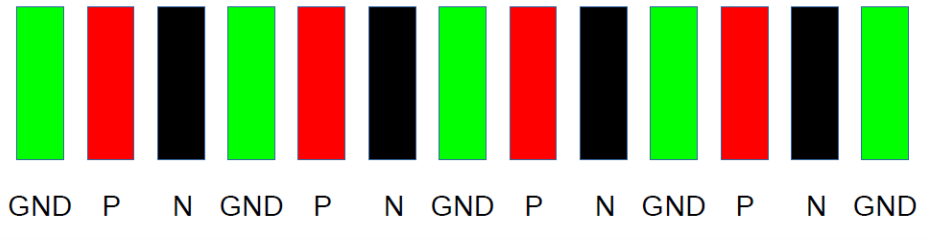
ERM5-050

FE-RDO connector





32 pairs => 64 pins + 32 ground pins => 96 pins

SAMTEC ERM5-050... (100 pin)

Staggered PCB position due to the alignment pins

Sheet1

ALCOR_FE_DUAL1				ALCOR_FE_DUAL2			
FireFly ACLOR1		FireFly ALCOR2		FireFly ACLOR3		FireFly ALCOR4	
B2	Q0_1N	B2	Q0_2N	B2	Q0_3N	B2	Q0_4N
B3	Q0_1P	B3	Q0_2P	B3	Q0_3P	B3	Q0_4P
B5	CLK_OUT1N	B5	CLK_OUT2N	B5	CLK_OUT3N	B5	CLK_OUT4N
B6	CLK_OUT1P	B6	CLK_OUT1P	B6	CLK_OUT3P	B6	CLK_OUT4P
B8	Q1_1N	B8	Q1_2N	B8	Q1_3N	B8	Q1_4N
B9	Q1_1P	B9	Q1_2P	B9	Q1_3P	B9	Q1_4P
B11	Q2_1N	B11	Q2_2N	B11	Q2_3N	B11	Q2_4N
B12	Q2_1P	B12	Q2_2P	B12	Q2_3P	B12	Q2_4P
B15	SS_N_1N	B15	SS_N_2N	B15	SS_N_3N	B15	SS_N_4N
B14	SS_N_1P	B14	SS_N_2P	B14	SS_N_3P	B14	SS_N_4P
B17	SDO_1N	B17	SDO_2N	B17	SDO_3N	B17	SDO_4N
B18	SDO_1P	B18	SDO_2P	B18	SDO_3P	B18	SDO_4P
A2	Q3_1N	A2	Q3_2N	A2	Q3_3N	A2	Q3_4N
A3	Q3_1P	A3	Q3_2P	A3	Q3_3P	A3	Q3_4P
A6	TP_1N	A6	TP_2N	A6	TP_3N	A6	TP_4N
A5	TP_1P	A5	TP_2P	A5	TP_3P	A5	TP_4P
A9	NRES_1N	A9	NRES_2N	A9	NRES_3N	A9	NRES_4N
A8	NRES_1P	A8	NRES_2P	A8	NRES_3P	A8	NRES_4P
A12	CLK_1N	A12	CLK_2N	A12	CLK_3N	A12	CLK_4N
A11	CLK_1P	A11	CLK_2P	A11	CLK_3P	A11	CLK_4P
A15	SDI_1N	A15	SDI_2N	A15	SDI_3N	A15	SDI_4N
A14	SDI_1P	A14	SDI_2P	A14	SDI_3P	A14	SDI_4P
A18	SCLK_1N	A18	SCLK_2N	A18	SCLK_3N	A18	SCLK_4N
A17	SCLK_1P	A17	SCLK_2P	A17	SCLK_3P	A17	SCLK_4P

FAKE_FEB ("MASTER")					
ERM5-050-…..					
26	GND	49	GND	20	GND
28	Q0_1N	51	Q0_4N	22	NRES_1
30	Q0_1P	53	Q0_4P	24	NRES_2
32	GND	55	GND	19	GND
34	Q1_1N	57	Q1_4N	21	NRES_3
36	Q1_1P	59	Q1_4P	23	NRES_4
38	GND	61	GND	86	GND
40	Q2_1N	63	Q2_4N	88	SS_N_1
42	Q2_1P	65	Q2_4P	90	SS_N_2
44	GND	67	GND	85	GND
46	Q3_1N	69	Q3_4N	87	SS_N_3
48	Q3_1P	71	Q3_4P	89	SS_N_4
50	GND	8	GND	80	GND
52	Q0_2N	10	CLK_12N	82	SDO_1N
54	Q0_2P	12	CLK_12P	84	SDO_1P
56	GND	7	GND	79	GND
58	Q1_2N	9	CLK_34N	81	SDO_2N
60	Q1_2P	11	CLK_34P	83	SDO_2P
62	GND	14	GND	2	GND
64	Q2_2N	16	TP_12N	4	SDO_3N
66	Q2_2P	18	TP_12P	6	SDO_3P
68	GND	13	GND	1	GND
70	Q3_2N	15	TP_34N	3	SDO_4N
72	Q3_2P	17	TP_34P	5	SDO_4P
25	GND	74	GND		
27	Q0_3N	76	SDI_12N		
29	Q0_3P	78	SDI_12P		
31	GND	73	GND		
33	Q1_3N	75	SDI_34N		
35	Q1_3P	77	SDI_34P		
37	GND	92	GND		
39	Q2_3N	94	SCLK_12N		
41	Q2_3P	96	SCLK_12P	98	GND
43	GND	91	GND		
45	Q3_3N	93	SCLK_34N		
47	Q3_3P	95	SCLK_34P	97	GND

ALCOR64_FEB ("MASTER")					
ERM5-050-…..					
26	GND	49	GND	20	GND
28	Q0_1N	51	Q4_2N	22	NRES_1N
30	Q0_1P	53	Q4_2P	24	NRES_1P
32	GND	55	GND	19	GND
34	Q1_1N	57	Q5_2N	21	NRES_2N
36	Q1_1P	59	Q5_2P	23	NRES_2P
38	GND	61	GND	86	GND
40	Q2_1N	63	Q6_2N	88	SS_N_1N
42	Q2_1P	65	Q6_2P	90	SS_N_1P
44	GND	67	GND	85	GND
46	Q3_1N	69	Q7_2N	87	SS_N_2N
48	Q3_1P	71	Q7_2P	89	SS_N_2P
50	GND	8	GND	80	GND
52	Q4_1N	10	CLK_1N	82	SDO_1N
54	Q4_1P	12	CLK_1P	84	SDO_1P
56	GND	7	GND	79	GND
58	Q5_1N	9	CLK_2N	81	SDO_2N
60	Q5_1P	11	CLK_2P	83	SDO_2P
62	GND	14	GND	2	GND
64	Q6_1N	16	TP_1N	4	CLKOUT_1N
66	Q6_1P	18	TP_1P	6	CLKOUT_1P
68	GND	13	GND	1	GND
70	Q7_1N	15	TP_2N	3	CLKOUT_2N
72	Q7_1P	17	TP_2P	5	CLKOUT_2P
25	GND	74	GND		
27	Q0_2N	76	SDI_1N		
29	Q0_2P	78	SDI_1P		
31	GND	73	GND		
33	Q1_2N	75	SDI_2N		
35	Q1_2P	77	SDI_2P		
37	GND	92	GND		
39	Q2_2N	94	SCLK_1N		
41	Q2_2P	96	SCLK_1P	98	GND
43	GND	91	GND		
45	Q3_2N	93	SCLK_2N		
47	Q3_2P	95	SCLK_2P	97	GND

Pending points

- Power supply connectors. One for each FE board should be preferred
- Local LDO on each FE board
- MOSFET drivers. Digital domain in analogue connector. Not good
- Temperature sensor. NTC?
- Fake FE: carefully check space for insertion FireFly connectors
- Many others points I forgot!