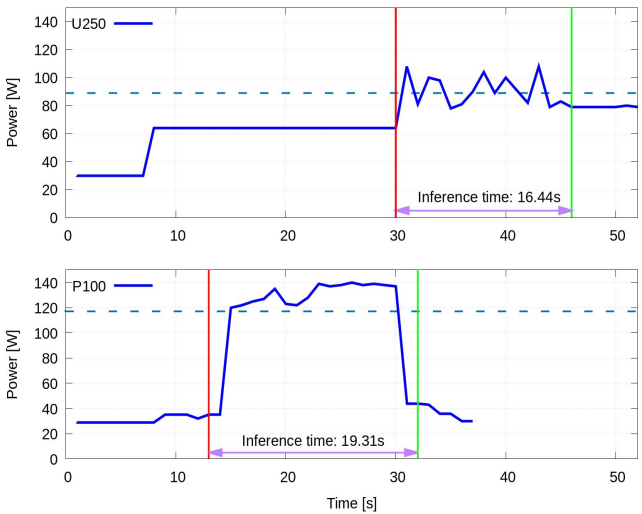
FPGA acceleration activities at INFN Ferrara

- FER (FPGA Empirical Roofline), a C/HLS benchmark developed to evaluate FPGAs as HPC accelerators:

  E. Calore and S. F. Schifano, "FER: A Benchmark for the Roofline Analysis of FPGA Based HPC Accelerators," in *IEEE Access*, vol. 10, pp. 94220-94234, 2022, doi: 10.1109/ACCESS.2022.3203566.

  Code available as Free Software: https://baltig.infn.it/EuroEXA/FER

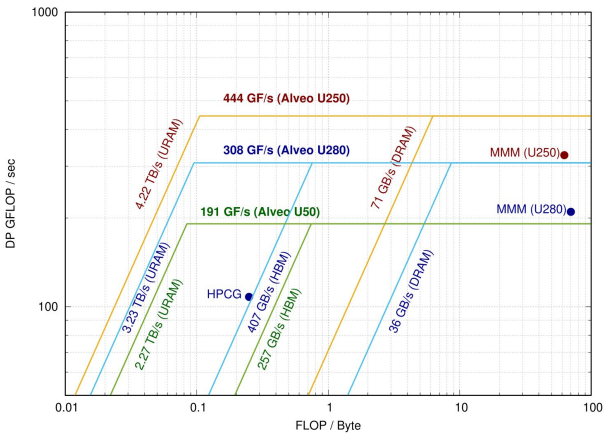
- Performance analysis of FPGAs as inference accelerators:



Metrica	P100	U250	Δ
Dice Score	0.94	0.92	-2%
Perf. [img/s]	480	495	+3%
E_{tot} [J/Kimg]	280	180	-36%
E_{dyn} [J/Kimg]	210	50	-76%

V. Sisini, "Analisi delle prestazioni di acceleratori basati su FPGA per la segmentazione di immagini", M.Sc. Thesis, University of Ferrara, 2023.

FER results on Alveos:



Alveo U250: