SuperB Meeting Queen Mary London:
ETD3 Parallel Session

Status of SVT front-end electronics

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on behalf of INFN and University of Milan

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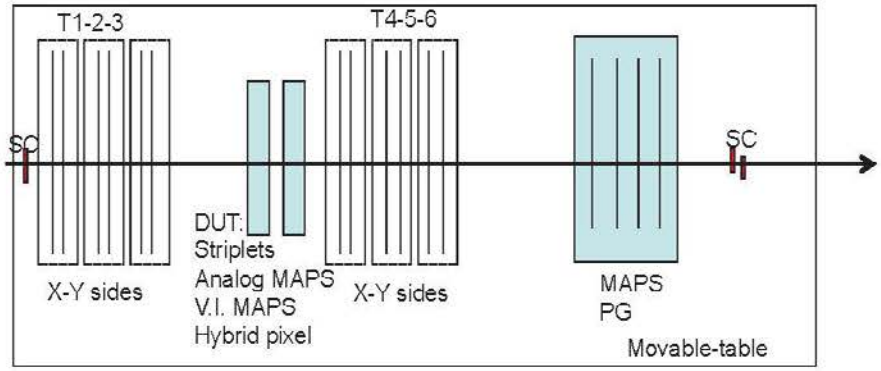
SVT System (1 of 2)

Giuliana Rizzo

Testbeam @CERN starting next week

- Most of the SVT group working hard over the summer to get things ready
  - Thanks to S. Bettarini for the organization
- Several pixel structures and striplets on test



New flexibility implemented in DAQ system (Bologna) to test all the different DUT's

Analysis team (Pi+BO+MI) is getting the new code ready

5 new telescope modules with FSSR2 readout built in Trieste to a have a 3+3 telescope configuration.

More robust movable table (Torino)

SVT System (2 of 2)

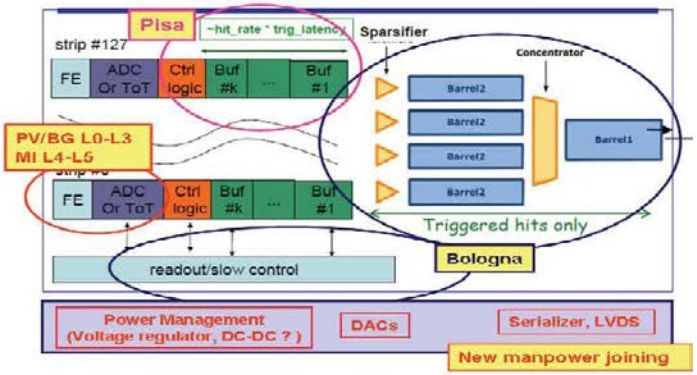
Giuliana Rizzo

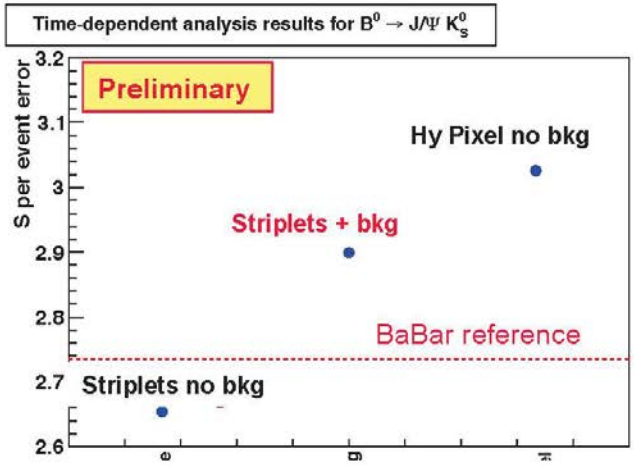
- Progress on Baseline configuration (Striplets L0+L1-L5 design)

Readout chips for striplets/strip:

- detailed plan for chip development by Italian groups presented to INFN.
  - Develop fast (L0-L3) and slow (L4-5) channels & adapt readout architecture used for pixel.
    - Full VHDL simulation for TDR.
    - Prototypes chips in 2012 & 2013
    - Production run in 2014

Readout chip for strips

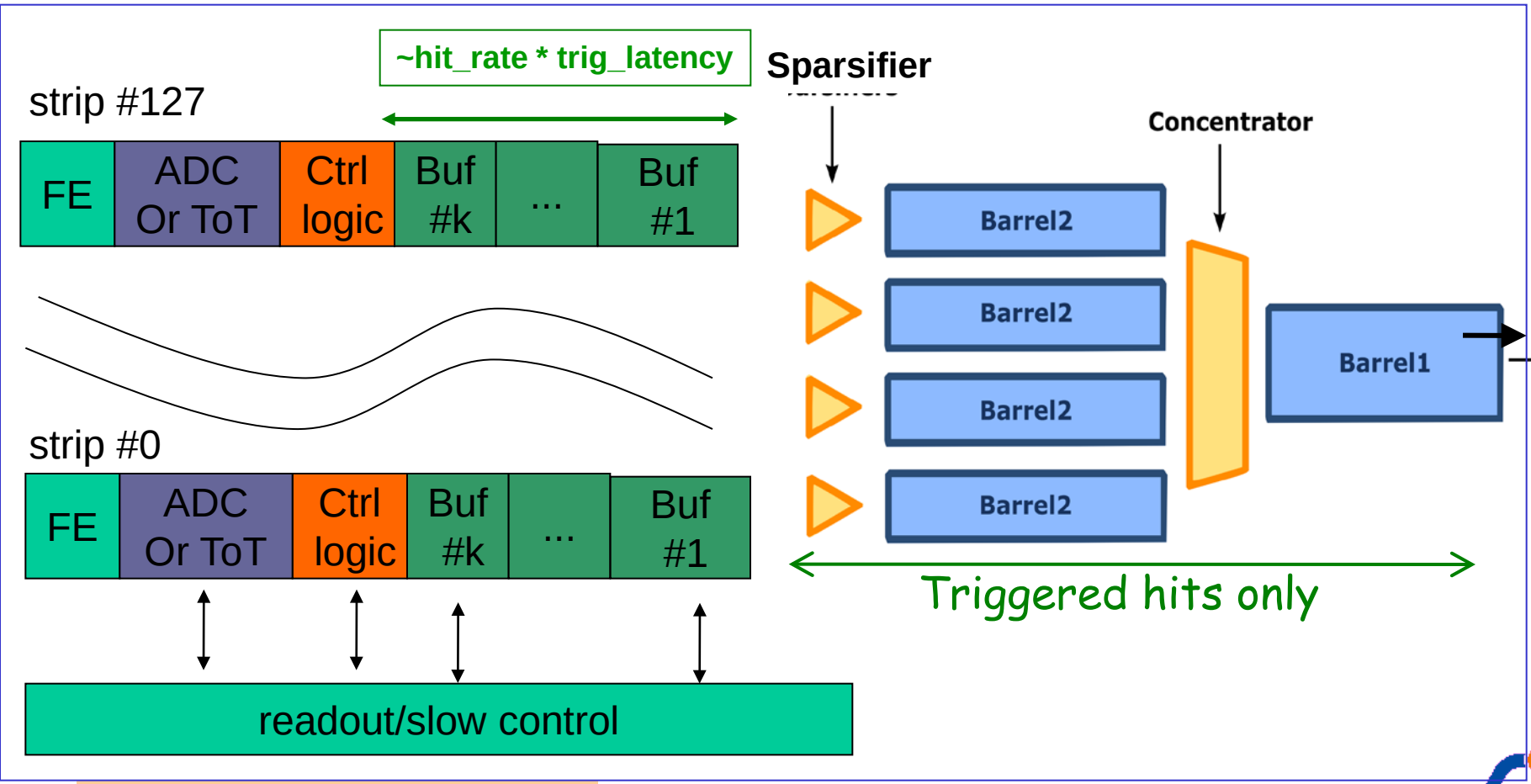




First preliminary results on striplets performance in high background with Fastsim

- Hits from background pairs added to signal for time dependent analysis.
  - Still safety factor not included on back rates.
- Checks on fundamental quantities still to be done and and several technical problems need to be fixed to perform systematic studies.

Readout chip for strips



How many buffers?
How many barrels?

Asynchronous logic assumed

Parameter Space

Mauro Villa

Gangling/Occupancy/Simulations

Several unknowns: exact background rate; hit multiplicities

Trigger

As presented in Elba

frequency: 150 kHz (1.5 S.F)

jitter: 100 ns (the goal is to go down to 30 ns)

latency: 10 us (1.7 SF; LVL1 design is 6 us)

DAQ window: 100ns + 2 Time stamps

or 300 ns

Time stamping: 33 MHz (T(BCO)=30 ns)

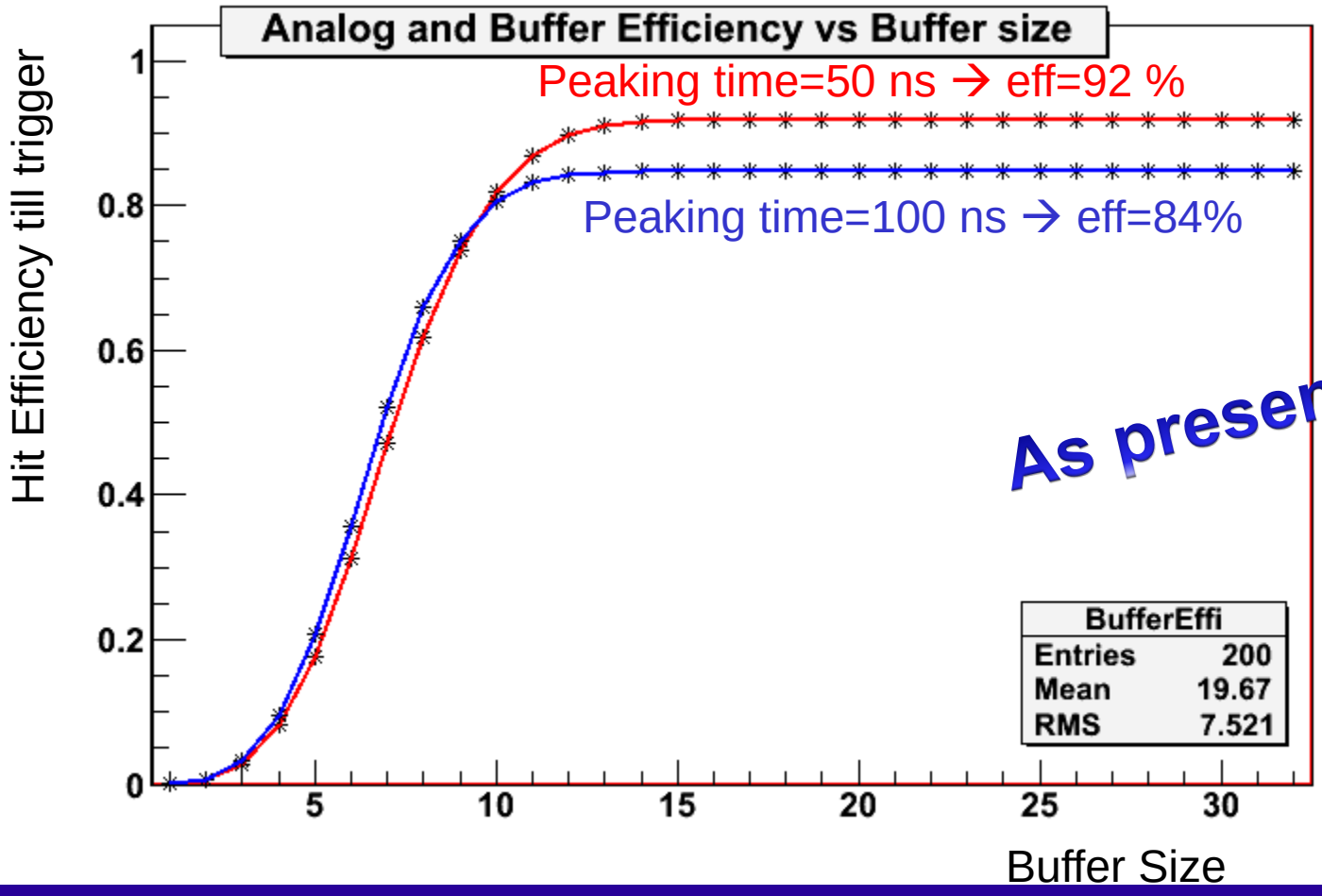
Chip readout clock: 66 MHz (T(RDclk)=15 ns)

L1 simulation: 687 kHz/strip

Mauro Villa

Analog efficiency and limited buffer lenghts

Single strip simulation



As presented in Elba

Efficiencies vs rate and dead times

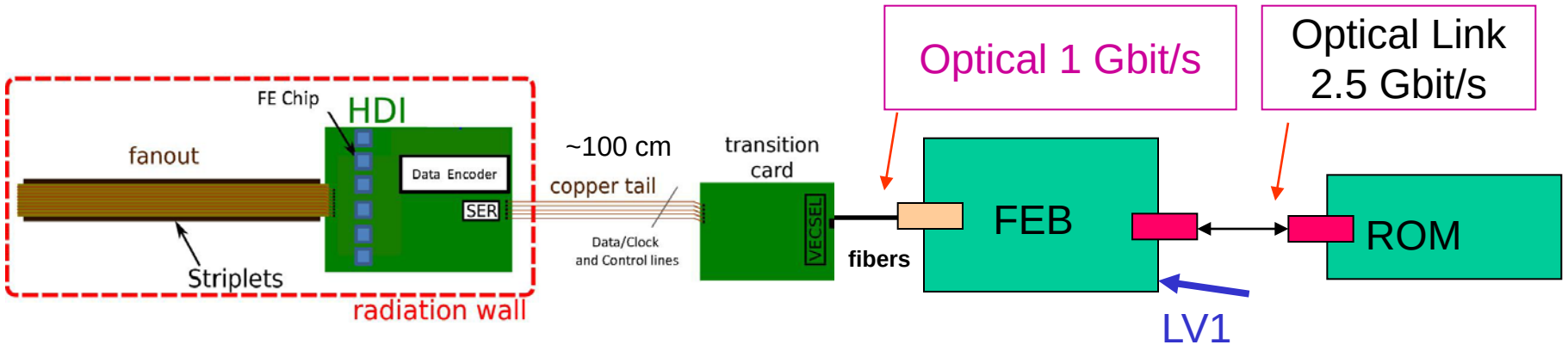
Layer	C_D [pF]	t_p [ns]	ENC from R_S [e rms]	ENC [e rms]	Hit rate/strip [kHz]	MMC Efficiency
0	11.2	25	220	680	2060	(0.732)
1	26.7	50	650	1190	687	**0.917**
		100	460	930		**0.841**
2	31.2	50	830	1400	422	**0.948**
3	45.8	50	1480	2130	325	**0.960**
4	52.6	1000	340	820	47	**0.893**
5	67.5	1000	500	1010	28	**0.934**

Conditions: 20 buffers, 150 kHz trigger rate, 300 ns time window for all layers.

DAQ reading chain for L0-L5

DAQ chain independent on the chosen FE options

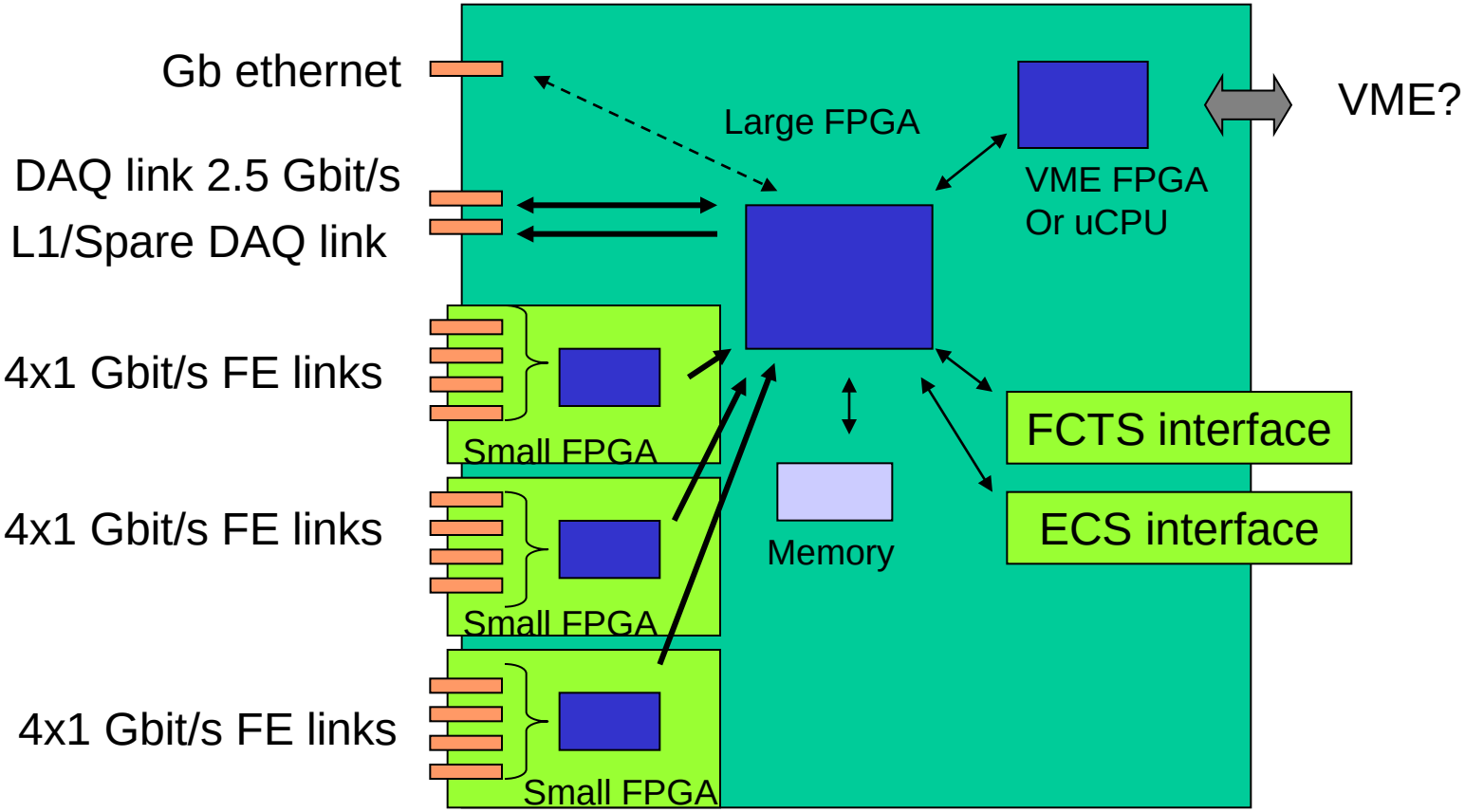
HDI +Transition card+FEB+ROM



HDI prototyping will start in October → Z properties mostly
Encoder IC Specs linked to FE chip finalization → End of year
Rad-hard serializer choice → Still LOC1, ongoing
Copper tail: lenght vs data transfer →tests are progressing

FEB + ROM → Work focused on the optical-link mezzanine

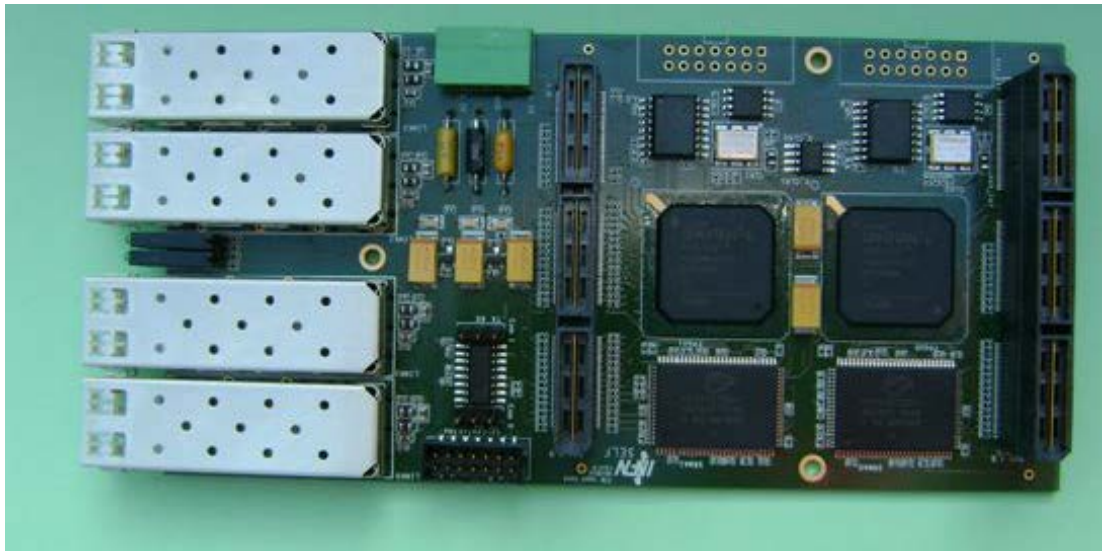
SuperB-FEB Board schematics



FCTS, ECS protocols to be decided experiment-wide
Large FPGA for data shipping and monitoring
VME FPGA or uCPU might be included in the large FPGA.

Optical link mezzanine card for EDRO

Developed as a part of ATLAS/FTK project



4 optical links at 1 Gbit/s; FPGA Xilinx, 40/100 MHz clk (programmable)

First prototype under tests.

Usable as link test mezzanine in SuperB (fall 2011)

Conclusions

First core of a Mini Monte Carlo for the Strip readout chip is available, containing

- Hit and trigger generation
- Analog inefficiency, buffers and barrels
- Several improvements can be foreseen: input hit multiplicities and correlations, etc

Mauro Villa

Good indications that for L1 the pixel readout architecture can be reused fruifully

Two parameters were found to be (very) critical:

- T(BCO) vs T(RD)
- Analog dead time

Analysis on other layers foreseen

Similar to Elba

Data chain is progressing by defining all the elements of the chain ....