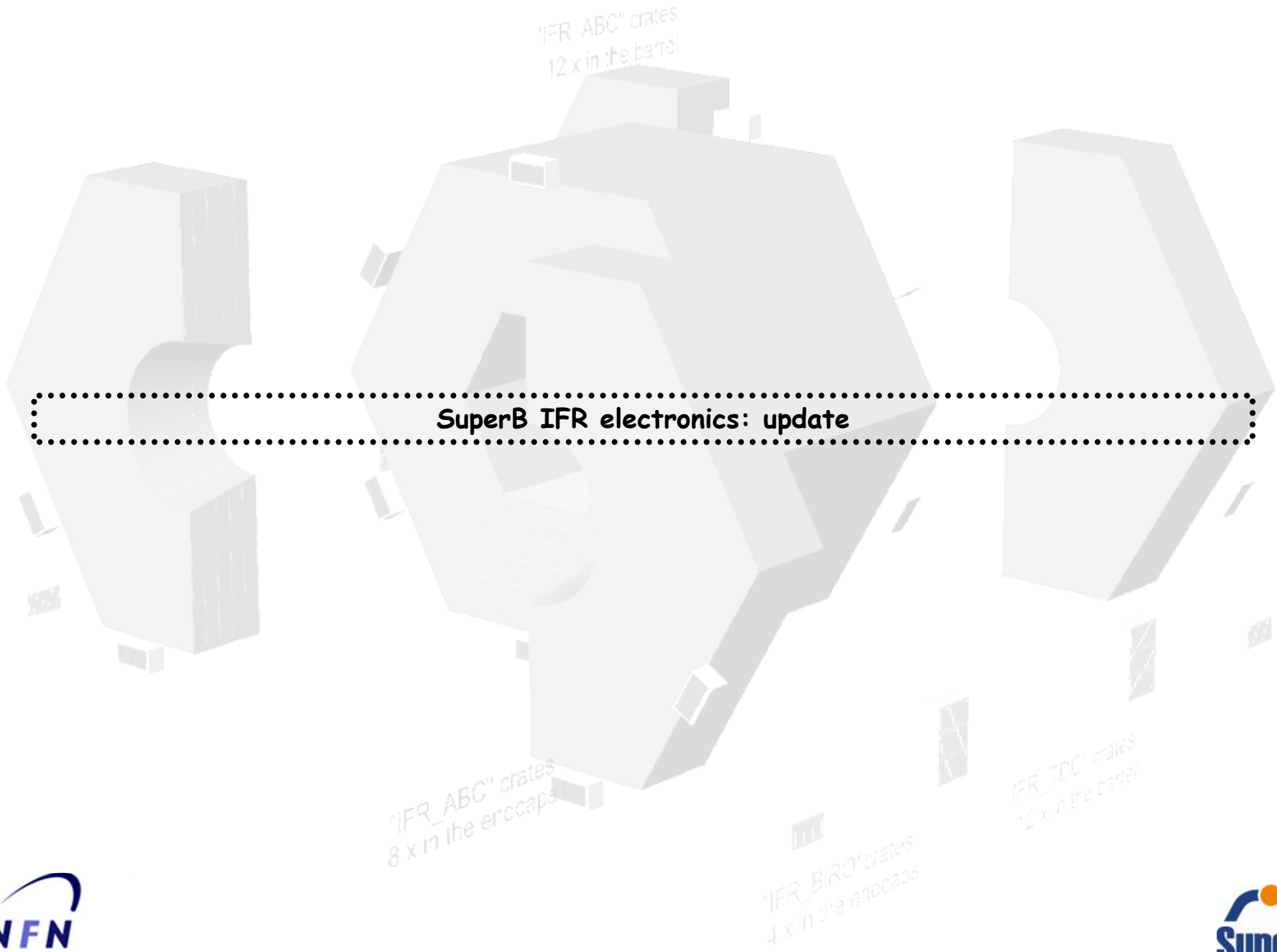


SuperB IFR electronics: update

SuperB IFR electronics: update

summary:

- recalling features of the baseline design

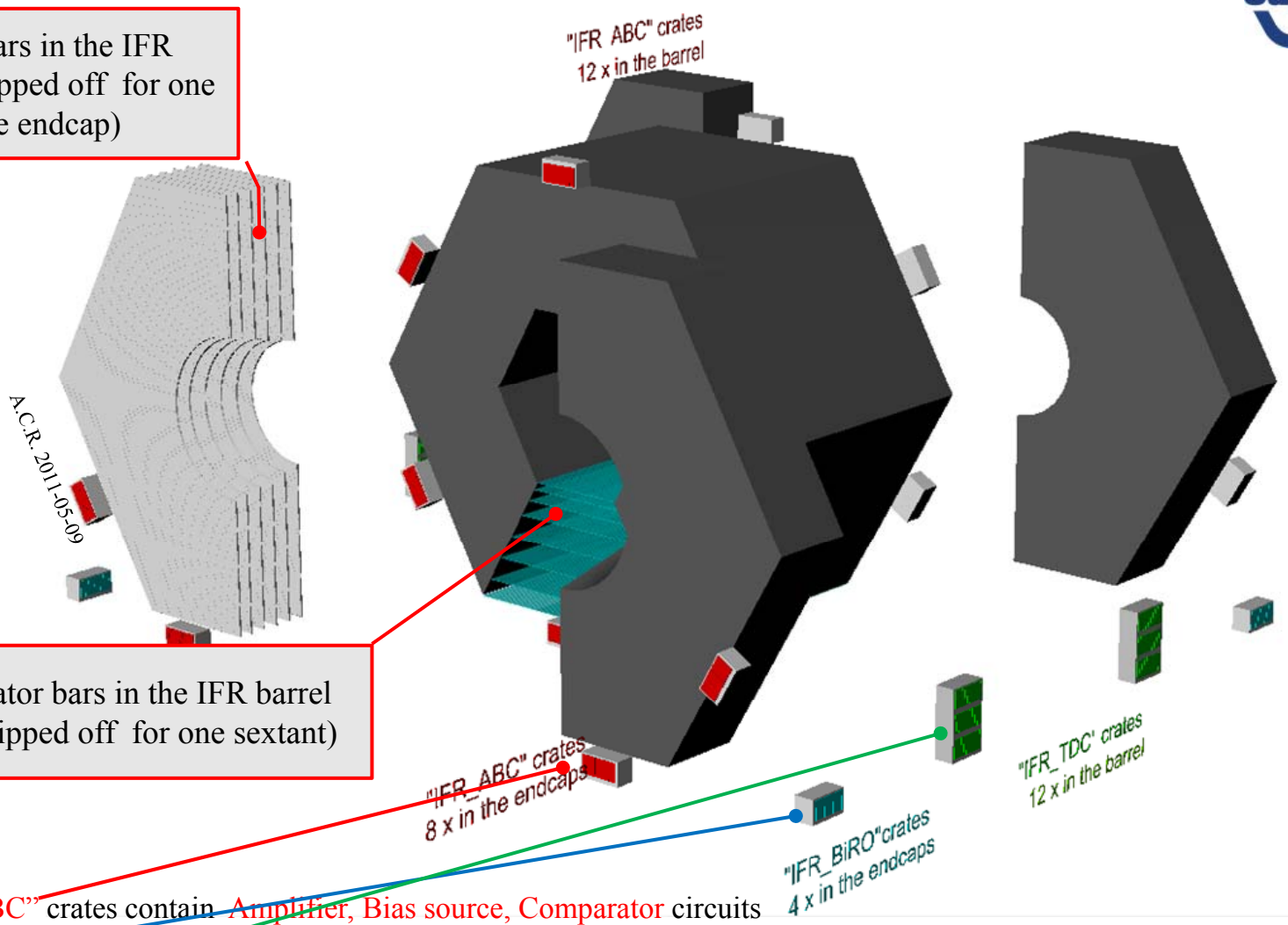
- evolving from the baseline design: exploring an all "binary mode" ("BiRO") readout for the IFR

- update:
  - SiPM test in Krakow (W. Kucewicz, Jerzy Barszcz, Mateusz Baszczyk, Piotr Dorosz, Sebastian Glab)
  - IFR prototype beam test at Fermilab in July/August
  - developing a compact front end for "BiRO": the "EASIROC" ASIC (by Omega at LAL, Orsay)
  - developing a compact front end for "BiRO": testing FPGAs and design techniques for radiation mitigation

- next milestones:
  - planning irradiation test to get an estimate of the failure rates of a prototype "compact" front end card

SuperB IFR electronics: recalling features of the baseline design

Scintillator bars in the IFR endcap (iron stripped off for one half of the endcap)



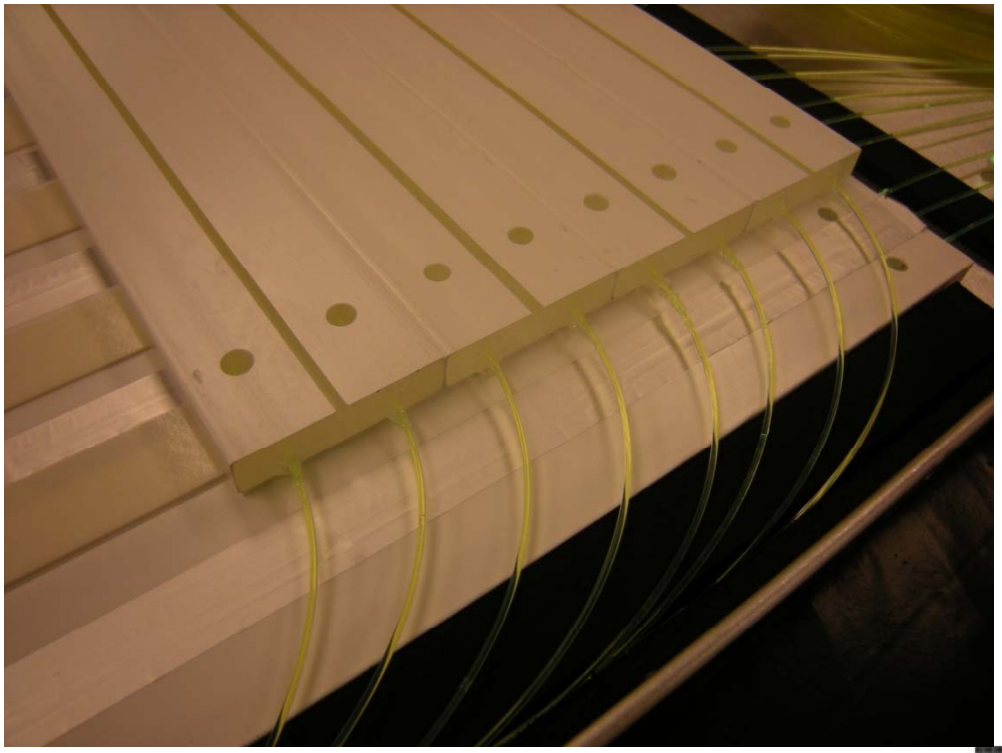
Scintillator bars in the IFR barrel (iron stripped off for one sextant)

Legenda:

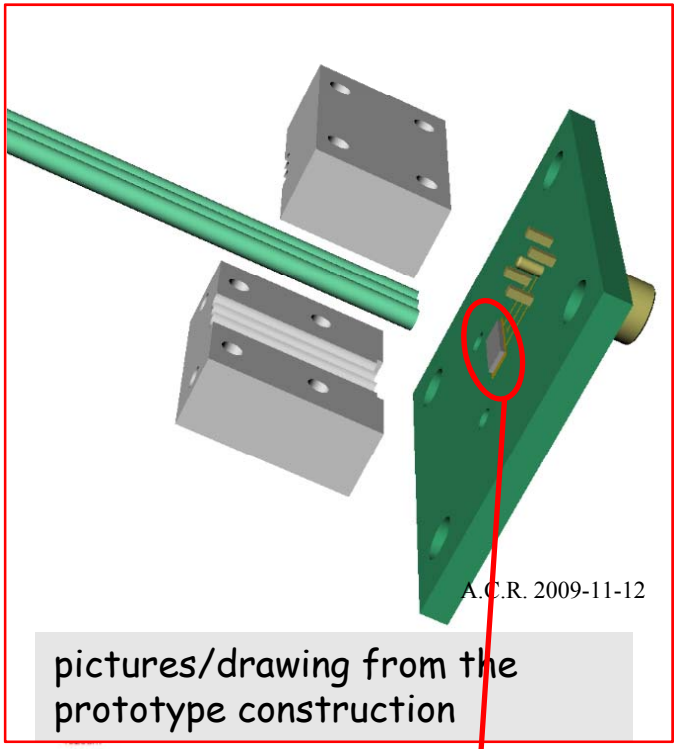
- "IFR_ABC" crates contain Amplifier, Bias source, Comparator circuits
- "IFR_BiRO" crates contain sampling circuits and buffer memories to Read Out the IFR_ABC cards in Binary mode
- "IFR_TDC" crates contain TDC circuits and buffer memories to readout the IFR_ABC cards in timing mode

In the baseline design the splitting of functions was meant to allow the digitizers (TDC ASICs mainly) and latency buffers to be positioned as far as possible away from the high radiation region of the detector and surroundings.

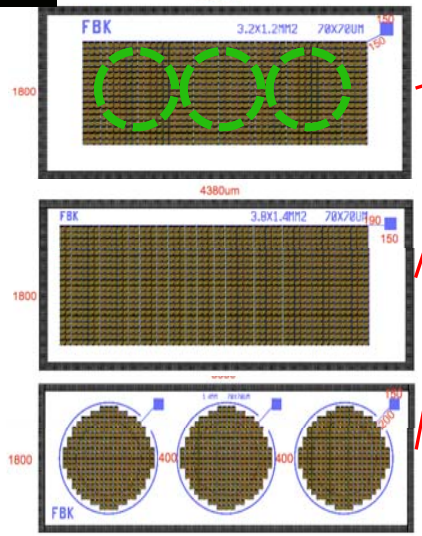
SuperB IFR electronics: recalling features of the baseline design



SuperB IFR : the scintillating bars are equipped with wavelength shifting fibers (3 for each bar in the prototype), which are then coupled to a SiPM device by means of precisely machined plastic supports.



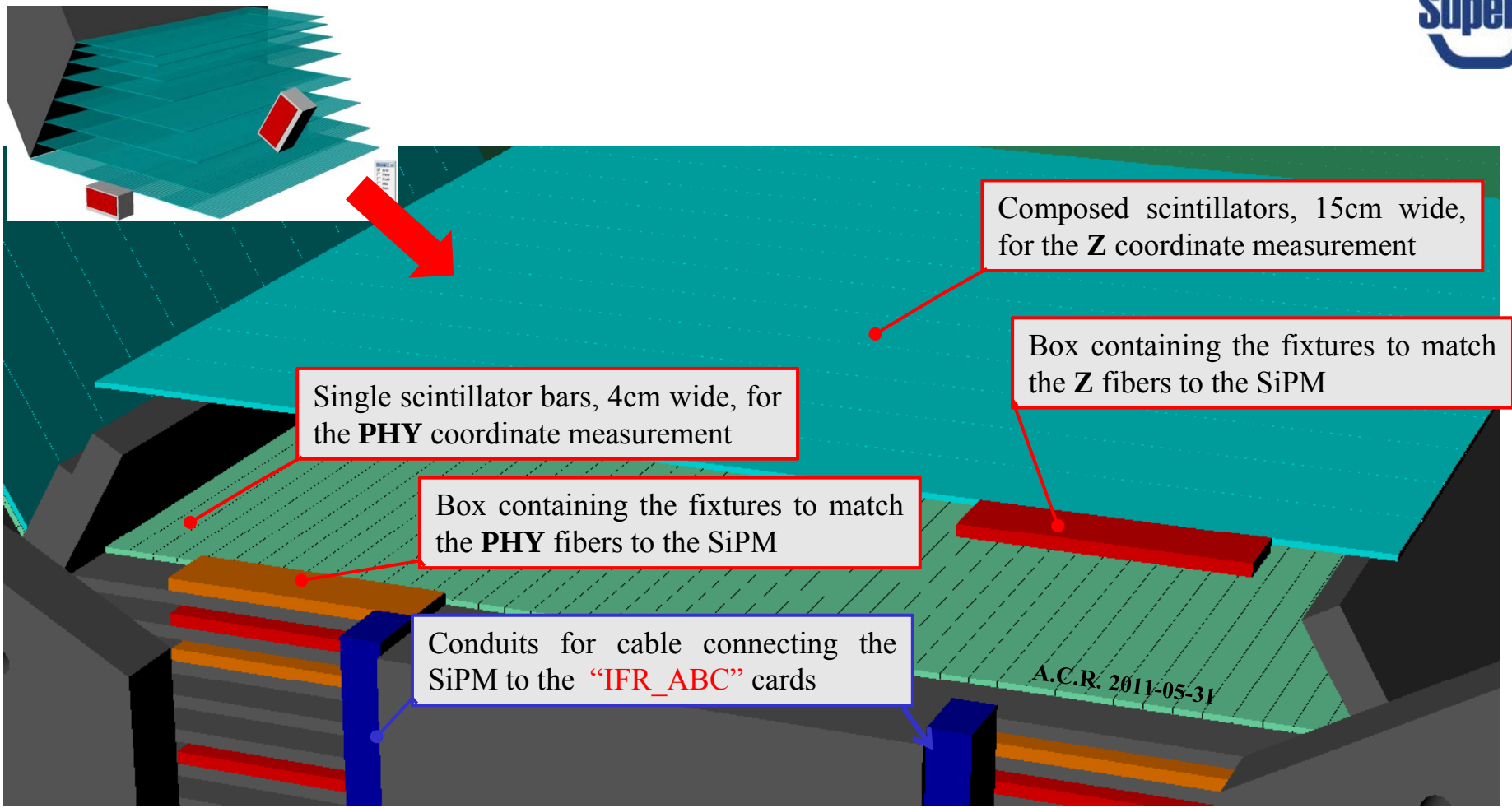
pictures/drawing from the prototype construction



SiPM by FBK, Trento. 70x70um² cell size, n-on-p.

Bonding of the SiPM to the carrier PCB was performed at INFN Perugia thanks to G. Ambrosi, M. Ionica

SuperB IFR electronics: exploring an all "binary mode" ("BiRO") readout for the IFR

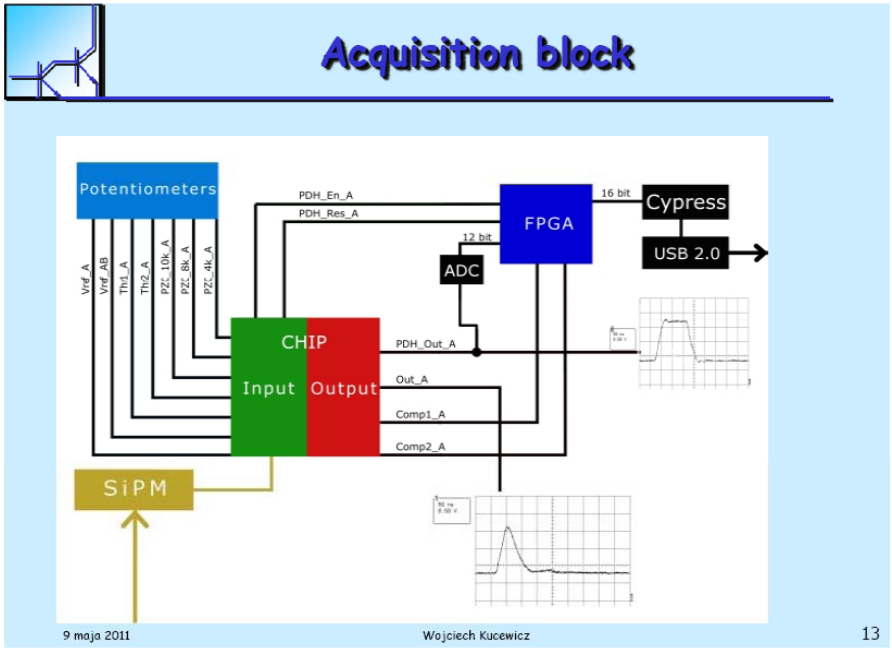


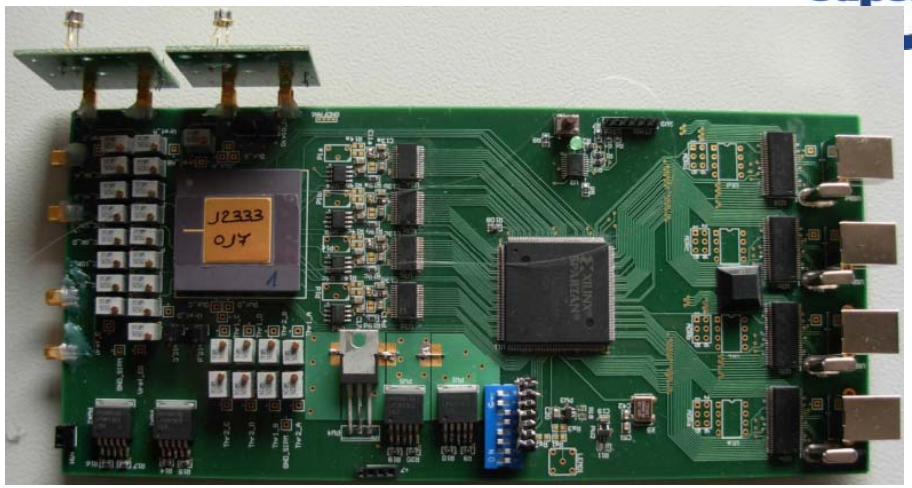
Note: the Z and the PHY layers have been separated in this picture to show them distinct

The actual implementation of the X-Y detector planes is being defined; they will result from the **union of smaller X-Y modules, whose design is underway.**

The number of electronics channels needed to read the barrel might need some adjustment.

SuperB IFR electronics: SiPM test in Krakow





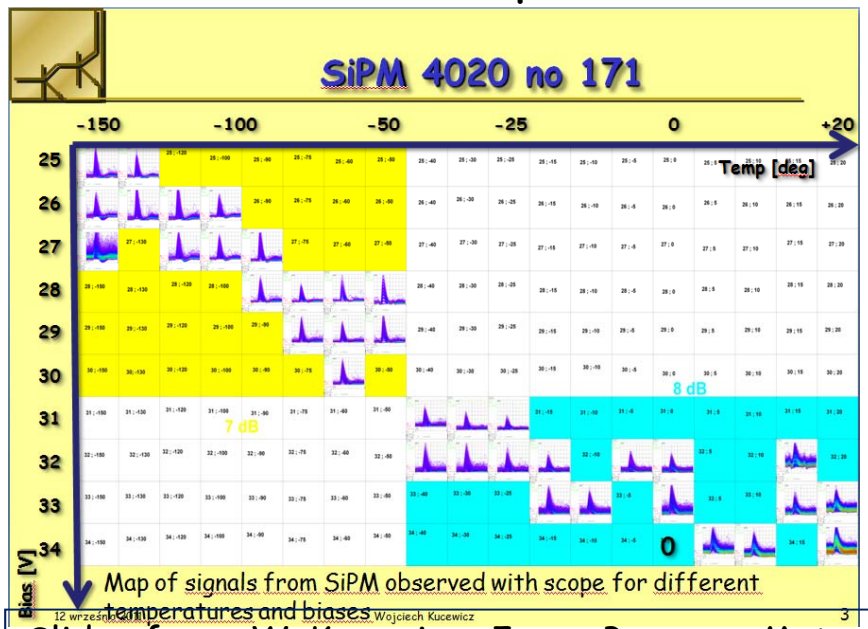
From:
"**Silicon Photomultiplier Activity at AGH-University of Science and Technology**",
W. Kucewicz, J. Barszcz, S. Głąb, M. Sapor.

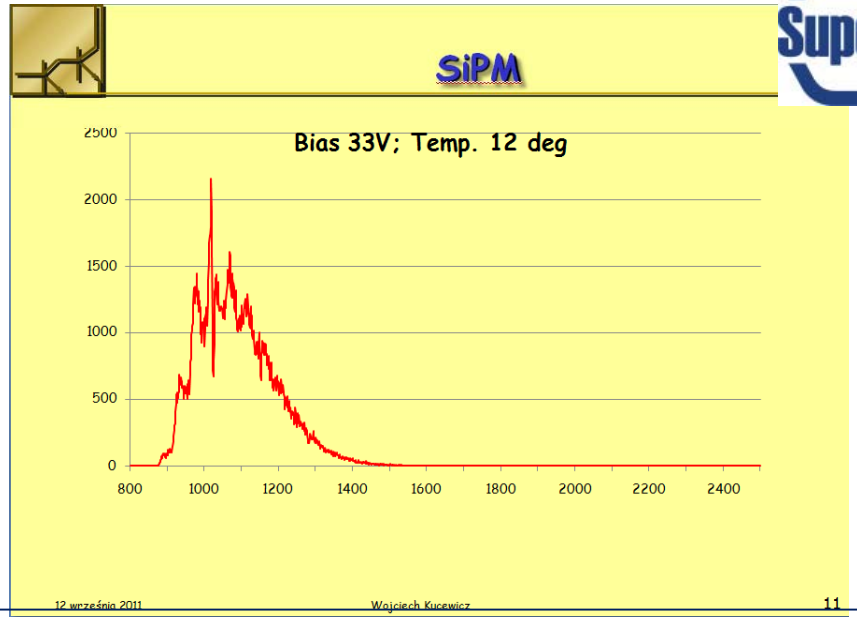
Prof. Kucewicz and his team (Jerzy Barszcz, Mateusz Baszczyk, Piotr Dorosz, Sebastian Glab) have characterized our SiPMs (FBK model 4020) with their test board for ASIC#2.

The preliminary results have been presented at IFR session of this collaboration meeting.

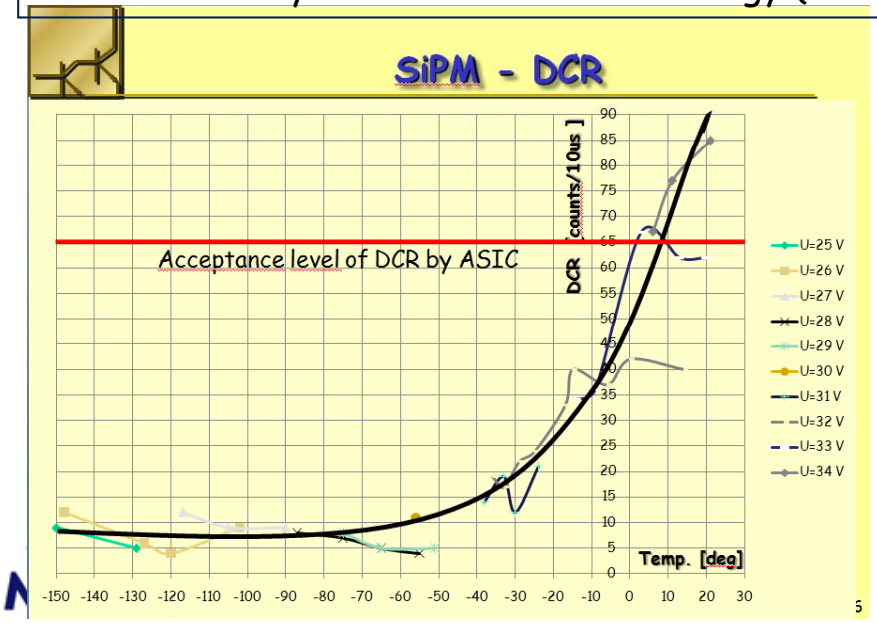
SiPM characterization for the IFR detector is a major task and this work already shows that it is in good hands !

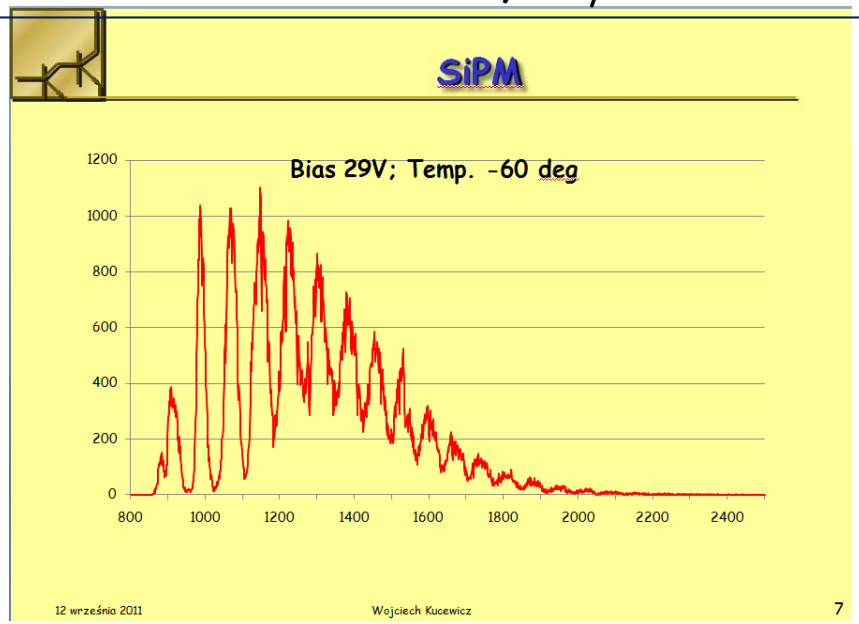
SuperB IFR electronics: SiPM test in Krakow





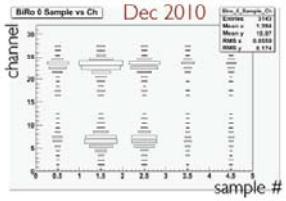
Slides from: W. Kucewicz, Jerzy Barszcz, Mateusz Baszczyk, Piotr Dorosz, Sebastian Glab
AGH University of Science and Technology (AGH), Krakow: "SiPM from Ferrara", July 2011





At the IFR sessions of this meeting a report on the recent test beam at Fermilab have been presented. See: "**Beam Test**: G. Cibinetto on behalf of the beam test and analysis team"

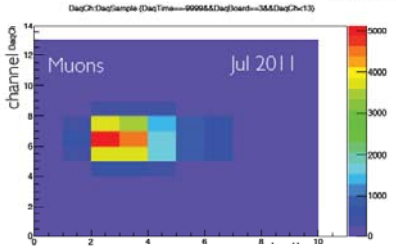
Increasing of the number of samples

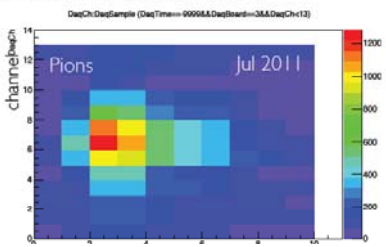


That's a feature of the Binary Readout that could be very helpful for the muon ID.

The number of samples has been doubled since the December test, allowing the possibility to detect the slowest part of the hadronic shower.

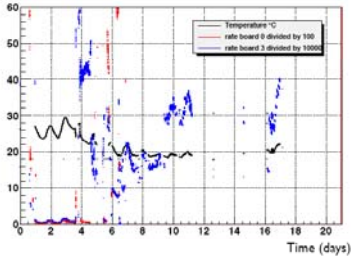
Results are not always easy to understand.

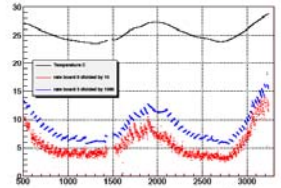


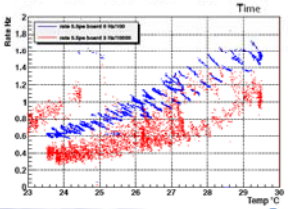


London, Sep 15 201

Temperature monitoring and Vbias correction







Automatic correction of the Vbias to follow the temperature changes, in order to keep the SiPM gain constant over the time.

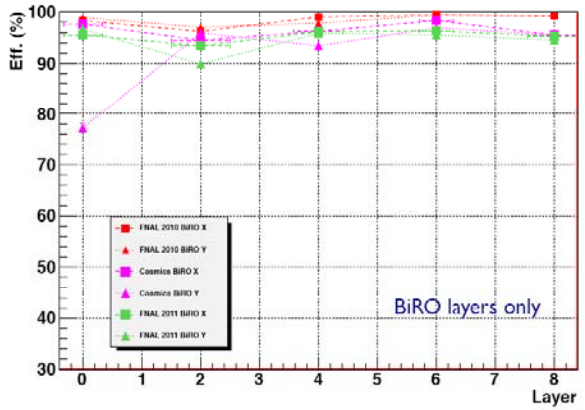
London, Sep 15 2011 G. Cibinetto 8

A few features of the front end / DAQ modules have been upgraded to enlarge the sampling window around the trigger (it seems to help identification).

Most improvements were on the side of the Detector Control System, such as an automated regulation of the bias against temperature changes.

Preliminary results confirm the basic performances shown in the December 2010 test.

Efficiency measurement



Raw (sandwich) detection efficiency calculated using muon events.

Performances are confirm previous results.

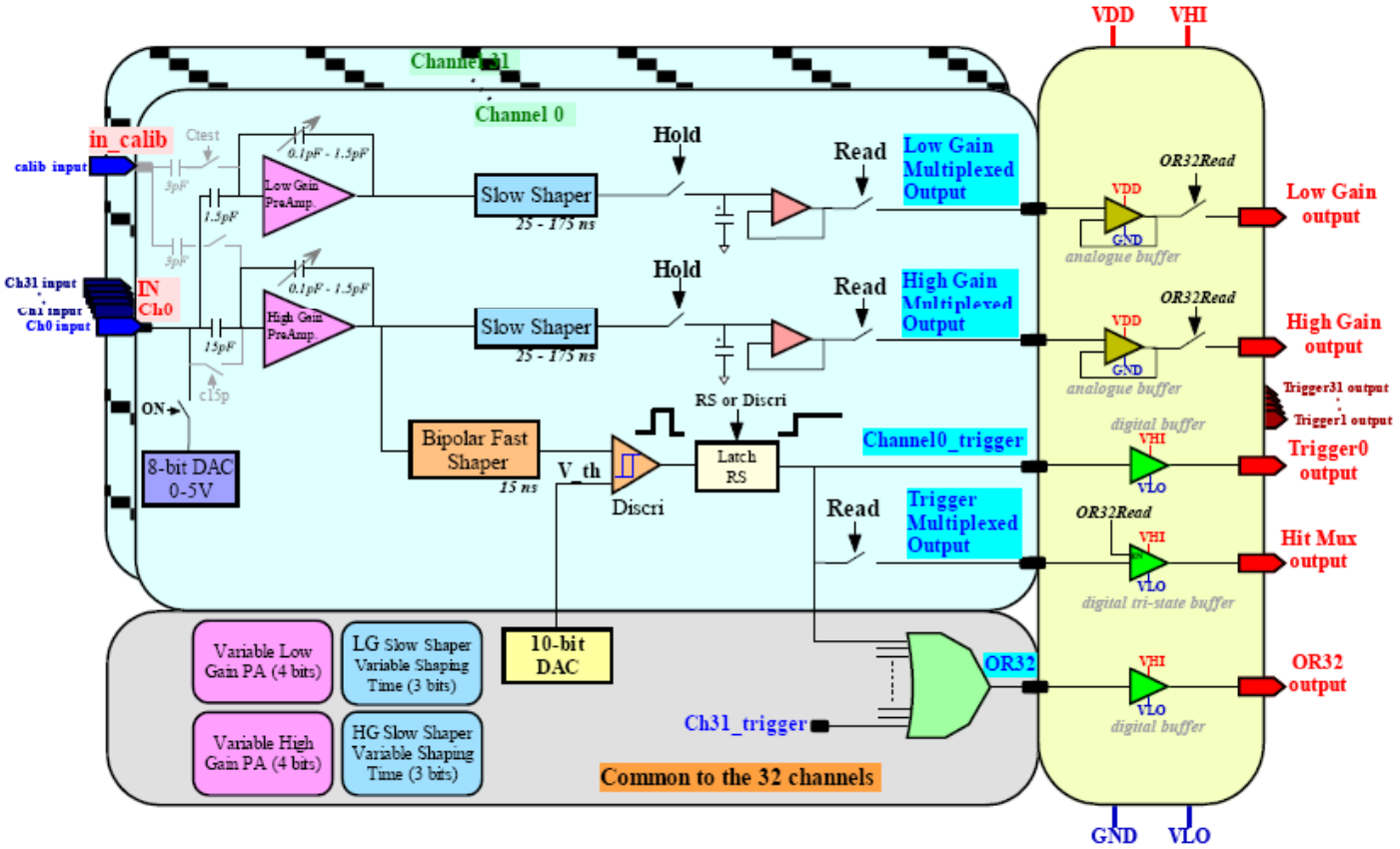
Efficiency for Time readout modules (not shown) are also in agreement with previous results.

More precise efficiency evaluation (done fitting the tracks) is under way: see Jarek talk for more details.

London, Sep 15 2011 G. Cibinetto 23

SuperB IFR electronics : developing a compact front end for "BiRO": the "EASIROC" ASIC

The "EASIROC" by the OMEGA group of LAL in Orsay is being considered as a candidate ASIC suitable for the front end stage of a "binary mode" readout of the IFR detector



It has an individual trigger output for each of 32 channels plus 32 individual bias setting DACs and a common threshold setting DAC.

The EASIROC was not designed to operate in a high radiation area, BUT the OMEGA group is working at a newer version featuring improved radiation tolerance

USER GUIDE Omega

EASIROC

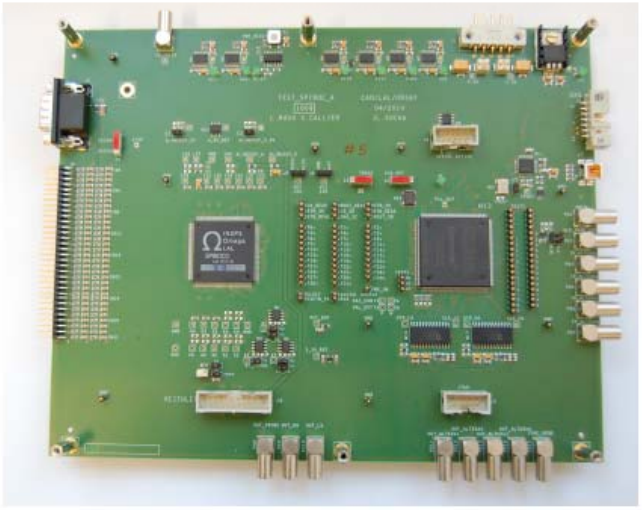
SOFTWARE & TEST BOARD USER GUIDE

Version: 11 April 2011

Abstract

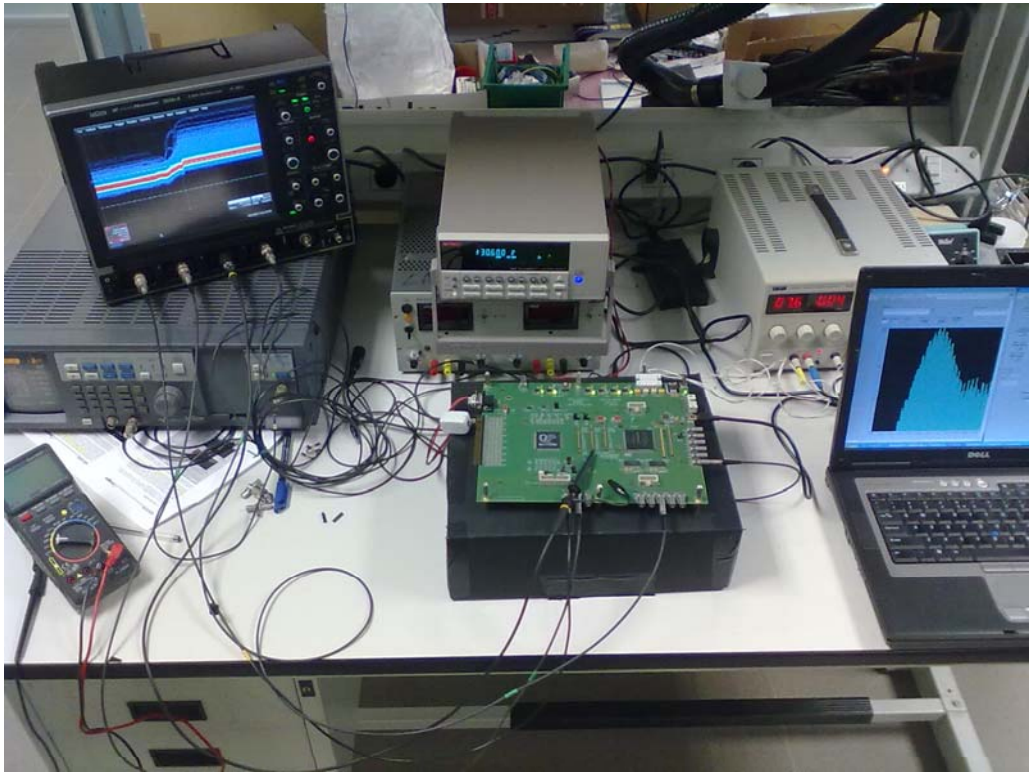
EASIROC (previously SPIROC0), standing for *Extended Analogue Silicon pm Integrated Read Out Chip*, is a 32-channel fully-analogue front end ASIC dedicated to the gain trimming and read-out of SiPM detectors.

This guide explains how to install & use the test board for EASIROC and how to operate with the associated software.



Orsay MicroElectronics Group Associated

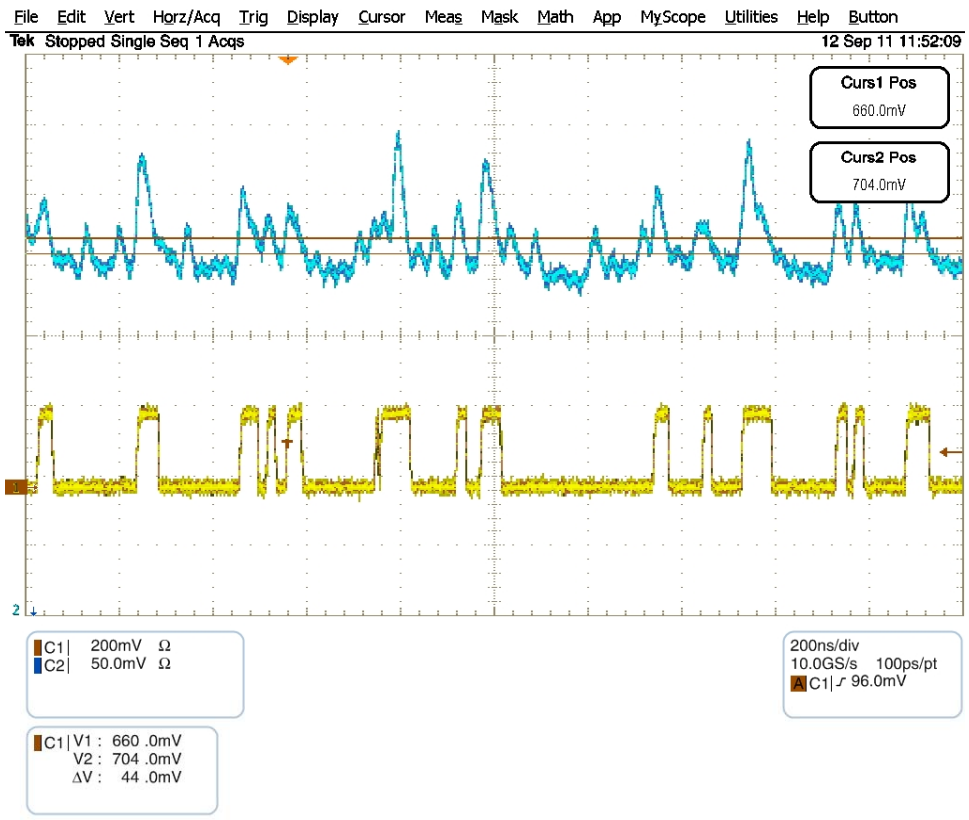
The IFR-Ferrara group has been in touch with Gisèle MARTIN-CHASSARD and Stephane CALLIER of OMEGA who have shown interest in the project and provided us not only plenty of information and support but also a complete hardware and software test system.



SO:
The plan is now to apply an "EASIROC" to a "pizza box" detector prototype and to perform cosmic ray tests to determine the overall efficiency.

Some preliminary test are being carried out to determine the proper operating parameters (bias and threshold) for our FBK SiPMs applied to the EASIROC (acknowledgements to Roberto Malaguti, INFN-Ferrara)

For this test a SiPM #5 of the 4380 type from FBK was connected to channel 4 of the ASIC.
A fiber illuminated by a blue LED was connected to the SiPM. The SiPM support had to be modified to adapt to the different biasing scheme imposed by the ASIC.

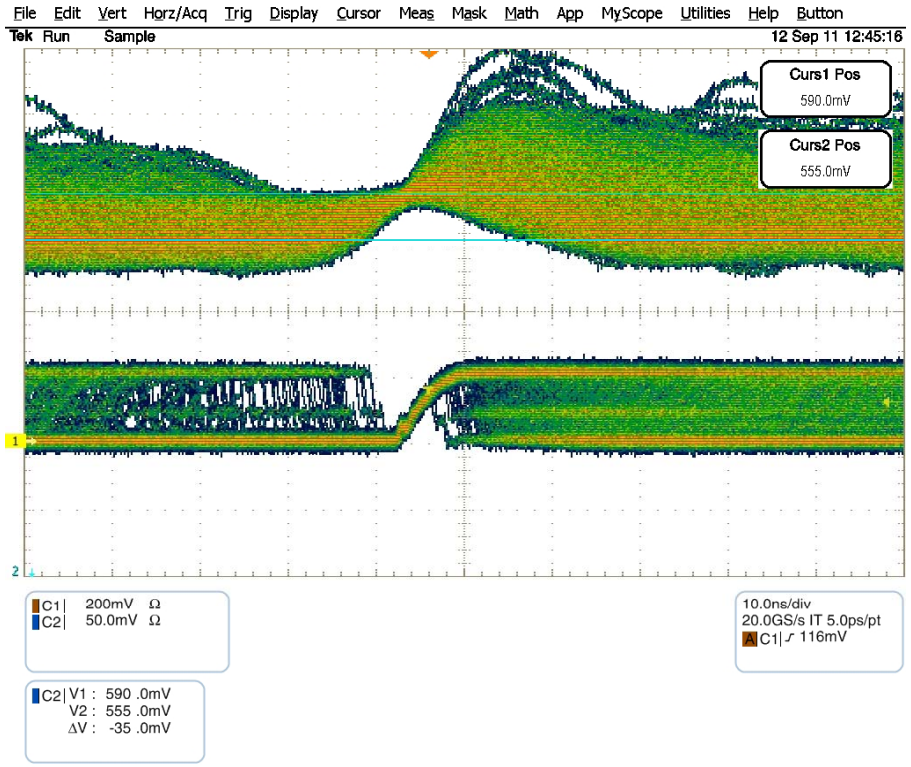


For this test SiPM #5 of the 4380 type from FBK was connected to channel 4 of the ASIC.

The SiPM was biased @ 32.3V and the LED pulser was OFF → what is shown in the waveform is a sample of dark counts

The waveforms reported here represent:
-blue trace: the output of channel 4's internal 15ns fast shaper. This internal signal is observed at the "probe" output of the EASIROC test board (attenuated a factor of 2)
- yellow trace: the output of channel 4 "trigger" comparator

The dark count rate at room temperature is about 12.5MHz if one looks at the blue "spikes" a little less at the "trigger" output with DAC threshold setting of 904 (≈ little above 1 p.e.)



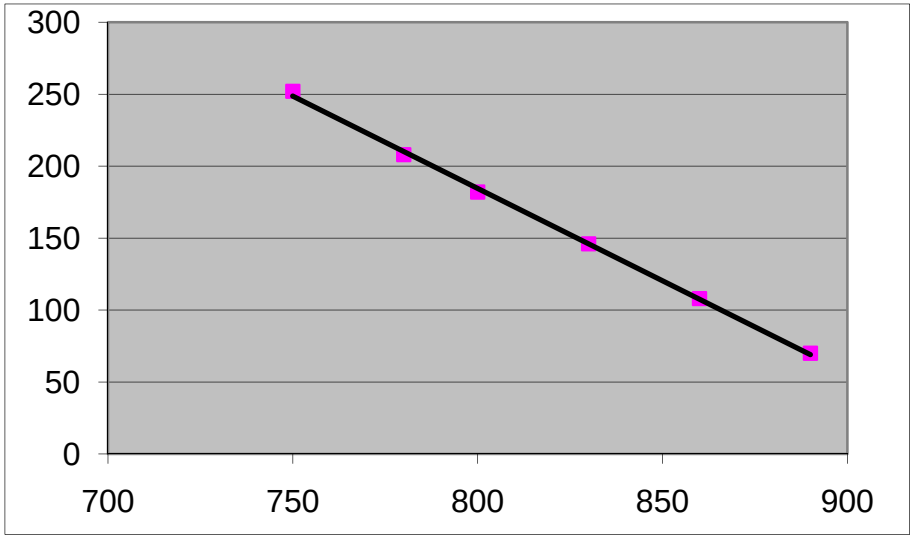
For this test SiPM #5 of the 4380 type from FBK was connected to channel 4 of the ASIC.

The SiPM was biased @ 32.3V and the LED pulser was ON → what is shown are accumulated samples of dark counts + stimulated response

The accumulated waveforms reported here represent:
- top trace: the output of channel 4's internal 15ns fast shaper. This internal signal is observed at the "probe" output of the EASIROC test board (attenuated a factor of 2)
- bottom trace: channel 4 's "trigger" output

We estimated that the output of the internal fast shaper has a sensitivity of about 36 mV per p.e.

The test allowed us to calibrate the threshold DAC setting in terms of p.e. (about 30 counts per p.e.).



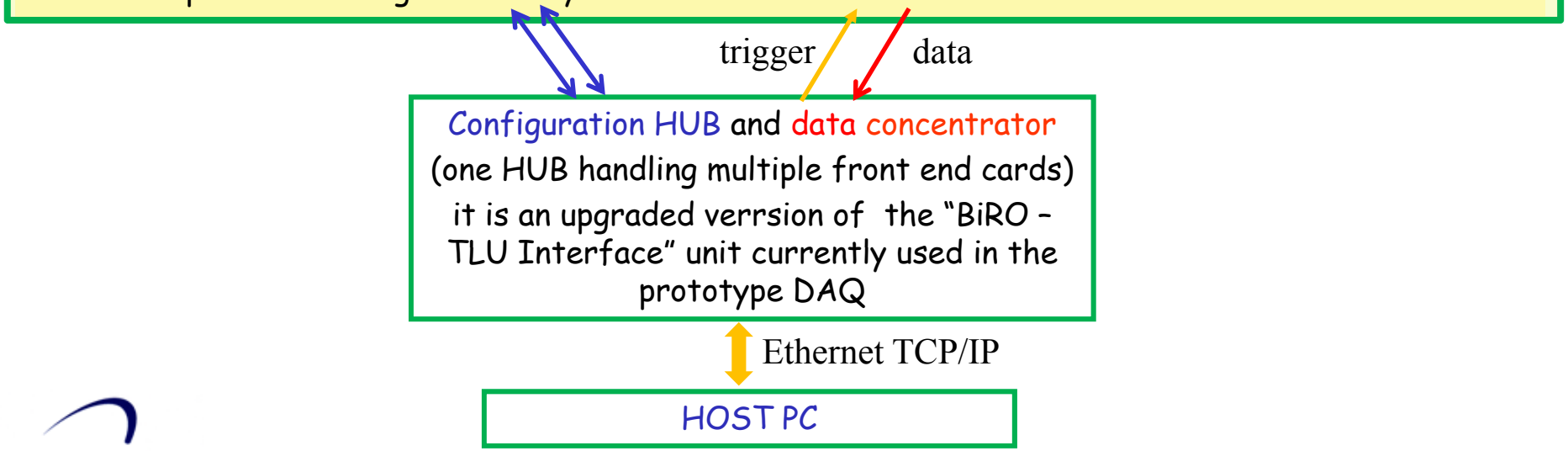
SuperB IFR electronics : developing a compact front end for "BiRO": the "EASIROC" ASIC

SO:
The plan is now to apply an "EASIROC" to a "pizza box" detector prototype and to perform cosmic ray tests to determine the overall efficiency.

Next steps:

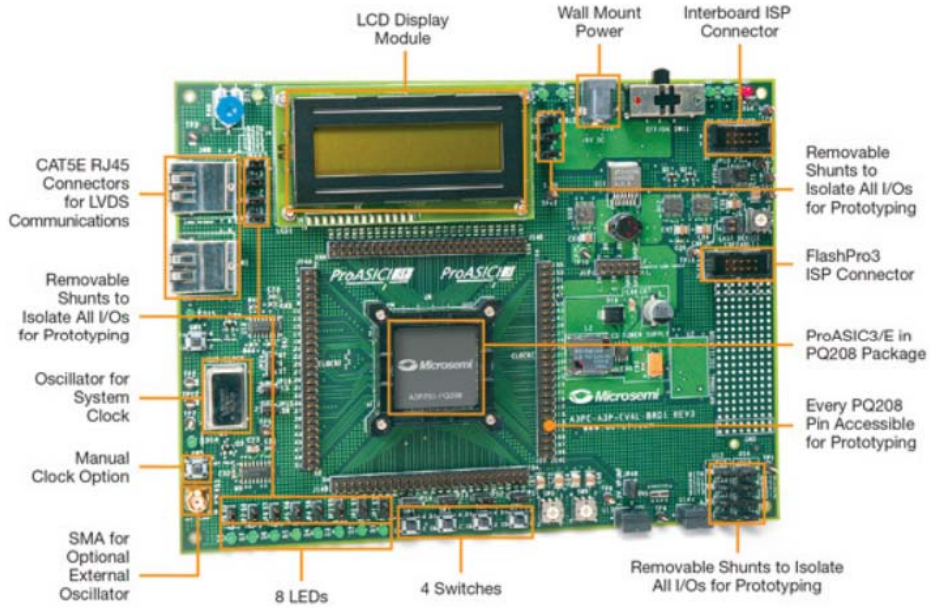
• to evaluate at the same time the performance of the EASIROC ASIC coupled to the prototype IFR detector and the radiation tolerance of the assembly, we will design a board (which would also be used for radiation tolerance test) hosting:

- one EASIROC
- EASIROC power supply with latchup detection / protection
- flash based FPGA for EASIROC configuration & data processing; the FPGA would be connected by LVDS links to the HUB, capable of handling multiple front end cards. We plan to use the Precision Hi-Rel synthesizer by Mentor which includes "automatically" Hamming coding and TRM to improve the design reliability

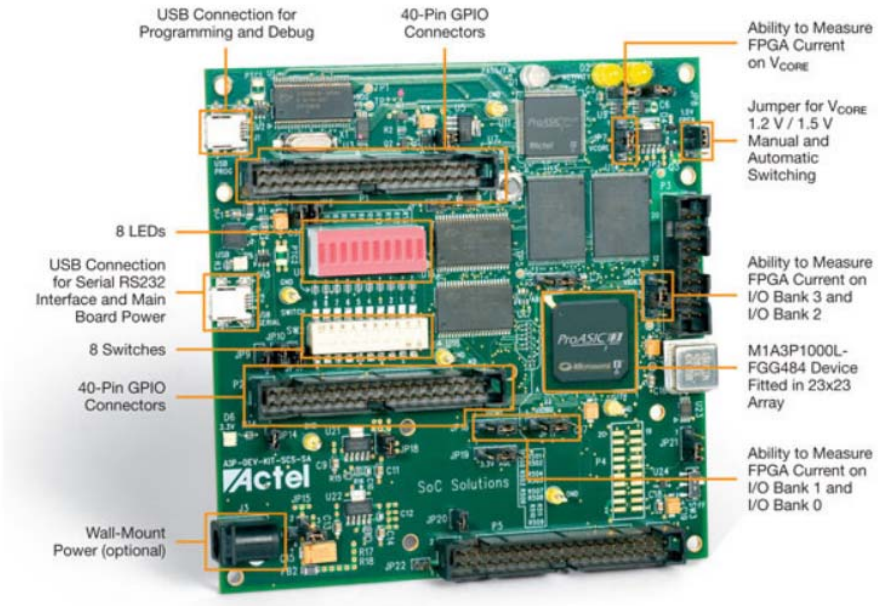


SuperB IFR electronics : testing FPGAs and design techniques for radiation mitigation

We have procured two development cards based on different ACTEL ProASIC devices:

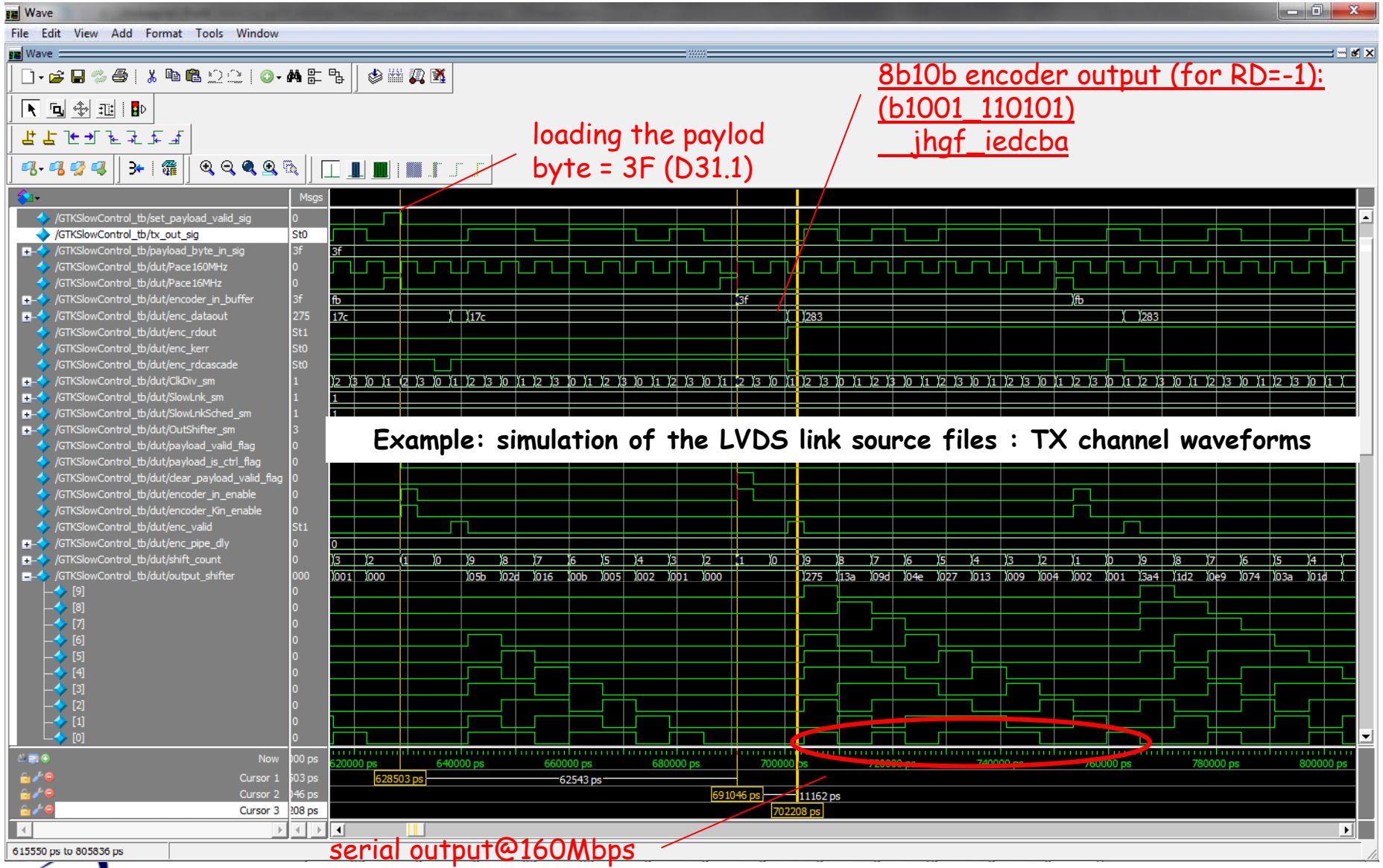


Evaluation board with an A3PE1500-PQ208 FPGA



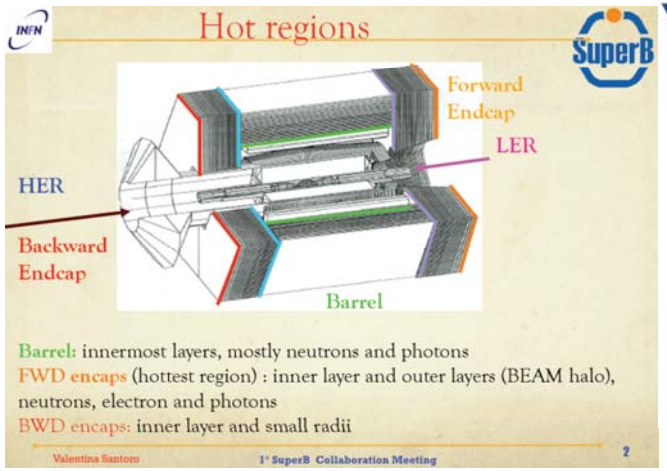
Development board with an M1A3P1000L-FGG484 device

As a first excercise we are implementing:
- the EASIROC configurator unit and its local storage controller, interfaced to the HUB via a high speed link exploiting the LVDS ports of the proASIC 3 devices (undergraduate thesis work assigned)
- we are planning to encode the serial stream will be 8b/10b encoded to achieve a DC balanced signal that could be sent through a fiber link and to have some inherent protection against error induced by noise or single events


Wave
File Edit View Add Format Tools Window
loading the paylod
byte = 3F (D31.1)
8b10b encoder output (for RD=-1):
(b1001_110101)
jhgf_iedcba
Example: simulation of the LVDS link source files : TX channel waveforms
serial output@160Mbps

SuperB IFR electronics : planning irradiation test to get an estimate of the failure rates of a prototype "compact" front end card

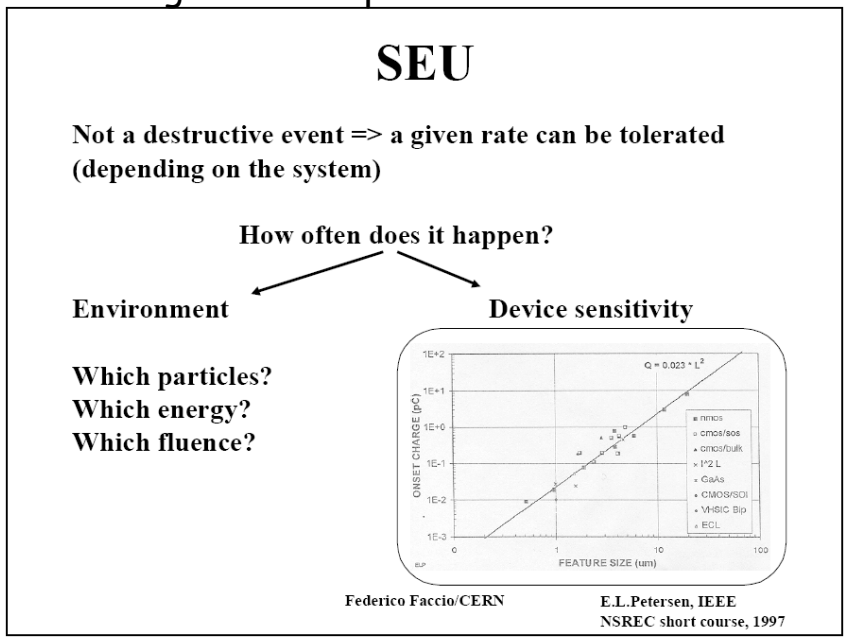
Reliable data on expected radiation sources and spectra at different locations of the IFR are now being delivered. See for reference yesterday's presentation at the IFR session: "IFR Background Status" Valentina Santoro INFN Ferrara



• while SiPM have to be studied and tested to determine cumulative effects from the Total Integrated Dose (TID)

• the front end electronics should be studied to determine the cross section of Single Event Effects (SEE) such as:

- Single Event Latchup
- Single Event Upset



Quoting "**Radiation effects in the electronics for CMS**", Federico Faccio, CERN:

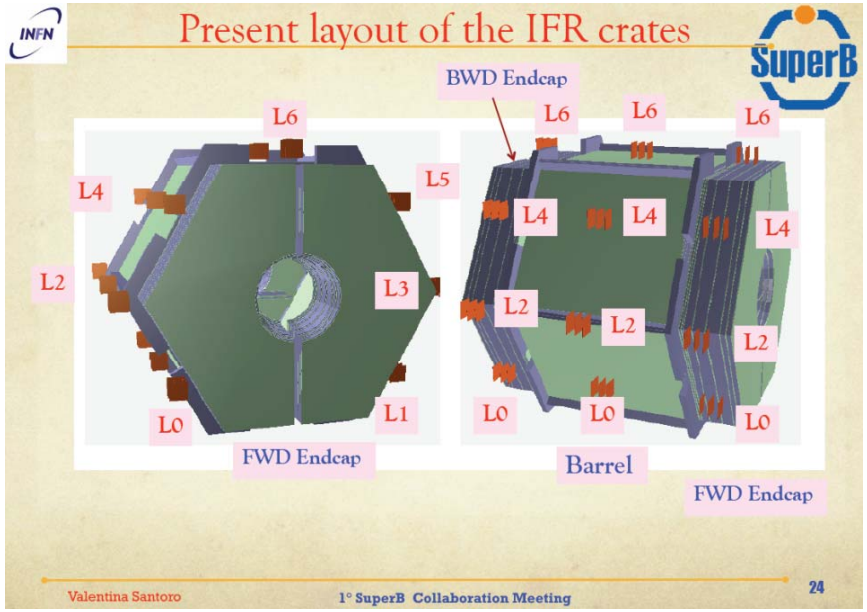
… To do so (estimate SEU rates), one needs to know:

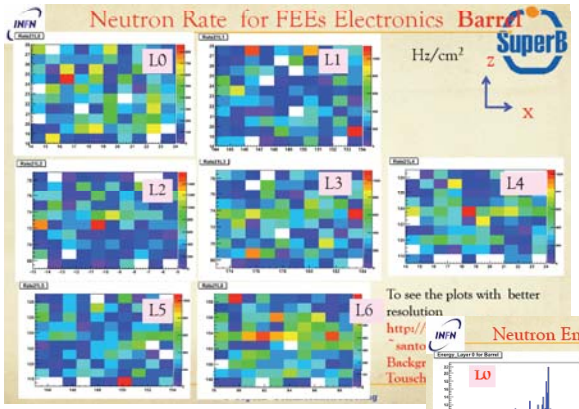
1) **The radiation environment.** Not only the kind of particles, but also their energy distribution and their fluence. For instance, it is impossible to get to an estimate of the upset rate starting from an environment description in terms of TID and equivalent 1MeV neutron fluence.

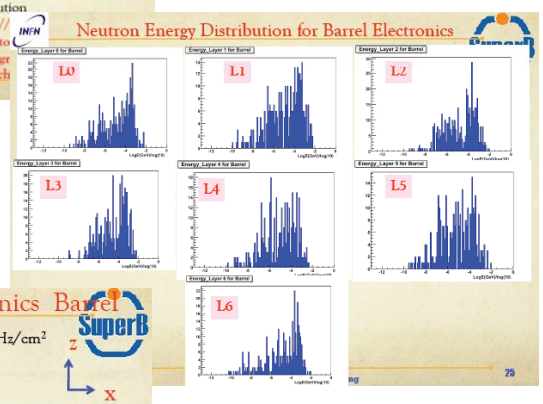
2) **The specific sensitivity of the device**. This might be argued by the technology used, but in general there is such a variability that **one needs to test the device to really know**. In that case, it is important to well target the irradiation source used in the test. **This source has to be representative of the real environment** (for example, using 1MeV neutrons for testing when the environment is represented by neutrons with energy up to 400MeV is NOT representative and will lead to completely meaningless results).

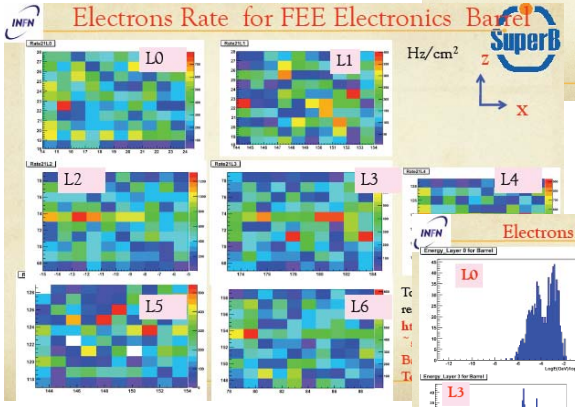
SuperB IFR electronics : planning irradiation test to get an estimate of the failure rates of a prototype "compact" front end card

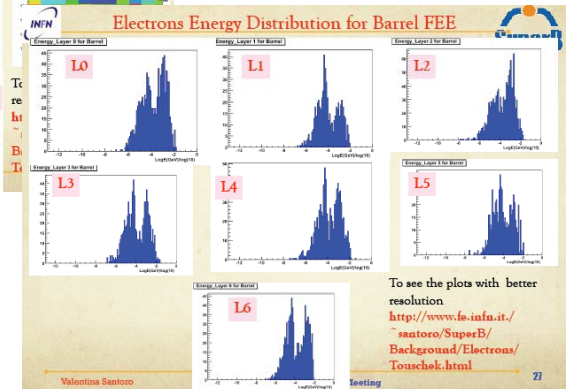
From: "IFR Background Status" Valentina Santoro INFN Ferrara











Thanks to this work we have now an estimate of the expected radiation doses at the locations of the front end electronics crates, according to the baseline design.

This will allow us to properly plan the irradiation tests of the "compact" front end design based on the EASIROC.