Updates on the SVT activities in Bologna

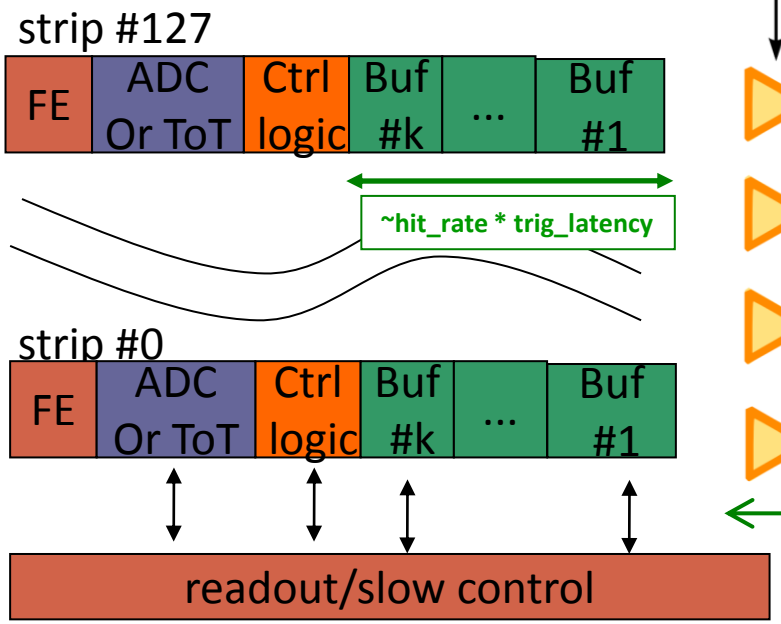
F.M. Giorgi – INFN Bologna

Summary

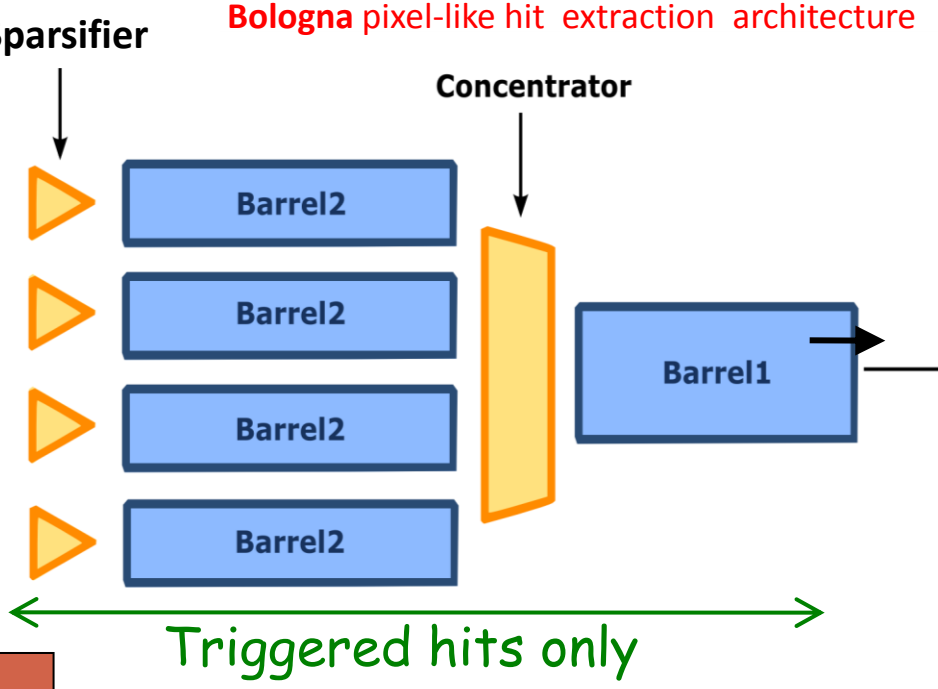
- L0 strip readout circuit upgrade
- INMAPS submission
- Test Beam Sept. 2011

Strip readout upgrade under investigation

Pre-trigger buffer array proposed by PISA
(**F.Morsani G. Rizzo**)



Bologna pixel-like hit extraction architecture



Asynchronous logic assumed:

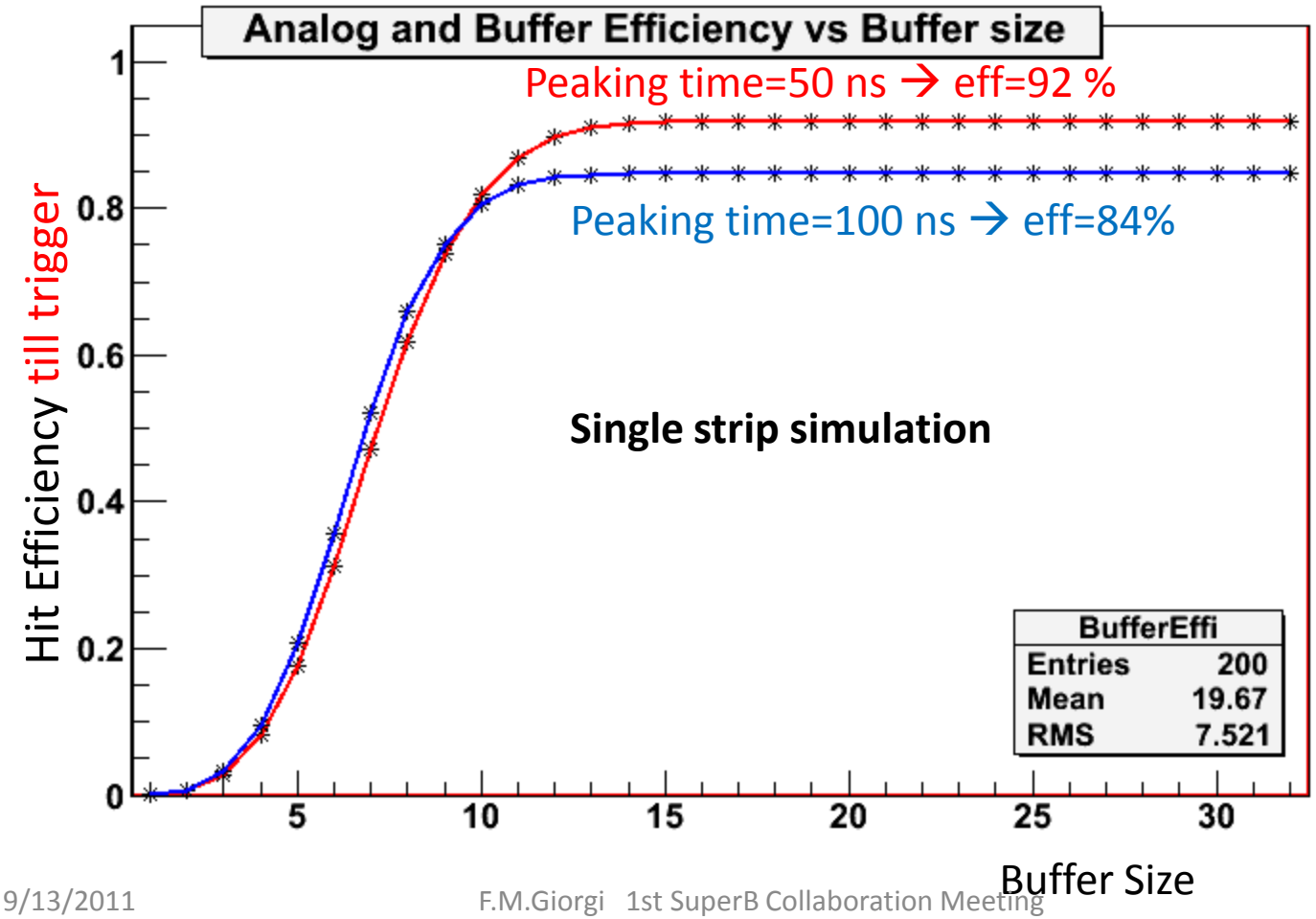
Triggered event size not known a-priori
(thus readout time also)

Efficiency Study (by M. Villa)

- Parameter Space:
  - Trigger
    - frequency: 150 kHz (1.5 Safety Factor)
    - jitter: 100 ns (the goal is to go down to 30 ns)
    - latency: 10 us (1.7 S.F.; LVL1 design is 6 us)
  - Triggered window: 100ns + 2 Time stamps .
  - Time stamping: 33 MHz (T(BCO)=30 ns)
  - Chip readout clock: 66 MHz (T(RDclk)=15 ns)
- Strip dead time equal to 2.4 peaking time
- Strip rates as given by Riccardo C. (5/13/11)
- High level simulation (C++) of MAIN features of a readout chip: Preliminary Toy Monte Carlo

L1 simulation: 687 kHz/strip

Inefficiency sources: Analog peaking time and limited buffer size.



MIP full charge release in the strip, no charge sharing → saturation efficiency underestimated.

INMAPS 32x32 Matrix Submission

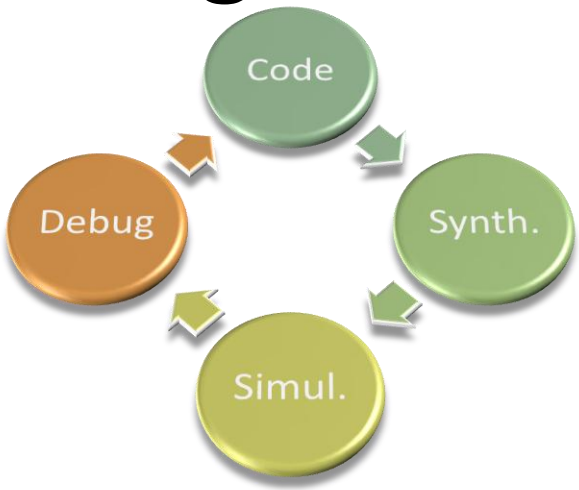
July 2011

The project

- CMOS 180 nm, 4-well process
- INMAPS pixel sensors (INFN PV-BG, ref. to **L. Ratti** presentation)
- 32x32 pixels matrix (INFN PI, F. Morsani G. Rizzo)
  - Column addressable with in-pixel TS selection
  - Parallel output
- Integrated readout, SQUARE architecture:
  - Synthesizable VHDL architecture model.
  - 2 sub-matrices control with parallel hit extraction
  - 1 column sparsification in 1 clock.
  - Cluster compression algorithm
  - Triggered and Data push working mode
  - Parallel output bus.
  - I2C-like slow control.

Readout Architecture Design Flow:

- Conceptual design
- VHDL coding
- Behavioral simulations with Montecarlo hit generator on pixel
- Extracted hits cross-checking
- VHDL Synthesis
- Post synthesis simulations
- Behav. and P.S. sim. compare
- Physical synthesis and implementation (chip layout)
- Post Layout simulations
- P.L. and P.S. sim. compare

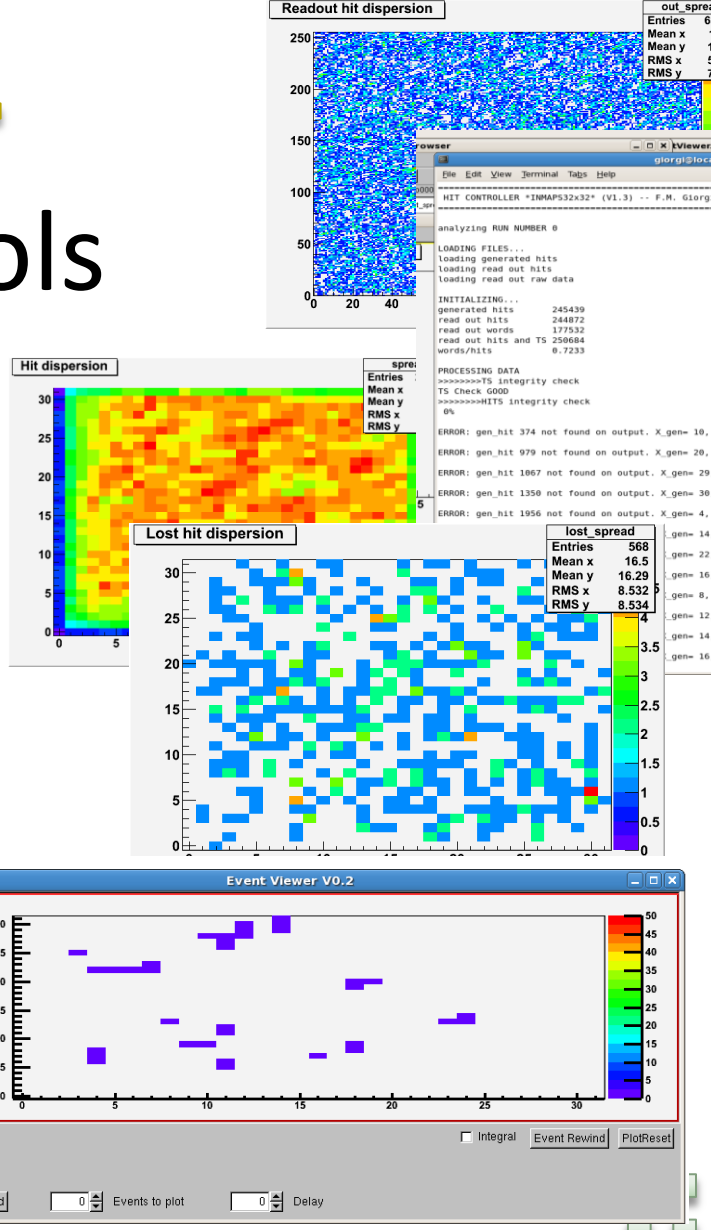


Real matrix model
(by F. Morsani)

Simulation check tools

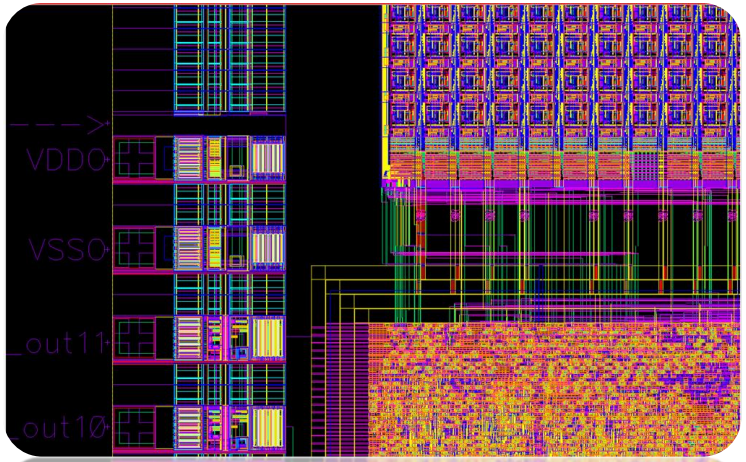
- Several **debug tools** were developed during last years to help us with simulation checks.

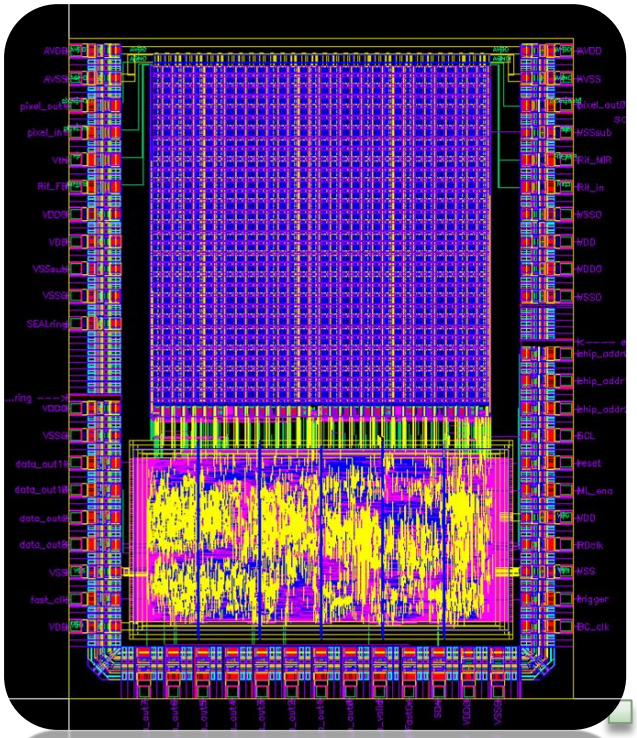
  - VHDL Monte Carlo generator based tuned on physics simulation data (data provided by **R.Cenci**)
  - Efficiency estimators
  - X-check tools
  - Event display
  - Cluster analysis



INMAPS Submission summary

- Behavioral and post layout simulation in good agreement.
- Placed 35k-cell peripheral readout circuit.
- Collaboration submitted chip in June 2011.





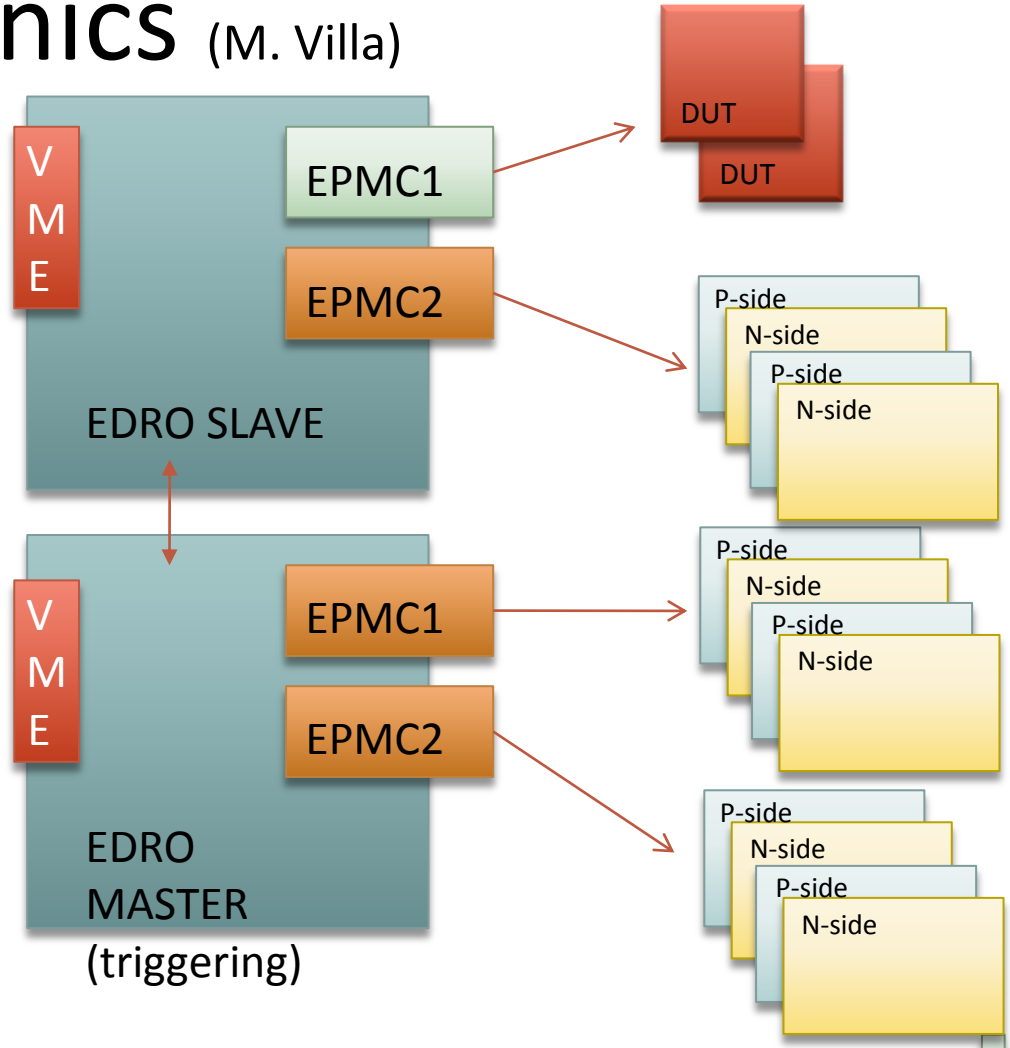
CERN Test Beam September 2011

Bologna Updates

DAQ electronics (M. Villa)

- 2 EDRO boards
- 6 Strip modules
  - (4 triggering + 2)
- 2 DUTs module

New DUT EPMC firmware developed for this Test Beam



TDAQ integration updates

(by C. Sbarra, S. Valentinetti)

- Table positions logger
- Data monitoring and data quality
- Updated run configurations data-base

Conclusion

- New L0 strip readout architecture (pixel-like) under investigation.
- Latest pixel readout architecture implemented on a 4-well INMAPS process: now at foundry.
- Now packing and moving to Geneva: Test Beam @CERN SPS next week.

Back-Up

Strip Rates

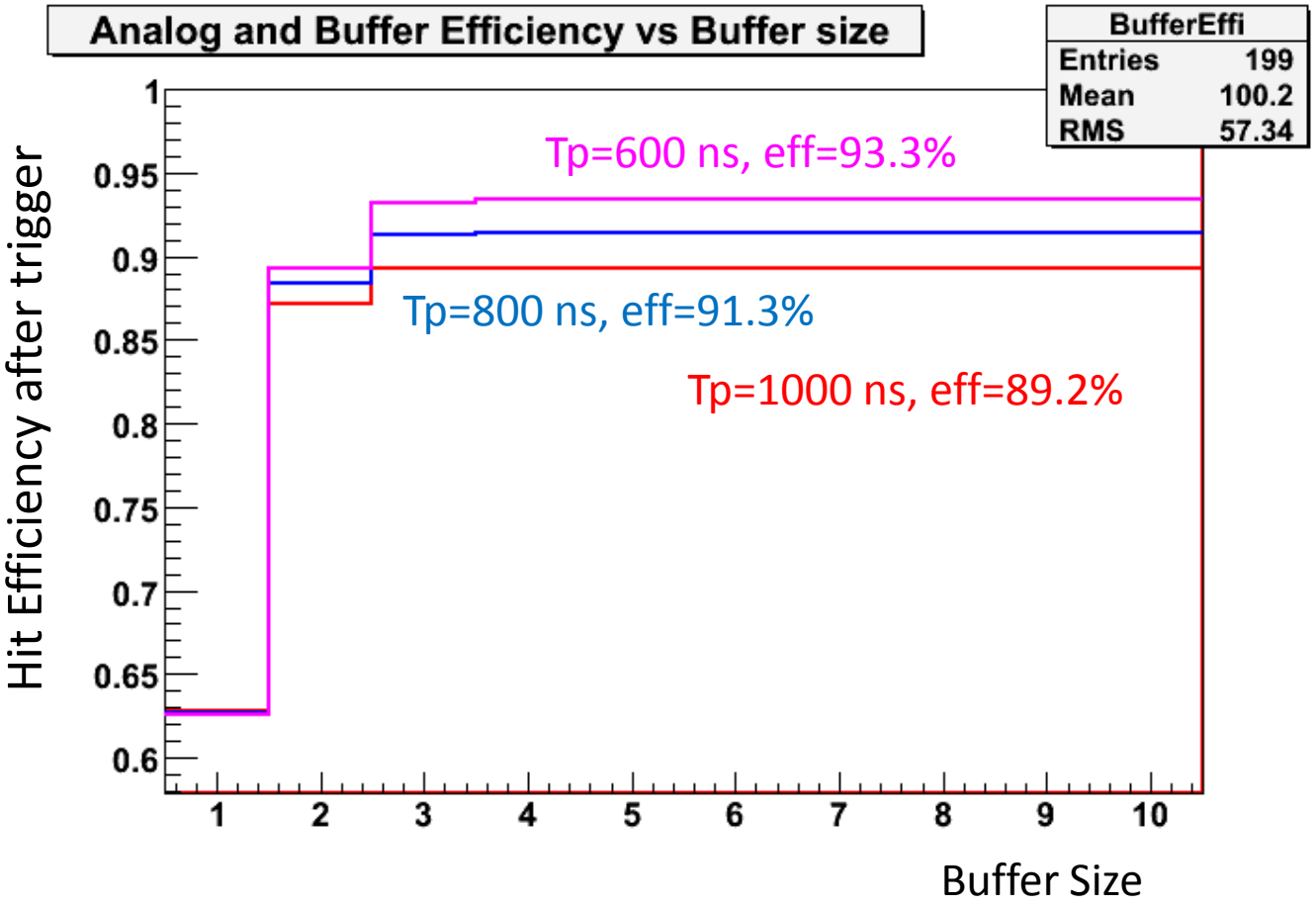
- Strip rates as given by Riccardo C. (5/13/11):

new values	old values
• L0: 2060 kHz/strip	~ =
• L1: 687 kHz/strip	(268 kHz/strip)
• L2: 422 kHz/strip	(179 kHz/strip)
• L3: 325 kHz/strip	(52.5 kHz/strip)
• L4: 47 kHz/strip	(21.9 kHz/strip)
• L5: 28 kHz/strip	(18.7 kHz/strip)

Max peaking times (ns) at fixed strip efficiency

Target strip efficiency	97.6%		95%		91%	
	SF=5	SF=1	SF=5	SF=1	SF=5	SF=1
L0	5	25	10	52	19	95
L1	15	74	31	156	57	286
L2	24	120	51	253	93	466
L3	31	156	66	329	121	605
L4	215	1077	455	Max	836	Max
L5	361	1807	763	Max	1403	Max

L4: 47 kHz/strip but longer deadtimes

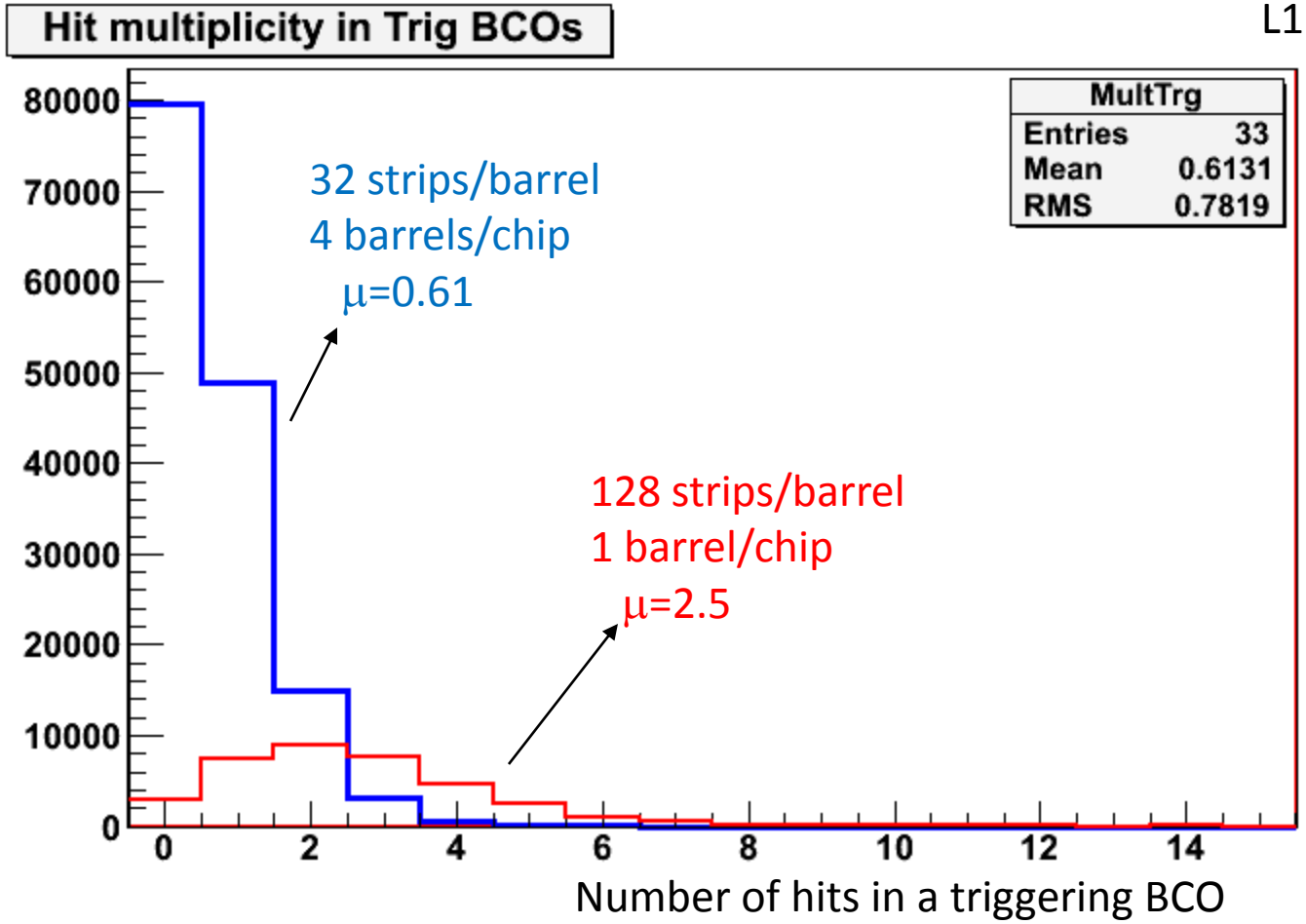


For outer layers (smaller hit rate) the buffer size is not a problem: 5 buffers/strip seem enough. The dominant parameter is the analog dead time.

M. Villa

Hits in triggered BCO

L1: 687 kHz/strip



Even with just one barrel, the average multiplicity is LOW.

If T(BCO)>2T(RD) there is enough time to read the hits out

Efficiencies vs rate and dead times

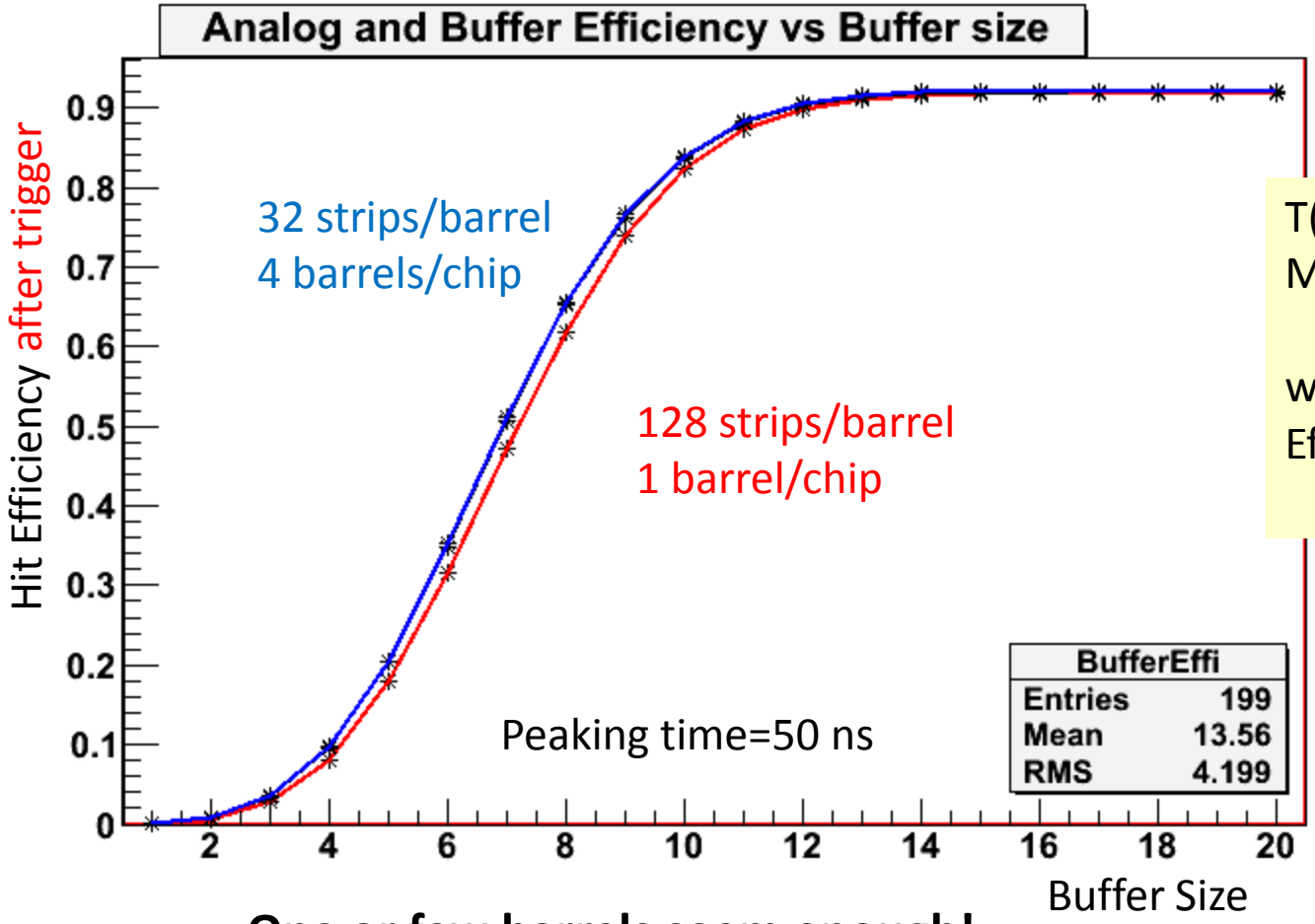
Layer	C_D [pF]	t_p [ns]	ENC from R_S [e rms]	ENC [e rms]	Hit rate/strip [kHz]	MMC Efficiency
0	11.2	25	220	680	2060	(0.732)
1	26.7	50	650	1190	687	**0.917**
		100	460	930		**0.841**
2	31.2	50	830	1400	422	**0.948**
3	45.8	50	1480	2130	325	**0.960**
4	52.6	1000	340	820	47	**0.893**
5	67.5	1000	500	1010	28	**0.934**

Pessimistic: Cluster size 1, no charge sharing, worst peaking time

Conditions: 20 buffers, 150 kHz trigger rate, 300 ns time window for all layers.
Buffer overflow on Layer 0

Strip chip: how many barrels ?

Inefficiency sources: Analog peaking time, limited buffer size, sparsification time.



T(BCO)>2T(RD)
Mandatory!

when T(BCO)=T(RD)
Efficiencies at zero

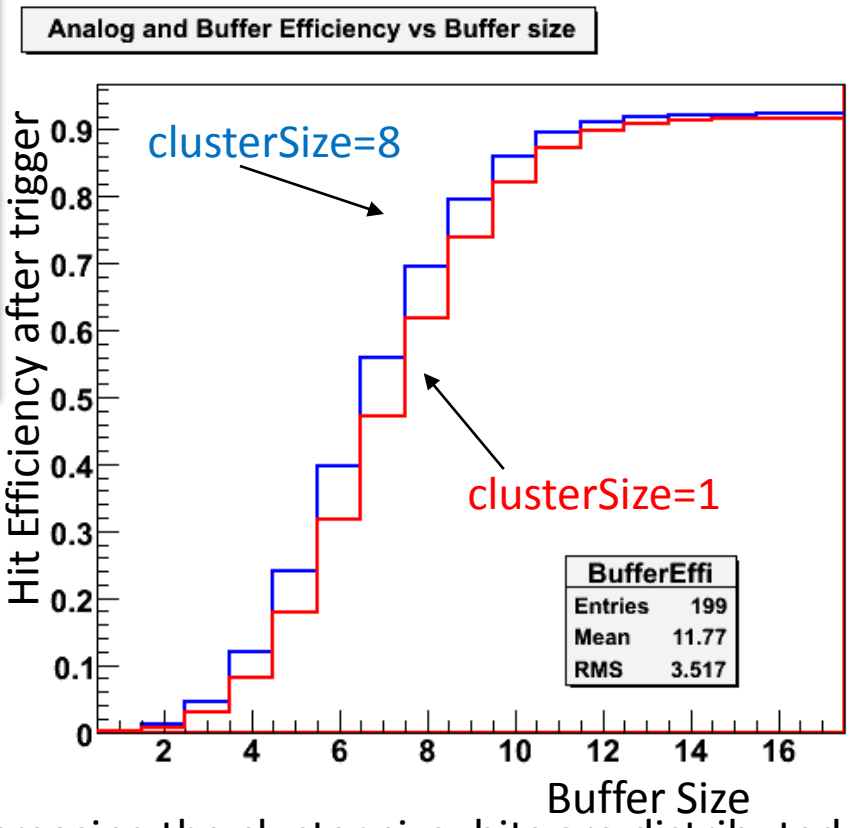
150 kHz trig rate
300 ns DAQ
time window

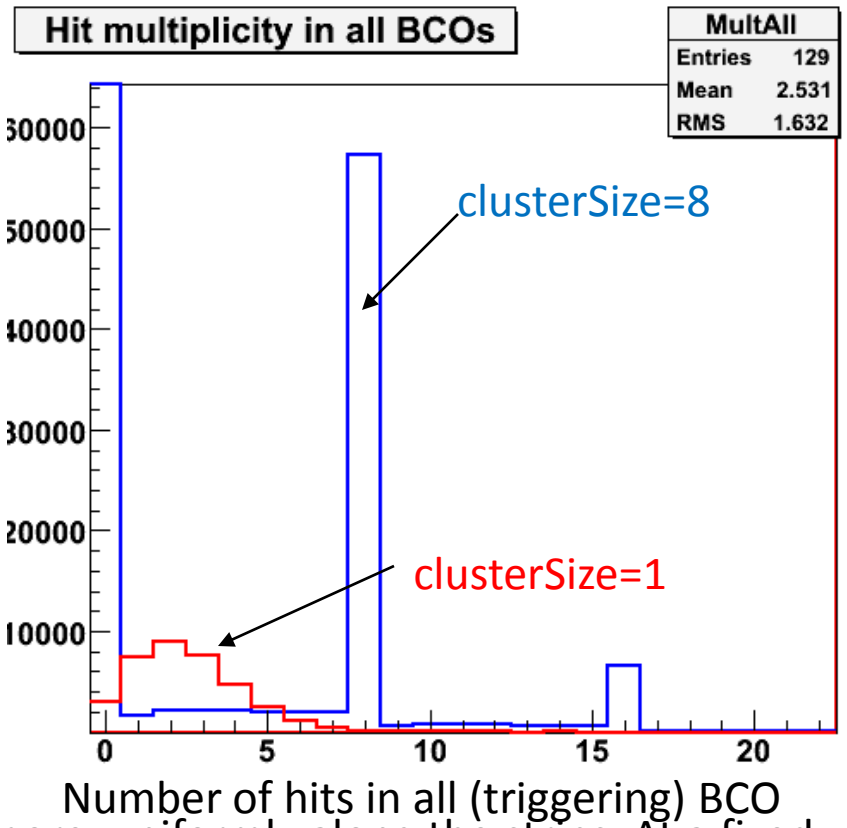
One or few barrels seem enough!

Cluster size effects

fixed hit chip rate
L1: 687 kHz/strip

Peaking time=50 ns, 128 strips/barrel, 1 barrel/chip





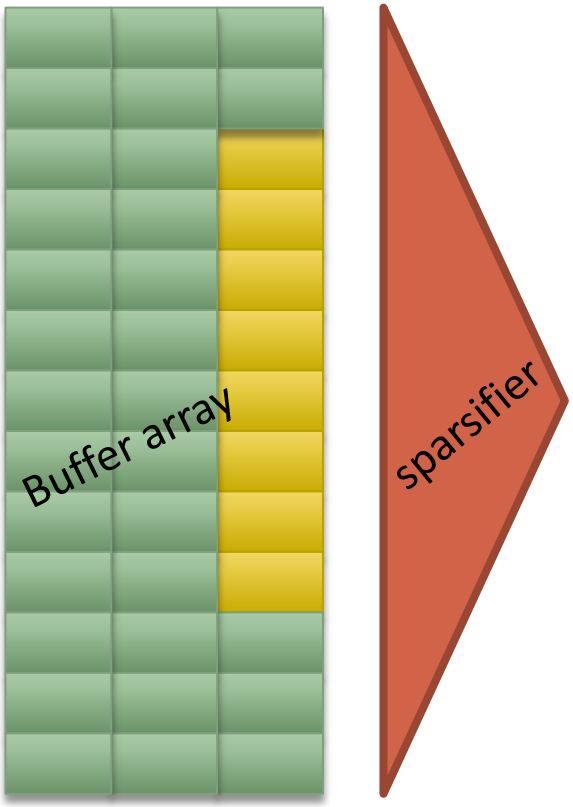
Increasing the cluster size, hits are distributed more uniformly along the strips. At a fixed hit chip rate, less buffers are needed!

Despite a longer reading time on triggering BCO for BCO with hits, they are rarer.

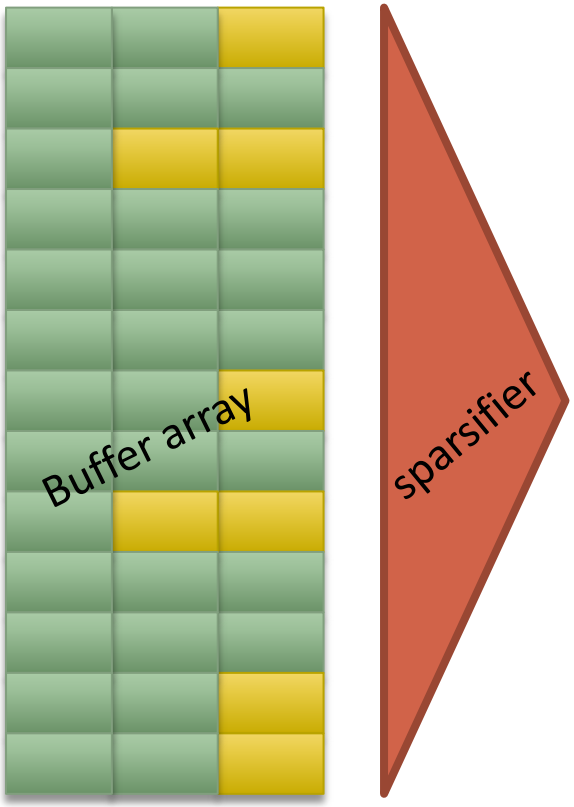
Cluster size effects

Same rate

Cluster factor 8



Cluster factor 1



More likely pile-up in buffers,
More buffering needed.