Update on microstrip front-end and Layer0 pixel upgrade

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OUTLINE

- Microstrip front-end processor
  - design features
  - first simulation results
- Monolithic pixels in INMAPS CMOS technology
  - general features
  - layout characteristics
- 3D analog front-end for hybrid pixels
  - design modification for p-on-n sensors

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Technology options for the SuperB SVT

- **Design of the SVT layer0 at SuperB has to comply with severe requirements**
  - large background, >5 MHz/cm^2, small thickness, <1% X_0
- **Microstrips/striplets**
  - **Baseline option** – fast (layers 0 to 3) and slow (layers 4 and 5) front-end based on a 130 nm planar technology
- **3D Hybrid pixel detectors**
  - **vertically integrated, mixed-signal circuit** for a pixel detector in high resistivity silicon - fine pitch (50 μm) bump bonding (IZM, Munich) or more advanced technologies (direct bonding by Ziptronix or T-Micro) – based on a 130 nm dual tier CMOS process - **128x32** element chip to be submitted in the next run
- **3D DNW and INMAPS monolithic sensors**
  - **deep N-well sensors** were proposed to enable fast readout through pixel-level sparsification and time stamping - DNW sensor in an undepleted substrate, analog front-end for capacitive detectors, analog and digital blocks integrated in separate layers – based on a 130 nm dual tier CMOS process - a **128x96** pixel chip is being designed for the next run
  - **INMAPS sensors** - based on a quadruple well 180 nm CMOS technology featuring a high resistivity epitaxial layer – test chip submitted end of July

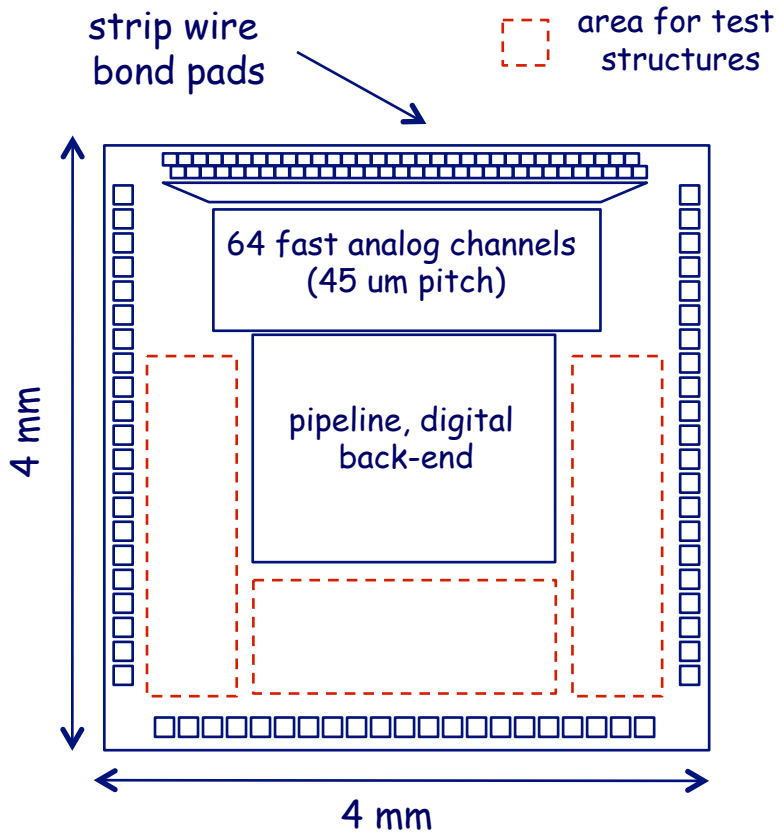
Microstrip detector: proposed layer grouping

Layer	C_D [pF]	available t_p [ns]	selected t_p [ns]	ENC from R_S [e rms]	ENC [e rms]	Channel width [μm]	Hit rate/ strip [kHz]	Efficiency 1/(1+N)
0	11.2	25, 50, 100, 200	25	220	740	3000	2060	0.890
1	26.7		100	460	940		697	0.857
2	31.2		100	590	1100		422	0.908
3	34.4		200	410	940		325	0.865
4	52.6	400, 600, 800, 1000 (or 500 and 1000)	500	490	1000	9000	47	0.947
			600	440	940			0.937
5	67.5		800	560	1090		28	0.949
			1000	500	1030			0.937

RC²-CR shaping, I_D=500 μA, L=200 nm, N-channel input device, analog dead time=2.4 t_p

Strip front-end development

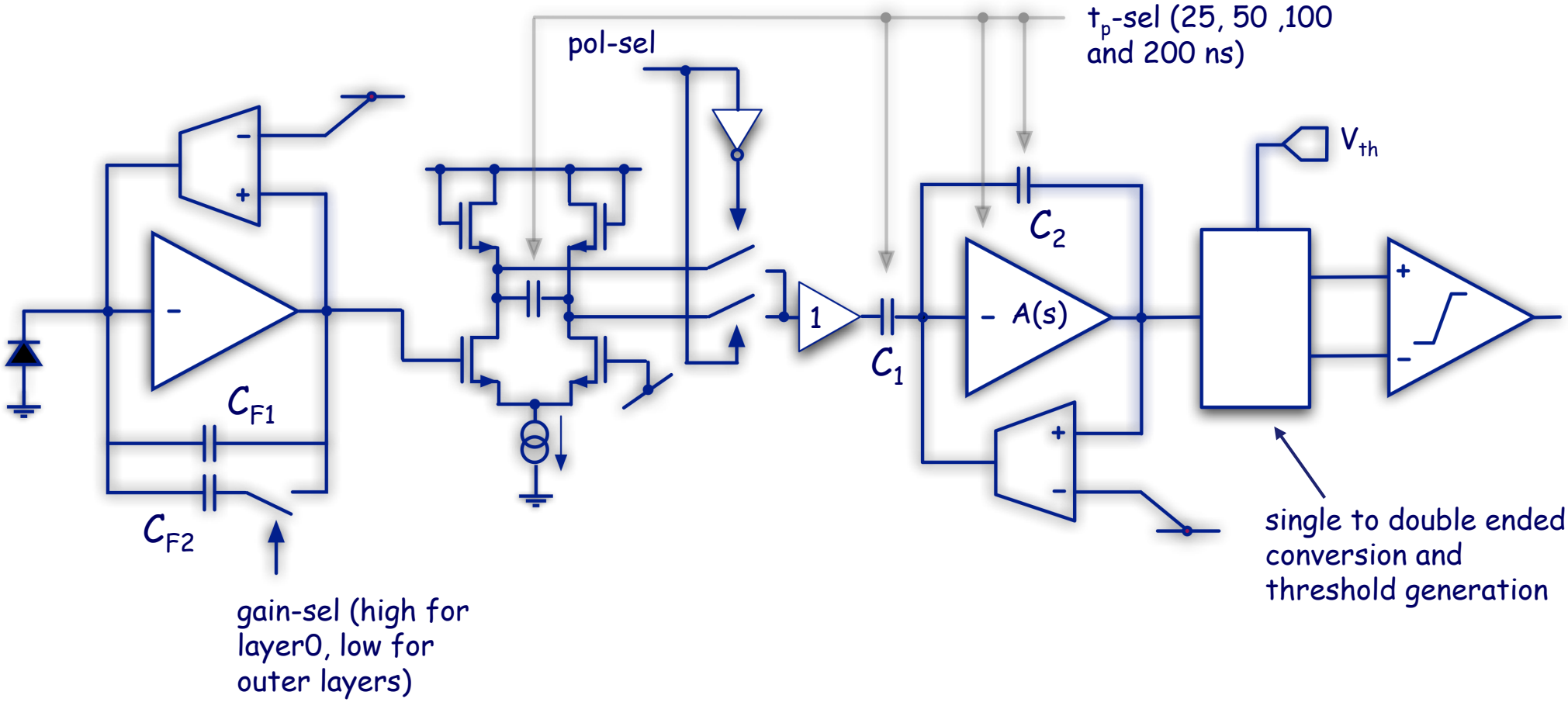
- Fast and slow front-end prototype chip (IBM 130 nm) – slow front-end will is being developed by the group of Carlo Fiorini in Milan



- Milestones for strip front-end development
  - 2012: first test structures - 2 x 64 channels (fast and slow front-end), auxiliary blocks
  - 2013: first fully operational prototype chip – 2 x 128 channels (fast and slow readout)
  - 2014: production run
  - Account for some contingency after the first or the second step

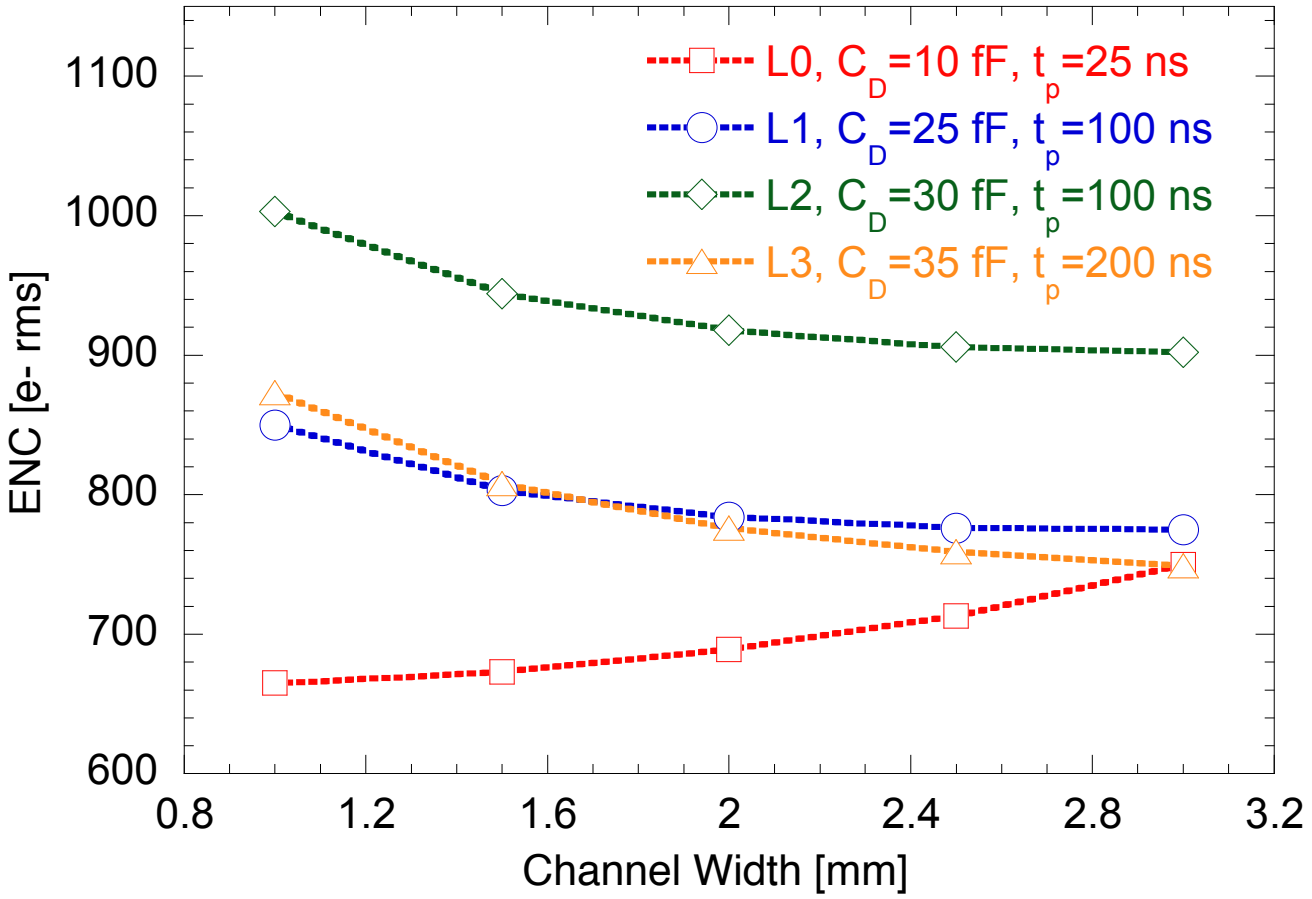
Fast front-end block diagram

- Simulation results available for a preliminary version of the charge preamplifier (I_D=500 μA)



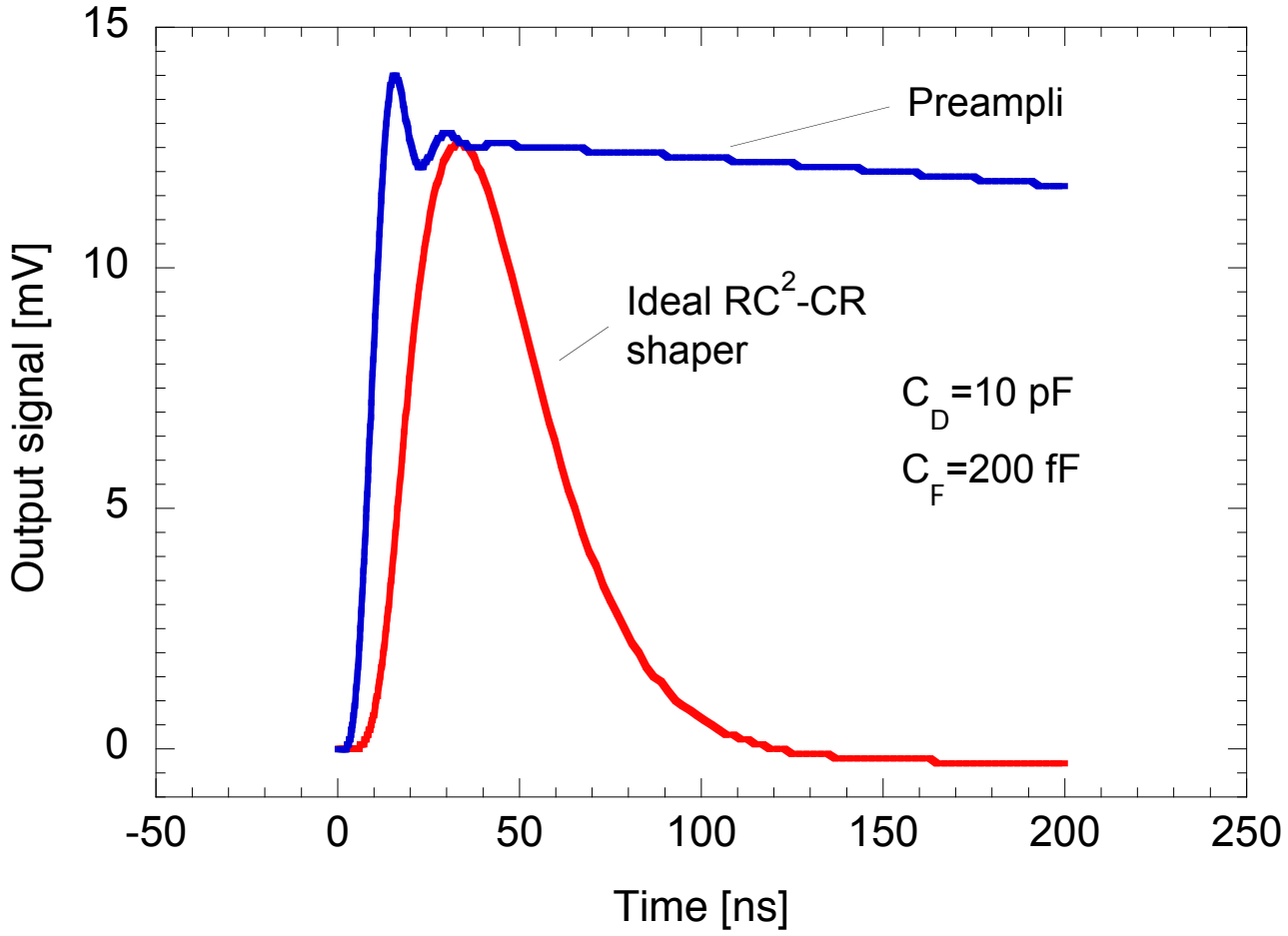
Equivalent noise charge

- Results obtained with ideal RC^2-CR shaper and ideal bias network



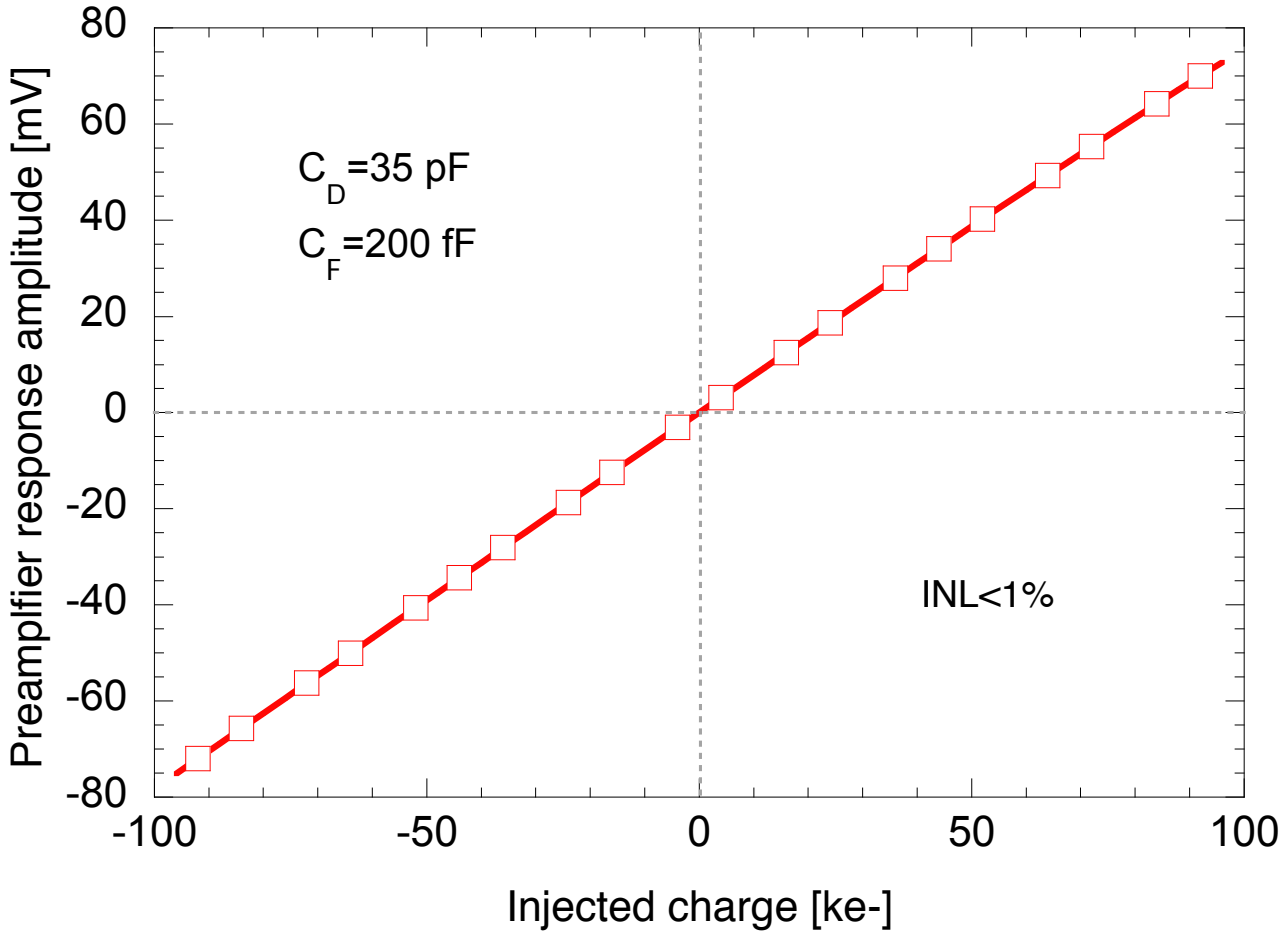
Response to a charge signal

- Response to a 1600 e^- input charge



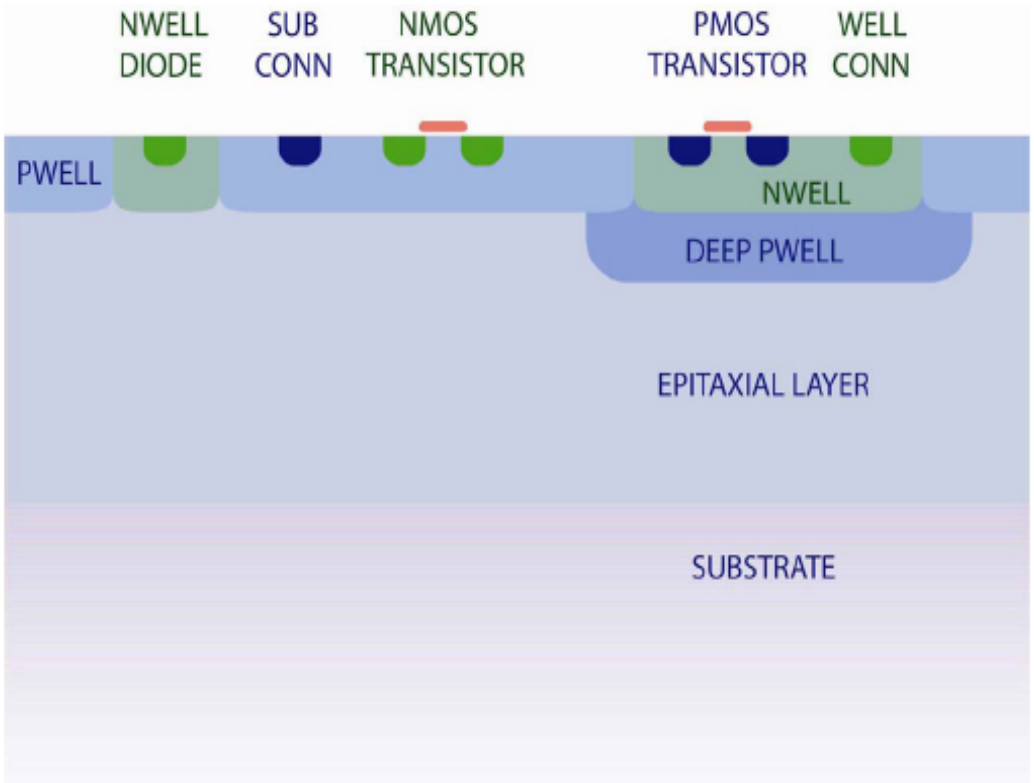
Charge preamplifier response linearity

- Input charge from -96 ke$^-$ to 96 ke$^-$



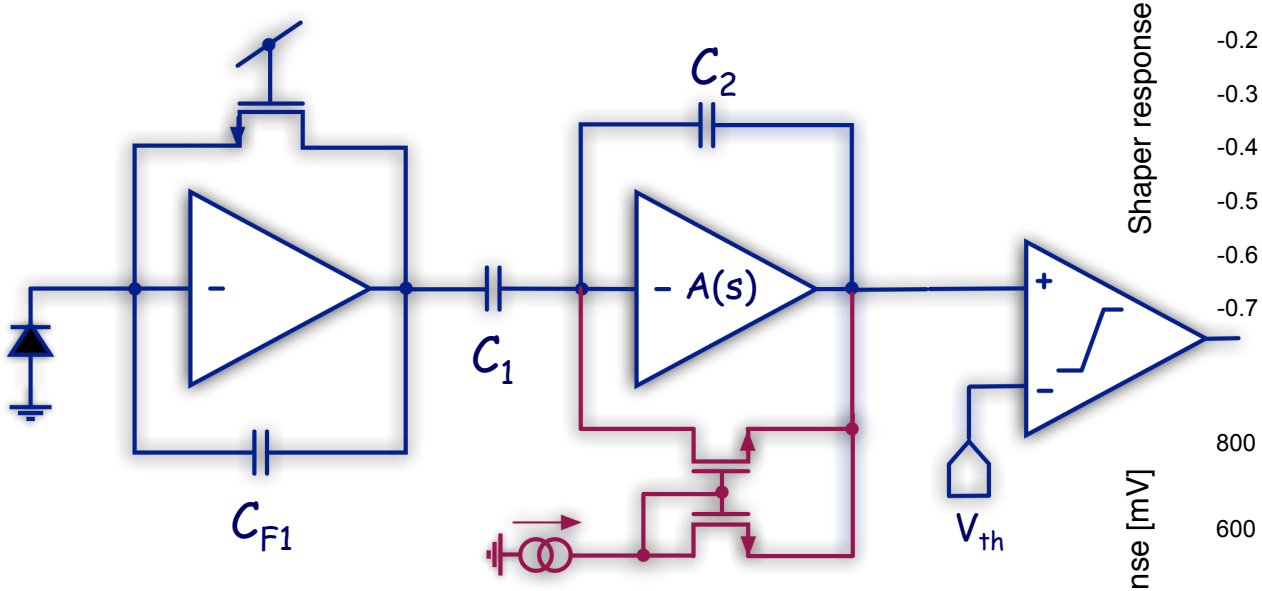
INMAPS technology

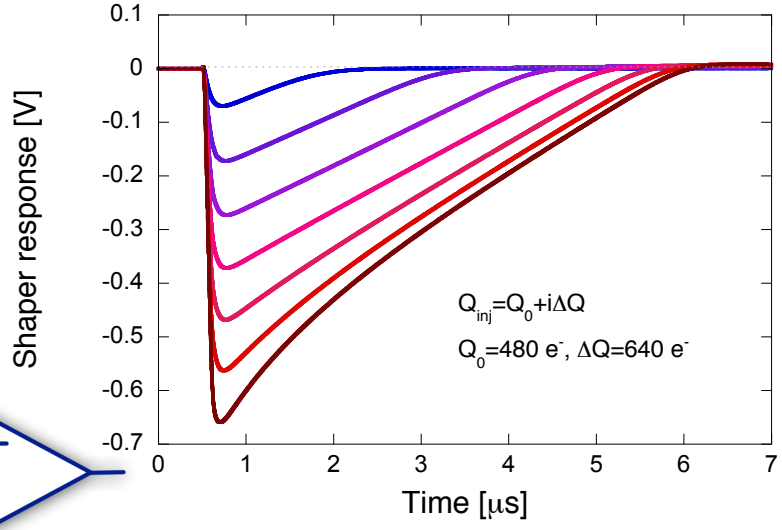
- Avoid charge collection in parasitic N-wells by means of a buried P-type layer (deep P-well)
- Improved charge collection by means of high resistivity epitaxial layer (~1 kOhm cm)

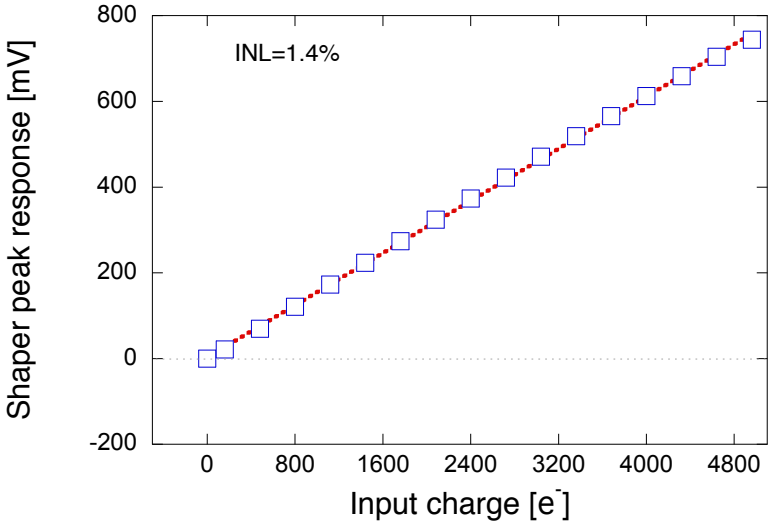


Front-end for MAPS in INMAPS technology

- 180 nm CMOS technology



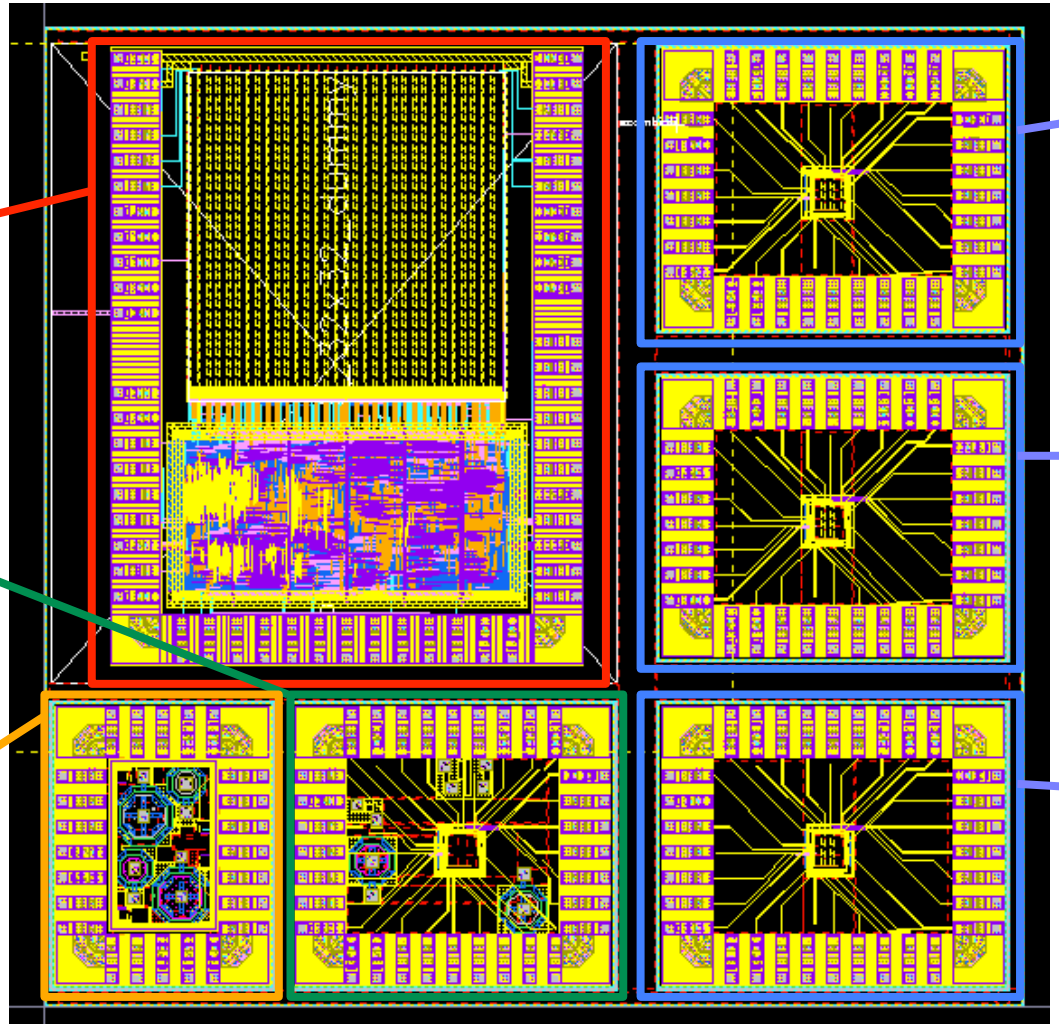




- Power dissipation: 18 μW/pixel
- Peaking time: 230 ns
- ENC=30 e⁻ rms (C_D=40 fF)
- Threshold dispersion: 23 e⁻ rms
- Charge sensitivity: 970 mV/fC

Prototype chip (submitted end of July)

- In 3x3 matrices all the analog outputs are available and an injection capacitor is connected to the central pixel



32x32 matrix (4-diode pixels) with sparsified digital readout architecture

3x3 matrix, 4-diode, no DPW, preampli input device with EL structure, Nw/Pepi diodes and accumulator capacitors

Nw/Pepi diodes, single channels

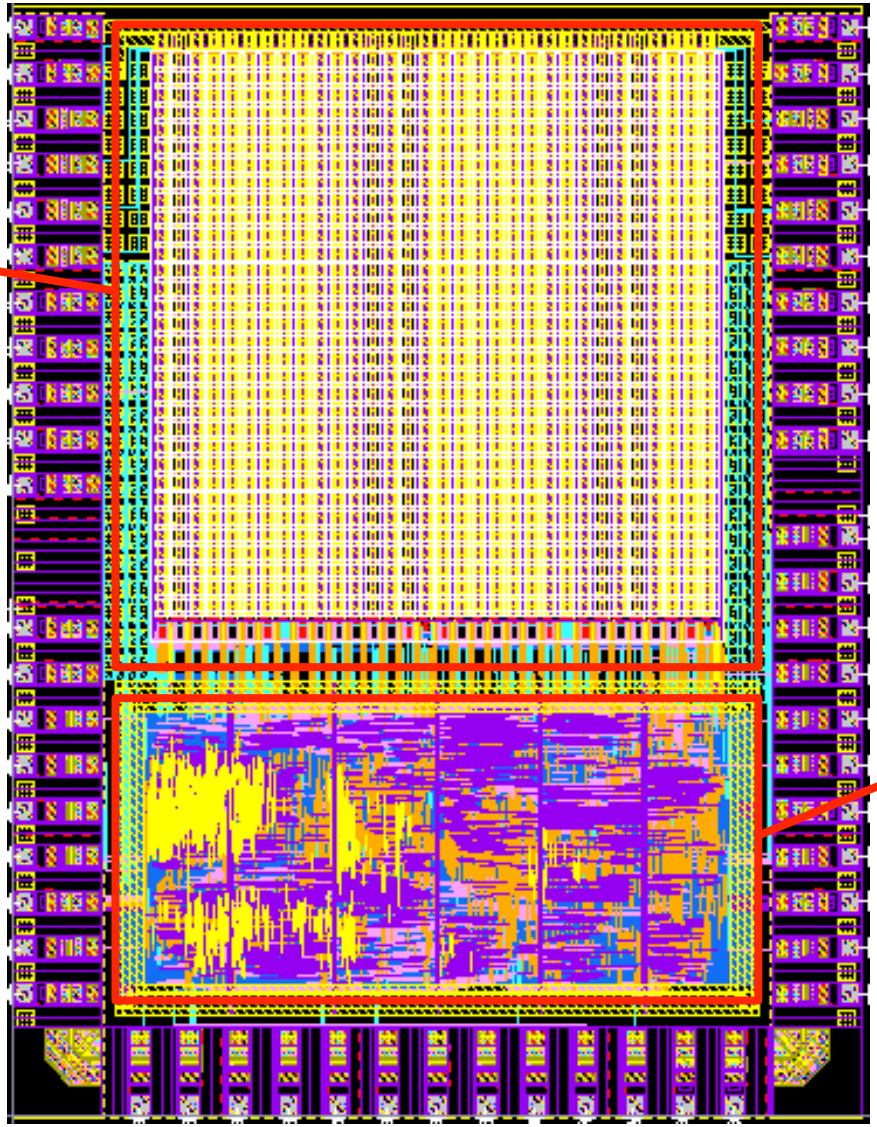
3x3 matrix, 4-diode pixels, DPW, preampli input device with EL structure

3x3 matrix 4-diode pixels, DPW, preampli input device with open structure

3x3 matrix 2-diode pixels, DPW, preampli input device with EL structure

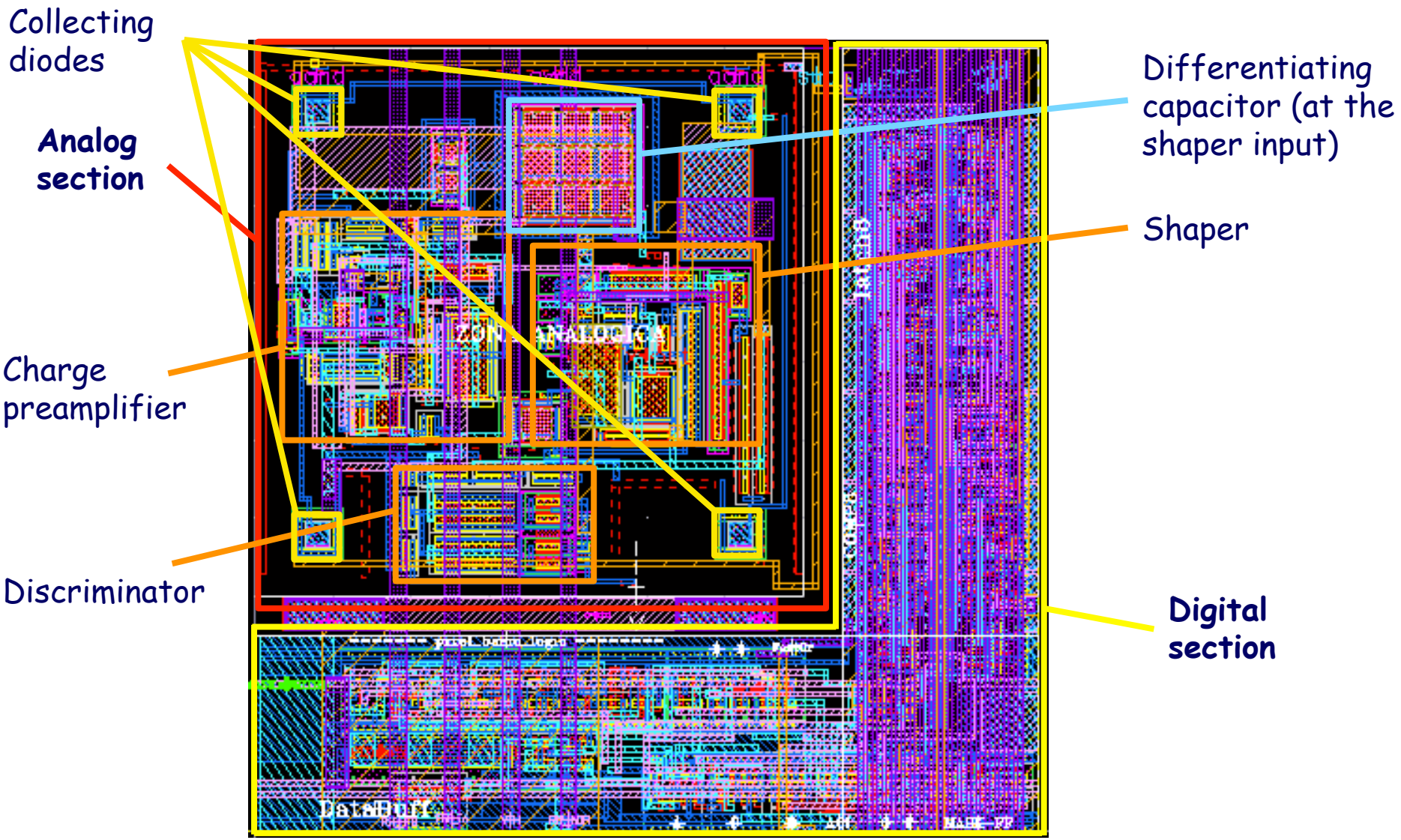
32x32 sparsified readout matrix with time stamp

Sensor matrix
(4-diode pixel)



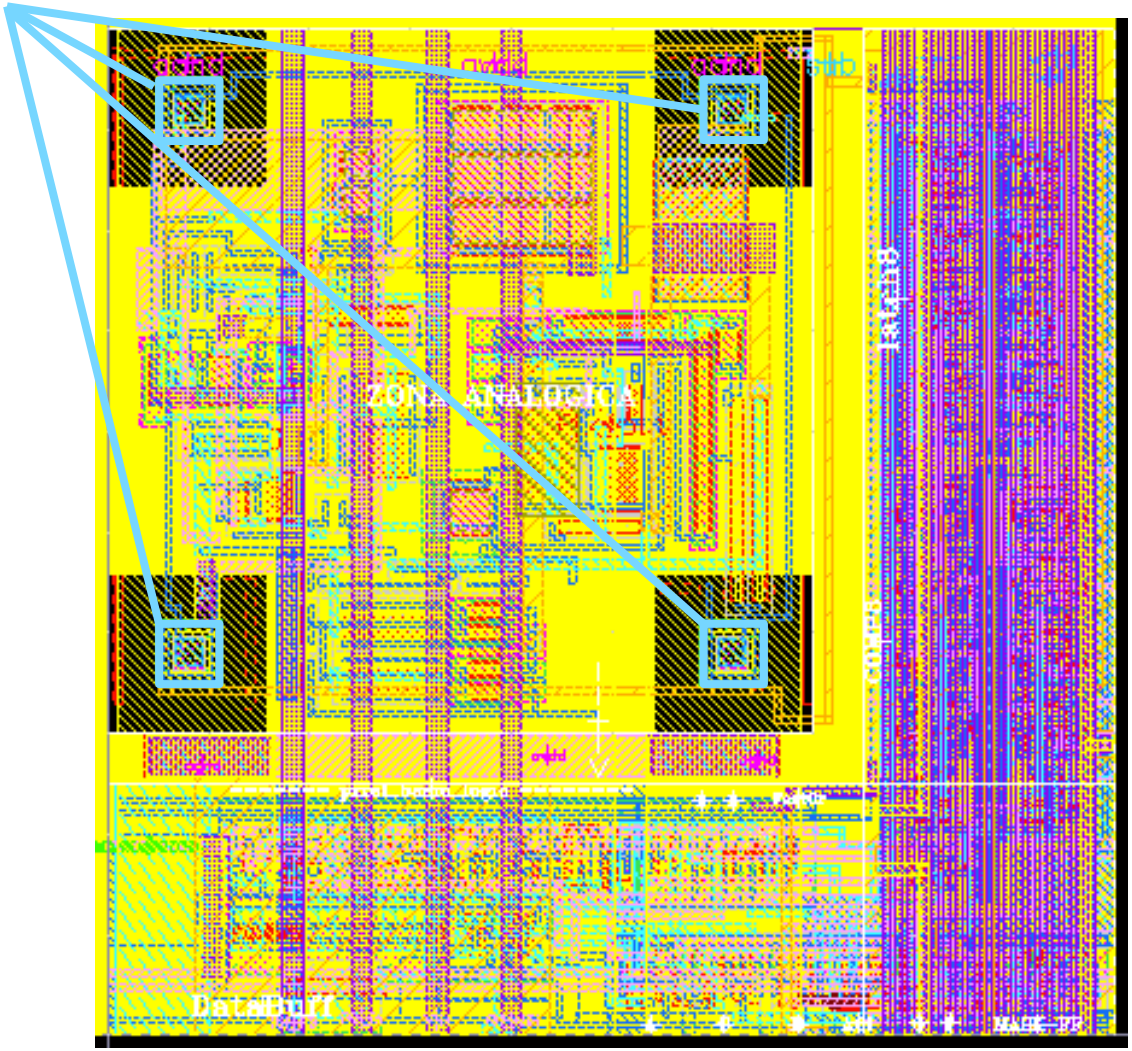
Digital readout
section
(buffering, I/O)

Elementary cell

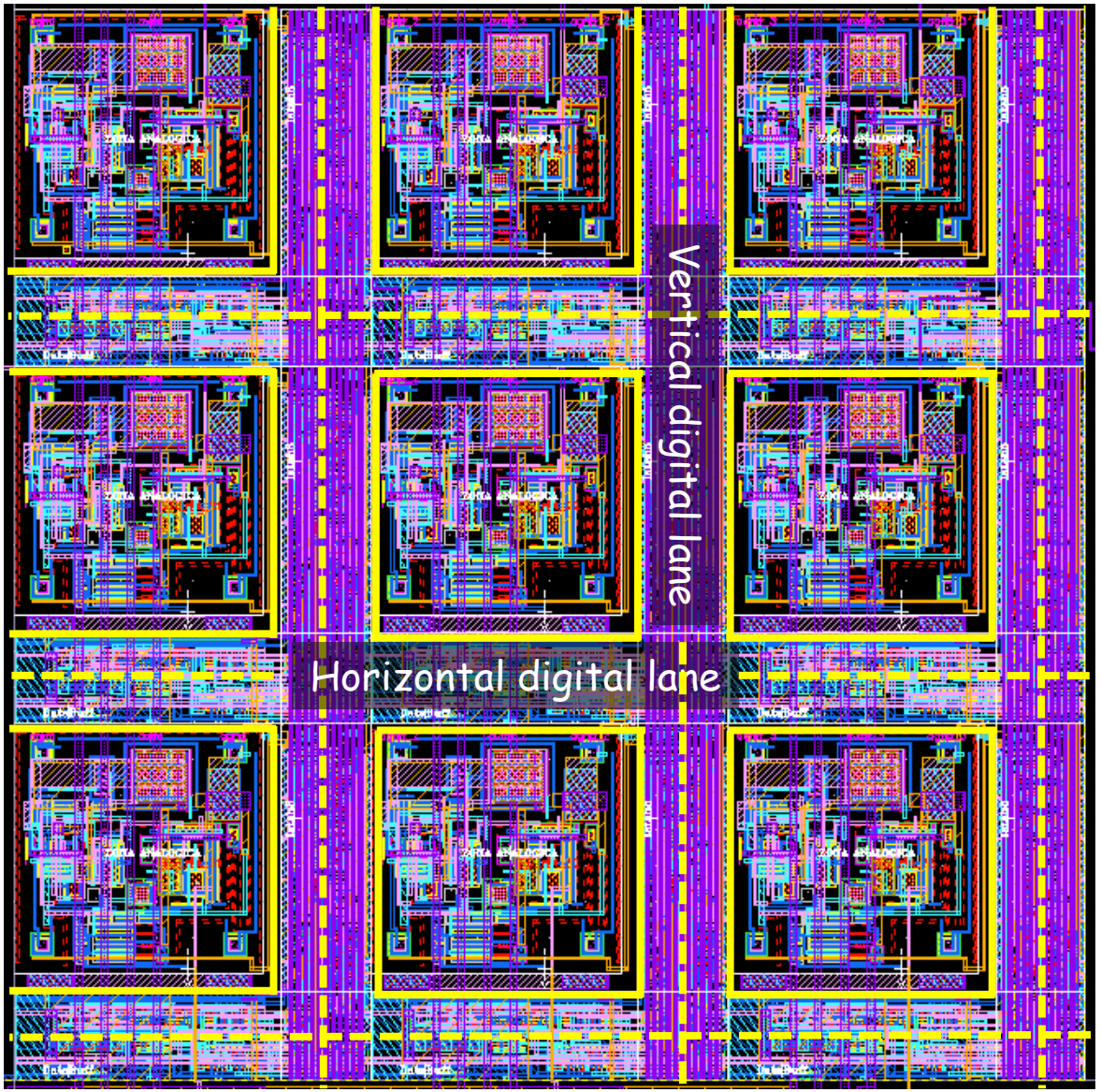


Elementary cell (emphasis on DPW layer)

Collecting diodes



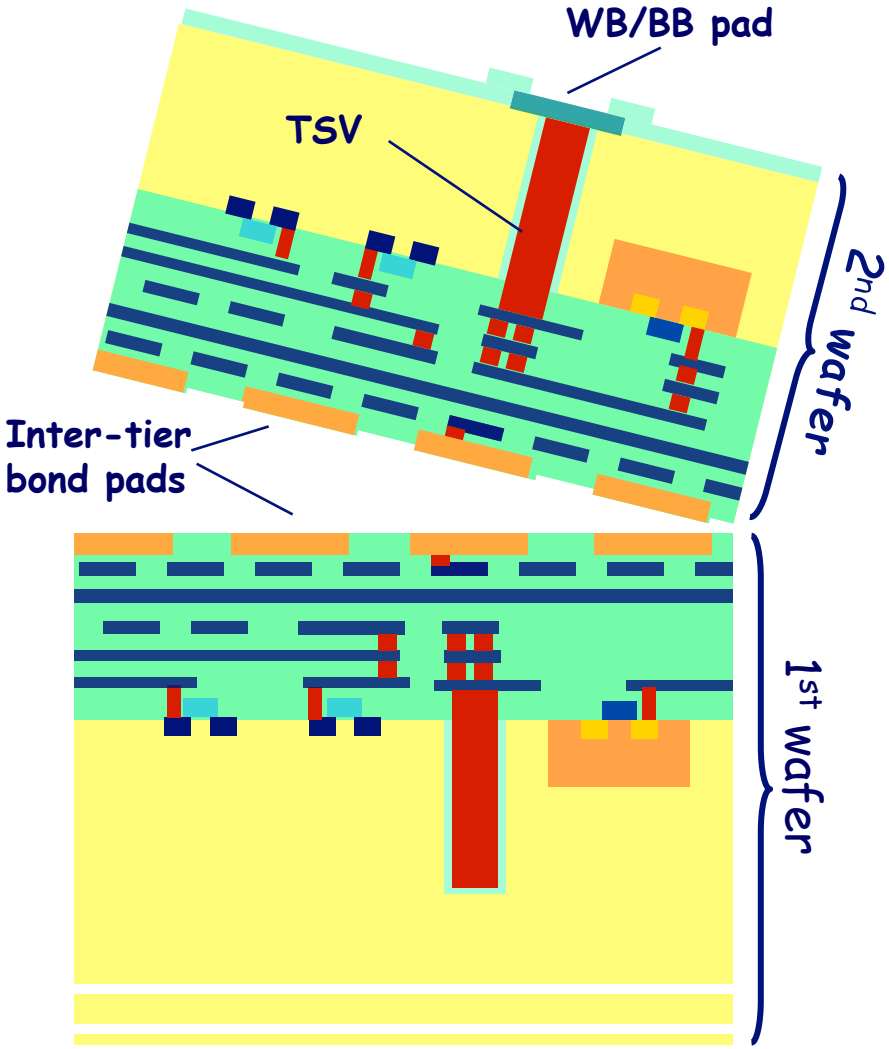
Digital signal routing



L. Ratti, "Update on microstrip front-end and Layer0 pixel upgrade", I SuperB Collaboration Meeting

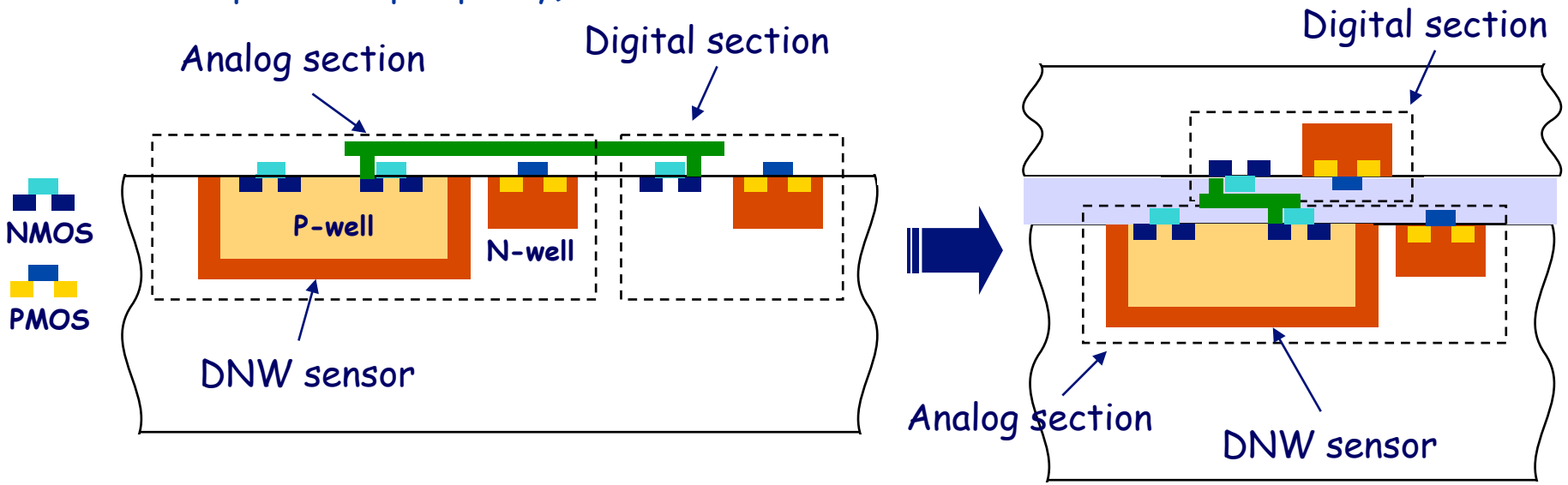
Vertical integration (3D) technologies

- In wafer-level, three-dimensional processes, multiple strata of planar devices are stacked and interconnected using through silicon vias (TSV)
- 3D processes rely upon the following enabling technologies
  - Fabrication of electrically isolated connections through the silicon substrate (TSV formation)
  - Substrate thinning (below 50 μm)
  - Inter-layer alignment and mechanical/ electrical bonding
- Tezzaron Semiconductor technology (via first approach) can be used to vertically integrate two 130 nm CMOS layers specifically processed by Chartered Semiconductor



From 2D to 3D MAPS

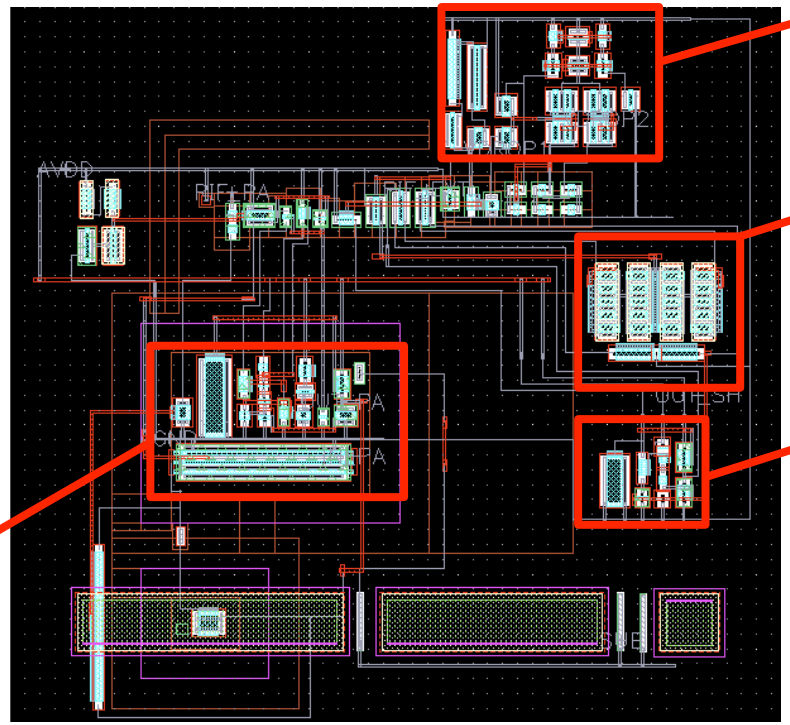
- Analog and digital blocks integrated in separate layers to minimize cross-talk between digital blocks and sensor/analog circuits
  - less PMOS in the sensor layer → improved collection efficiency
  - more room for both analog and digital power and signal routing (in planar CMOS MAPS scaling to suitably large matrices is forbidden by the need for point-to-point lines from macropixels to periphery)



- Tier 1: collecting electrode and mainly NMOS parts from the analog front-end
- Tier 2: PMOS parts from the analog front-end, digital front-end and peripheral digital readout electronics

3D DNW MAPS layout

Analog tier



Voltage drop compensation

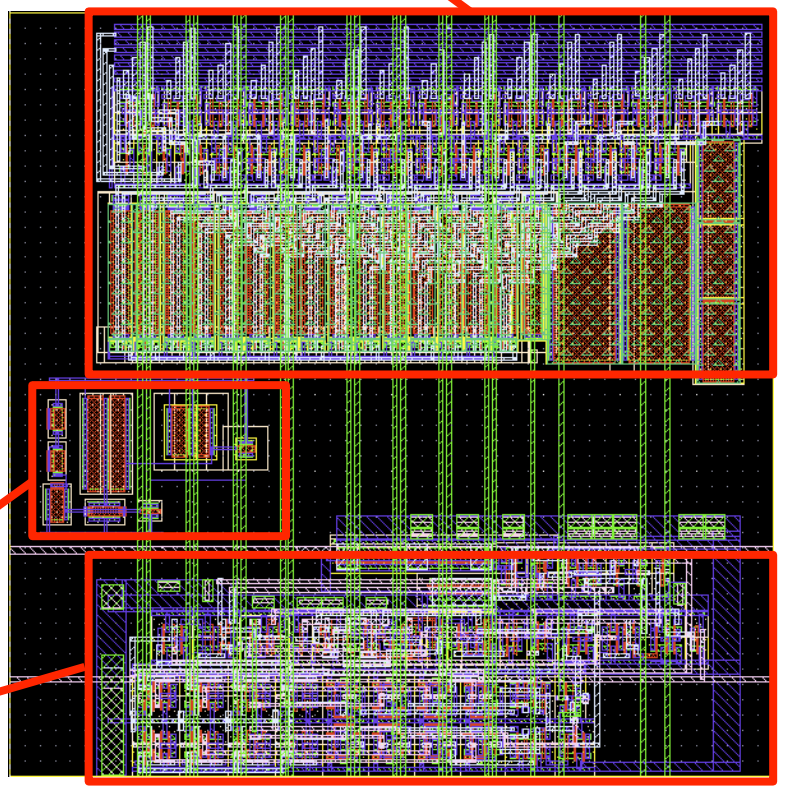
Transconductor

Shaper

PA

Threshold DAC

Digital tier

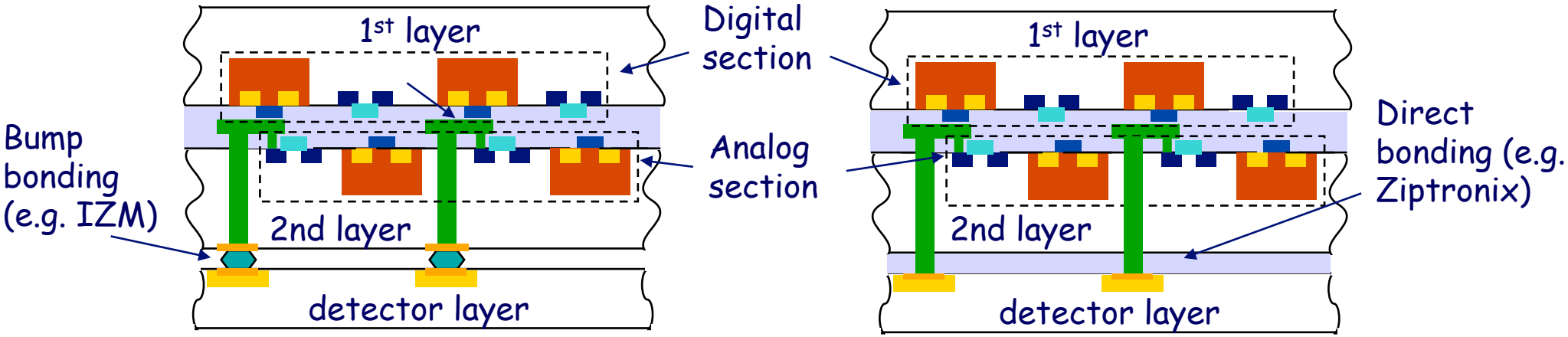


Discriminator

In-pixel logic

3D hybrid pixels

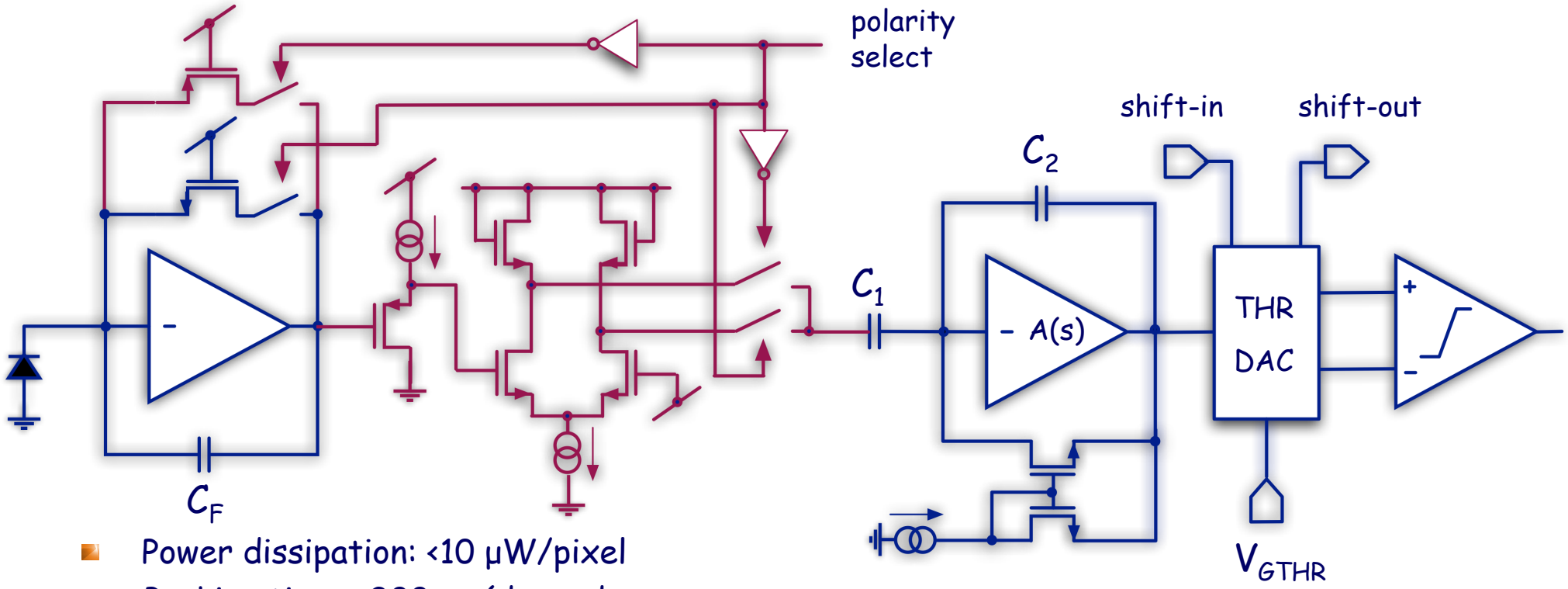
- Development of a 3D front-end chip to be vertically integrated with fully depleted detectors through some more (bump bonding) or less (direct bonding) standard technique



- Larger signal available from the detector ($\geq$ 4000 e^- for 200 μm thickness)
- More advantageous trade-off between S/N and dissipated power

3D front-end for hybrid pixels: polarity selection

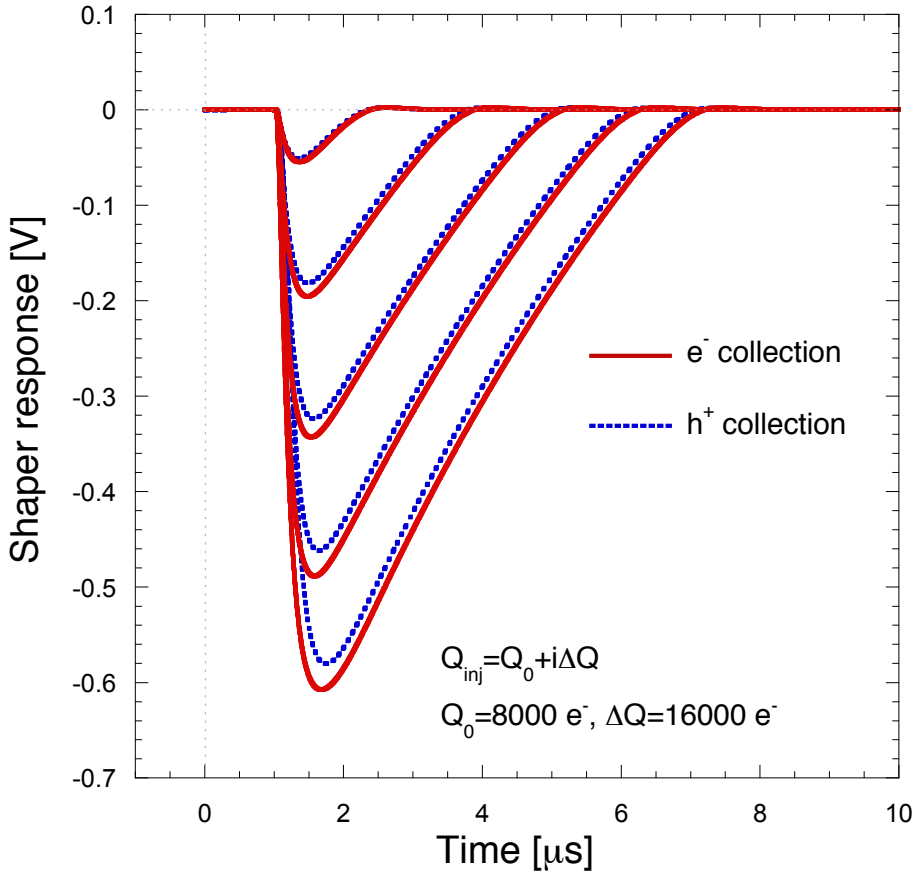
- Changes in the 3D hybrid pixel front-end to make signal processing possible from both n-on-n and p-on-n sensors

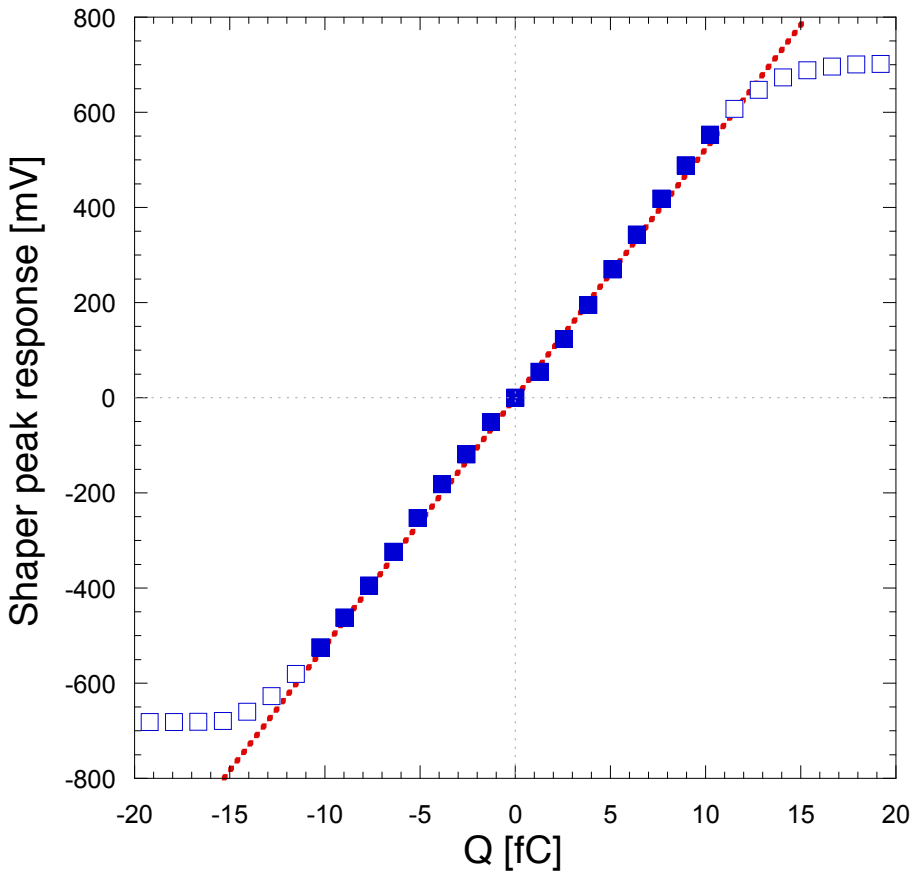


- Power dissipation: <10 µW/pixel
- Peaking time: >300 ns (depends on input charge)
- ENC=200 e^- rms (C_D=150 fF)
- Charge sensitivity: 50 mV/fC
- Threshold dispersion: not evaluated yet

Channel response

- Slight nonlinearity due to the nonlinear shaper feedback network





Conclusion

- Design of the front-end channel for striplets/microstrips has started – submission planned for mid-2012
- Monolithic pixels in INMAPS CMOS technology submitted at the end of July – hips expected to be back in a couple of months
- Design of 3D front-end for hybrid pixels modified to enable signal processing also from p-on-n sensors – ready to submit (both 3D DNW MAPS and 3D front-end for hybrid pixels) 3 months after testing the devices from the first 3D run
- Wafers from the first 3D run are now being diced and should be available soon for characterization