SVT- Status

1st SuperB Collaboration Meeting
QMUL (UK) - September 15 2011

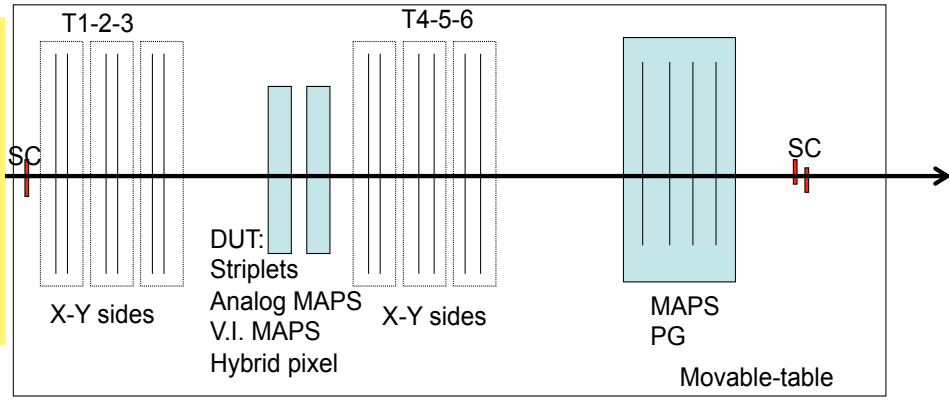
- Giuliana Rizzo
- Universita' & INFN Pisa

SVT Strategy

- SVT Baseline
  - Striplets in Layer0 @ R~1.5 cm
  - 5 layers of silicon strip modules (extended coverage w.r.t BaBar)
  - Main activities:
    - Layer0 striplets:
      - module design (quite complex in a very crowded region)
      - evaluate performance in high background
    - Front-end chips for striplets/strips need to be developed
    - Engineering design of the full detector
- Upgrade Layer0 to thin pixel for full luminosity run
  - more robust against background occupancy
  - SVT Mechanics will allow a quick access/removal of Layer0
  - Several pixel options still open & under development: R&D continue in 2012 after TDR → decision on pixel technology in 2013
    1. CMOS MAPS: continue R&D on readout speed and rad hardness
    2. Hybrid Pixels: FE chip 50x50 um pitch and R&D to reduce material < 1% X0.
    3. Pixel 3D with Vertical Integration: can we access this technology in a (time) reliable and stable way?

SVT Testbeam @CERN next week

- Most of the SVT group working hard over the summer to get things ready
  - Thanks to S. Bettarini for the organization
- Several pixel structures and striplets on test



•New flexibility implemented in DAQ system (Bologna) to test all the different DUT's

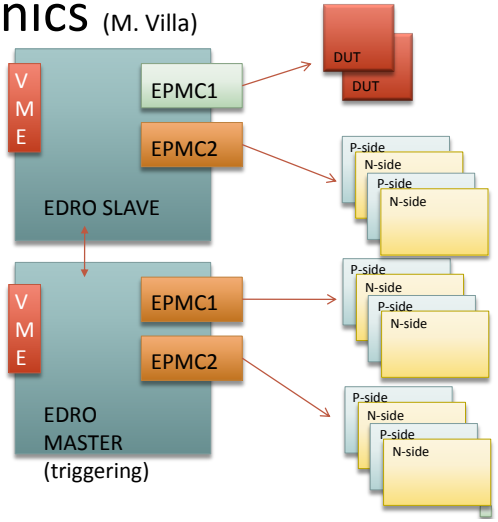
•Analysis team (PI+BO+MI) is getting the new code ready

•More robust movable table (Torino)

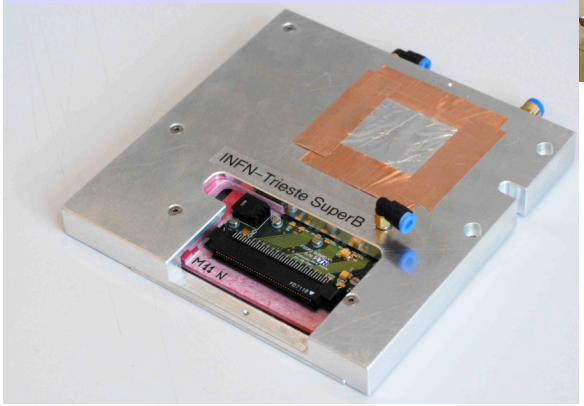
DAQ electronics (M. Villa)

- 2 EDRO boards
- 6 Strip modules
  - (4 triggering + 2)
- 2 DUTs module

New DUT EPMC firmware developed for this Test Beam



•5 new telescope modules with FSSR2 readout built in Trieste to a have a 3+3 telescope configuration.



Front-end chip for strip/striplets

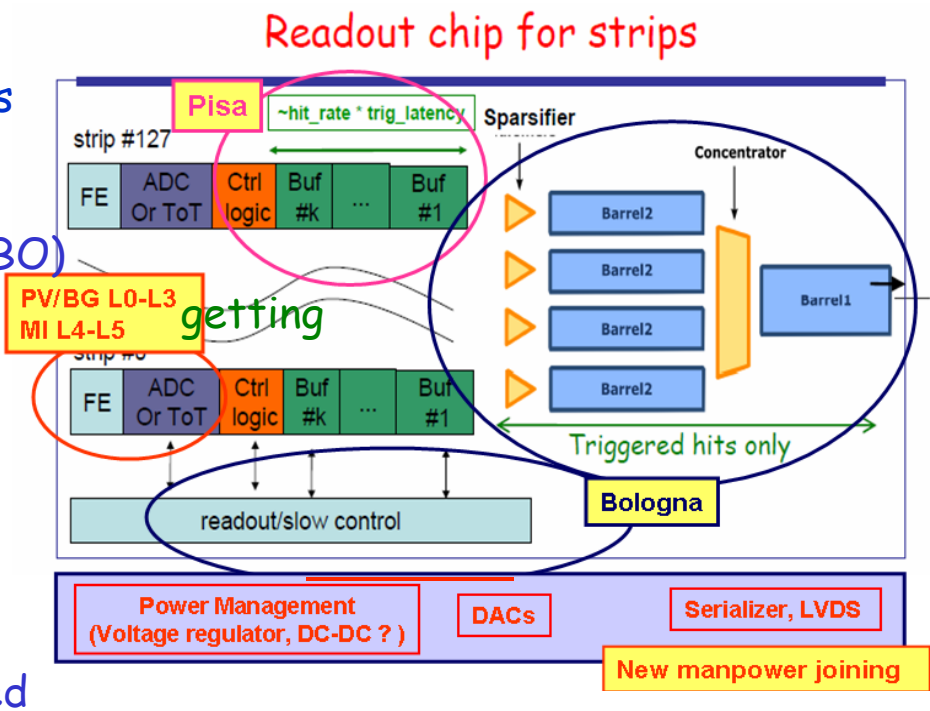
- Clearer definition of the requirements for strip modules in the last months
- Need to develop 2 new chips since existent chips do not match all the requirements : analog info, high rates in inner Layers (2 MHz/strip in L0) & short shaping time (25-100ns), long shaping time (0.5-1 us) in Layers 4-5

Current Plan presented at INFN referees:

- Develop fast (L0-L3) and slow (L4-5) channels
- Adapt readout architecture developed for pixel for strip readout chips.
- Full VHDL sim, of the chips for TDR (PV/PI/BO)
- For real chip development/construction new manpower on board.

Responsibility :

- Analog Front-end: fast channels for L0-L3 (PV/BG), slow channels L4-L5 (MI)
- Control Logic-in strip (PI)
- Readout architecture (BO)
- Auxiliary blocks (All groups + blocks developed from CERN IBM 130 nm)



SVT Parallels

11:00->*12:30* **Parallel 1 - SVT** (Convener: Giuliana Rizzo (*PI*)) (Francis Bancroft Bldg - room 240 (FB))

Description:

EVO Details:
http://evo.caltech.edu/evoNext/koala.jnlp?meeting=eBele2vtv9aaavIvauIB The web password is superb

People can connect via the EVO phone bridge, using an appropriate number from
http://evo.caltech.edu/evoGate/telephone.jsp and the following codes:
Phone Bridge ID: 10 9383 Phone Bridge Password: 5939

11:00	Introduction (10')	Giuliana Rizzo (*PI*)
11:10	Pixel & Strip FE Electronics Update (20')	Lodovico Ratti (*PV*)
11:30	Update on activities in Bologna (20')	Filippo Maria Giorgi (*BO*)
11:50	Striplets performance in high background conditions (20')	Nicola Neri (*MI*)

14:00->*16:30* **Parallel 2 - SVT** (

•Mostly devoted to Mechanics discussion

om 240

14:20	Update on activities in Strasbourg (20')	Isabelle Ripp-Baudot (*IPHC, CNRS/IN2P3 Strasbourg*)
14:00	Update on activities in UK (20')	Fergus Wilson (*RAL*)
14:20	SVT Mechanics (20')	Filippo Bosi (*PI*)
14:40	Technical Discussion on SVT Mechanics (50')	

16:00->*17:30* **Parallel 3 - SVT** (Convener: Giuliana Rizzo (*PI*)) (Francis Bancroft Bldg - room 240 (FB 240))

16:00	Update on HDI design and periphel electronics (20')	Mauro Citterio (*MI*)
16:20	Update on activities in Trieste (phone) (20')	Carlo Stella (*TS*)
16:40	Update on background simulation (phone) (20')	Riccardo Cenci (*PI*)

Strip and Pixel front-end Update

L.Ratti - PV

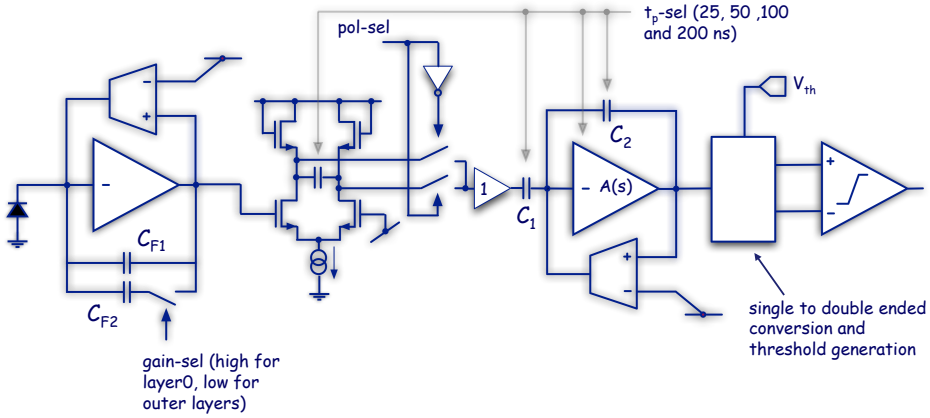
OUTLINE

- Microstrip front-end processor
  - design features
  - first simulation results
- Monolithic pixels in INMAPS CMOS technology
  - general features
  - layout characteristics
- 3D analog front-end for hybrid pixels
  - design modification for p-on-n sensors

- First simulation of the analog blocks for the fast channels (L0-1-2-3)

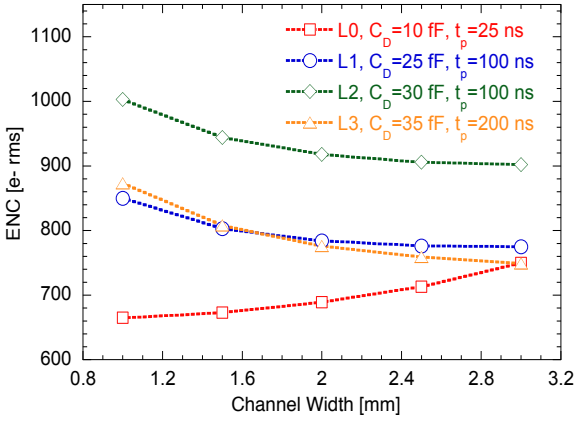
Fast front-end block diagram

- Simulation results available for a preliminary version of the charge preamplifier (I_D=500 μA)



Equivalent noise charge

- Results obtained with ideal RC^2-CR shaper and ideal bias network

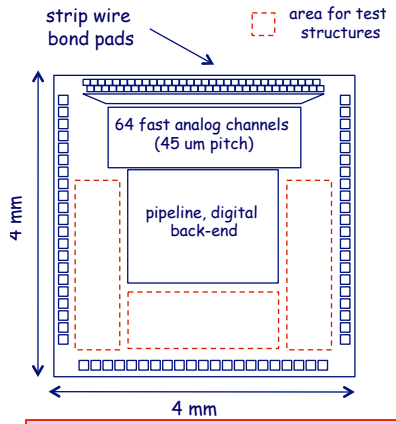


Front-end chip for strip/striplets (II)

L.Ratti

- First evaluation of noise performance for all layers done
- Some optimization still needed

Layer	C_D [pF]	available t_p [ns]	selected t_p [ns]	ENC from R_S [e rms]	ENC [e rms]	Channel width [μm]	Hit rate/ strip [kHz]	Efficiency 1/(1+N)
0	11.2	25, 50, 100, 200	25	220	**740**	3000	1400	0.92
1	26.7		100	460	**940**		430	0.90
2	31.2		100	590	**1100**		244	0.94
3	34.4		200	410	**940**		191	0.91
4	52.6	400, 600, 800, 1000 (or 500 and 1000)	500	490	**1000**	9000	18	0.98
			600	440	**940**			0.97
5	67.5		800	560	**1090**		12	0.98
			1000	500	**1030**			0.97



RC²CR shaping, I_D=500 μA, L=200 nm, N-channel input device,

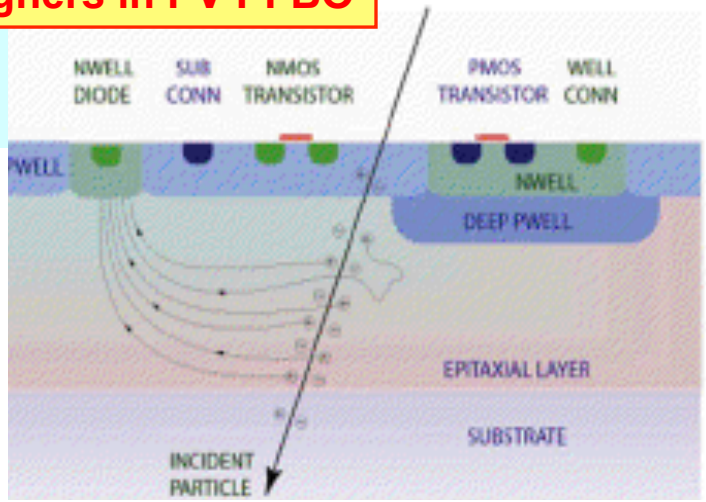
- Efficiency (due to analog dead time) is underestimated.
- Need to use correct energy deposited/strip now available from back. simulation

Milestones for chip development:

- 2012: first test structures 2x64 (fast & slow) channels, auxiliary blocks
- 2013: first fully operational prototype chips 2x128 channels
- 2014: production run

First APSEL MAPS with INMAPS process submitted

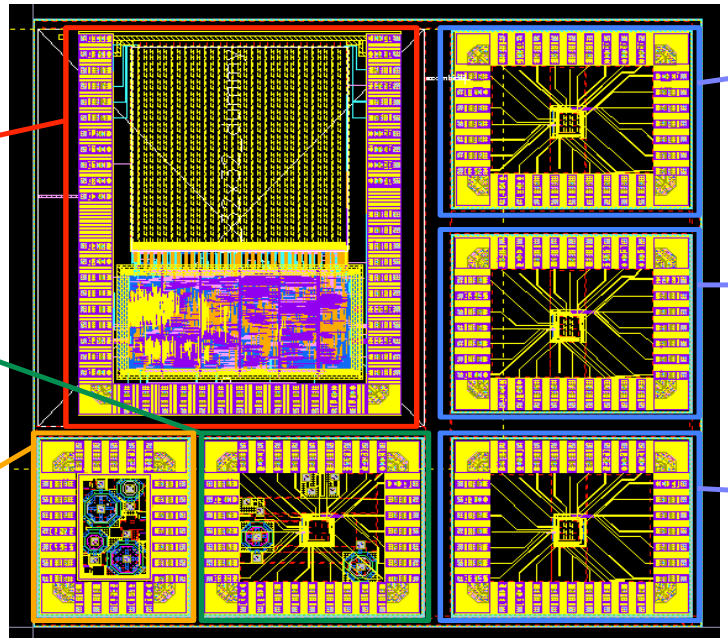
Designers in PV-PI-BO



- high-Ω epilayer available for improved charge collection and radiation hardness!
- 4th well (deep Pwell), below nwells for in-pixel logic, is used to avoid charge collection in competition with sensing electrode.

Prototype chip (submitted end of July)

- In 3x3 matrices all the analog outputs are available and an injection capacitor is connected to the central pixel



32x32 matrix (4-diode pixels) with sparsified digital readout architecture

3x3 matrix, 4-diode, no DPW, preampli input device with EL structure, Nw/Pepi diodes and accumulator capacitors

Nw/Pepi diodes, single channels

3x3 matrix, 4-diode pixels, DPW, preampli input device with EL structure

3x3 matrix 4-diode pixels, DPW, preampli input device with open structure

3x3 matrix 2-diode pixels, DPW, preampli input device with EL structure

Update on activities in Bologna

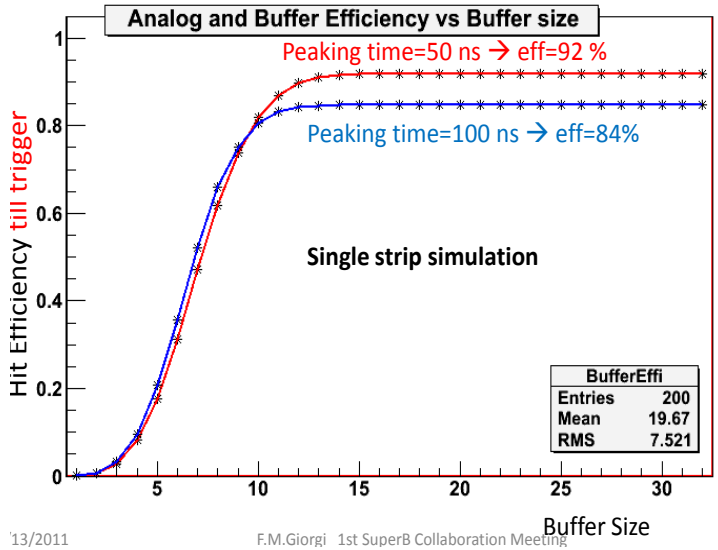
F. Giorgi - BO

- L0 strip readout circuit upgrade
- INMAPS submission
- Test Beam Sept. 2011

High level simulation (C++) of MAIN features of a readout chip: Preliminary Toy Monte Carlo

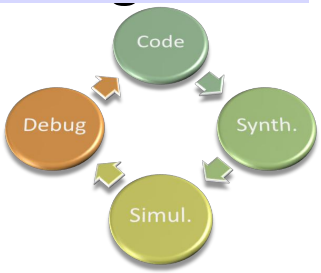
L1 simulation: 687 kHz/strip

Inefficiency sources: Analog peaking time and limited buffer size.



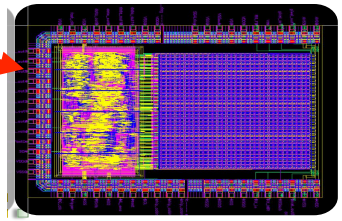
MIP full charge release in the strip, no charge sharing → saturation efficiency underestimated.

- Revised Architecture Design Flow for INMAPS submission



- Conceptual design
- VHDL coding
- Behavioral simulations with Montecarlo hit generator on pixel
- Extracted hits cross-checking
- VHDL Synthesis
- Post synthesis simulations
- Behav. and P.S. sim. compare
- Physical synthesis and implementation (chip layout)
- Post Layout simulations
- P.L. and P.S. sim. compare

Real matrix model (by F. Morsani)

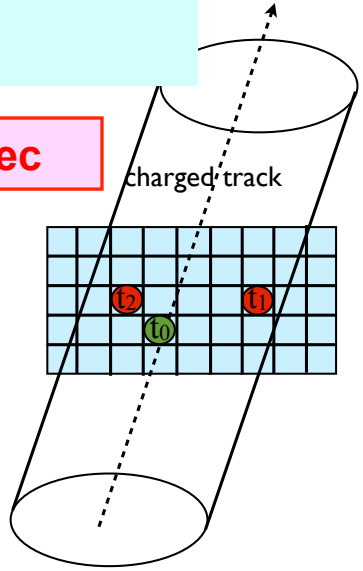


- Behavioral and post layout simulation in good agreement

First evaluation of striplets performance in high background with Fastsim

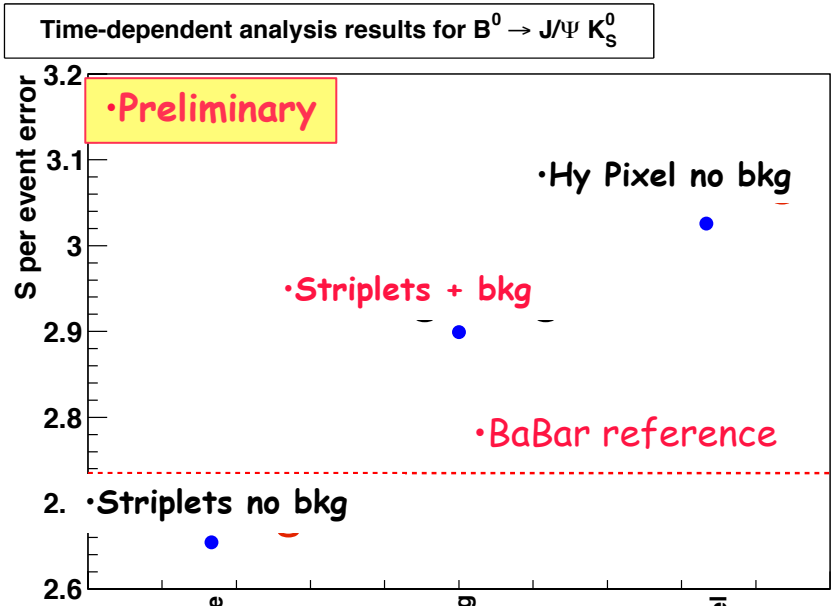
N. Neri - MI

PatRec



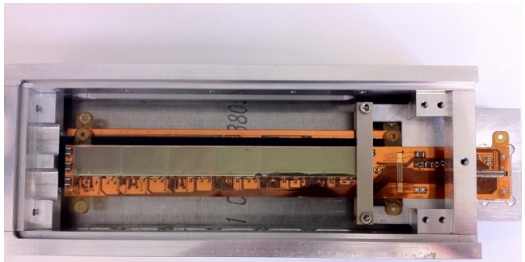
- Effect of background studied on time dependent analysis
- Hits from background pairs added to signal in Fastsim:
  - Hit merging & PatRec confusion tools
  - PatRec confusion is probably the bigger effect: is driven more by the track resolution and dominates for low momentum tracks.

- Results presented are preliminary
  - Checks on fundamental quantities still to be done and several technical problems need to be fixed to perform systematic studies.
    - Safety factor not included on back rates.
- Main deterioration seen in tag vertex resolution (low momentum tracks!)
- Still to evaluate effect on pixel although deterioration expected to be smaller:
  - detector occupancy determines number of back. hit added to signal: striplets occupancy is 300 times higher then pixel occupancy!



Update on activities in Strasbourg

I. Ripp-Baudot - Strasbourg



PLUME ladder

- A first double-sided ladder equipped with 12 MIMOSA 26 sensors (0.35 µm) has been constructed and will be tested on beam at CERN in November 2011 (PLUME project).
- A first submission of a sensor in a 0.18 µm technology will be done in October 2011.
- Strasbourg and Frankfurt organised last week a "Workshop on system integration of highly granular and thin vertex detector" : http://indico.cern.ch/conferenceDisplay.py?confId=144152
This workshop has served to exchange experiences and to search for synergies between the different vertex detector projects as carried out for example at CBM, STAR, ALICE, ILC, eIC and PANDA experiments.
- We continue to perform simulations of different geometries, studying the differences of performances with single- and double-sided layers. This is done up to now in the specific frame of the ALICE vertex detector upgrade, but conclusions may be used also for the SuperB vertex detector. We mainly investigate the improvement on pointing resolution and momentum reconstruction by using the mini-vector approach (correlating hits between the 2 sides of the double-sided layer).
- The final sensor for the STAR vertex detector (ULTIMATE, a 2x2 cm^2 sensor) has been validated and constructed, and integration is underway by STAR.

Update on activities in UK

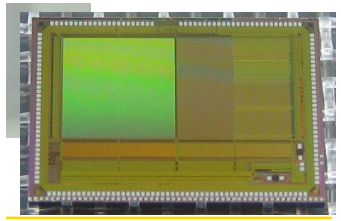
F. Wilson - RAL

- ARACHNID R&D project on MAPS pixel for future vertex detector recently submitted by UK groups

Generic R&D program.
Targets: SuperB, ALICE upgrade and T2K upgrade
€500k requested for 15 month programme.
Decision was made mid-July but still not announced!

Arachnid Work Packages

- *1) MAPS Device characterisation*
  - Test stand setup
  - Detailed characterization
  - Laser tests
  - Gain calibration with radioactive sources
- *2) Radiation Hardness and test beams*
  - Alpha, beta and gamma irradiation
  - DESY/CERN test beams
- *3) Advanced MAPS operation*
  - Thin detector development
  - Cryogenic Operation
  - High Magnetic Field operation
  - Surface Coatings
- *4) Sensor design for real-world applications ready for fabrication.*
  - SuperB
  - ALICE

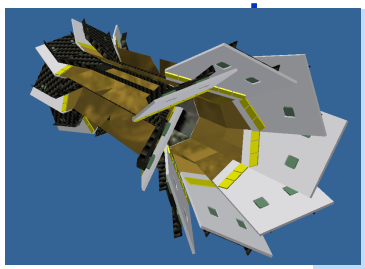


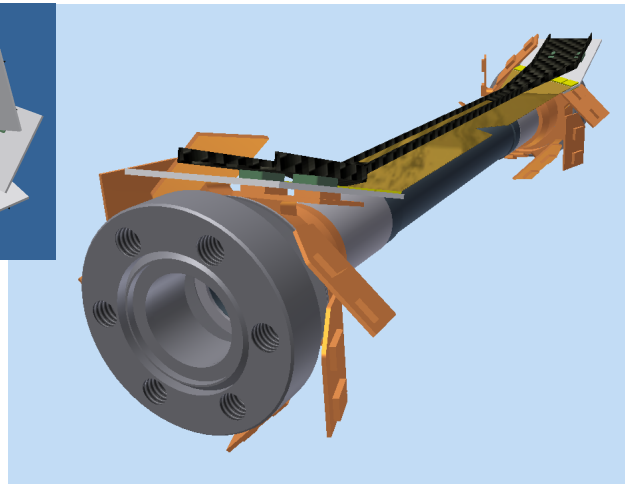
- Characterization of several MAPS chips (already produced for other applications) will give important information on the technology.
- The design of a MAPS chip with SuperB specs can be done during this R&D project:
  - no funding for chip prototype production.

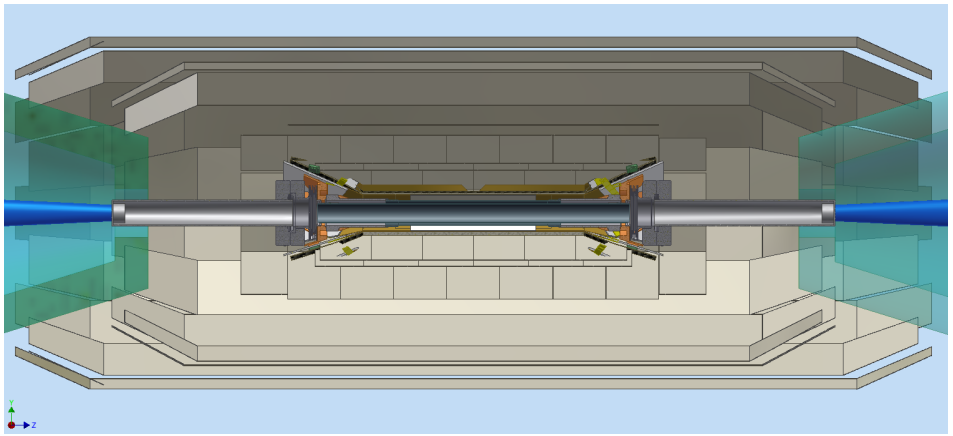
Update on SVT Mechanics

F. Bosi- Pisa

Layer0 design with striplets revised and L1-L5 module design started







- Problems of penetation of L0 HDI with L1-L2 sensors.
- Several solutions will be investigated

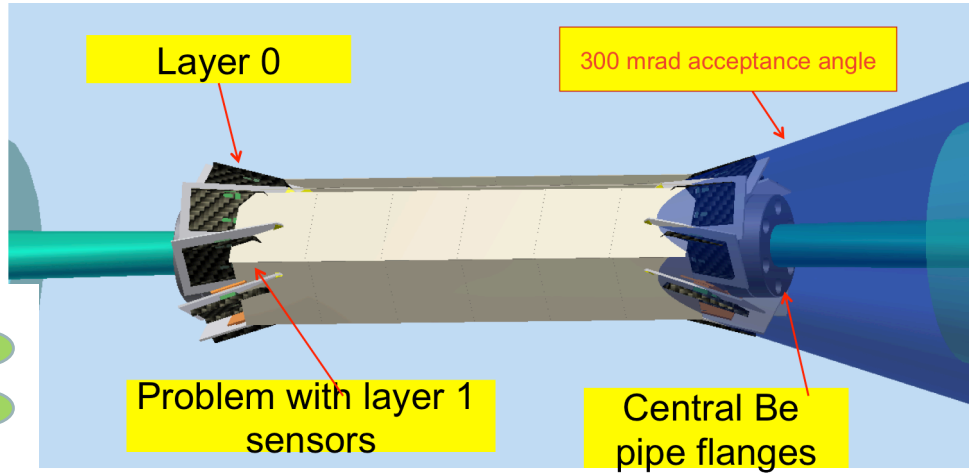
1) modify the HDI/supp. structure and layer 0 geometry

-HDI and C.F. support structure reduced in dimensions

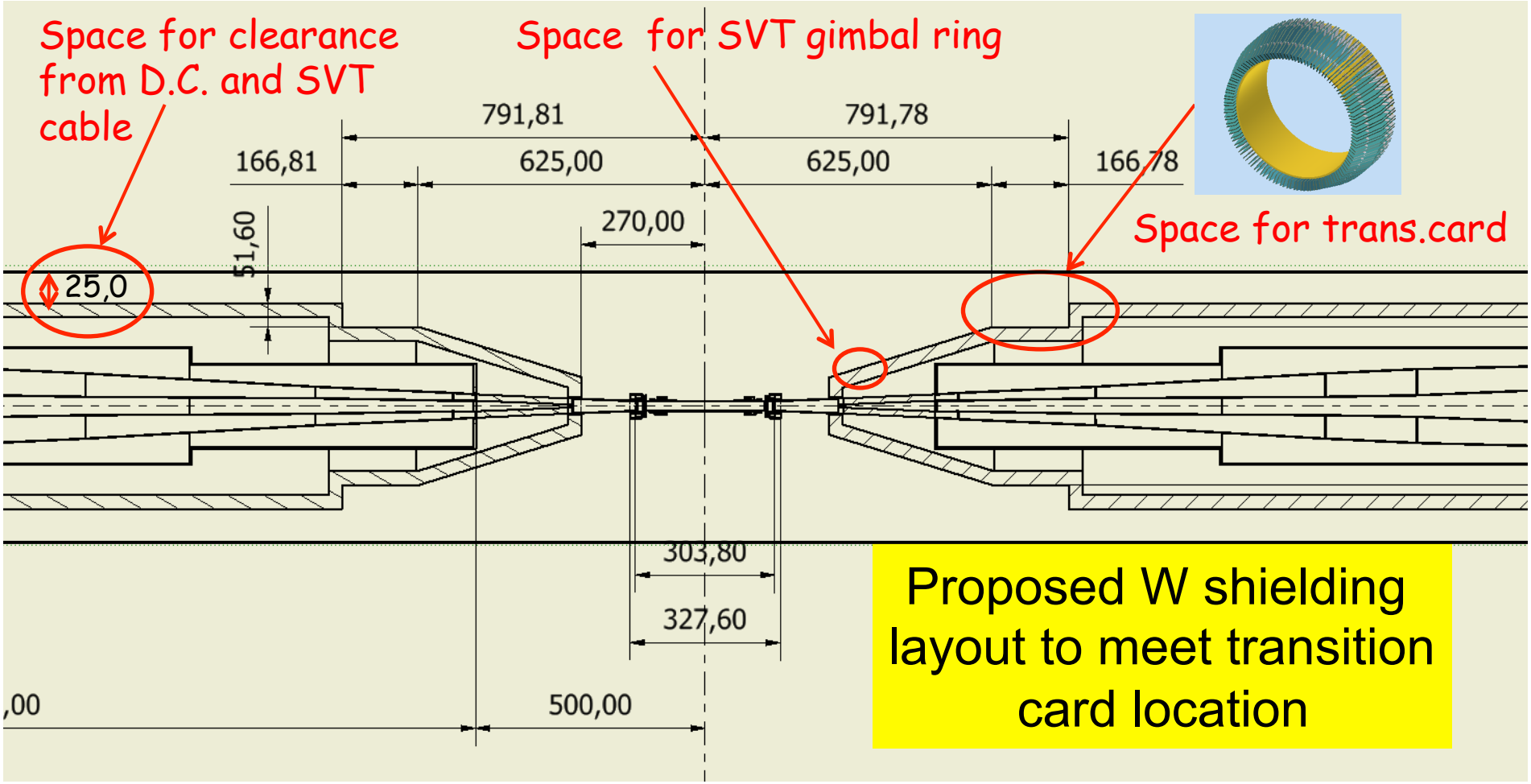
-position of HDI nearer of 3-4 mm to the L0 sensor

2) Move the Be pipe flanges forward in z of about 10-12 mm in order to reduce radial L0 HDI position

3) Position at larger radius L1-2 (+ 5-10 mm)



Shielding layout



Proposed W shielding layout to meet transition card location

Conclusion

F. Bosi- Pisa

SVT Engineering situation

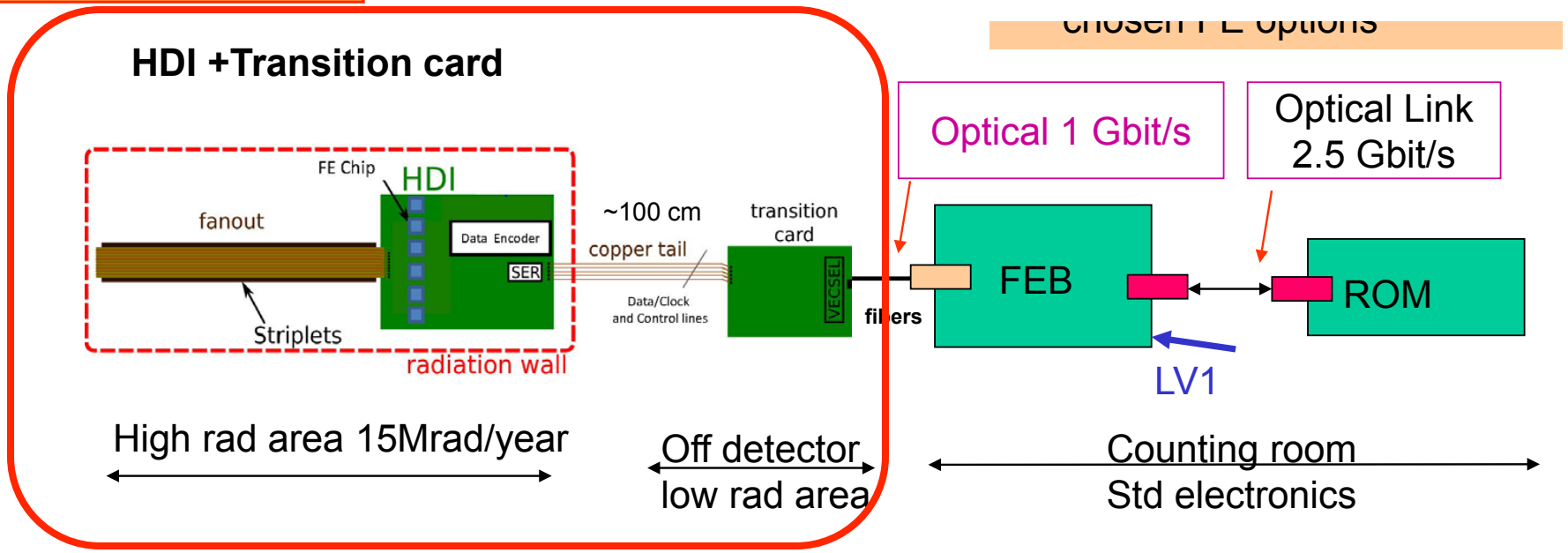
1) QM Engineers started to work on the items they agree to cover (space/ frame and support cone)
2) N.1 Young engineer will begin (October 1st) his work in Pisa (planned to work on the jig and features design for SVT Modules prototype production)
3) N.1 Engineer at 50% will be operative beginning of next year at INFN Milan to work on trans. Card support and cooling

-A significant acceleration in the engineering design is expected in the next months due to the larger number of engineers involved.

*Priority on the baseline design (strplets+L1-5) and to eliminate the conflict with layer 1-2
* Works on pixel prototype modules has lower priority until TDR is ready
* Quick demounting procedure and IR layout , are still strongly depending on beam pipe dimension definition , W shielding dimension, criostat and QD0 design, etc. but anyway one engineering proposal has to be presented to the Tech. Board as soon as possible
* Work on TDR mechanical chapter has started

Update on activities in Milano

M. Citterio - Milano



Al bus for pixel module prototype not yet started @ CERN.

Search of other than CERN commercial partner for Fanout (for strip) production is still ongoing:

- Italian company will build a first prototype first quarter of 2012
- New contact with USA firm initiated.

HDI prototyping will start in October	→ Z properties mostly
Encoder IC Specs linked to FE chip finalization	→ End of year
Rad-hard serializer choice	→ Still LOC1, ongoing
Copper tail: lenght vs data transfer	→tests are progressing

Update on background simulation

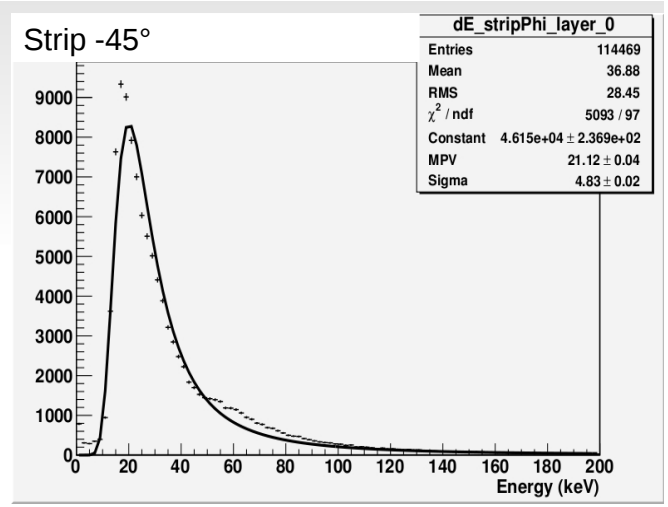
R. Cenci - Maryland **C. Stella - Trieste**

- Strip detail implemented in Bruno by R. Cenci for a more accurate rate calculation.
- Very useful contribution from Trieste in the last months on background studies.
- After Elba Riccardo and Carlo were in touch to cross check their results and get more solid background estimates.
- Fair agreement now

Rates from pairs production (Elba production)

Layer	RO PitchZ (or +45°) μm	Cenci Rate Z or +45° (MHz / cm^2)	Rate Z or +45° (MHz / cm^2)	RO Pitch ϕ (or -45°) μm	Cenci Rate ϕ or -45° (MHz / cm^2)	Rate ϕ or -45° (MHz / cm^2)
0	50	29.9	24.3	50	23.3	24.3
1	100	0.7	0.93	50	1.5	1.61
2	100	0.35	0.4	55	0.72	0.73
3	100	0.097	0.12	55	0.19	0.19
4	210	0.0076	0.0036	100	0.012	0.007
5	210	0.0041	0.0024	100	0.006	0.005

Energy deposited/strip (pairs) Layer0



- Several sanity distributions produced
- Distributions of cluster multiplicity and energy deposited/strip are now available and will be used for readout chip simulation
- Still no new results from Official-London production (Rad Bhabha/ Toucheck/Beam gas)

SVT-TDR subchapters & editors

1. Vertex Detector Overview (12) – G. Rizzo
2. Backgrounds (4) – R. Cenci
3. Detector Performance Studies (6) – N. Neri
4. Silicon Sensors (8) – L. Bosisio
5. Fanout Circuits (8) – L. Vitale
6. Electronics Readout (28)
    1. Readout Chips (10) – V. Re
    2. Hybrid Design (10) – M. Citterio
    3. Data Transmission (8)– M. Citterio
    4. Power Supplies (1??) -???
    - SVT DAQ (M. Villa) will be in the ETD section
7. Mechanical Support & Assembly (14) – S. Bettarini/F. Bosi
8. Layer0 pixel upgrade options (10) – G. Rizzo/L. Ratti/ + others
9. Services, Utilities (2) -??

- Chapter editors produced a first draft of detailed outline
- The first estimate of pages is too high: TOT ~ 92!
- We should try to end up with ~60-70 pages max.

Conclusions

- Most of the work over the summer on testbeam preparation
- Some progress on baseline design for TDR:
  - Front-end chip readout for striplets/strip
  - Striplets performance with high background
  - More solid background rate estimates
  - Mechanics
    - Very fruitful discussion with QM engineers during this meeting.
- Still a lot of work to do to get a solid design for the baseline for the TDR.

backup

SVT Institutions

Groups already working for the SVT:

- Trieste: Silicon sensors, striplets, fanout
- Pavia/BG: MAPS & Front-End chips for pixel and strip (analog cells)
- RomaIII: MAPS
- Milano: pixel bus/fanout Layer0 & peripheral electronics, SVT performance studies, SVT mechanics (HDI cooling rings, transition cards support, beam pipe)
- Bologna: SVT DAQ , MAPS & FE chips (digital architecture).
- Torino: testbeams mechanics.
- Pisa: SVT coordination, MAPS & FE chips for pixel & strip (in-pixel logic, readout architecture, chips final layout, test of prototypes), module assembly & testing, SVT mechanics and cooling, testbeams.

« New » groups getting involved:

- Trento – pixel sensors, strip sensors
- University of Insubria – Mi-B - external layers fanout
- Bari - Hybrid Pixel, Peripheral Electronics (encoder/serializer)
- Mi - C. Fiorini FE chips (analog cell external layers)
- UK: QM (SVT mechanics, sensors?), RAL (MAPS)
- Strasbourg (MAPS)